AND, AT THE WAFER LEVEL

For many in the industry, performing final test at the wafer level is still a novel idea. While providing some much needed solutions, it also comes with its own set of challenges. The four papers in this session look at wafer-level test from a number of different perspectives. The first one discusses the mechanical and electrical differences between wafer-level probe and wafer-level test using spring pins, focusing on requirements for performing final test at the wafer-level. The second presentation provides a comparison between traditional probe test for an RF wafer level chip scale package (WLCSP) and a final test socket solution. TSV issues lead our third author to share technologies that can bridge between 3D stacking and the 3D IC without TSVs. Finally, we'll gain insight into what some consider the holy grail of burn-in and test – wafer-level burn-in (WLBI). Now that WLBI is possible, it's important to understand when it's appropriate to consider WLBI versus other burn-in alternatives.

This Paper

Spring Probes and Probe Cards for Wafer-Level Test
Jim Brandes—Multitest

A Comparison of Probe Solutions for an RF WLCSP Product
James Migliaccio—RF Micro Devices

Bridging Between 3D and 3D TSV Stacking Technologies
Belgacem Haba, Ph.D.—Invensas

Wafer-Level Burn-in Decision Factors
Steve Steps—Aehr Test Systems

Spring Probes and Probe Cards for Wafer-Level Test

Jim Brandes
Multitest

2013 BiTS Workshop
March 3 - 6 2013

Outline

- Differences between probing and WL test
- Electrical differences dictate spring probes
- Mechanical differences also important
- Focus on compliance requirements
- Comparison of various probe technologies
- Importance of board flatness
- Techniques to ensure board flatness
- Improved planarity validation method

Wafer Probe and WL Test Differences

- There are many differences between wafer probing and Wafer Level (WL) test
  - Electrical
  - Mechanical
  - Language
  - Obvious differences
  - Subtle differences

Electrical Differences

- Wafer level test is final test
  - Wafer probing is an abbreviated functional test
- Must have all capabilities of package test
  - Low, consistent resistance for DC tests
  - High bandwidth for at-speed functional tests
  - Low inductance for power delivery
  - High conductance for at-limit DC tests
  - High conductance for power delivery
  - Kelvin capability

Electrical Requirements Dictate Spring Probes

Technology	Pogo™ Probe	Spring Probe	Spring Probe	Membrane	Vertical 1	Vertical 2
Type	CSP050	MER040	MER030*			
Inductance	1.22 nH	0.9 nH	1.7 nH	0.2 nH**	N/A	N/A
DC Current	1.7 A	1.8 A	1.5 A	200 mA***	0.5 A	1.6 A
Resistance	100 mΩ typ.	70 mΩ typ.	150 mΩ typ.	< 200 mΩ	< 2 Ω	N/A
Bandwidth	5.7 GHz	18 GHz	12.4 GHz	20 - 33 GHz	1.3 GHz	N/A

* In Development ** Tip Only *** On Solder

Membrane and Vertical Probe specifications from internet

Mechanical Performance

- **Mechanical characteristics are also different**
  - **Just as important as electrical**
- **Pressure – More required to penetrate solder ball**
  - **Solder has thicker oxides**
  - **More potential for debris due to further processing**
  - **Achieved by higher force and sharp tip geometry (pressure = force / area)**
- **Compliance – WL requires more than wafer probe**
  - **Redistribution layer and solder balls add tolerance**
  - **Allows force to be adjusted with overdrive**
  - **This is the focus of the rest of this presentation**

Mechanical Requirements Dictate Spring Probes

Technology	Pogo™ Probe	Spring Probe	Spring Probe	Membrane	Vertical 1	Vertical 2
Type	CSP050	MER040	MER030*			
Test Height	6.45 mm	3.3 mm	3.5 mm	0.065mm**	3 - 7 mm	5.95 mm
Compliance	0.51 mm	0.44 mm	0.55 mm	0.25 mm	0.125 mm	0.3 mm
Min. Pitch	0.5 mm	0.4 mm	0.3 mm	0.15 mm	0.15 mm	0.2 mm
Force***	35 g	30 g	15 g	16 g	25 g	6g
Tip Shape	3 or 4 points	2 points	2 points	1 point	1 point	4 points
Probe Mark	off apex	off apex	off apex	at apex	at apex	off apex

* In Development ** Tip Only *** At test height

Membrane and Vertical Probe specifications from internet

Electrical & Mechanical Performance

- Electrical, mechanical performance inter-related
- Shorter gives better electrical performance
  - Spring probe cannot add anything to signal, only degrade it
  - The shorter the spring probe, the less degradation
- Longer gives better mechanical performance
  - Force and compliance easier to achieve
- External Springs help satisfy all requirements
  - Higher force and more compliance in a short probe

Comparison of traditional Pogo-style probe and newer technology

- CSP is a POGO probe with four components
- Two plungers, barrel and internal spring:

0.5 mm pitch Pogo-style probe

- Mercury has two flat components and an external spring

0.4 mm-pitch flat probe

0.3 mm-pitch flat probe

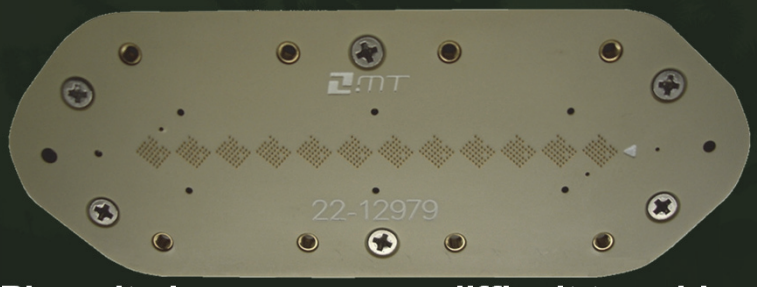
Spring probes drawn to scale

Board Planarity

- Board planarity is important
- Spring probes make solderless connection to board
- Spring probes are preloaded on board side
  - Prevents board chatter
  - Reduces board wear
- Any non-planarity consumes some spring probe compliance
  - Less available for the DUT side of contactor

Board Planarity

- Larger devices are being tested at wafer-level
- Multiple sites provide economic advantage
- The most-distant sites are getting farther apart



- Planarity becomes more difficult to achieve

Improving Board Planarity

- Several techniques improve board planarity

Balanced Stack-Ups

Balancing Mixed Laminates

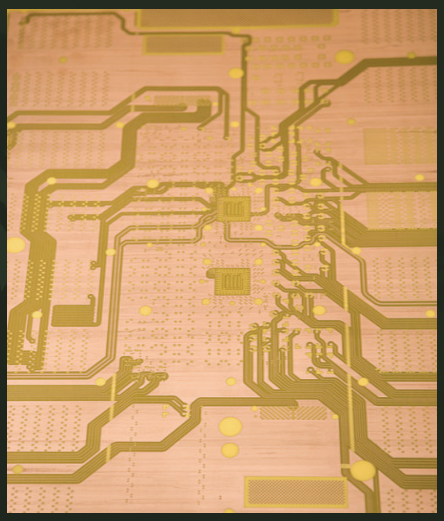
Monolithic Books

Surface Planarization

Improving Board Planarity

Balanced Stack-Ups

- Inner-layer copper pour (thieving)
- Distributes copper more evenly
- Maintains uniform thickness
- Does not affect electrical performance



Improving Board Planarity

Balancing Mixed Laminates

- Used when design calls for mixed materials
  - Thickness of each laminate kept symmetrical from center
  - Each material moves differently during lamination
  - Minimizes impact on warp
- Need to consider other attributes
  - C_{TE} of resin
  - Weave direction

Dielectric Thickness

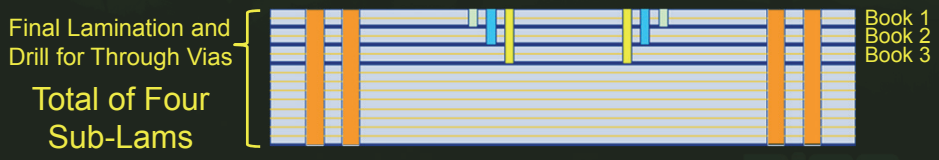
50.6	Layers 1-16 Nelco N4000-13EP
22.7	Layers 16-18 Rogers 4350
40.4	Layers 20-29 N4000-13EP
22.7	Layers 30-33 Rogers 4350
50.6	Layers 34-48 Nelco N4000-13EP

Overall Thickness
0.187" ± 0.01"

Improving Board Planarity

Monolithic Books

- Most WL test applications at 0.4 mm pitch
- Boards need to be thick
  - Rigidity to maintain planarity
  - Multiple routing layers due to fine pitch, multi-site
- Many fabricators use multiple lamination cycles
  - Contributes to board warp
  - Adds cost

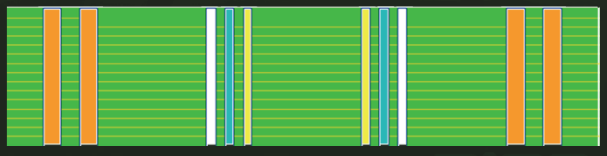


Improving Board Planarity

Monolithic Books

- Require high-aspect-ratio vias
- Single lamination cycle
  - Results in less stress to laminate resins
    - Stress contributes to PCB warp
  - Single lamination results in flatter boards
  - Single lamination costs less

Single Lamination, Plating, Plated-Through-Hole Drill, and Via Fill Cycles



Improving Board Planarity

Surface Planarization

- All boards will exhibit some bow and twist regardless of steps taken to minimize it
- Boards also suffer from *Football Effect*
  - Term that describes tendency to be thicker in the center area than on the edges

Football Effect

Improving Board Planarity

Surface Planarization

- Boards processed with polishing steps
- UltraFlat provides permanent improvement
  - Processes such as flat-baking are temporary
  - Flat-baked boards take on moisture over time, return to their original shape

UltraFlat™ Technology

Validating Board Planarity

- Validating planarity is also important
  - Improved method
  - More accurately reflects in-situ performance
- Warpage tolerances getting tighter
  - 0.5% acceptable historically
  - (0.005" / inch of diameter)
  - 0.3% becoming norm for WL boards
- Traditional validation method:
  - Place board on flat reference (granite table)
  - Insert gauge pins around perimeter
  - Does not confirm planarity in critical DUT area
    - More warpage allowable around periphery

Validating Board Planarity

Improved Validation Method:

- Place board on precise stands on the table
  - Board is designed with pads in specific locations
- Height gauge measures contact pads on board
  - Gauge zeroed on one pad
  - Differential to other pads measured and recorded

Validating Board Planarity

Improved Validation Method:

- Delta between contact pads calculated
  - Compared to pass/fail criteria
- Information is more relevant
  - Contact pads rather than substrate measured
  - Data in critical DUT area

Summary

- Unique challenges require fresh look at mechanical requirements of WL test interface
- Traditional probe technologies and PCB manufacturing methods are not adequate
  - Can have negative impact on test yields
  - Can shorten hardware life
- Leading-edge approaches provide best results

Acknowledgements

- Thanks to Chris Cuda for his help with this presentation

- POGO is a trademark of Everett Charles Technologies