BETTER BY DESIGN

The greatest results always begin with a good design. In the world of test and burn-in, the variations are endless. That's why this session features a broad assortment of design topics and perspectives. Beyond socket design, we'll learn about designing the right handler for the job. Next is a birds-eye view of a socket's creation from design concept to final assembly, followed by a specific look at designs and applications for package-on-package (PoP) device testing.

Special Designs and Applications for PoP Device Testing

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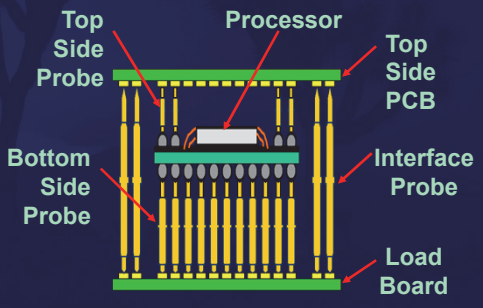
Content

Introduction

- PoP sockets have been widely available since 2009
- Fundamental archetype defined and widespread
- Typical application is a processor tested prior to memory attach
- Memory function is supplied by the tester through the load board



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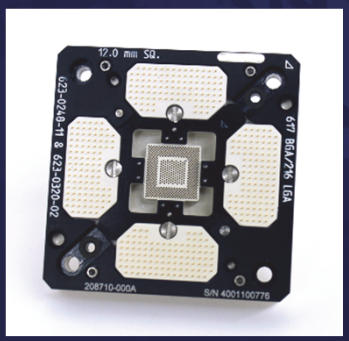
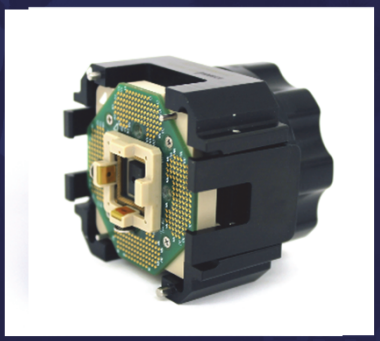
Introduction

- Socketing for typical applications has become routine
- PoP-specific challenges (topside alignment, force balancing) exist but are addressed through standards and analysis tools





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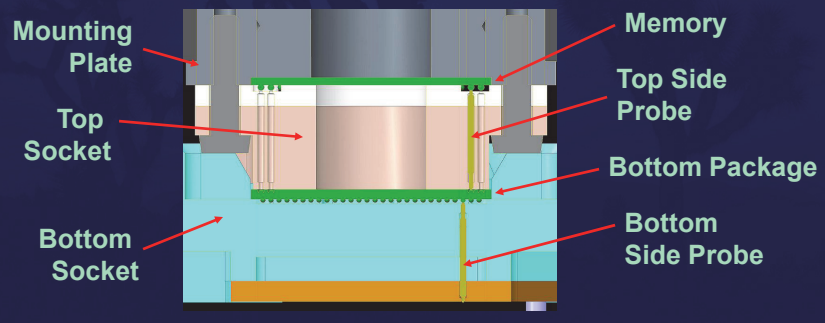
Introduction

Several variations have been requested and developed which differ from the typical archetype:

1. Embedded memory in top socket
2. Top side PCB with connectors
3. Testing with dual memory devices
4. Heating/cooling with micro air-flow channels
5. Impedance controlled interface

Design 1: Embedded Memory Device

- Differs from typical in use of actual 'golden' memory device to supply memory function
- Used in HVM and characterization, principally for system level test (SLT)
- Top side contactor probes interface directly to memory
- Thermal consideration applied in design

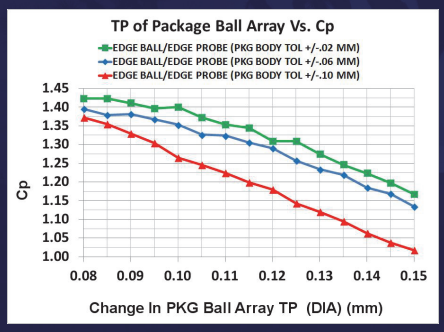


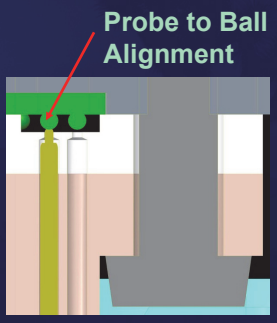
Cross Section

Design 1: Embedded Memory Device

Special Design Requirements

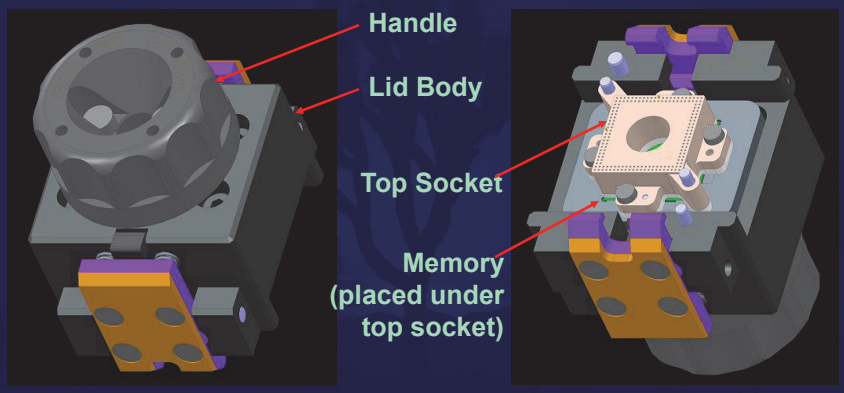
- Tight tolerance on memory device size and solder ball true position for better probe to ball alignment
- Tight fit between memory device and pocket in mounting plate to minimize movement and prevent probe bending





Design 1: Embedded Memory Device

Sample Lid Design

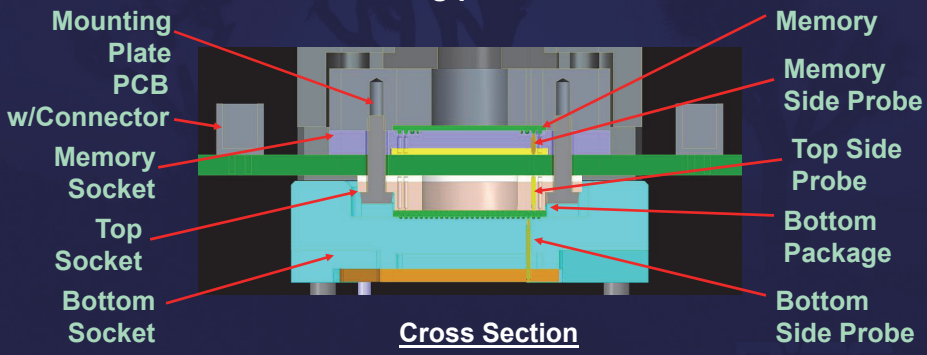


Top ISO View

Bottom ISO View

Design 2: Embedded Memory Device (and daughter board)

- Testing of bottom package and memory device with 3 sets of test probes and top side PCB
- A good known memory device, memory socket, top side PCB (with connectors) and top socket are stacked together and attached to lid mounting plate



Cross Section

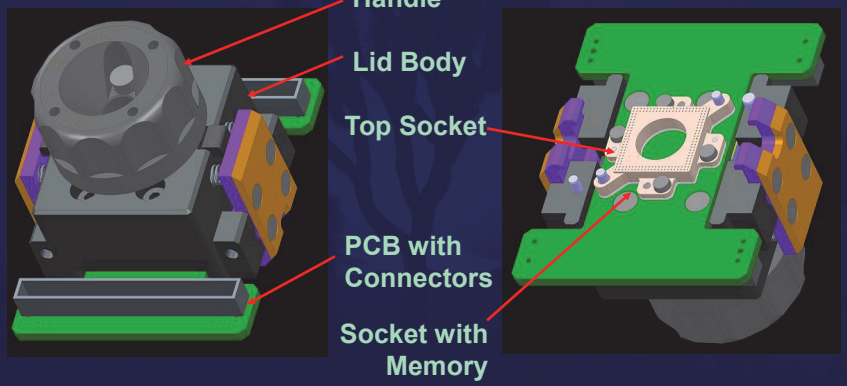
Design 2: Embedded Memory Device (and daughter board)

Key Features

- Same specifications from Design 1 applied
- Connectors or probe marks can be added to top side PCB to monitor the performance of memory signal
- Overall CRES will be higher due to stack-up
- Signal Integrity may not be adequate if the connectors are not actively attached to measurement tool

Design 2: Embedded Memory Device (and daughter board)

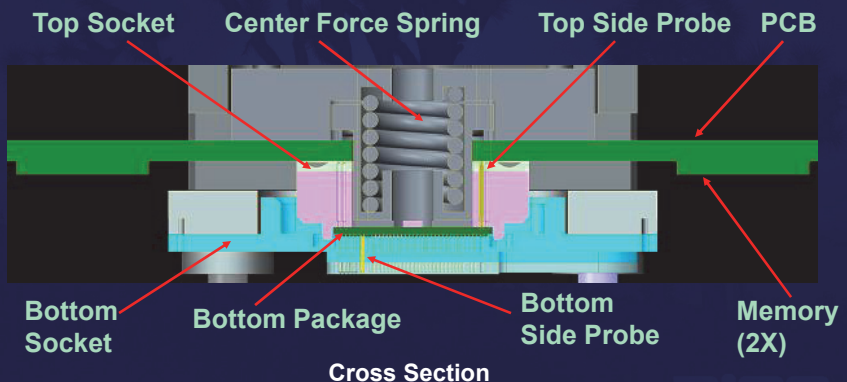
Sample Lid Design



Top ISO View (placed under PCB) Bottom ISO View

Design 3: Top Side PCB with Dual Memory Devices

- Testing of bottom package with two memory devices attached to top side PCB and two sets of test probes
- Use for bottom package with two die design

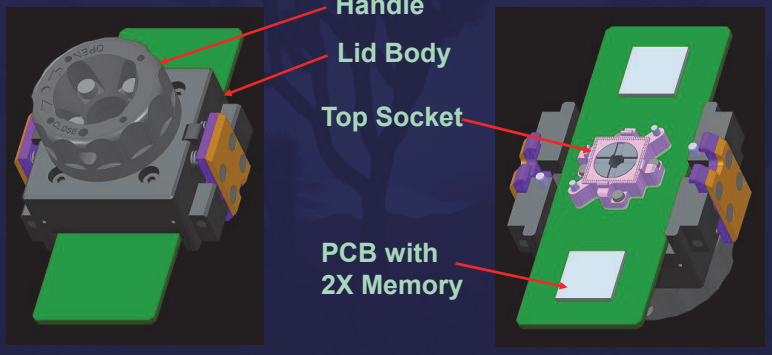


Cross Section

Design 3: Top Side PCB with Dual Memory Devices

Sample Lid Design

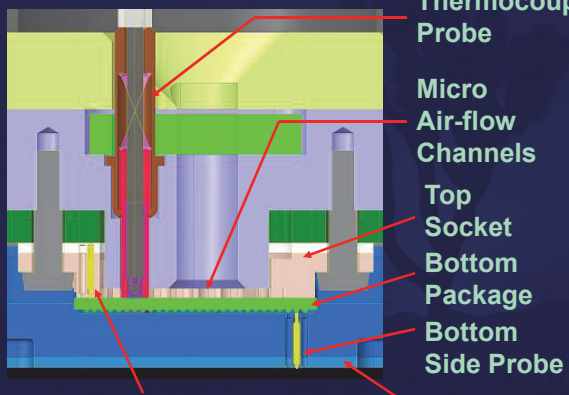
- Package top side signals need to be split into 2 memory devices



Top ISO View

Bottom ISO View

Design 4: Thermocouple Probe and Micro Air-flow Channels



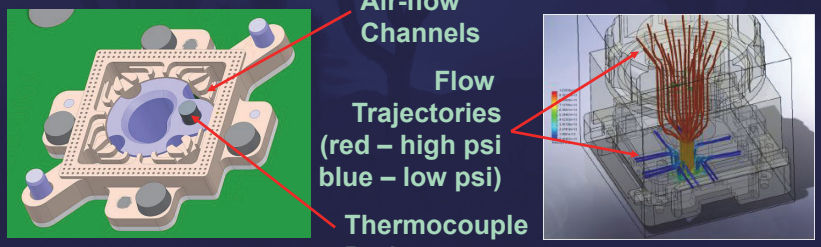
Cross Section

- Active temperature control of device under test
- Off-center thermocouple probe to monitor temperature
- Micro air-flow channels to dissipate heat through convection

Design 4: Thermocouple Probe and Micro Air-flow Channels

Key Features

- Custom thermocouple probe embedded into lid platen
- Air-flow channels from inlet to exit
- Thermal stream < 5 CFM
- Thermal Analysis to validate the performance



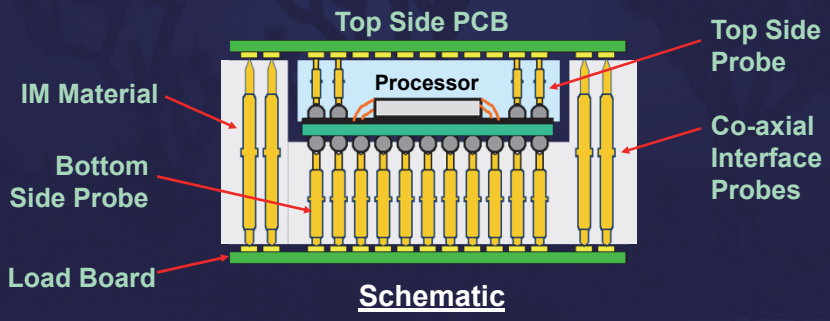
Design 4: Thermocouple Probe and Micro Air-flow Channels

Sample Lid Design

Lid ISO View (TOP) Lid ISO View (BTM)

Design 5: Controlled Impedance Interface

- Conventional application with consideration for high speed memory
- Optimized interface signal integrity through controlled impedance using state-of-the-art coaxial test socket technology

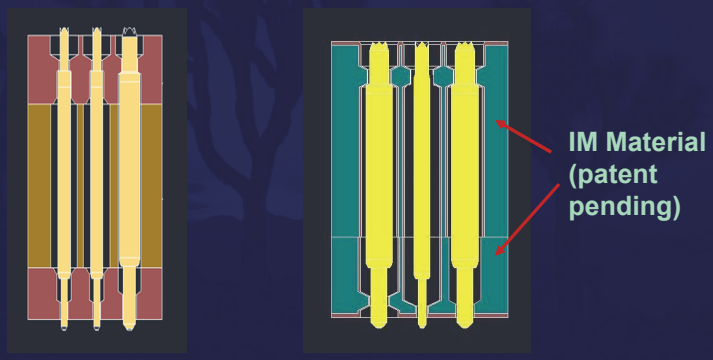


Schematic

Design 5: Controlled Impedance Interface

Key Features

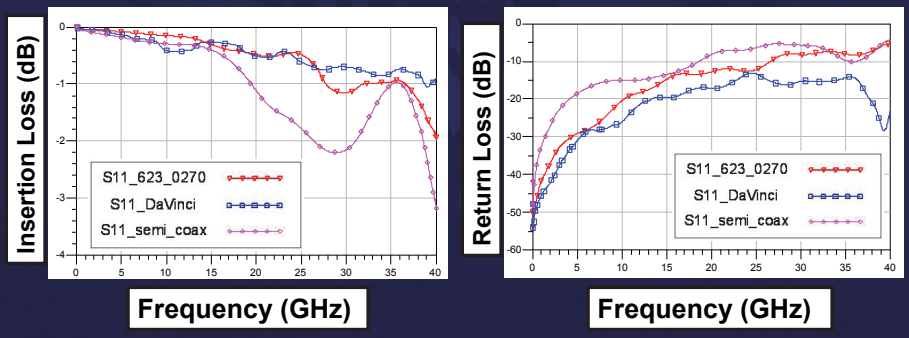
- Insulated metal (DaVinci) housing
- Proven design – hundreds of fielded test sockets
- 35 GHz bandwidth



Conventional Coax DaVinci

Design 5: Controlled Impedance Interface

- Signal Integrity (SI) Improvement



Summary

- Expertise and experience leads to special challenges
- Special analysis tools (SI, thermal, and mechanical) necessary to any PoP engagement
- Innovation through partnership with innovative customers