

BETTER BY DESIGN

The greatest results always begin with a good design. In the world of test and burn-in, the variations are endless. That's why this session features a broad assortment of design topics and perspectives. Beyond socket design, we'll learn about designing the right handler for the job. Next is a birds-eye view of a socket's creation from design concept to final assembly, followed by a specific look at designs and applications for package-on-package (PoP) device testing.

A Novel Nested Doll Concept in Universal Kit for Test Handler

Yee Wei Tiang—Intel (Malaysia)

Anatomy of a Socket

Paul F. Ruo—Aries Electronics, Inc.

Special Designs and Applications for PoP Device Testing

Siang Soh, Frank Zhou, Jon Diller, James Spooner, Khaled Elmadbouly
—Interconnect Devices, Inc.



This Paper

COPYRIGHT NOTICE

The paper(s) in this publication comprise the Proceedings of the 2013 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2013 BiTS Workshop. This version of the papers may differ from the version that was distributed in hardcopy & softcopy form at the 2013 BiTS Workshop. The inclusion of the papers in this publication does not constitute an endorsement by BiTS Workshop, LLC or the workshop's sponsors.

There is NO copyright protection claimed on the presentation content by BiTS Workshop, LLC. (Occasionally a Tutorial and/or TechTalk may be copyrighted by the author). However, each presentation is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop, LLC. All rights reserved.

Special Designs and Applications for PoP Device Testing

**Siang Soh, Frank Zhou, Jon Diller,
James Spooner, Khaled Elmadbouly
Interconnect Devices, Inc.**



2013 BiTS Workshop
March 3 - 6, 2013

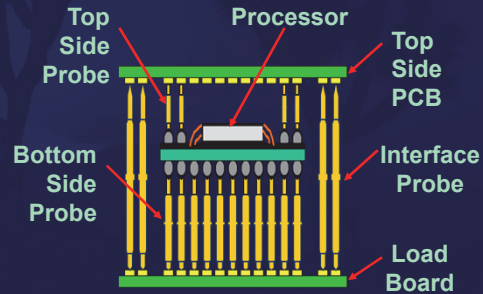


Content

- Introduction
 - Typical PoP Device Testing
 - Variations for Typical PoP Device Testing
 - Special Designs and Applications
- Test Schematics
- Design 1: Embedded Memory Device
- Design 2: Embedded Memory Device (and daughter board)
- Design 3: Top Side PCB with Dual Memory Devices
- Design 4: Thermocouple Probe and Micro Air-flow Channels
- Design 5: Co-axial Return Probes and Insulated Metal (IM)
- Summary

Introduction

- PoP sockets have been widely available since 2009
- Fundamental archetype defined and widespread
- Typical application is a processor tested prior to memory attach
- Memory function is supplied by the tester through the load board



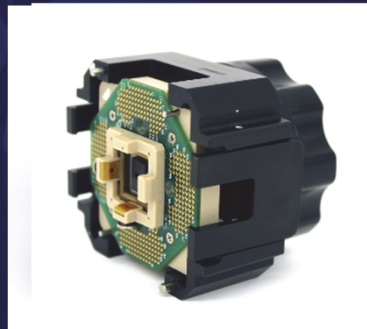
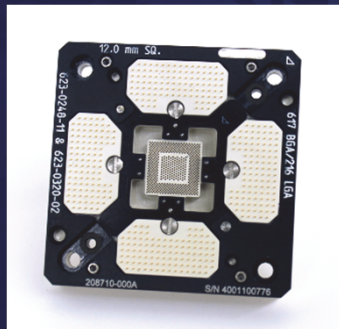
03/2013

Special Designs and Applications for PoP Device Testing

3

Introduction

- Socketing for typical applications has become routine
- PoP-specific challenges (topside alignment, force balancing) exist but are addressed through standards and analysis tools



03/2013

Special Designs and Applications for PoP Device Testing

4

Introduction

Several variations have been requested and developed which differ from the typical archetype:

1. Embedded memory in top socket
2. Top side PCB with connectors
3. Testing with dual memory devices
4. Heating/cooling with micro air-flow channels
5. Impedance controlled interface

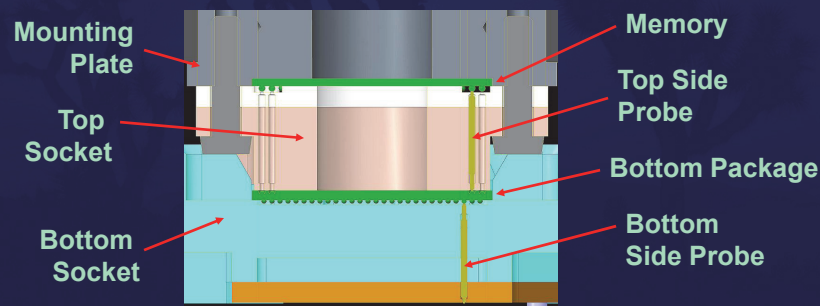
03/2013

Special Designs and Applications for PoP Device Testing

5

Design 1: Embedded Memory Device

- Differs from typical in use of actual 'golden' memory device to supply memory function
- Used in HVM and characterization, principally for system level test (SLT)
- Top side contactor probes interface directly to memory
- Thermal consideration applied in design



Cross Section

03/2013

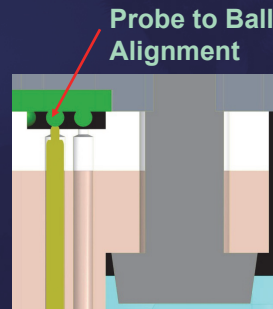
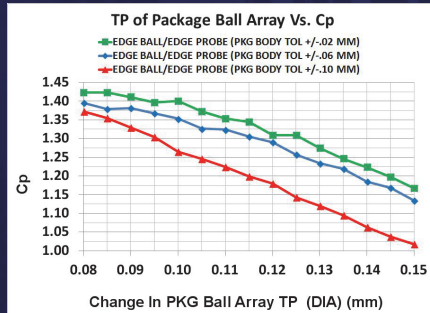
Special Designs and Applications for PoP Device Testing

6

Design 1: Embedded Memory Device

Special Design Requirements

- Tight tolerance on memory device size and solder ball true position for better probe to ball alignment
- Tight fit between memory device and pocket in mounting plate to minimize movement and prevent probe bending



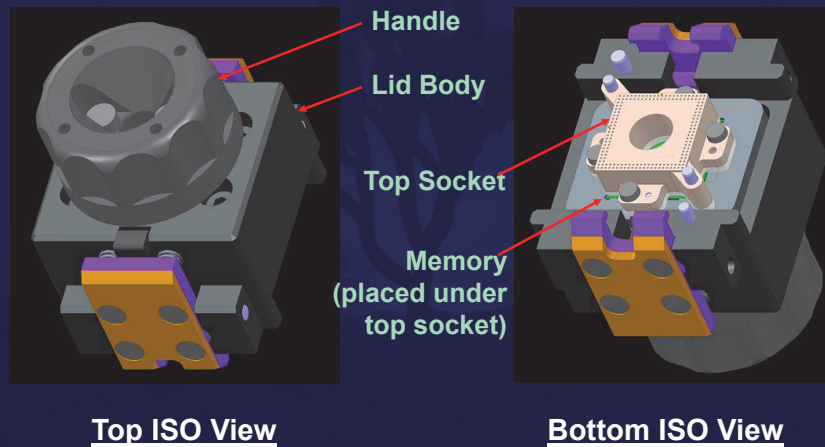
03/2013

Special Designs and Applications for PoP Device Testing

7

Design 1: Embedded Memory Device

Sample Lid Design



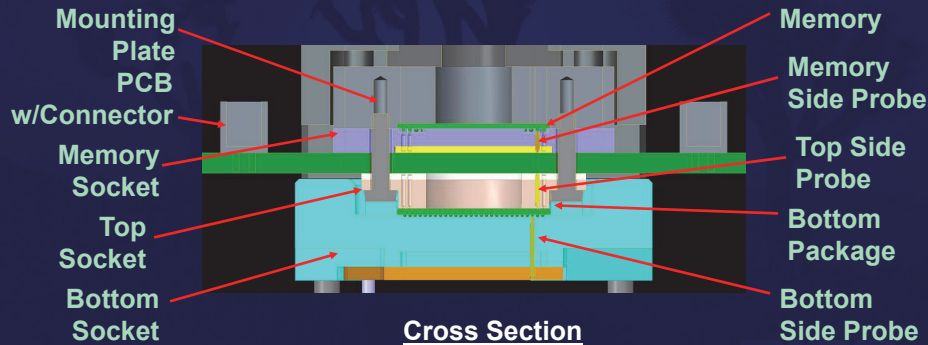
03/2013

Special Designs and Applications for PoP Device Testing

8

Design 2: Embedded Memory Device (and daughter board)

- Testing of bottom package and memory device with 3 sets of test probes and top side PCB
- A good known memory device, memory socket, top side PCB (with connectors) and top socket are stacked together and attached to lid mounting plate



03/2013

Special Designs and Applications for PoP Device Testing

9

Design 2: Embedded Memory Device (and daughter board)

Key Features

- Same specifications from Design 1 applied
- Connectors or probe marks can be added to top side PCB to monitor the performance of memory signal
- Overall CRES will be higher due to stack-up
- Signal Integrity may not be adequate if the connectors are not actively attached to measurement tool

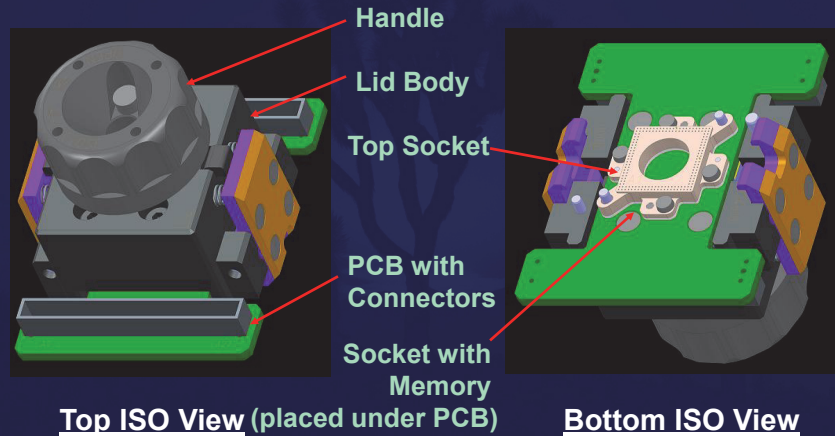
03/2013

Special Designs and Applications for PoP Device Testing

10

Design 2: Embedded Memory Device (and daughter board)

Sample Lid Design



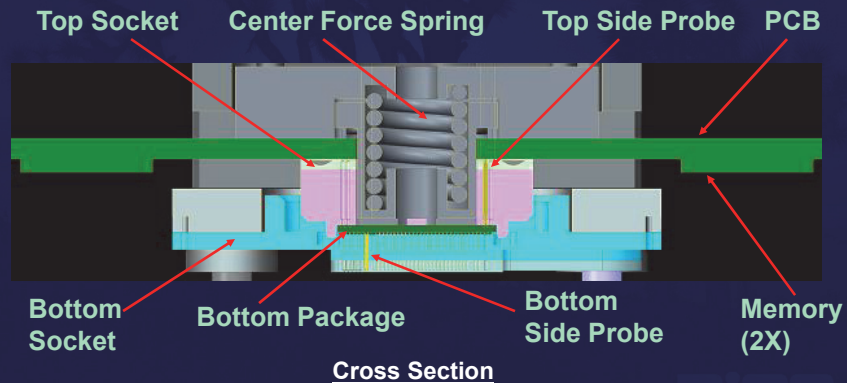
03/2013

Special Designs and Applications for PoP Device Testing

11

Design 3: Top Side PCB with Dual Memory Devices

- Testing of bottom package with two memory devices attached to top side PCB and two sets of test probes
- Use for bottom package with two die design



Cross Section

03/2013

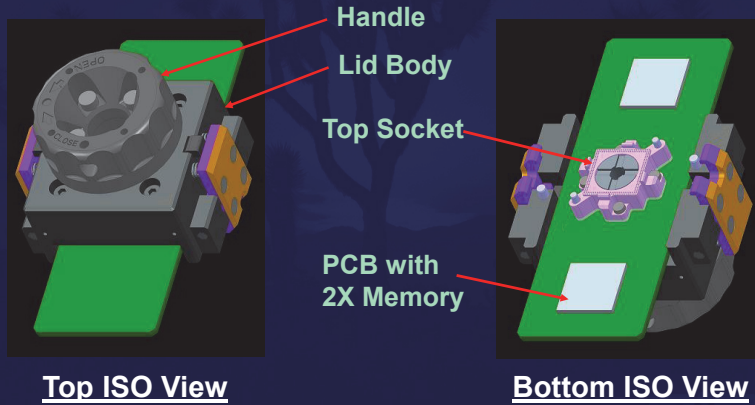
Special Designs and Applications for PoP Device Testing

12

Design 3: Top Side PCB with Dual Memory Devices

Sample Lid Design

- Package top side signals need to be split into 2 memory devices

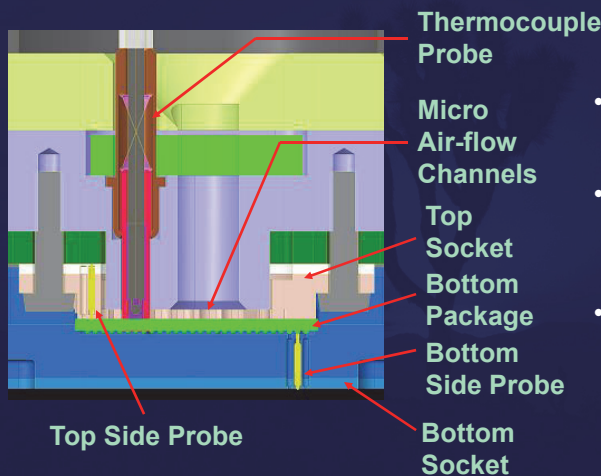


03/2013

Special Designs and Applications for PoP Device Testing

13

Design 4: Thermocouple Probe and Micro Air-flow Channels



- Active temperature control of device under test
- Off-center thermocouple probe to monitor temperature
- Micro air-flow channels to dissipate heat through convection

Top Side Probe

Cross Section

03/2013

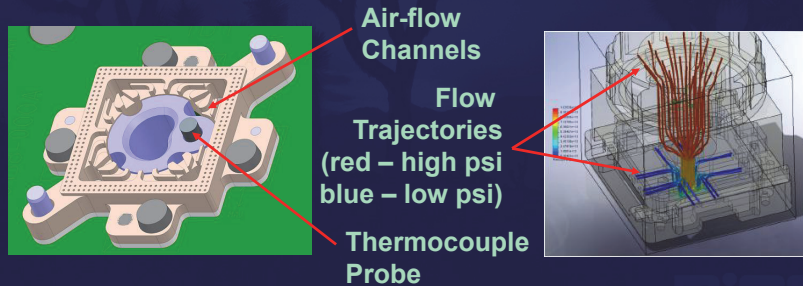
Special Designs and Applications for PoP Device Testing

14

Design 4: Thermocouple Probe and Micro Air-flow Channels

Key Features

- Custom thermocouple probe embedded into lid platen
- Air-flow channels from inlet to exit
- Thermal stream < 5 CFM
- Thermal Analysis to validate the performance



03/2013

Special Designs and Applications for PoP Device Testing

15

Design 4: Thermocouple Probe and Micro Air-flow Channels

Sample Lid Design



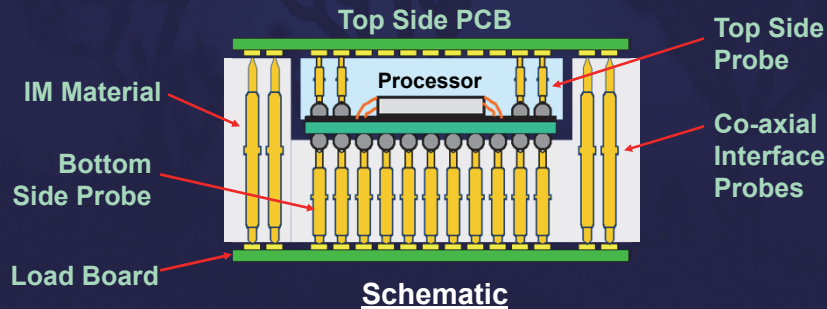
03/2013

Special Designs and Applications for PoP Device Testing

16

Design 5: Controlled Impedance Interface

- Conventional application with consideration for high speed memory
- Optimized interface signal integrity through controlled impedance using state-of-the-art coaxial test socket technology



03/2013

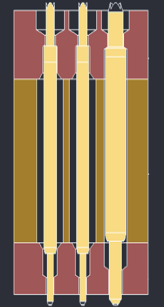
Special Designs and Applications for PoP Device Testing

17

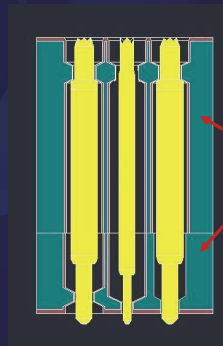
Design 5: Controlled Impedance Interface

Key Features

- Insulated metal (DaVinci) housing
- Proven design – hundreds of fielded test sockets
- 35 GHz bandwidth



Conventional Coax



DaVinci_

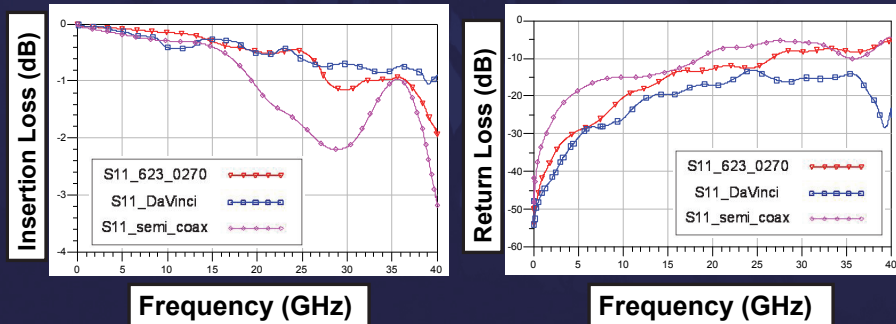
03/2013

Special Designs and Applications for PoP Device Testing

18

Design 5: Controlled Impedance Interface

- Signal Integrity (SI) Improvement



03/2013

Special Designs and Applications for PoP Device Testing

19

Summary

- Expertise and experience leads to special challenges
- Special analysis tools (SI, thermal, and mechanical) necessary to any PoP engagement
- Innovation through partnership with innovative customers

03/2013

Special Designs and Applications for PoP Device Testing

20