BRING IT TO THE BOARD (PCB)

The device under test (DUT) board is sometimes overlooked as a critical element in test-and burn-in strategies. This session brings PCBs into the limelight. The first presentation will cover some of the challenges that various DUT layouts present, demonstrating to semiconductor and ASICS design engineers the importance of considering final test hardware when designing device layouts. Another important consideration, covered in the second presentation, is the importance of performing RF characterization and simulation in-house to accurately measure the materials' electrical performance.

This Paper

Building Optimized Test PCB's Starts at the DUT
Joe Birtola—CMR Summit Technologies

High Frequency PCB Material Characterization and Simulation
Ryan Satrom—Multitest

MARKET REPORT

As a bonus in this session, you'll get a look at the marketplace for test equipment and test consumables

Market Trends in Test Equipment and Test Consumables
John West—VLSI Research

Building Optimized Test PCB's Starts at the DUT

Joe Birtola
CMR Summit Technologies

2013 BiTS Workshop
March 3 - 6, 2013

An Ideal Signal Trace -

- No Vias (Microstrip)
- No Signal Degradation Influences

Reality is -

- Multiple vias in transmission lines.
- Lengthy Indirect trace paths.
- Narrow resistive higher-loss trace geometries.
- Congested signal launch and termination pin fields.
- Loads / circuitry in trace paths.

Reality May =

- Signal performance below expectations.
- Higher board development cost
- Overall increased cost for Test
- Risk of project and test delays, failure to meet time to market expectations.
- A Grumpy CEO.

YOU CAN HELP!!!

Optimizing Device Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	GND	I/O	I/O	I/O	I/O	SERDES_VCC	VCC	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O
B	I/O	I/O	I/O	SERDES_VCC	SERDES_VCC	I/O	GND	I/O	GND	I/O	I/O	GND	I/O	GND	I/O	I/O	GND	I/O
C	I/O	GND	SERDES_VCC	I/O	SERDES2_TX_N	SERDES2_TX_P	GND	VCC	I/O	SERDES_VCC	GND	I/O	SERDES_VCC	VCC	I/O	VCC	I/O	I/O
D	I/O	I/O	I/O	GND	I/O	VCC	I/O	I/O	I/O	I/O	I/O	VCC	I/O	GND	I/O	GND	I/O	I/O
E	I/O	I/O	VCC	I/O	GND	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	SERDES_VCC	I/O	I/O	I/O	VCC
F	I/O	VCC	I/O	SERDES_VCC	I/O	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCCIO	I/O	I/O	I/O	I/O	GND
G	I/O	I/O	GND	I/O	GND	I/O	I/O	GND	GND	GND	GND	VCC	VCCIO	I/O	I/O	VCC	I/O	I/O
H	I/O	GND	I/O	GND	I/O	VCC	VCC	I/O	GND	GND	GND	VCC	VCCIO	GND	VCC	I/O	GND	I/O
J	I/O	I/O	GND	I/O	I/O	GND	GND	GND	GND	GND	GND	VCC	VCCIO	GND	GND	I/O	I/O	I/O
K	VCC	I/O	I/O	GND	GND	SERDES_VCC	SERDES_VCC	GND	GND	GND	GND	VCC	VCCIO	SERDES_VCC	I/O	I/O	I/O	I/O
L	I/O	GND	GND	I/O	I/O	SERDES4_TX_N	SERDES4TX_P	VCC	GND	GND	GND	VCC	VCCIO	I/O	I/O	SERDES_VCC	I/O	GND
M	GND	I/O	SERDES_VCC	VCC	VCCIO	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCCIO	I/O	I/O	GND	I/O	I/O
N	I/O	I/O	I/O	I/O	SERDES6_RX_N	SERDES6RX_P	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	SERDES_VCC	GND	I/O	I/O	I/O
P	I/O	I/O	GND	I/O	I/O	GND	VCC	I/O	SERDES_VCC	VCC	SERDES4_RX_N	I/O	SERDES4_TX_P	VCC	I/O	I/O	I/O	I/O
R	GND	SERDES_VCC	I/O	I/O	GND	SERDES_VCC	I/O	GND	GND	GND	SERDES4_RX_P	GND	SERDES4_TX_N	GND	I/O	VCC	GND	I/O
T	I/O	SERDES2_RX_P	SERDES2_RX_N	GND	I/O	I/O	GND	I/O	I/O	I/O	TCI	I/O	I/O	I/O	I/O	I/O	I/O	VCC
U	VCC	I/O	SERDES_VCC	I/O	I/O	I/O	I/O	I/O	I/O	SERDES3_RX_N	I/O	SERDES3_TX_P	SERDES_VCC	SERDES5_RX_N	I/O	SERDES5_TX_P	I/O	GND
Y	I/O	VCC	SERDES1_RX_P	SERDES1_RX_N	GND	SERDES1_TX_N	SERDES1_TX_P	GND	I/O	SERDES3_RX_P	GND	SERDES3_TX_N	I/O	SERDES5_RX_P	GND	SERDES5_TX_N	I/O	I/O

LOOP BACK NON-OPTIMIZED PIN PLACEMENT

LOOP BACK OPTIMIZED PIN PLACEMENT

Optimizing Device Pin Assignments

	1	2	3	4	5	6	7	8
A	GND	I/O	I/O	I/O	I/O	SERDES_VCC	VCC	I/O
B	I/O	I/O	I/O	SERDES_VCC	SERDES_VCC	I/O	GND	I/O
C	I/O	GND	SERDES_VCC	I/O	SERDES2_TX_N	SERDES2_TX_P	GND	VCC
D	I/O	I/O	I/O	GND	I/O	VCC	I/O	I/O
E	I/O	I/O	VCC	I/O	GND	VCCIO	VCCIO	VCCIO
F	I/O	VCC	I/O	SERDES_VCC	I/O	VCC	VCC	VCC
G	I/O	I/O	GND	I/O	GND	I/O	I/O	GND
H	I/O	GND	I/O	GND	I/O	VCC	VCC	I/O
J	I/O	I/O	GND	I/O	I/O	GND	GND	GND
K	VCC	I/O	I/O	GND	GND	SERDES_VCC	SERDES_VCC	GND
L	I/O	GND	GND	I/O	I/O	SERDES6_TX_N	SERDES6TX_P	VCC
M	GND	I/O	SERDES_VCC	VCC	VCCIO	VCC	VCC	VCC
N	I/O	I/O	I/O	I/O	SERDES6_RX_N	SERDES6RX_P	VCCIO	VCCIO
P	I/O	I/O	GND	I/O	I/O	GND	VCC	I/O
R	GND	SERDES_VCC	I/O	I/O	GND	SERDES_VCC	I/O	GND
T	I/O	SERDES2_RX_P	SERDES2_RX_N	GND	I/O	I/O	GND	I/O
U	VCC	I/O	SERDES_VCC	I/O	I/O	I/O	I/O	I/O
V	I/O	VCC	SERDES1_RX_P	SERDES1_RX_N	GND	SERDES1_TX_N	SERDES1_TX_P	GND

LOOP BACK NON-OPTIMIZED PIN PLACEMENT

3/2013 Building Optimized Test PCB's Starts at the DUT 7

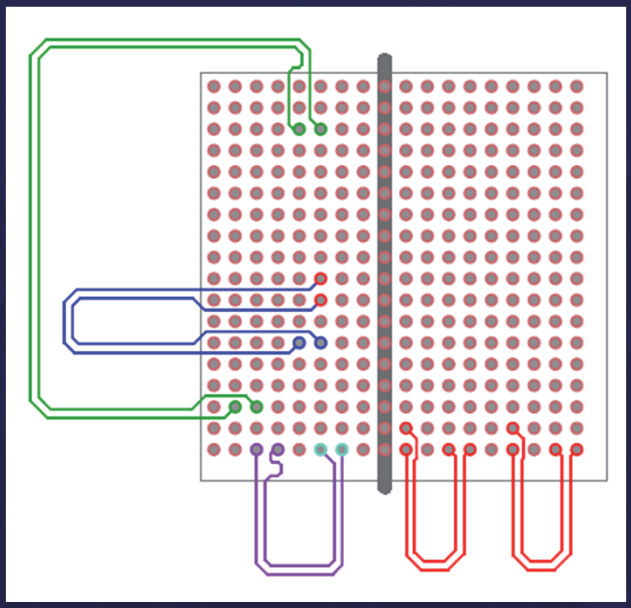
Optimizing Device Pin Assignments

	10	11	12	13	14	15	16	17	18
	I/O	VCC	I/O	I/O	I/O	I/O	VCC	I/O	I/O
	I/O	I/O	GND	I/O	GND	I/O	I/O	GND	I/O
	SERDES_VCC	GND	I/O	SERDES_VCC	VCC	I/O	VCC	I/O	I/O
	I/O	I/O	VCC	GND	GND	I/O	GND	I/O	I/O
CIO	VCCIO	VCCIO	VCCIO	VCCIO	SERDES_VCC	I/O	I/O	I/O	VCC
C	VCC	VCC	VCC	VCCIO	I/O	I/O	I/O	I/O	GND
D	GND	GND	VCC	VCCIO	I/O	I/O	VCC	I/O	I/O
D	GND	GND	VCC	VCCIO	GND	VCC	GND	GND	I/O
D	GND	GND	VCC	VCCIO	GND	GND	I/O	I/O	I/O
D	GND	GND	VCC	VCCIO	SERDES_VCC	I/O	I/O	I/O	I/O
D	GND	GND	VCC	VCCIO	I/O	I/O	SERDES_VCC	I/O	GND
C	VCC	VCC	VCC	VCCIO	I/O	I/O	GND	I/O	I/O
CIO	VCCIO	VCCIO	VCCIO	VCCIO	SERDES_VCC	GND	I/O	I/O	I/O
S_VC	VCC	SERDES4_RX_N	I/O	GND	VCC	I/O	I/O	I/O	I/O
D	GND	SERDES4_RX_P	GND	SERDES4_TX_N	SERDES4_TX_P	I/O	VCC	GND	I/O
	I/O	TCI	I/O	GND	I/O	I/O	I/O	I/O	VCC
	SERDES3_RX_N	I/O	GND	SERDES_VCC	GND	SERDES5_RX_N	GND	I/O	GND
	SERDES3_RX_P	GND	SERDES3_TX_N	SERDES3_TX_P	SERDES_VCC	SERDES5_RX_P	SERDES_VCC	SERDES5_TX_N	SERDES5_TX_P

LOOP BACK OPTIMIZED PIN PLACEMENT

3/2013 Building Optimized Test PCB's Starts at the DUT 8

Optimizing Device Pin Assignments



High-Speed / Critical Signal Pin Placement

- Locate loop-back, differential, RF signal pins at outer edge of package matrix (BGA)
- Assign to a location that promotes equal trace length at board level.
- Locate relative pair pins centrally, avoiding cross matrix loop-back routing.
- Assign these pins at a position that reduces routing through power pin fields.

Optimizing Device Pin Assignments

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O	ASIG	ASIG	I/O	I/O
I/O	I/O	I/O	I/O	I/O	DGND	I/O	DGND	GND	I/O	I/O	AVCC	AGND	AGND	AGND	AVCC	DGND
I/O	I/O	I/O	I/O	I/O	I/O	AVCC	I/O	I/O	DGND	DGND	I/O	ASIG	AGND	ASIG	AGND	I/O
I/O	I/O	I/O	I/O	AVCC	AVCC	ASIG	I/O	I/O	I/O	I/O	DGND	AGND	AGND	AGND	I/O	I/O
I/O	I/O	DGND	I/O	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	ASIG	ASIG	I/O	I/O
I/O	I/O	I/O	I/O	VCCIO	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCCIO	AGND	ASIG	I/O	DGND
I/O	I/O	I/O	DGND	VCCIO	ASIG	DGND	DGND	GND	DGND	DGND	DGND	VCCIO	ASIG	AGND	AVCC	I/O
I/O	I/O	I/O	I/O	ASIG	VCC	ASIG	AGND	GND	DGND	DGND	VCC	VCCIO	AGND	I/O	I/O	I/O
I/O	I/O	I/O	I/O	VCCIO	VCC	DGND	AGND	GND	DGND	DGND	VCC	VCCIO	AGND	I/O	DGND	I/O
I/O	I/O	I/O	DGND	VCCIO	AGND	AGND	DGND	GND	DGND	DGND	VCC	DGND	AVCC	DGND	I/O	I/O
I/O	DGND	DGND	AVCC	AGND	VCC	DGND	DGND	GND	DGND	DGND	DGND	VCCIO	I/O	AVCC	I/O	I/O
I/O	I/O	I/O	I/O	ASIG	AGND	AGND	VCC	VCC	VCC	VCC	VCC	VCCIO	I/O	I/O	I/O	I/O
I/O	I/O	I/O	I/O	AGND	DGND	VCCIO	AGND	VCCIO	VCCIO	VCCIO	VCCIO	VCCIO	DGND	I/O	I/O	I/O
I/O	I/O	I/O	DGND	AGND	AVCC	DGND	ASIG	PRDES_VC	I/O	DGND	I/O	I/O	I/O	I/O	I/O	I/O
I/O	DGND	I/O	DGND	I/O	AGND	AVCC	DGND	GND	DGND	I/O	DGND	I/O	I/O	I/O	DGND	I/O
I/O	I/O	I/O	I/O	DGND	I/O	DGND	I/O	I/O	I/O	DGND	I/O	DGND	I/O	I/O	I/O	DGND
I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O	I/O	I/O	I/O

NON-OPTIMIZED MIXED SIGNAL PIN PLACEMENT

OPTIMIZED MIXED-SIGNAL PIN PLACEMENT

Optimizing Device Pin Assignments

	1	2	3	4	5	6	7	8	9
A	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/
B	I/O	I/O	I/O	I/O	I/O	DGND	I/O	DGND	GN
C	I/O	I/O	I/O	I/O	I/O	I/O	AVCC	I/O	I/
D	I/O	I/O	I/O	I/O	AVCC	AVCC	ASIG	I/O	I/
E	I/O	I/O	DGND	I/O	VCCIO	VCCIO	VCCIO	VCCIO	VC
F	I/O	I/O	I/O	I/O	VCCIO	VCC	VCC	VCC	VC
G	I/O	I/O	I/O	DGND	VCCIO	ASIG	DGND	DGND	GN
H	I/O	I/O	I/O	I/O	ASIG	VCC	ASIG	AGND	GN
J	I/O	I/O	I/O	I/O	VCCIO	VCC	DGND	AGND	GN
K	I/O	I/O	I/O	DGND	VCCIO	AGND	AGND	DGND	GN
L	I/O	DGND	DGND	AVCC	AGND	VCC	DGND	DGND	GN
M	I/O	I/O	I/O	I/O	ASIG	AGND	AGND	VCC	VC
N	I/O	I/O	I/O	I/O	AGND	DGND	VCCIO	AGND	VC
P	I/O	I/O	I/O	DGND	AGND	AVCC	DGND	ASIG	ERDE
R	I/O	DGND	I/O	DGND	I/O	AGND	AVCC	DGND	GN
T	I/O	I/O	I/O	I/O	DGND	I/O	DGND	I/O	I/
U	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O	I/
V	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/

NON-OPTIMIZED MIXED SIGNAL PIN PLACEMENT

Optimizing Device Pin Assignments

	10	11	12	13	14	15	16	17
O	I/O	DGND	I/O	I/O	ASIG	ASIG	I/O	I/O
ND	I/O	I/O	AVCC	AGND	AGND	AGND	AVCC	DGND
O	DGND	DGND	I/O	ASIG	AGND	ASIG	AGND	I/O
O	I/O	I/O	DGND	AGND	AGND	AGND	I/O	I/O
CIO	VCCIO	VCCIO	VCCIO	VCCIO	ASIG	ASIG	I/O	I/O
CC	VCC	VCC	VCC	VCCIO	AGND	ASIG	I/O	DGND
ND	DGND	DGND	DGND	VCCIO	ASIG	AGND	AVCC	I/O
ND	DGND	DGND	VCC	VCCIO	AGND	I/O	I/O	I/O
ND	DGND	DGND	VCC	VCCIO	AGND	I/O	DGND	I/O
ND	DGND	DGND	VCC	DGND	AVCC	DGND	I/O	I/O
ND	DGND	DGND	DGND	VCCIO	I/O	AVCC	I/O	I/O
CC	VCC	VCC	VCC	VCCIO	I/O	I/O	I/O	I/O
CIO	VCCIO	VCCIO	VCCIO	VCCIO	DGND	I/O	I/O	I/O
S_VC	I/O	DGND	I/O	I/O	I/O	I/O	I/O	I/O
ND	DGND	I/O	DGND	I/O	I/O	I/O	DGND	I/O
O	I/O	DGND	I/O	DGND	I/O	I/O	I/O	DGND
O	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O
O	I/O	I/O	DGND	I/O	I/O	I/O	I/O	I/O

OPTIMIZED MIXED-SIGNAL PIN PLACEMENT

Mixed Signal Package Pin Assignment Considerations

- Keep analog ground pins in same area of package array and away from digital ground
- Keep analog signal pins near analog ground pins. *(likewise for digital pins)*
- Keep analog power pins adjacent to analog ground pins for decoupling optimization.

Optimizing Device Pin Assignments

1	2	3	4	5	6	7	8	
	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/
	I/O	I/O	I/O	I/O	DGND	I/O	DGND	GI
I/O	I/O	I/O	I/O	I/O	I/O	AVCC	I/O	I/
I/O	I/O	I/O	I/O	AVCC	AVCC	ASIG	I/O	I/
I/O	I/O	DGND	I/O	VCCIO	VCCIO	VCCIO	VCCIO	VC
I/O	I/O	I/O	I/O	VCCIO	VCC	VCC	VCC	VC
I/O	I/O	I/O	DGND	VCCIO	ASIG	DGND	DGND	GI
I/O	I/O	I/O	I/O	ASIG	VCC	ASIG	AGND	GI
I/O	I/O	I/O	I/O	VCCIO	VCC	DGND	AGND	GI
I/O	I/O	I/O	DGND	VCCIO	AGND	AGND	DGND	GI
I/O	DGND	DGND	AVCC	AGND	VCC	DGND	DGND	GI
I/O	I/O	I/O	I/O	ASIG	AGND	AGND	VCC	VC
I/O	I/O	I/O	I/O	AGND	DGND	VCCIO	AGND	VC
I/O	I/O	I/O	DGND	AGND	AVCC	DGND	ASIG	SERDE
I/O	DGND	I/O	DGND	I/O	AGND	AVCC	DGND	GI
I/O	I/O	I/O	I/O	DGND	I/O	DGND	I/O	I/
I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O	I/
I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/

NON-OPTIMIZED POWER PIN PLACEMENT

3/2013 Building Optimized Test PCB's Starts at the DUT 15

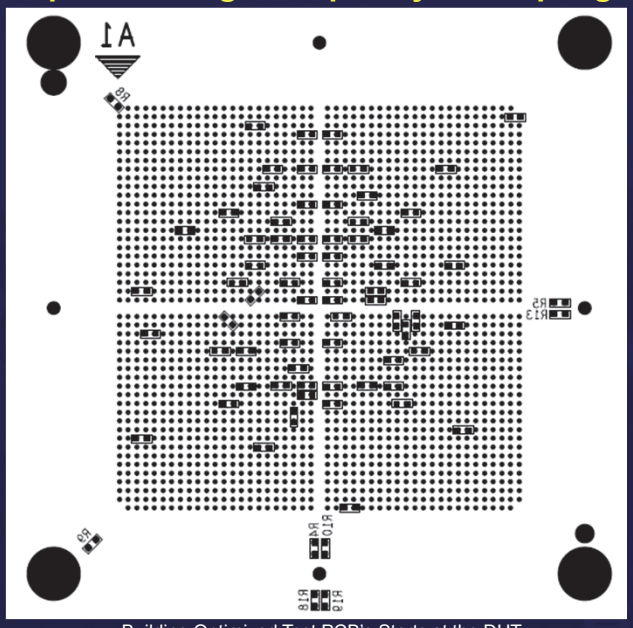
Optimizing Device Pin Assignments

	10	11	12	13	14	15	16	17
	I/O	DGND	I/O	I/O		ASIG	I/O	I/O
D	I/O	I/O	AVCC	AGND		AGND	AVCC	DGND
	I/O	I/O	I/O	ASIG	AGND	ASIG	AGND	I/O
	DGND	DGND	DGND	AGND	AGND	AGND	I/O	I/O
IO	VCCIO	VCCIO	VCCIO	VCCIO	ASIG	ASIG	I/O	I/O
C	VCC	VCC	VCC	VCCIO	AGND	ASIG	I/O	DGND
D	DGND	DGND	DGND	VCCIO	ASIG	AGND	AVCC	I/O
D	DGND	DGND	VCC	VCCIO	AGND	I/O	I/O	I/O
D	DGND	DGND	VCC	VCCIO	AGND	I/O	DGND	I/O
D	DGND	DGND	VCC	DGND	AVCC	DGND	I/O	I/O
D	DGND	DGND	DGND	VCCIO	I/O	AVCC	I/O	I/O
C	VCC	VCC	VCC	VCCIO	DGND	I/O	I/O	I/O
IO	VCCIO	VCCIO	VCCIO	VCCIO	DGND	I/O	I/O	I/O
S_VCC	I/O	DGND	I/O	DGND	I/O	I/O	I/O	I/O
D	DGND	I/O	DGND	I/O	I/O	I/O	DGND	I/O
	I/O	DGND	I/O	DGND	I/O	I/O	I/O	DGND
	I/O	I/O	I/O	I/O	I/O	DGND	I/O	I/O
	I/O	I/O	DGND	I/O	I/O	I/O	I/O	I/O

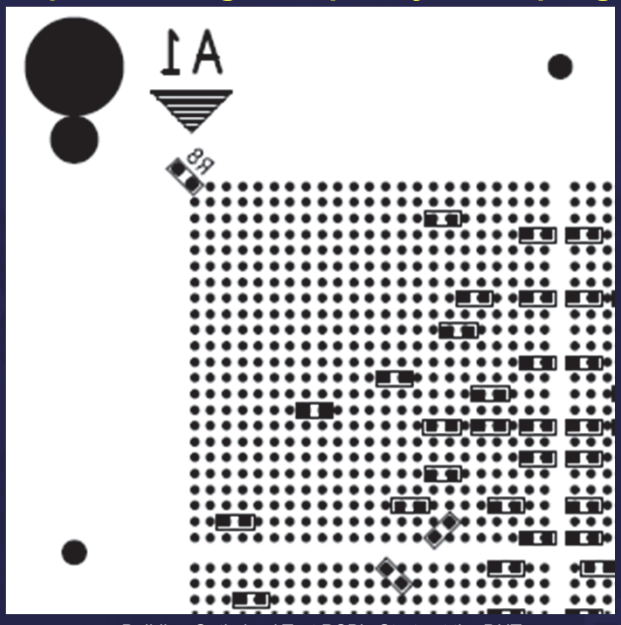
OPTIMIZED POWER PIN PLACEMENT

3/2013 Building Optimized Test PCB's Starts at the DUT 16

Optimized High-Frequency Decoupling



Optimized High-Frequency Decoupling



Optimized Pin Assignment Will Promote…

- Optimized test regimen / board performance.
- Expeditious board development.
- Lower board layer count and cost.
- A happy CEO!