FOURTEENTH ANNUAL
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Burn-in & Test Strategies Workshop™

Archive
Session 2

# TEST TOOLING MADE EASY

Whether you're testing conventional packages like QFNs and BGAs, or emerging 2.5D and 3D packages, you're only as successful as your test floor equipment. This session's presenters span the spectrum of tooling issues beginning with a method for 3D package handling through the integration of complex technologies. Next, you'll learn how to prevent semiconductor test system coolant leakage by implementing a hazardous warning system. Operator error in manual test handlers comes under scrutiny thanks to a failure analysis investigation in QFN packages. Lastly, we take a look at cost saving through homogenous spring pin tip implementation in a high volume manufacturing (HVM) environment.

## 3D Package Handling: A Simple Case of Integrating Complex Technologies

Zain Abadin—Advantest America, Inc.

## Innovative Way to Prevent Semiconductor Test Tester Coolant Leakage with Hazardous Warning System

Yee Wei Tiang—Intel (Malaysia)

This Paper

## Die-Cracking Failure Analysis of QFN Packages in Manual Test Handler

M.P. Divakar, PhD—Stack Design Automation

## Cost Saving Through Homogenous Spring Loaded Pin Tip Implementation in High Volume Manufacturing (HVM) Environment

Chin Siang (David) Chew, Nithya Nandhan Subramaniam—Intel Technology
Chin Chien Tee—Interconnect Devices, Inc.

# Die-Cracking Failure Analysis of QFN Packages in Manual Test Handler

**MP Divakar, PhD**
**Stack Design Automation**

2013 BiTS Workshop
March 3 - 6, 2013

## Content

## Background

- A series of failures were observed on a Digital Controller product packaged in 6x6mm 40-lead QFN during High Temperature Operating Life (HTOL) qualification tests run at two test houses, A (TH-A) and B (TH-B).
- Test program began at TH-B and then moved to TH-A.
- Failure modes ranged from loss of continuity to intermittency and opens.
- Packaged parts were tested on a Teradyne J750 mixed signal tester with manual handler.
- All parts were functional prior to the HTOL tests.

## Background

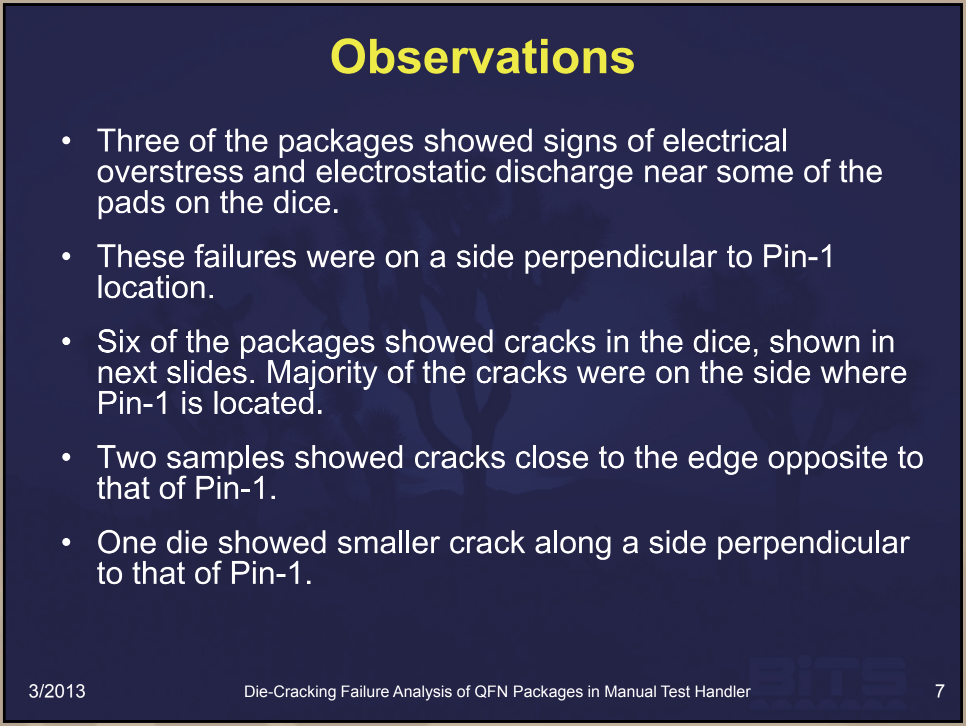
- A total of failed 9 parts (6 at TH-A and 3 at TH-B) were found;
- One sample was found failing functional tests prior to HTOL.
- A summary of failed parts is shown in the following table.
- Failures were first observed at TH-B. Due to this and other reasons, the test program was moved to TH-A.

## Summary of Failed Packages

| HTOL Start Date | Location | Lot # | Sample Size | # of Fails | Failure Symptom | Failure Cause | Tot # of Cracked Die |
|---|---|---|---|---|---|---|---|
| 20-May-xx | TH-A | E10007 | 40 Units 1 Lot | 3 1 at 84, 1 at 174 & 1 at 500 Hr | 2 Functional, 1 Continuity | EOS, ESD & Si Damage | None |
| 20-May-xx | TH-A | E10002 | 40 Units 1 Lot | 7 all at 212 Hr | Continuity | 1 EOS & 6 Die Crack | 6 |
| 19-Aug-xx | TH-B | E10010 | 80 1 Lot | 1, at 168 Hr | Functional | Die Crack Pkg#269 | 1 |
| 19-Aug-xx | TH-B | E10009 | 79 1 Lot | 1 at 500 Hr | Functional | Die Crack Pkg#101 | 1 |
| 19-Aug-xx | TH-B | E10008 | 80 1 Lot | NONE | Functional | Die Crack Pkg#11 | 1 |

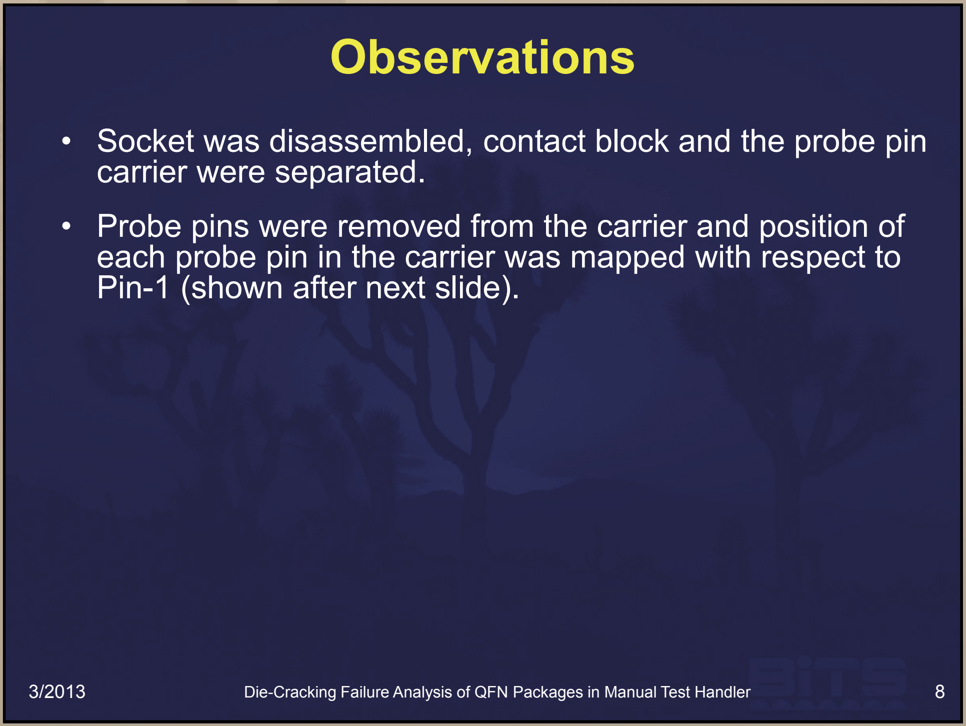
## Observations

- All failed packages were examined visually, using X-Ray imaging and Confocal Scanning Acoustic Microscopy (CSAM). These yielded no discernable clues to the cause/s of failure.
- External visual examination at 100X magnification showed that some of the package pads at the bottom had indentation marks left by the top side of probe pins from the socket.
- The indentations were biased more toward the side with Pin-1 location than the other sides.
- Further, some indentation marks were also seen in the middle of the package paddle.
- All packages were de-lidded for closer inspection.



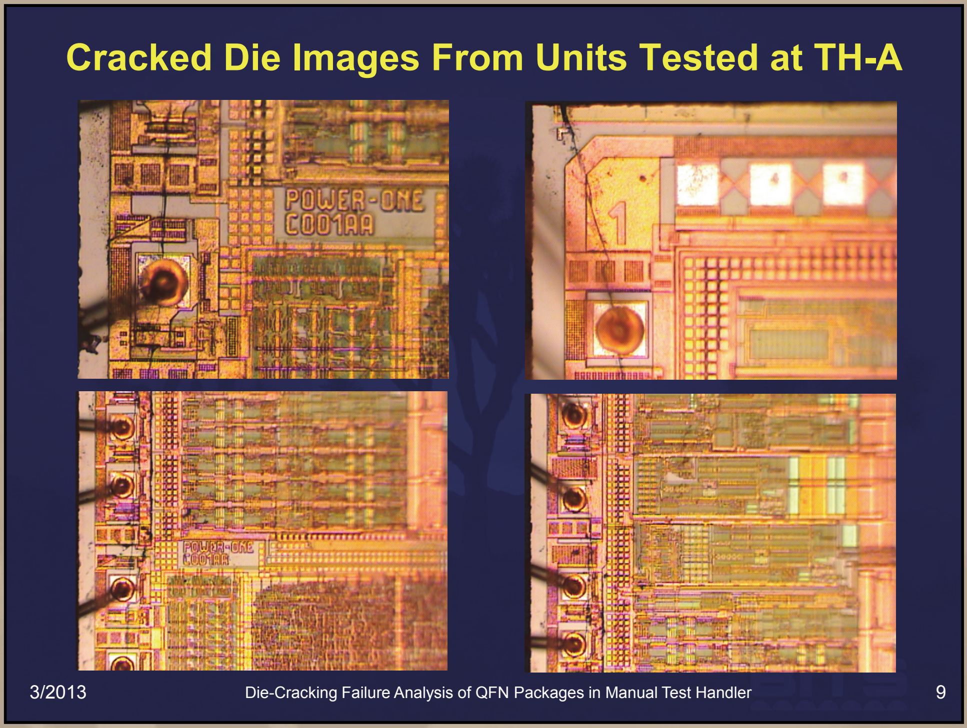
## Observations

- Three of the packages showed signs of electrical overstress and electrostatic discharge near some of the pads on the dice.
- These failures were on a side perpendicular to Pin-1 location.
- Six of the packages showed cracks in the dice, shown in next slides. Majority of the cracks were on the side where Pin-1 is located.
- Two samples showed cracks close to the edge opposite to that of Pin-1.
- One die showed smaller crack along a side perpendicular to that of Pin-1.



## Observations

- Socket was disassembled, contact block and the probe pin carrier were separated.
- Probe pins were removed from the carrier and position of each probe pin in the carrier was mapped with respect to Pin-1 (shown after next slide).



## Cracked Die Images From Units Tested at TH-A

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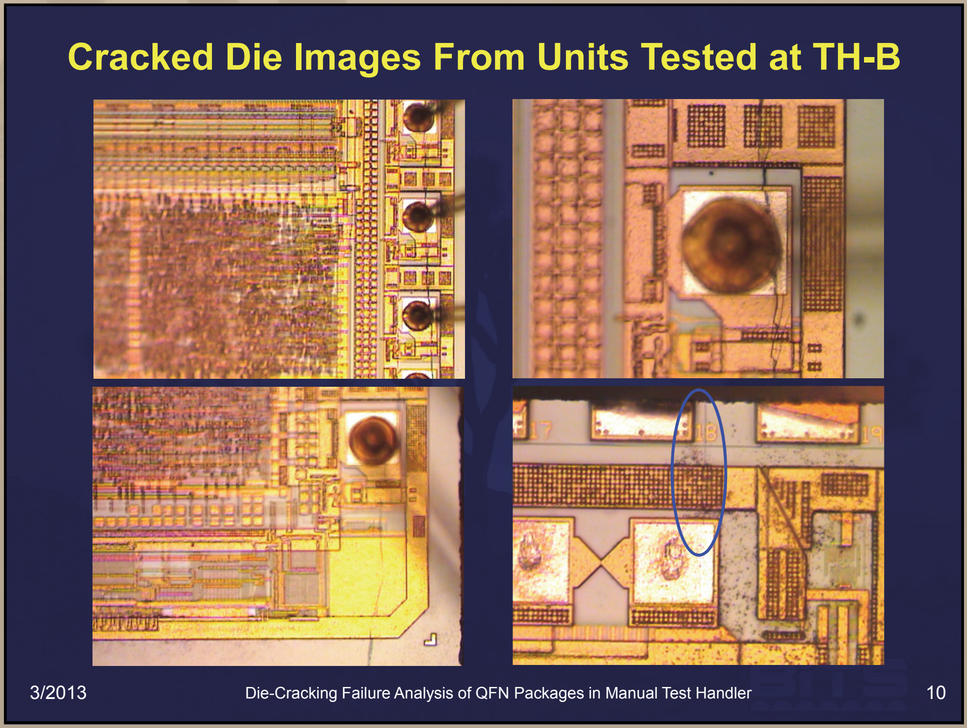

## Cracked Die Images From Units Tested at TH-B

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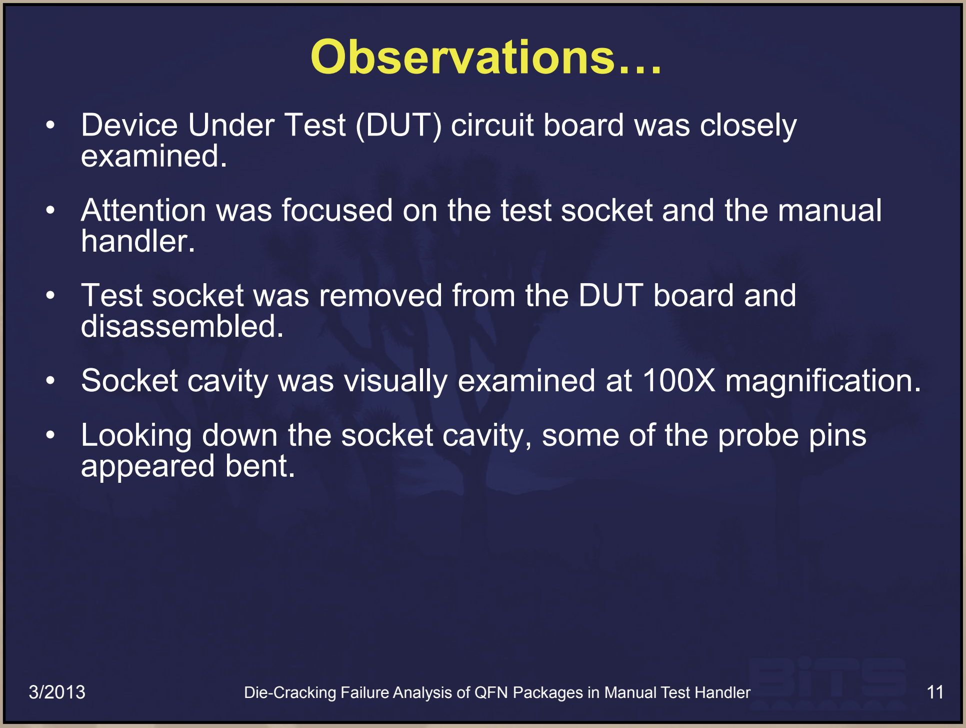
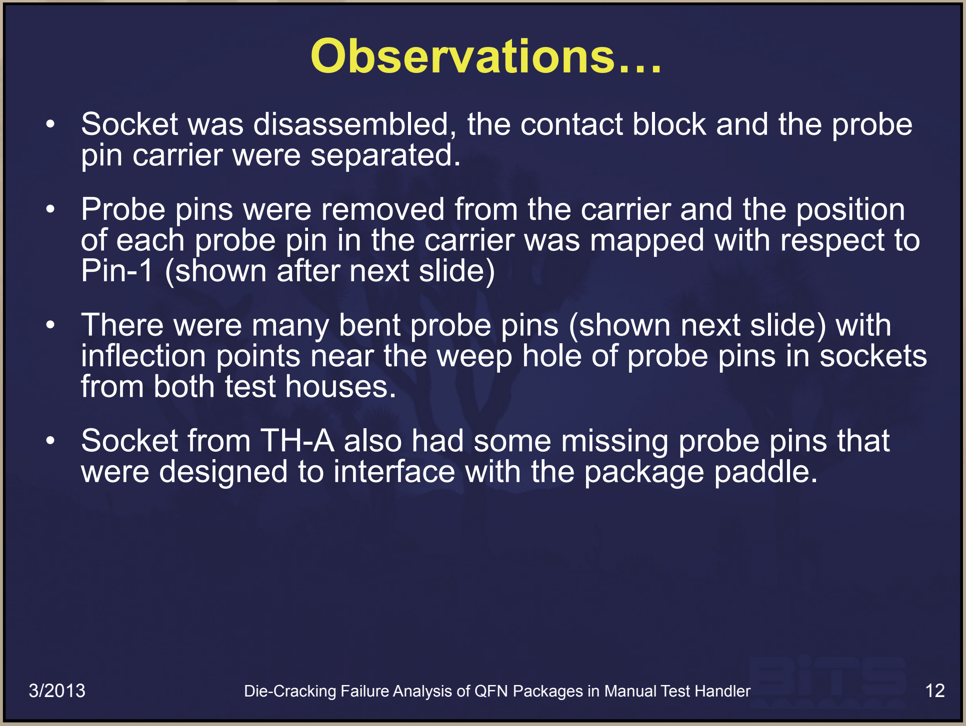


# Observations…

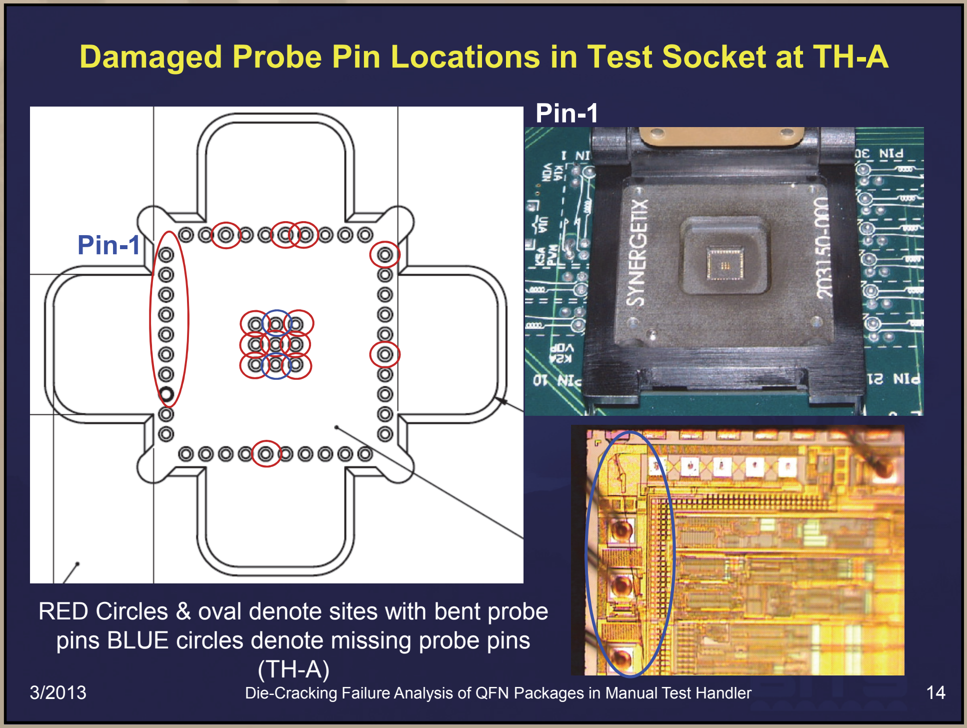
- Device Under Test (DUT) circuit board was closely examined.
- Attention was focused on the test socket and the manual handler.
- Test socket was removed from the DUT board and disassembled.
- Socket cavity was visually examined at 100X magnification.
- Looking down the socket cavity, some of the probe pins appeared bent.



# Observations…

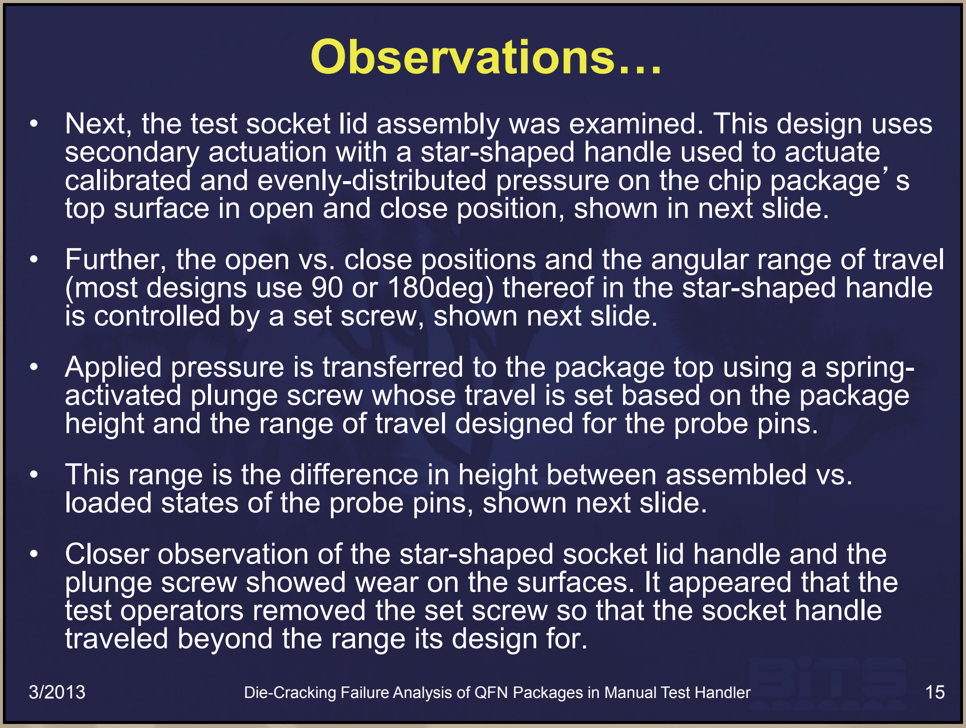
- Socket was disassembled, the contact block and the probe pin carrier were separated.
- Probe pins were removed from the carrier and the position of each probe pin in the carrier was mapped with respect to Pin-1 (shown after next slide)
- There were many bent probe pins (shown next slide) with inflection points near the weep hole of probe pins in sockets from both test houses.
- Socket from TH-A also had some missing probe pins that were designed to interface with the package paddle.

## Observed Damage in Probe Pins from TH-B Sockets



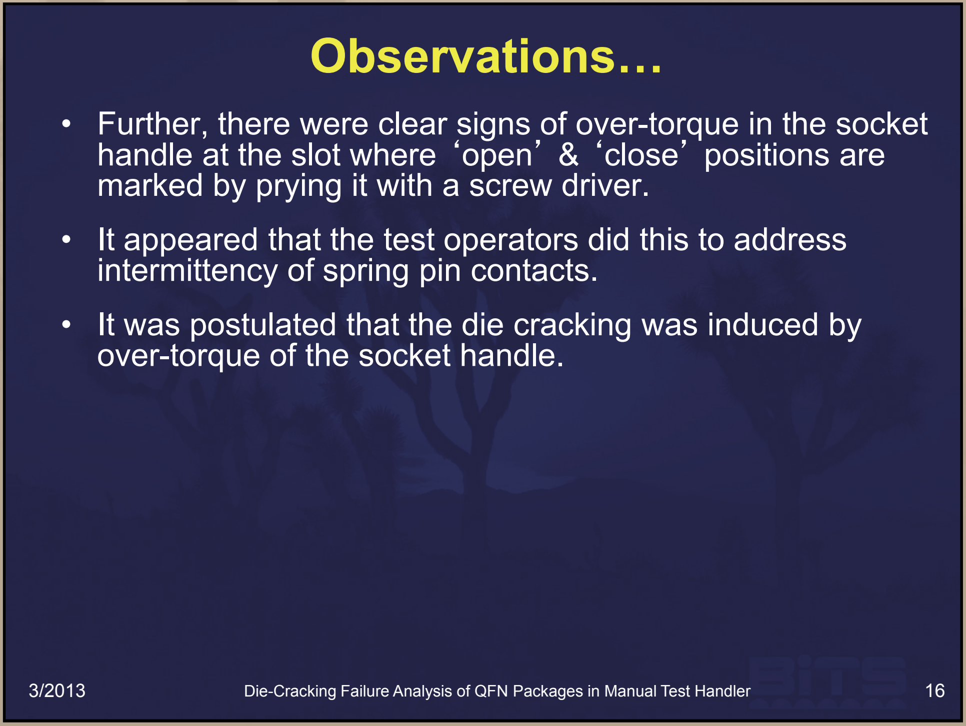
## Damaged Probe Pin Locations in Test Socket at TH-A

RED Circles & oval denote sites with bent probe pins BLUE circles denote missing probe pins (TH-A)



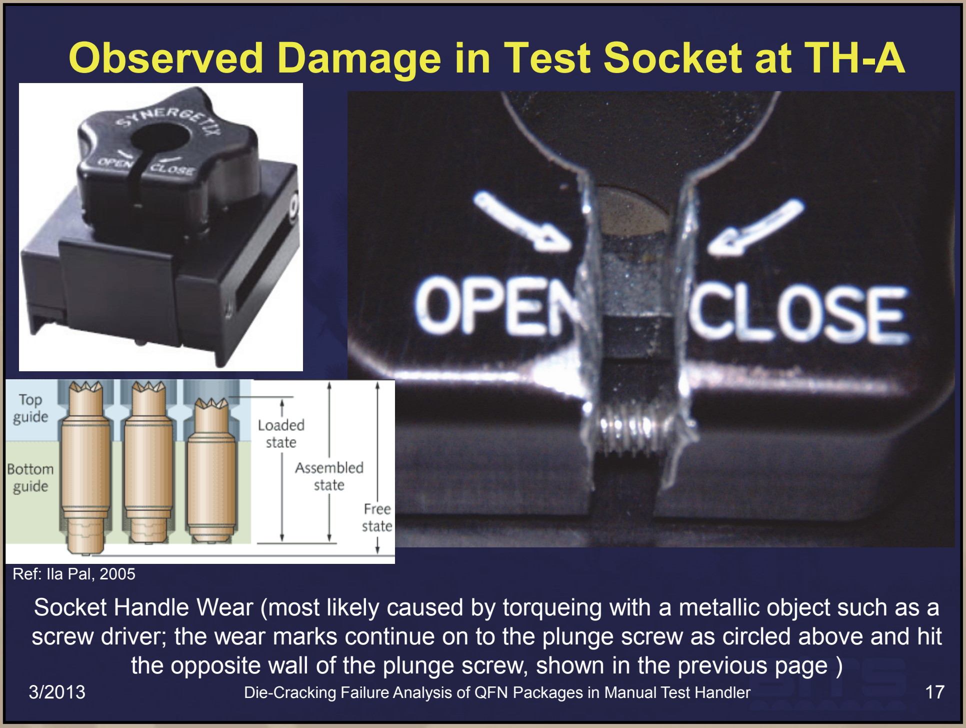
## Observations…

- Next, the test socket lid assembly was examined. This design uses secondary actuation with a star-shaped handle used to actuate calibrated and evenly-distributed pressure on the chip package's top surface in open and close position, shown in next slide.
- Further, the open vs. close positions and the angular range of travel (most designs use 90 or 180deg) thereof in the star-shaped handle is controlled by a set screw, shown next slide.
- Applied pressure is transferred to the package top using a spring-activated plunge screw whose travel is set based on the package height and the range of travel designed for the probe pins.
- This range is the difference in height between assembled vs. loaded states of the probe pins, shown next slide.
- Closer observation of the star-shaped socket lid handle and the plunge screw showed wear on the surfaces. It appeared that the test operators removed the set screw so that the socket handle traveled beyond the range its design for.



## Observations…

- Further, there were clear signs of over-torque in the socket handle at the slot where 'open' & 'close' positions are marked by prying it with a screw driver.
- It appeared that the test operators did this to address intermittency of spring pin contacts.
- It was postulated that the die cracking was induced by over-torque of the socket handle.



## Observed Damage in Test Socket at TH-A

Ref: Ila Pal, 2005

Socket Handle Wear (most likely caused by torqueing with a metallic object such as a screw driver; the wear marks continue on to the plunge screw as circled above and hit the opposite wall of the plunge screw, shown in the previous page )

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## Observed Damage in Test Socket at TH-A

Missing Set Screw Reinstalled

Plunge Screw Wear

Plunge Screw Wear (caused by torqueing with a metallic object, possibly a screw driver!)

Socket Plunge Screw Wear and Missing Set Screw

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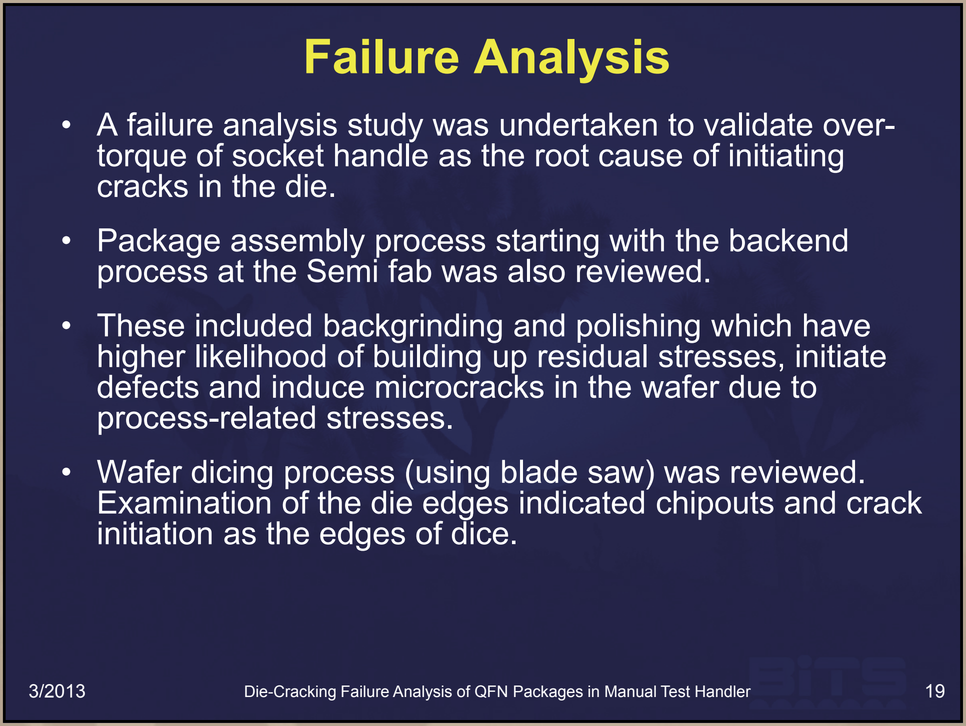
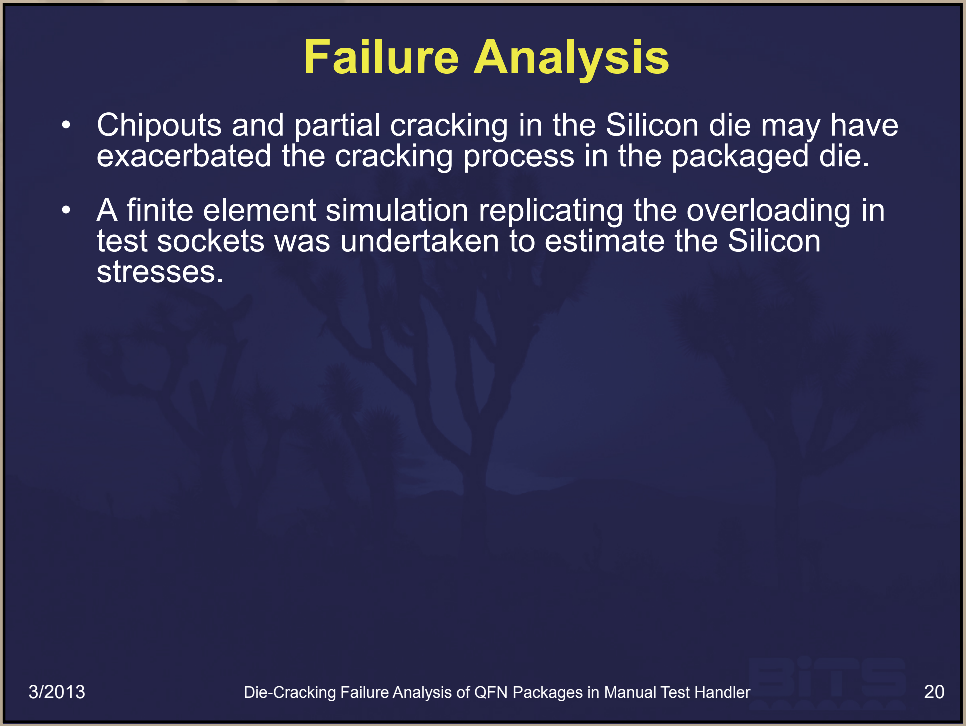


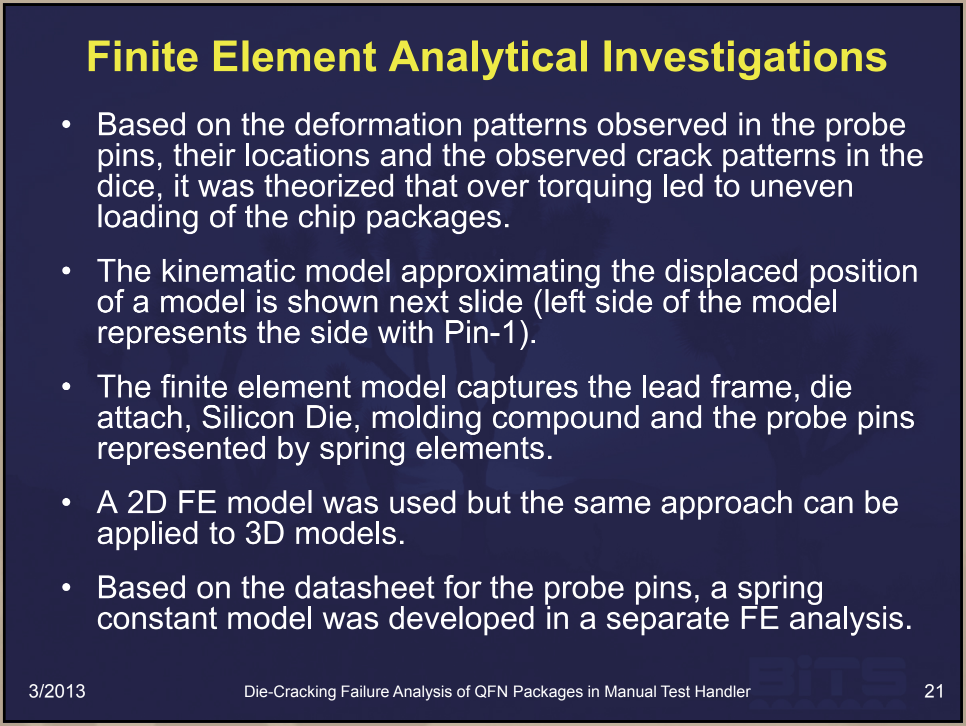
## Failure Analysis

- A failure analysis study was undertaken to validate over-torque of socket handle as the root cause of initiating cracks in the die.
- Package assembly process starting with the backend process at the Semi fab was also reviewed.
- These included backgrinding and polishing which have higher likelihood of building up residual stresses, initiate defects and induce microcracks in the wafer due to process-related stresses.
- Wafer dicing process (using blade saw) was reviewed. Examination of the die edges indicated chipouts and crack initiation as the edges of dice.



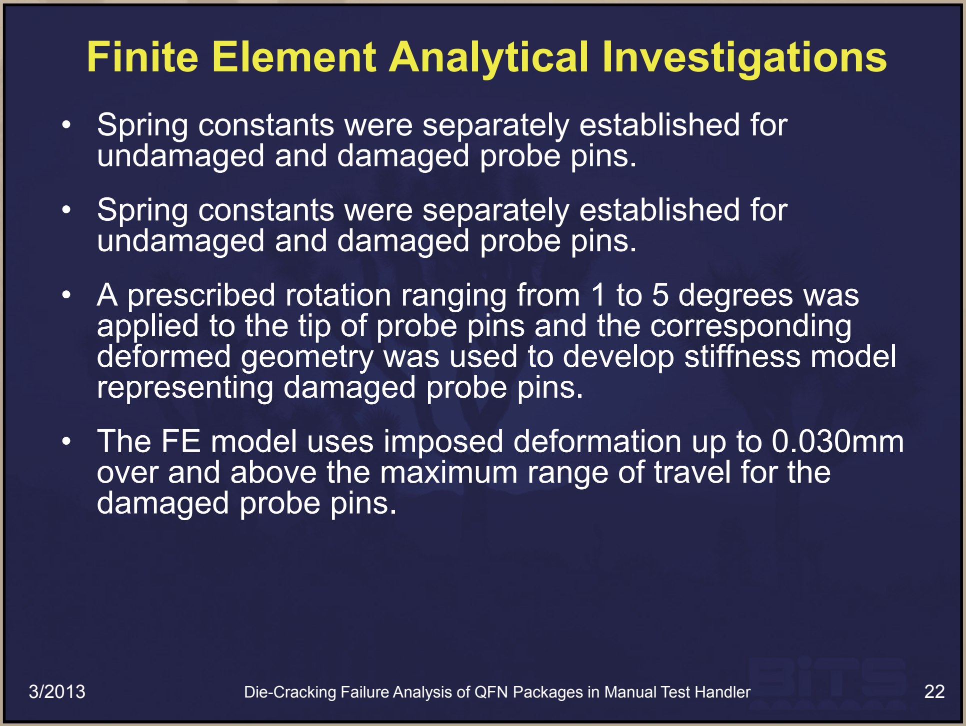
## Failure Analysis

- Chipouts and partial cracking in the Silicon die may have exacerbated the cracking process in the packaged die.
- A finite element simulation replicating the overloading in test sockets was undertaken to estimate the Silicon stresses.



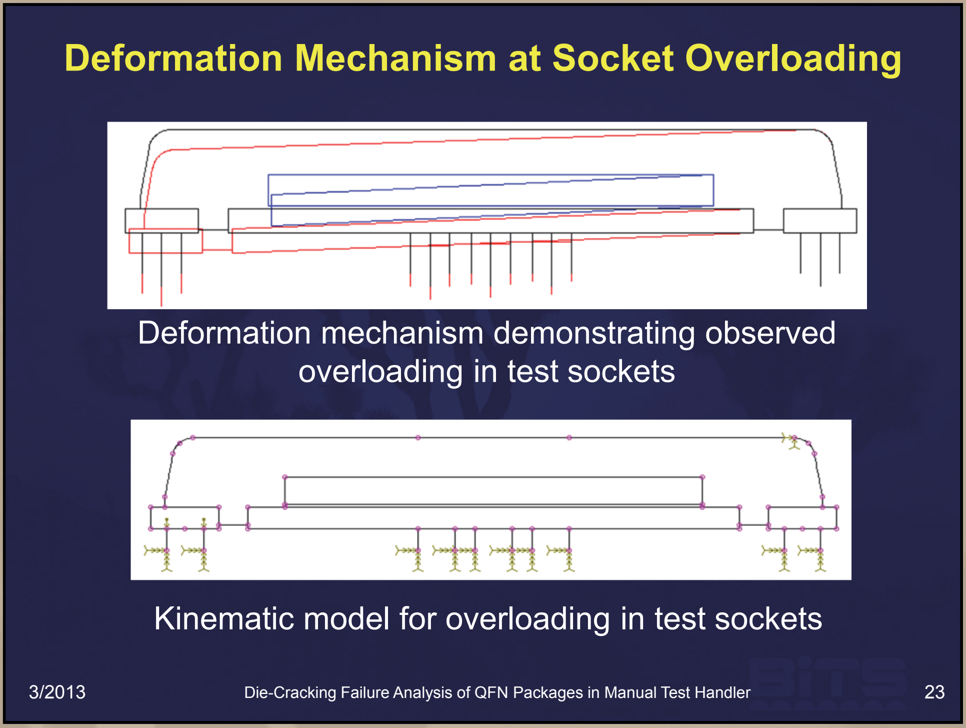
## Finite Element Analytical Investigations

- Based on the deformation patterns observed in the probe pins, their locations and the observed crack patterns in the dice, it was theorized that over torquing led to uneven loading of the chip packages.
- The kinematic model approximating the displaced position of a model is shown next slide (left side of the model represents the side with Pin-1).
- The finite element model captures the lead frame, die attach, Silicon Die, molding compound and the probe pins represented by spring elements.
- A 2D FE model was used but the same approach can be applied to 3D models.
- Based on the datasheet for the probe pins, a spring constant model was developed in a separate FE analysis.



## Finite Element Analytical Investigations

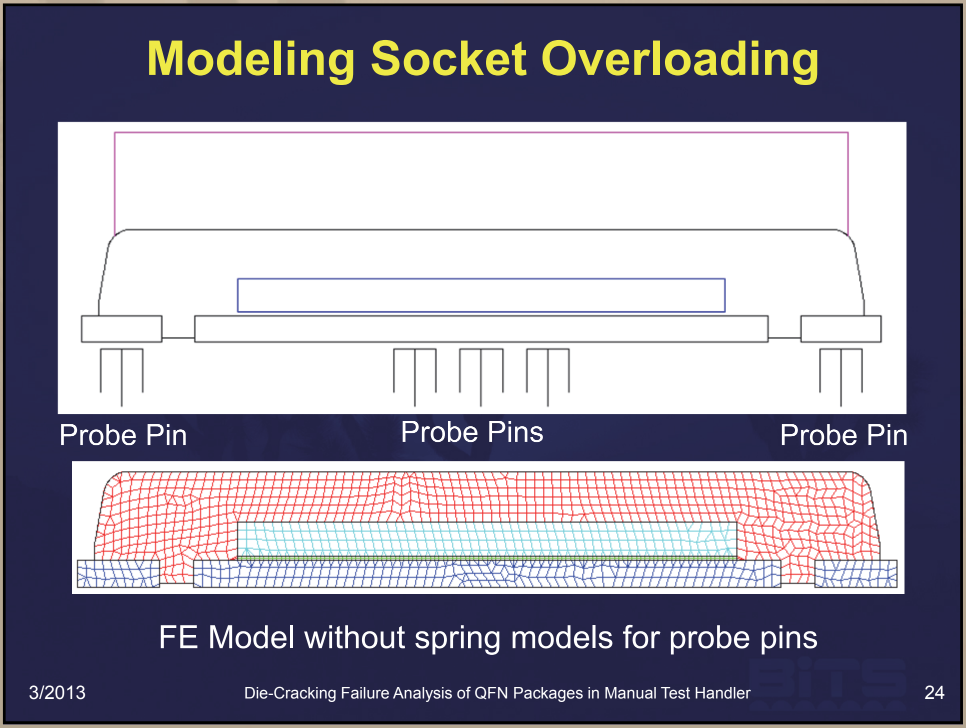
- Spring constants were separately established for undamaged and damaged probe pins.
- Spring constants were separately established for undamaged and damaged probe pins.
- A prescribed rotation ranging from 1 to 5 degrees was applied to the tip of probe pins and the corresponding deformed geometry was used to develop stiffness model representing damaged probe pins.
- The FE model uses imposed deformation up to 0.030mm over and above the maximum range of travel for the damaged probe pins.



## Deformation Mechanism at Socket Overloading

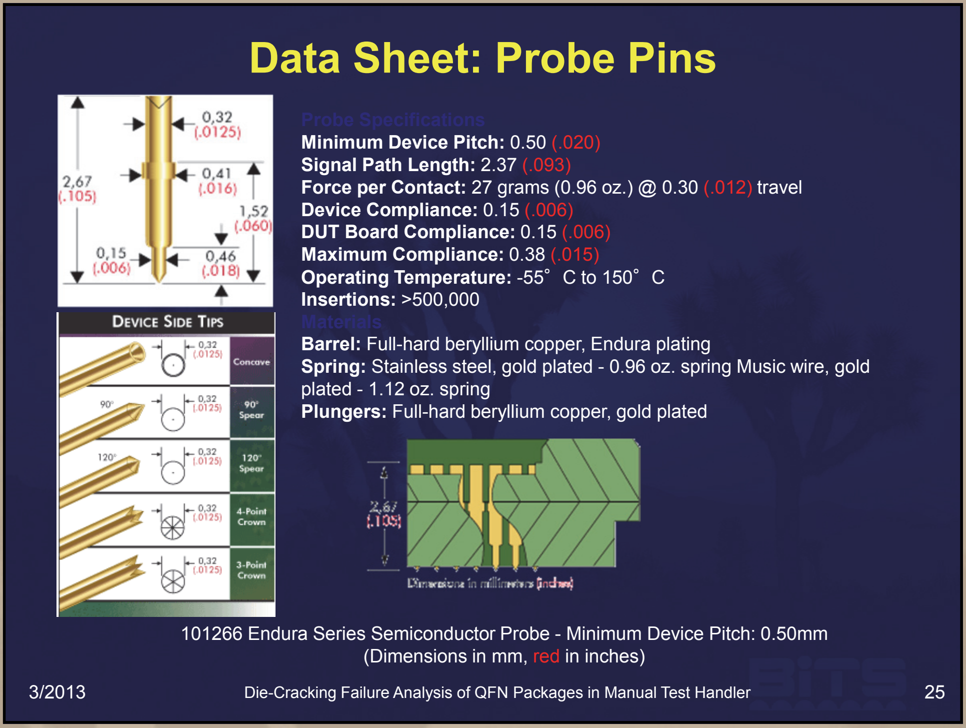
Deformation mechanism demonstrating observed overloading in test sockets

Kinematic model for overloading in test sockets



## Modeling Socket Overloading

FE Model without spring models for probe pins



## Data Sheet: Probe Pins

Probe Specifications

**Minimum Device Pitch:** 0.50 (.020)
**Signal Path Length:** 2.37 (.093)
**Force per Contact:** 27 grams (0.96 oz.) @ 0.30 (.012) travel
**Device Compliance:** 0.15 (.006)
**DUT Board Compliance:** 0.15 (.006)
**Maximum Compliance:** 0.38 (.015)
**Operating Temperature:** -55˚ C to 150˚ C
**Insertions:** >500,000

Materials

**Barrel:** Full-hard beryllium copper, Endura plating
**Spring:** Stainless steel, gold plated - 0.96 oz. spring Music wire, gold plated - 1.12 oz. spring
**Plungers:** Full-hard beryllium copper, gold plated

101266 Endura Series Semiconductor Probe - Minimum Device Pitch: 0.50mm
(Dimensions in mm, red in inches)

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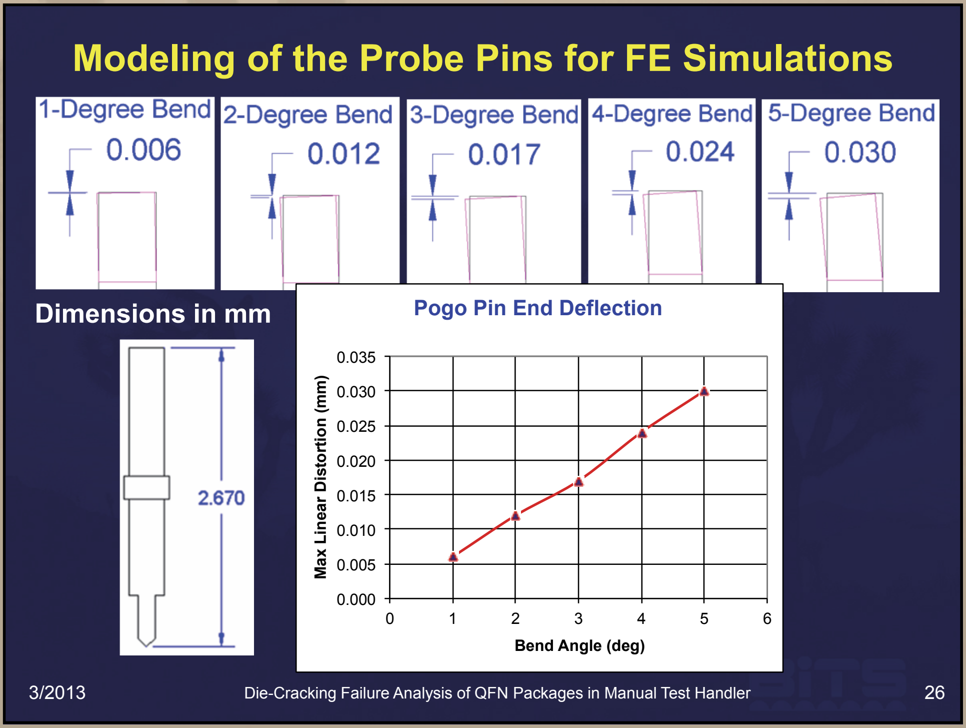

## Modeling of the Probe Pins for FE Simulations

Dimensions in mm

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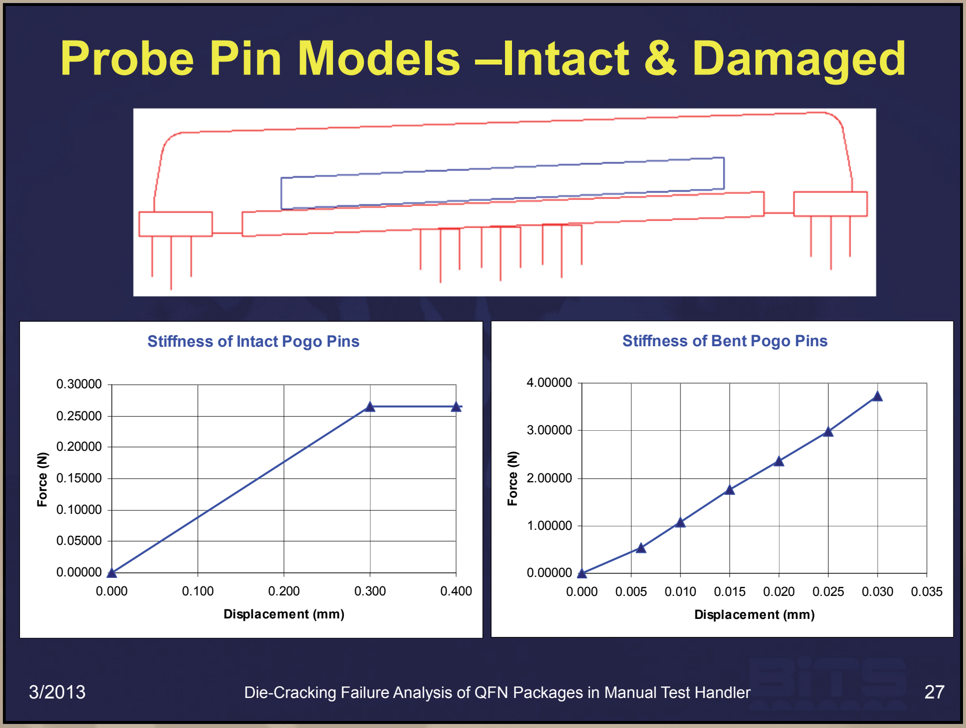


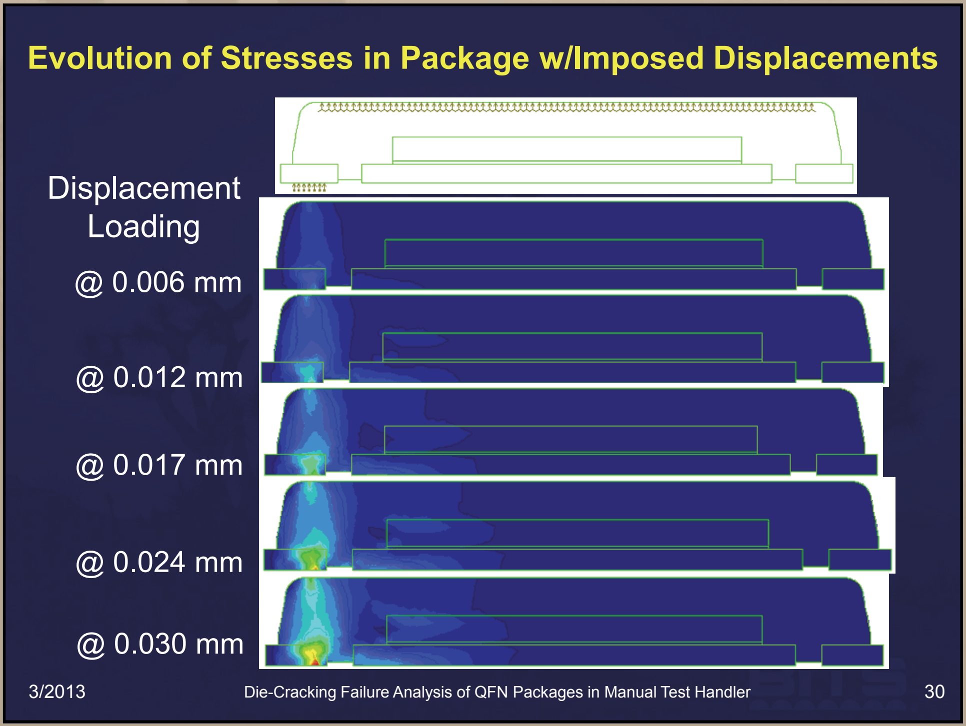
## Probe Pin Models –Intact & Damaged

## Findings

- As shown in the next two slides, the evolution of stresses due to increasing displacements on probe pins show von Mises stresses in Silicon die exceeding 600MPa.
- When imposed displacements were applied in the middle (package paddle) area in addition to the left edge the stress magnitudes were even higher.
- Research investigations documented so far clearly indicate a very significant drop in fracture strength of Silicon due to dicing chipouts, divots and backgrind-induced defects.
- In some cases the drop in fracture strength can be as high as 50%.

## Findings

- Appropriate compression of the probe pins is critical in the design of test sockets for successful and repeatable probe pin performance.
- A change in process incorporating double-saw for wafer dicing and the corresponding DOE run at Amkor has revealed no chipouts and dicing cracks.
- Subsequent HTOL tests and corrected sockets showed no failures.



## Evolution of Stresses in Package w/Imposed Displacements

Displacement Loading

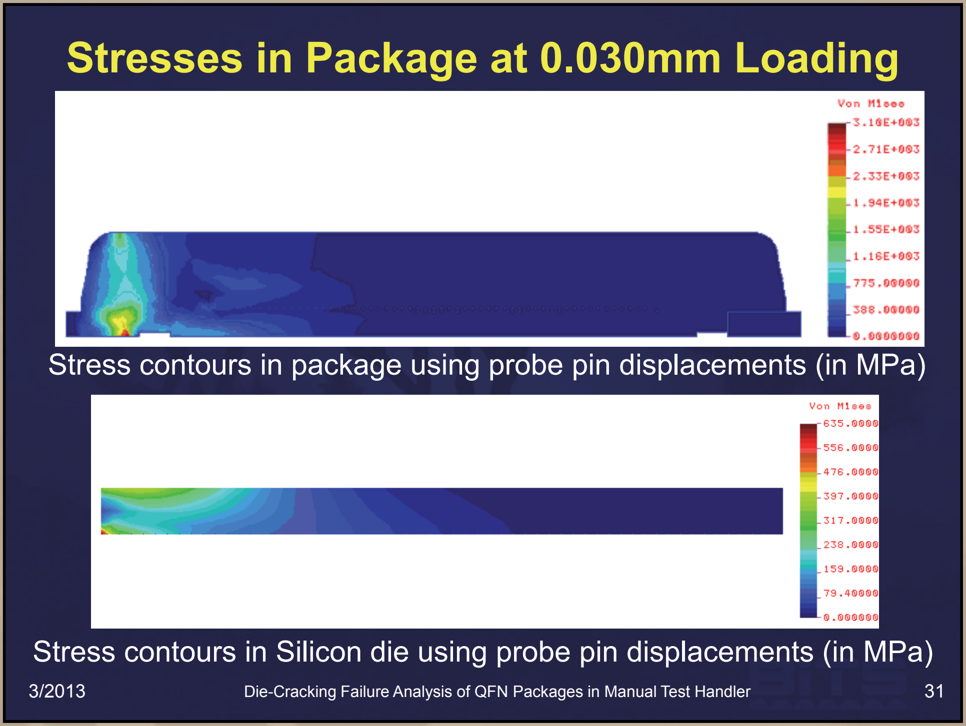
@ 0.006 mm

@ 0.012 mm

@ 0.017 mm

@ 0.024 mm

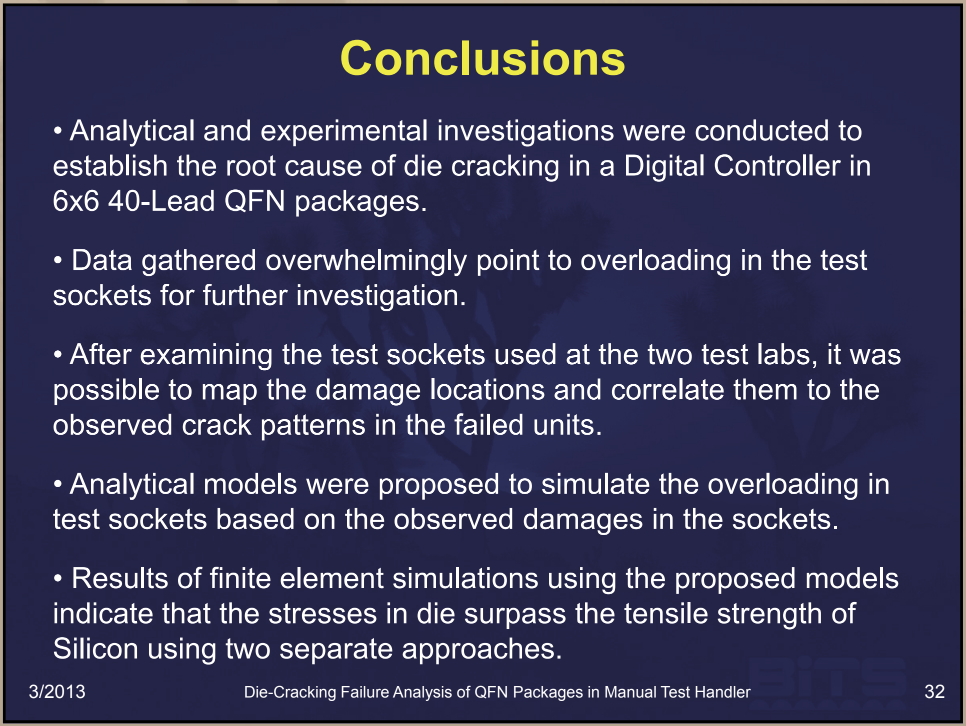
@ 0.030 mm



## Stresses in Package at 0.030mm Loading

Stress contours in package using probe pin displacements (in MPa)

Stress contours in Silicon die using probe pin displacements (in MPa)



## Conclusions

- Analytical and experimental investigations were conducted to establish the root cause of die cracking in a Digital Controller in 6x6 40-Lead QFN packages.
- Data gathered overwhelmingly point to overloading in the test sockets for further investigation.
- After examining the test sockets used at the two test labs, it was possible to map the damage locations and correlate them to the observed crack patterns in the failed units.
- Analytical models were proposed to simulate the overloading in test sockets based on the observed damages in the sockets.
- Results of finite element simulations using the proposed models indicate that the stresses in die surpass the tensile strength of Silicon using two separate approaches.

## References

- Desmond Y.R. Chong, W.E. Lee, B.K. Lim, John H.L. Pang & T.H. Low. “Mechanical Characterization In Failure Strength Of Silicon Dice,” IEE 2004 Inter Society Conference on Thermal Phenomena, pp 203-210.
- J.D. Wu , C.Y. Huang, C.C. Liao. “Fracture strength characterization and failure analysis of silicon dies,” Microelectronics Reliability 43 (2003), pp 269–277.
- C. Bohm, T. Hauck, A. Juritza & W.H. Müllertest. “Weibull Statistics of Silicon Die Fracture,” 2004 Electronics Packaging Technology Conference, pp 782-786.

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