FOURTEENTH ANNUAL BiTS 2013 Burn-in & Test Strategies Workshop

Archive
Session 2

TEST TOOLING MADE EASY

Whether you're testing conventional packages like QFNs and BGAs, or emerging 2.5D and 3D packages, you're only as successful as your test floor equipment. This session's presenters span the spectrum of tooling issues beginning with a method for 3D package handling through the integration of complex technologies. Next, you'll learn how to prevent semiconductor test system coolant leakage by implementing a hazardous warning system. Operator error in manual test handlers comes under scrutiny thanks to a failure analysis investigation in QFN packages. Lastly, we take a look at cost saving through homogenous spring pin tip implementation in a high volume manufacturing (HVM) environment.

3D Package Handling: A Simple Case of Integrating Complex Technologies
Zain Abadin—Advantest America, Inc.

Innovative Way to Prevent Semiconductor Test Tester Coolant Leakage with Hazardous Warning System
Yee Wei Tiang—Intel (Malaysia)

Die-Cracking Failure Analysis of QFN Packages in Manual Test Handler
M.P. Divakar, PhD—Stack Design Automation

Cost Saving Through Homogenous Spring Loaded Pin Tip Implementation in High Volume Manufacturing (HVM) Environment
Chin Siang (David) Chew, Nithya Nandhan Subramaniam—Intel Technology
Chin Chien Tee—Interconnect Devices, Inc.

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3D Package Handling

A Simple Case of Integrating Complex Technologies

Zain Abadin
Advantest America, Inc.

2013 BiTS Workshop
March 3-6, 2013

ADVANTEST

Contents

- Scope and Basic Assumptions
- 3D Package Trends
- 3D Package Handling Technologies
- 2/2.5/3D Package Handler
- Conclusions

Scope and Basic Assumptions

Scope
- Final Test
- 3D packages include 2D, 2.5D, 3D Singulated, SiP/PoP

Basic Assumptions
- New handling solutions
  - Improve or maintain current yield
  - Deliver competitive CoT
  - Suitable for HVM environment

Unit Cost = (Depreciation + Operating Cost) / Throughput (Yield Applied)

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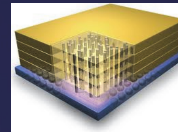
3D Package Trends

Market Forces



- Higher Performance
- More Features
- Smaller, Thinner
- Lower Cost

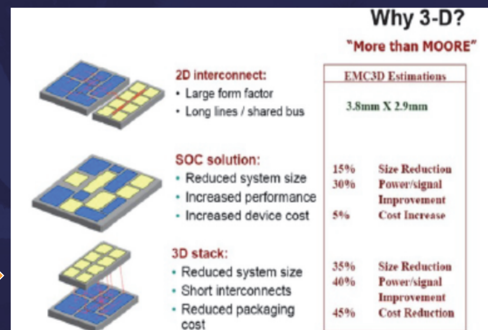


Figure AP16 Driving Forces for 3D Integration

Sources: Micron Technology, EE Times, ITRS 2009 Assembly, Google Images

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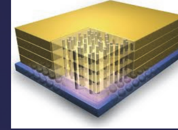
3D Package Trends

Market Forces



- Higher Performance
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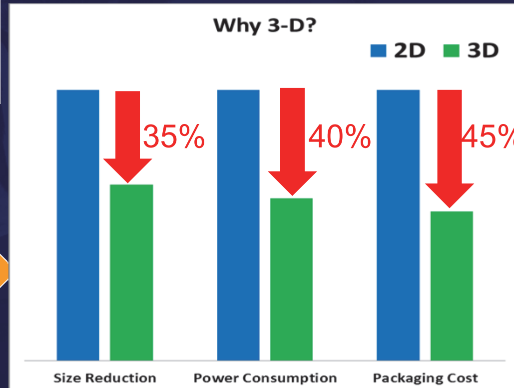

Sources: Micron Technology, EE Times, ITRS 2009 Assembly, Google Images

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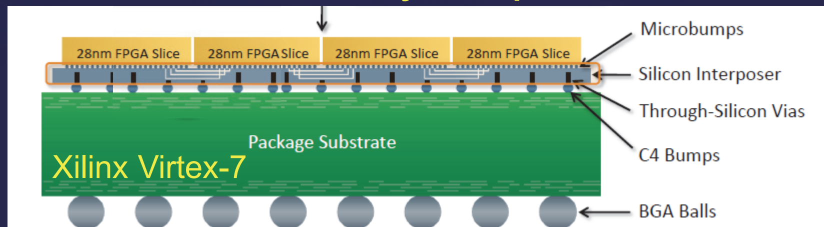
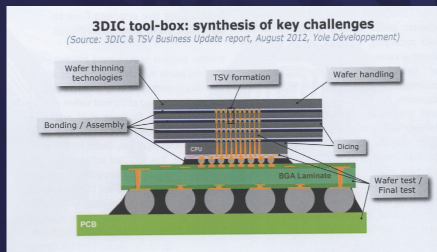
3D Package Trends

Industry Examples



Source: Xilinx 3-D_Artichectures



Source: Amkor Technologies, Inc

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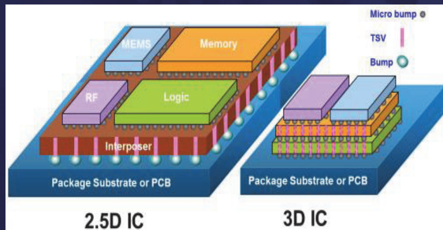
3D Package Trends
Packaging Trends and Handler Functions

Handler's Main Functions: Transfer, Align, Thermal Control



Source: Daniel Nenni, Semiconductor Packaging (3D IC) Emerging As Innovation Enabler!

Packaging Trends
- Finer Ball Pitch
- Heterogeneous Stacked Devices
- High Power Dissipation
- Thinner Packages
- High Pin Count

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3D Package Trends
Test Nodes

No industry consensus on test nodes yet

Niehls Bohr

"Prediction is very difficult, especially about the future."

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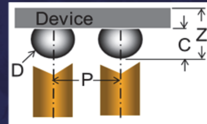
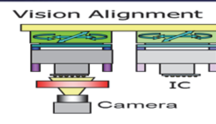
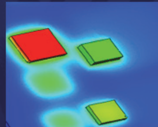
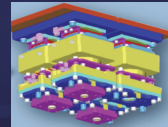
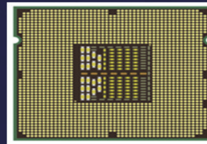
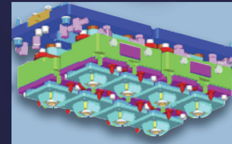
3D Package Handling Technologies

Packaging Trends and Handler Requirements

	Packaging Trends	Handler Requirements
Finer Ball Pitch		
Power Dissipation Heterogeneous Stacked Devices		
Thinner Packages High Pin Count		

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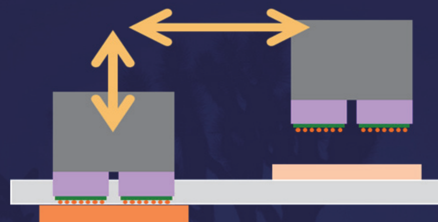
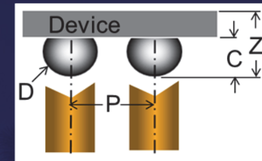
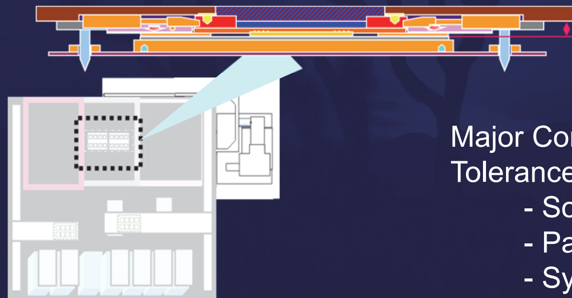
3D Package Handling: Alignment

Tolerance Stack Up @ Contact







Major Contributors to
Tolerance Stack up @ the Contact
- Socket
- Package
- System Positioning

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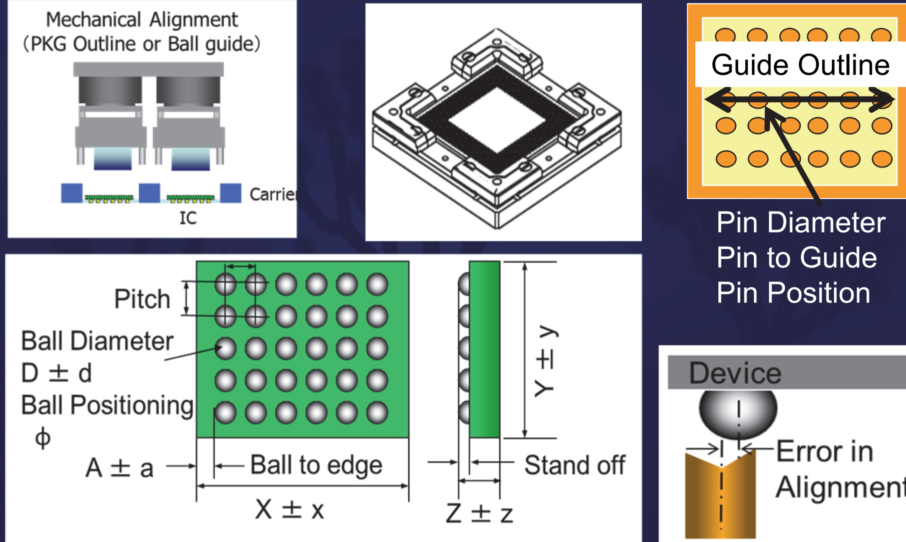
3D Package Handling: Alignment
Mechanical Alignment Method
Mechanical Alignment
(PKG Outline or Ball guide)
Carrier
IC
Guide Outline
Pin Diameter
Pin to Guide
Pin Position
Pitch
Ball Diameter
D ± d
Ball Positioning
ϕ
A ± a
Ball to edge
X ± x
Y ± y
Stand off
Z ± z
Device
Error in
Alignment
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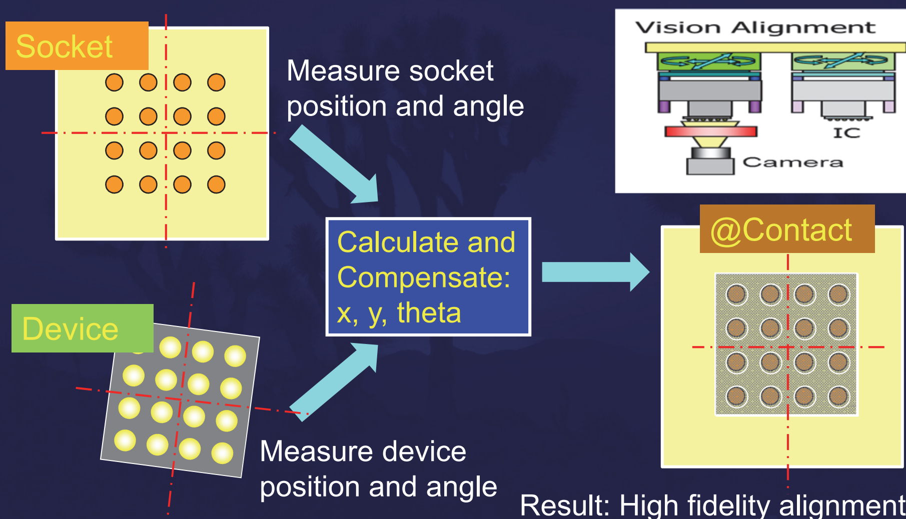
3D Package Handling - A Simple Case of Integrating Complex Technologies
11


3D Package Handling: Alignment
Vision Alignment Method
Socket
Measure socket
position and angle
Vision Alignment
IC
Camera
Calculate and
Compensate:
x, y, theta
@Contact
Device
Measure device
position and angle
Result: High fidelity alignment
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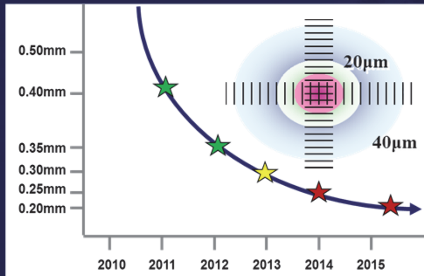
12

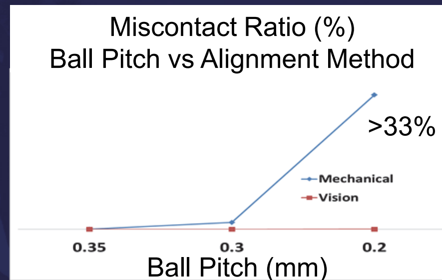
3D Package Handling: Alignment

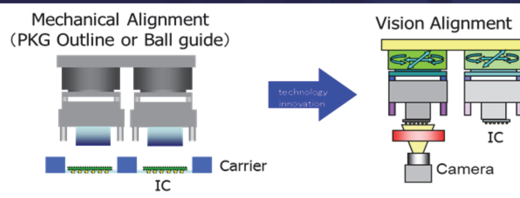
Trend towards Vision Alignment

Pitch Trend



Alignment Simulation





Benefits:

Improved yield

Lower CoT

3D Package Handling: Thermal

Current Handler Segmentation and Trends

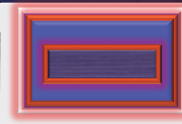
Memory Handler

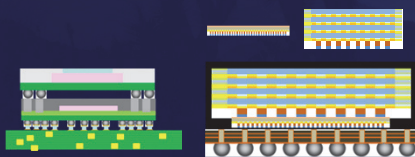
Chamber, LN2 for low temp

SoC Handler

For Low Power Dissipation:

For High Power Dissipation: ATC, PTC



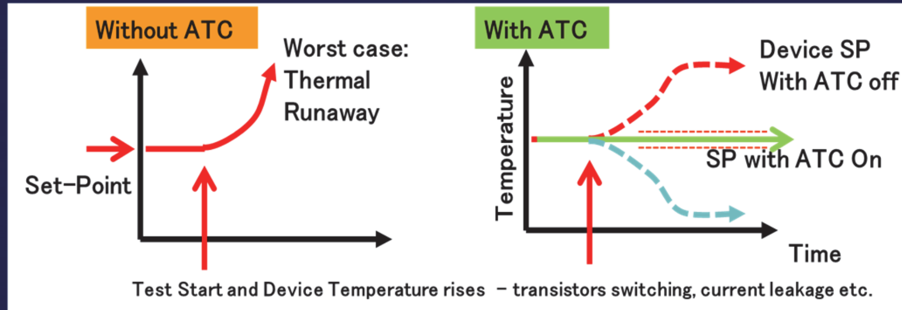


Trends:

- Segmentation disappearing
- Higher Power
- Higher Power Density
- Thinning Packages

3D Package Handling: Thermal

ATC Method and Performance



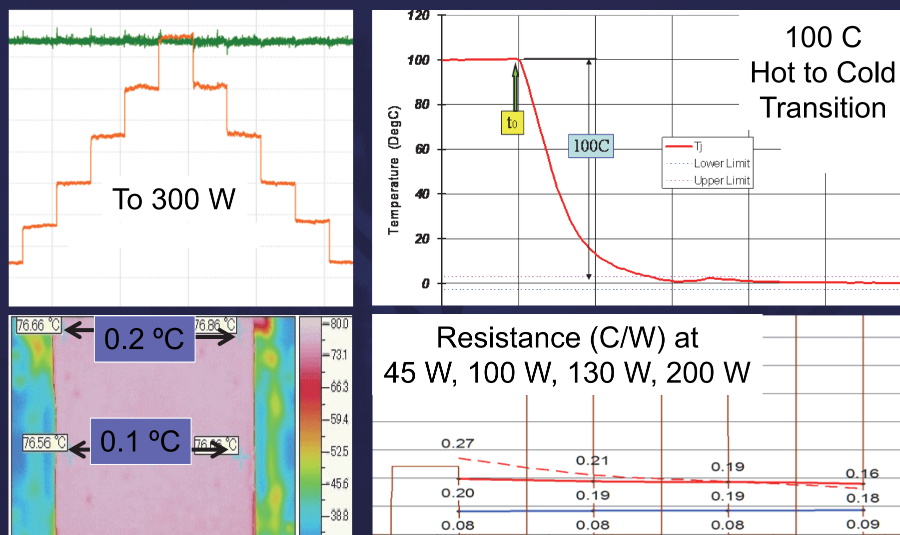
Watch for:

- Thermal Mass
  - Temp. Transition
  - Tj max/min,
  - Time to Guard Band
- Induced Gradient
- SP vs. Power/Power Density
- ATC+PTC in same system

3/2013 3D Package Handling - A Simple Case of Integrating Complex Technologies 15

3D Package Handling: Thermal

ATC Performance Examples

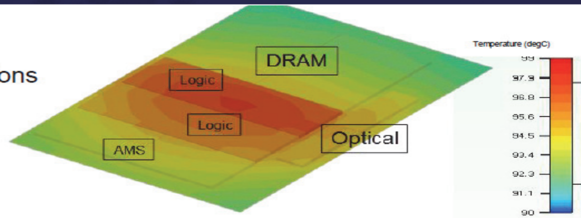


3/2013 3D Package Handling - A Simple Case of Integrating Complex Technologies 16

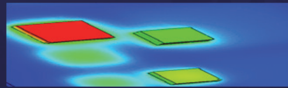
3D Package Handling: Thermal

Thermal Trend and ATC Need

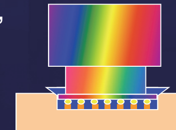
Power and Power Density



Power Density > 50 W/cm2



Benefits:
- Improved yield,
- Lower TT

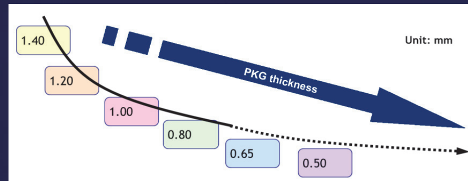


Lower CoT, Higher ASP

3/2013 3D Package Handling - A Simple Case of Integrating Complex Technologies 17

3D Package Handling: Thin

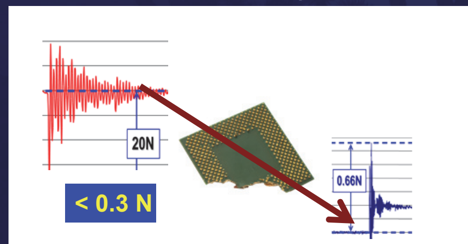
Impact Force and Force Centroid



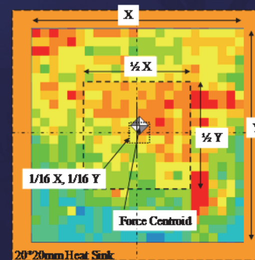
Source: Bernd Appelt: The Thin Package Challenge Never Ends, Semicon West 2012

Smart Phones < 8 mm
Tablets < 10 mm
Notebooks < 20 mm
Wearable Electronics

Impact Force During Transfer



Force Centroid



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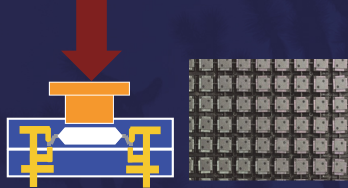
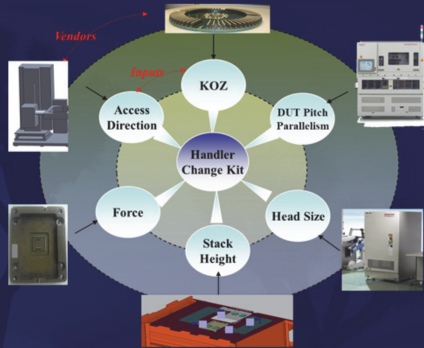
3D Package Handling: Pin Count

Insertion Force

#Pin * F/Pin

512/1024





Rapid Increase in Pin Count
Trend towards Higher Parallelism
Translate into Higher Insertion Force, >4000 kg

Collaboration: Lowering F/Pin will be great help

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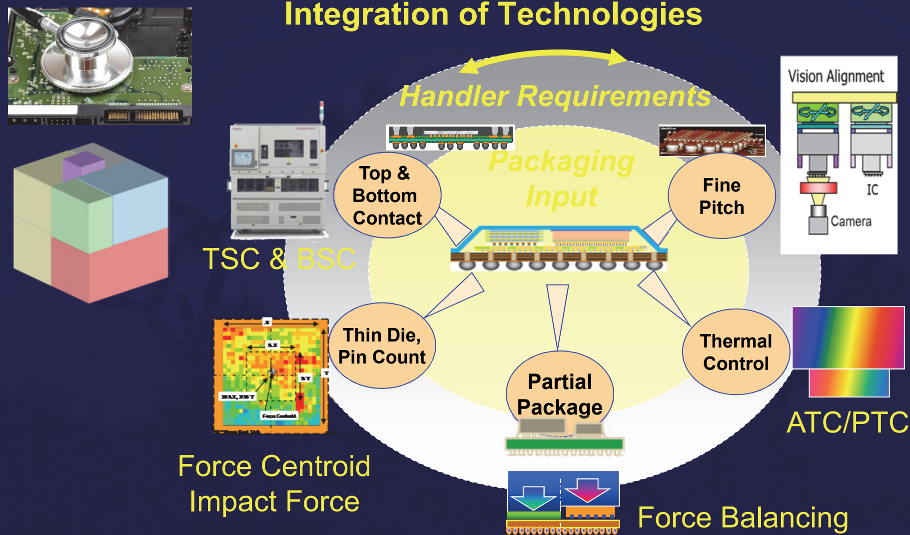
2/2.5/3D Package Handler

Integration of Technologies



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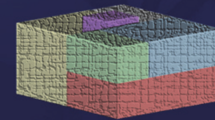
Summary

- 2.5D in production
- Packages becoming more complex, existing advanced technologies capable of handling each handling requirement - separately
- 3D package handling need an integration of ATC/PTC + VA and STH technologies
- Upgradeable solution needed to accommodate future migration to finer pitch, higher parallelism and higher pin count



– One correction:

3D Package Handling:
A Complex Case of Integrating Simple Technologies

3/2013 3D Package Handling - A Simple Case of Integrating Complex Technologies 21