STREAMLINING OPERATIONS

Test operations, generally considered costly, yet necessary, add value to device manufacturing when optimized for efficiency. This session offers a variety of approaches that promise high yields, lean manufacturing, maximized performance at minimal costs, and optimized production times. The first paper discusses a method of incorporating multidimensional Monte Carlo analysis simulation with known design parameters to focus manufacturing improvement efforts and maximize alignment performance while minimizing costs. Presented next is a method for redefining test tooling design rules to gain process margin and prevent substrate chipping caused by test handler misalignment. Zero-cost, software based, virtual tool checkers that bring the whole production area towards a manufacturing LEAN direction is then discussed. Wrapping things up is a paper on a screwless socket and dual pin testing concept said to greatly enhance the robustness and efficiency of IC testing.

Improving Socket Alignment Performance Using Monte Carlo Analysis Techniques and Manufacturing Controls

Daniel DelVecchio, Dustin Allison—Interconnect Devices Incorporated

This Paper

Tooling Stack-up Process Margin Improvement

Mook Koon Wong, Boon Hor Phee—Intel Malaysia

Zero Cost Virtual Tool Checker

Seong Guan Ooi—Intel Technology Sdn. Bhd.

Enablers for Robust & Fast Online Trouble-shooting for High Parallelism Testing

Benedict Loh—Infineon Technologies
Kohei Hironaka—NHK Spring Co. Ltd.
Michelle Ng—TestPro

Tooling Stack-up Process Margin Improvement

Wong Mook Koon
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2013 BiTS Workshop
March 3 - 6, 2013

Agenda

- Background
- Problem statement
- Current Status and Technical Challenges
- Solution
- Check Result
- Summary
- Acknowledgement

Background

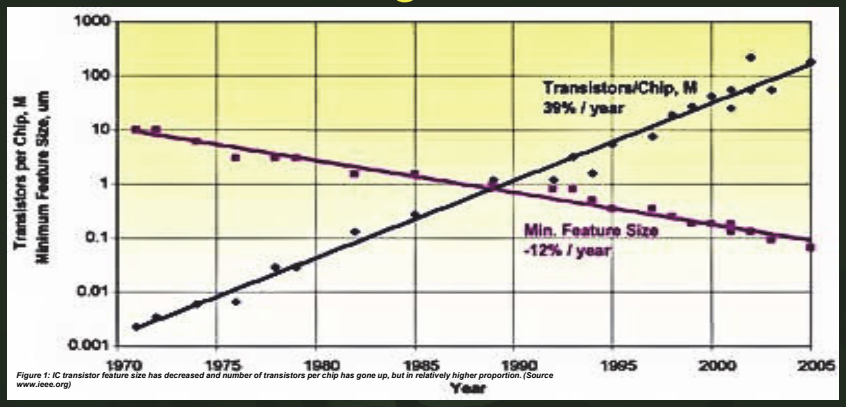


Figure 1: IC transistor feature size has decreased and number of transistors per chip has gone up, but in relatively higher proportion. (Source www.ieee.org)

- IC transistor size reducing ~12% per year
- Number of transistors increasing, ~39% per year
- Package IO increasing
  - Land/Ball Pitch need to be reduced to control package

Problem statement

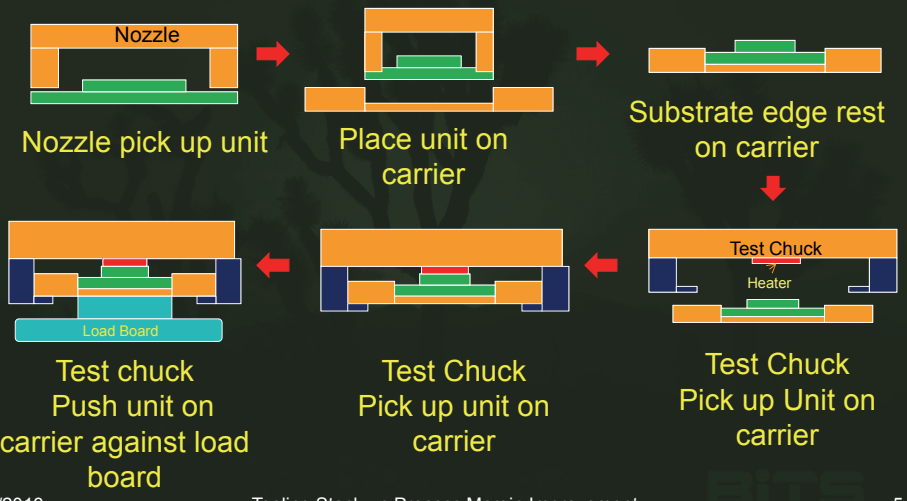
- Semiconductor process challenges: Number of IO increased and Ball Pitch reduced

  Impacts:

  1. Unit handling method inside handler at final test
     - Thermal contact resistance challenges at different M/C
     - Substrate real estate & Keep out Zone challenges (top and bottom side)
  2. Test tooling stack up process margin and test interface challenges
     - Low yield issue (Fail open test)
     - Quality issue (mechanical defects)
     - Tooling wear out

Current Status & Technical Challenge

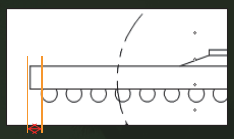
- Unit handling method inside handler at final test - Substrate edge handling



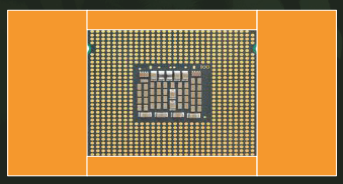
Current Status & Technical Challenge

- Inefficiency of substrate edge handling methodology
  - Substrate size, land & ball pitch to substrate edge reduced
  - Impact: space constrain at unit holding edge

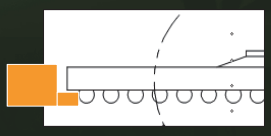
Substrate edge rest on carrier



SRO/Solder Ball distance to substrate perimeter decreased



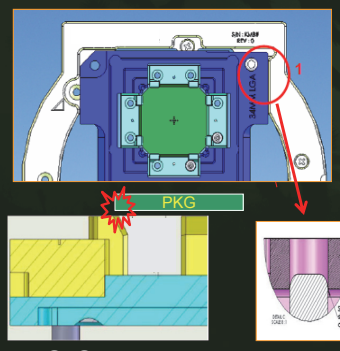
Bottom View Substrate edge rest on carrier



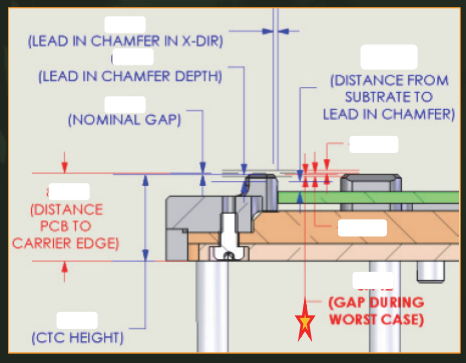
Solder Ball/Land Pad hit on Carrier edge

Current Status & Technical Challenge

- Test tooling stack up process margin and test interface challenges
  - Chuck Z-motion inside handler may cause package bottom surface to hit test socket's Anvil Surface under worst case condition

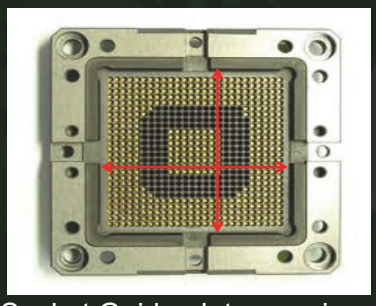


TS Side view

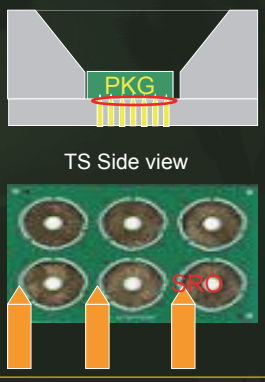


Current Status & Technical Challenge

- Test tooling stack up process margin and test interface challenges (cont'd)
  - Guide plate opening too loose, Test results fail open due to Pogo pin not contacting SRO



Socket Guide plate opening

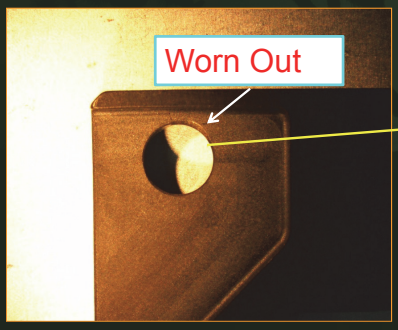


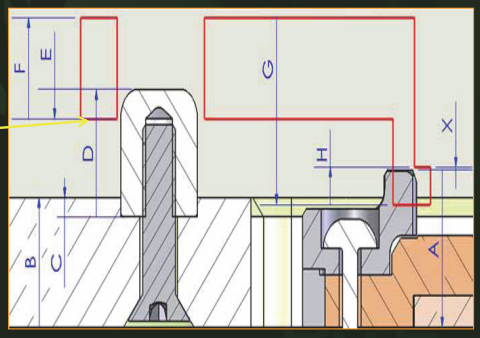
TS Side view

Pogo pin

Current Status & Technical Challenge

- Test tooling stack up process margin and test interface challenges
  - Carrier guide hole deterioration due to occasional crash by guide pin and wear out
  - Need to physically measure carrier guide hole dimensions to avoid substrate hit on Test Socket's top plate





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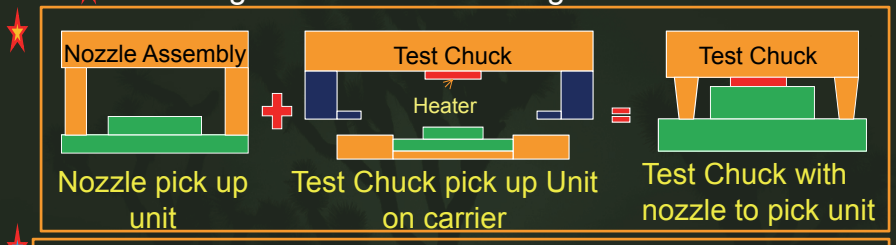
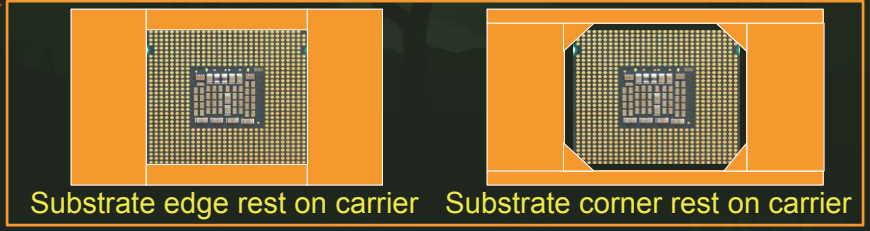
Solution- Problem 1

Unit handling method inside handler at final test

1. Combine Nozzle assembly with Test chuck
2. Change substrate rest at edge to Substrate corner





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Solution- Problem 1

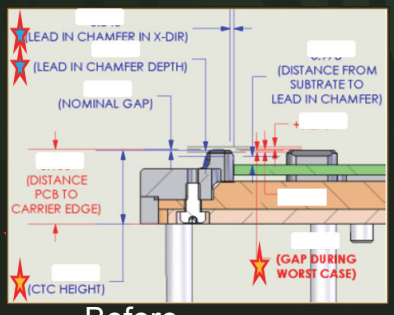
Unit handling method inside handler at final test

Unit handling Method	Need Bottom KOZ	Test Ball/Land Pad depopulate	Meet Thermal Resistance requirment	Substrate Warp	Cost effective
Substare edge(test Chuck with Carrier)	Yes	Yes	Yes	No	No
Combine Nozzle with Test Chuck	No	No	No	No	No
Substrate corner(Test check with Carrier)	Yes	Yes	Yes	No	Yes

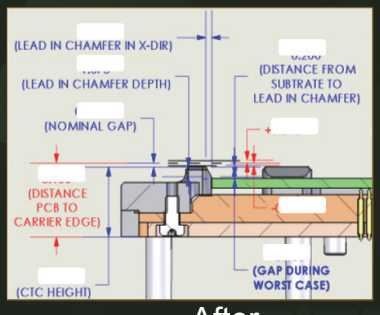
- 1st Substrate edge handling
  - High land/ball pad depopulate
  - Not cost effective due to increase in substrate real estate
- 2nd Combine Nozzle with Test Chuck
  - Thermal resistance not met, need longer soak time to start of test
  - Change equipment handler handling method, cost concern
- 3rd Substrate corner handling
  - Cost effective
  - Minimum solder ball depopulate
  - Maintain current thermal performance and run rate

Solution- problem 2

- Test tooling stack up process margin and test interface challenges
  - Re-design the Guide Plate to gain tooling stack up process margin
    - Optimize socket total height - Increase Z-height Gap from negative to positive during unit to test socket pre engagement
    - Optimize Lead In chamfer depth - Increase the X-directional allowance



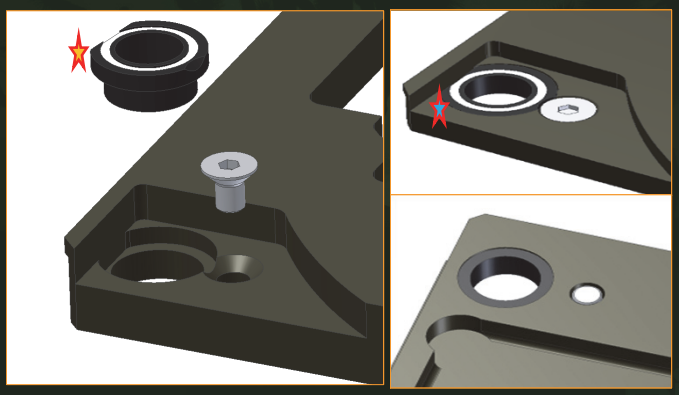
Before



After

Solution- problem 2

- Test tooling stack up process margin and test interface challenges
  - Strengthen Seal plate guide hole of carrier with metal sheet reinforcement
  - Carrier condition indication line to eliminate measurement



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Check results

DOE	Pusher Misalignment	Carrier' SP Guide hole	TS Guide plate	Chipping
1	Worse case	degraded	POR	Yes
2	Worse case	degraded	New	Yes
3	Worse case	Good	POR	Yes
4	Worse case	Good	New	No
5	No Worse case	degraded	POR	Yes
6	No Worse case	degraded	New	Yes
7	No Worse case	Good	POR	No
8	No Worse case	Good	New	No

- Results Summary
  - Under worst case Test Check misalignment condition, substrate damage will occur except if carrier is in good condition + with optimized socket guide
  - Minor misalignment will not cause substrate damage if the carrier is in good condition, regardless of POR or optimized socket guide
- Conclusion
  - Controlling the carrier guide hole condition is crucial in determining the substrate damage risk
  - Optimized socket guide will definitely buy additional process margin to prevent substrate damage

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Conclusion

- **Summary**
  - Optimized Test Socket Guide plate vertical wall and chamfer lead in depth demonstrated process margin improvement
  - Carrier guide hole condition is key factor to ensure good quality tooling stack up
  - Substrate Corner handling method is solution for Thermal concern, Substrate real estate and land pad/Ball depopulation issue

Acknowledgement

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