FOURTEENTH ANNUAL BiTS 2013 Burn-in & Test Strategies Workshop

Archive Poster Session

Poster Sessions are a great way to multitask during a break, stretch your legs after a long session, and even network through interaction with the poster presenters and other curious attendees. This year's session offers a variety of relevant topics that augment what you'll learn sitting in the general sessions.

CSH Coating for High Temperature

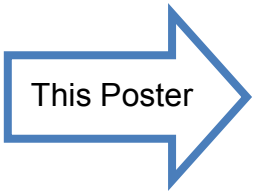
Ichiro Fujishiro—Yamaichi Electronics

Top Side Probing on Handler

Shaul Lupo—Intel Israel

"Auto-Centering Manual Actuator" — One Manual Lid for Different Package Sizes Testing

Ying Hoe Mah, Shamal Mundiyath—JF Technology Berhad



Novel Approach Of Enabling Customer Shadow EPROM aka "EXTERNAL-EPROM" In HVM Environment

Maroon Maroon, Mouller Keren—Intel Corporation

BiTS 2013

Novel Approach Of Enabling Customer Shadow EPROM aka "EXTERNAL-EPROM" In HVM Environment

Maroon Maroon, Mouller Keren
Intel Corporation

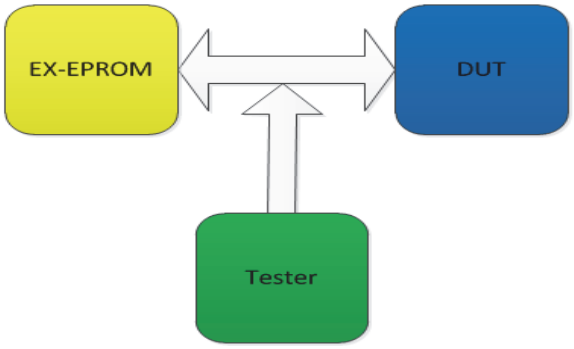
Most Netcom devices, Microprocessors and Chipsets use an external EPROM for initialization of Internal:

- Analog High speed configuration
- Digital parameters (security, chicken bits,..etc)
- Microcontrollers' u-code patches

This work explains a new methodology implemented to provide prompt and fast feedback to the design team and be fully aligned to the system and electrical validation environment

Motivation

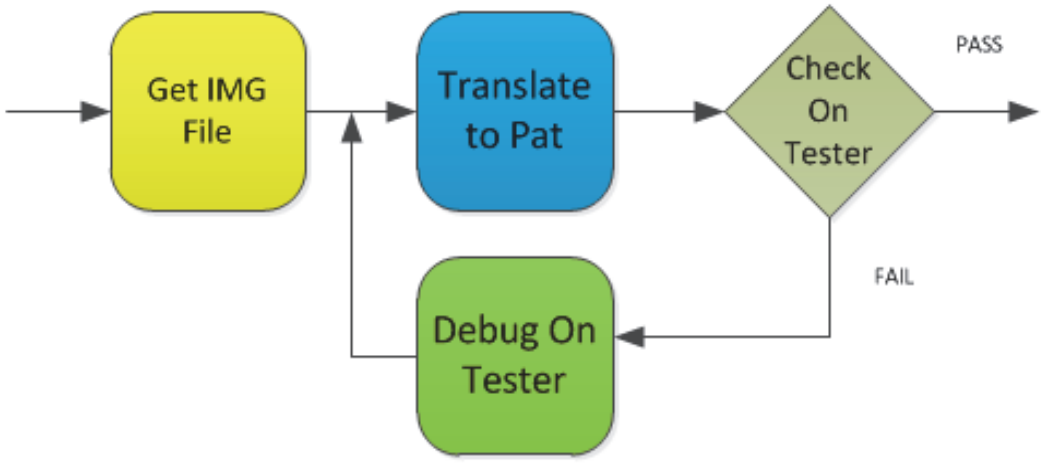
EX-EPROM content "IMG FILE" changes a lot, especially during 1st silicon debug, and also post PRQ as a patch to customers.
Every change in IMG file requires a full, painful & time consuming cycle, starting with generating **new patterns for various analog interfaces, then validation on ATE**.



As result of the above we enabled IMG file programming and loading in the production environment (TIU and SIU). Programing done on Open socket through tester, while loading done before test runs

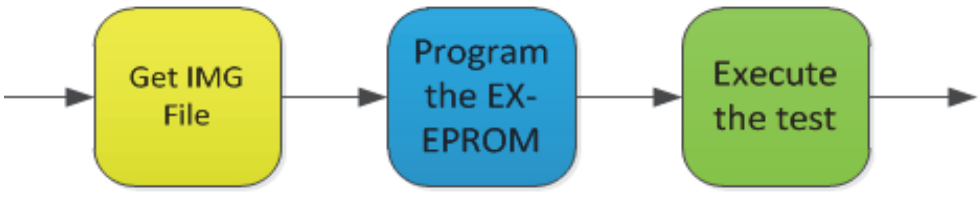
Old approach

In the old approach we generate patterns to include the EPROM IMG initialization through JTAG commands, the problem is if we miss one register or write a wrong value then we will need another full cycle of validation. Execution time **(TT) is long** due to JTAG Frequency, in more than 60% of the cases when we get a new IMG we are spending time on **translate➔Check➔Debug** .



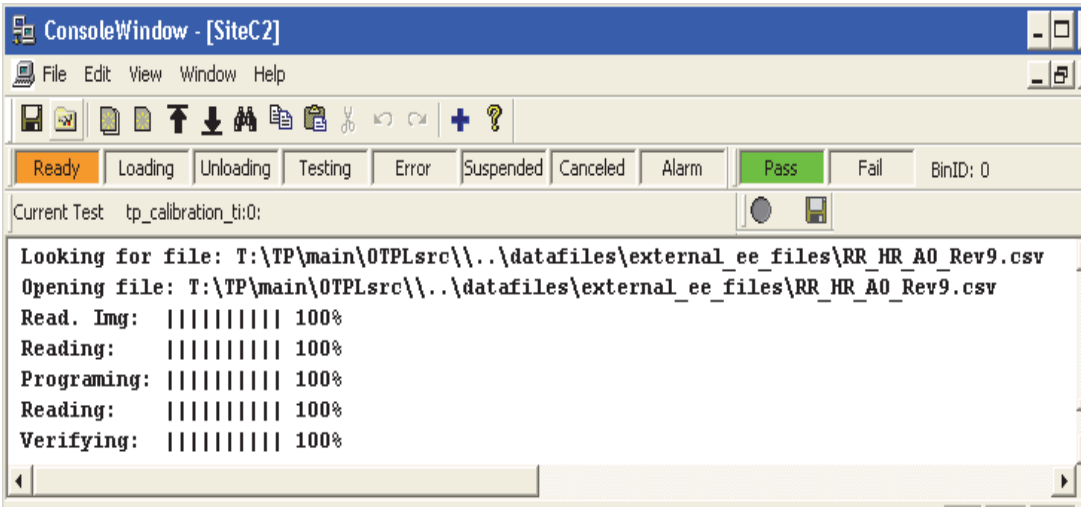
New methodology

In the new approach we will program the EX-EPROM with the needed IMG File automatically when the test program is loaded, negotiation is done between the DUT and EX-EPROM, the IMG data will be loaded to DUT then Test will be executed; **this process is exactly like the customer does.**



Programing IMG Flow:

1. Read the IMG File data
2. Read the EX-EPROM data
3. Compare the two data's - if no match, program EX-EPROM; if match, go to 6
4. Read the EX-EPROM data 2nd time
5. Compare data to IMG file
6. MATCH exit successfully, No MATCH exit with error message Problem with programing



Conclusion

This approach is a complete HVM solution already implemented in several products, enabling fast feedback in the HVM environment and alignment to electrical and system validation teams. In addition to having several IMG files and choosing which IMG to program by uservar in the Test Program.