#### Vol. 23 No. 04

### THE FINAL TEST REPORT



## **By Francoise von Trapp** Incites Group L.L.C It wasn't on the final agenda, but

thanks to a last-m



von Trapp

thanks to a last-minute presentation switch by BiTS Workshop keynoter Jim Feldhan, president of Phoenixbased Semico Research, 3D became a

featured topic at this year's event.

For the past few years, BiTS General Chair, Fred Taber, has contracted me to conduct video interviews at the event for the BiTS Workshop website. The fact that I had the opportunity to get another analyst's perspective on 3D was a bonus.

"3D is sexy, but it's still going through puberty. We expect the technology to be adopted faster than it is," noted Feldhan, adding that for 5 years we've been hearing that 3D will be adopted in two years. He says the hold-up is largely due to gating issues such as the ecosystem, EDA tools, assembly and test processes, and product life and reliability testing. Up until 2012, there have been reliable and low-cost solutions in traditional single die packages, and SiP with stacked die. However, the performance improvements from 2.5D interposer and 3D TSV devices will make them vital to memory in 2012 and memory + logic in 2014.

Addressing the question of whether 2.5D interposers are a stepping stone to 3D, Feldhan said no. He believes it will be a stand-alone technology because it's cheaper, and is likely to be adequate for many applications. He says he sees opportunities for large pitch interposers for MEMS, RF and high performance systems, Feldhan noted.

He added, "currently, TSMC is the main supplier of leading-edge interposers, and cost is double that of a 300-mm wafer. He expects some healthy competition will bring that cost down, and said GlobalFoundries, UMC, Samsung, and IBM all have plans to enter the market."

According to Feldhan, 2012 will see pilot production for 3D DRAM with high volume manufacturing (HVM) coming in 2013. The hybrid memory cube (HMC) of DRAM on logic will be in pilot production in 2013, with HVM in 2014. 3D NAND will also be in pilot production in 2013 and HVM in 2014. From an applications perspective, the first to adopt 3D will likely be data centers and base stations, where the 10X performance at lower power consumption benefits offsets the cost of implementation. Consumer products will follow.

By 2015, he expects market penetration for 3D devices in servers will be over 60 percent. "But when it comes to tablets and smartphones, how quickly we can get the price down will dictate how they will penetrate the market," says Feldhan. In smartphones, he says with 3D, smart phones can achieve 10X and 4X the battery life vs. traditional PCB/IC assembly. However, the semiconductor bill of materials costs must be reduced to between \$100 and \$125 for tablets, and \$80-100 for smart phones. Market penetration for 3D devices for tablets and smartphones is expected to reach just over 10 percent by 2015. Ultimately, Feldhan says the bottom line as seen by Semico Research is this: applications need performance that can be provided by 3D. Adoption is starting, but the eco system still needs development & maturity. Therefore, implementation will occur in stages and cost reduction is the Holy Grail.

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# Test Eqpt Goes Green?

**By Rich Yerganian** - VP of Corporate Marketing at LTX-Credence

Energy conservation is a good thing right? So what about applying energy conservation to semiconductor test equipment? It makes financial sense to consider operating costs, especially electricity costs, when selecting a test system. In some cases the savings on electricity costs over a multiyear period can lead to the tester actually paying for itself. Depending on the region and the testers being compared the annual savings per tester could reach \$30K - \$50K per year!

Of course the tester must be capable of testing the part but if it passes that test (pun intended!) operating costs have to be considered. If the electricity costs are less for one tester over another then it is highly likely the size of the tester is going to be relatively small as well which means floorspace requirements could be drastically reduced.

You could not only use a test system with significant electricity cost savings but also save your operations team from having to build another building for capacity expansion?

# **ATE/DFT MEETINGS**



*IEEE SW Test Worksbop* June 10-13, 2012 Rancho Bernardo Inn San Diego, CA www.swtest.org

SEMICON West July 10-12, 2012 Moscone Center San Francisco, CA www.semiconwest.org