THIRTEENTH ANNUAL BiTS 2012 Burn-in & Test Strategies Workshop

Session 6

ARCHIVE 2012

WE'VE GOT THE POWER (AND SIGNAL INTEGRITY)!

Power delivery and signal integrity have become increasingly important issues in device testing, especially for today's mobile electronics that require more of both to achieve the levels of functionality expected by consumers. As a result, they are becoming some of the greatest challenges in designing test interfaces. In this session, presenters report on a number of specific developments that address these challenges. The first presentation will address the point of diminishing returns on socket pin length from a signal integrity perspective. Next, we'll learn about the anatomy of PCB vias in single-ended and differential signal paths. The third speaker will offer solutions for improving power delivery in the test interface. Finally, innovative interconnect evaluation metrics for design optimization will be explained.

Point of Diminishing Returns on Socket Pin Length From a Signal Integrity Perspective

Sasha N. Oster, Sermet Akbay—Intel Corporation

The Anatomy of PCB Vias in Single-ended and Differential Signal Paths

Zaven Tashjian, Kevin Chan—Circuit Spectrum, Inc.

Improving Power Delivery in the Test Interface

Ryan Satrom—Multitest

New Interconnect Evaluation Metrics for Design Optimization

Se-Jung Moon, Richard Mellitz, Erkan Acar—Intel Corporation

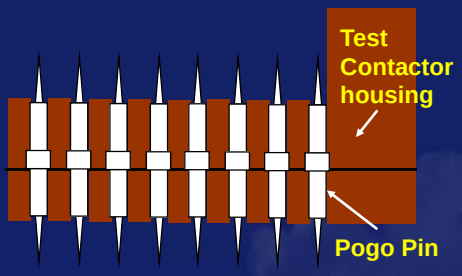
Point of Diminishing Returns on Socket Pin Length From a Signal Integrity Perspective

Sasha Oster, Sermet Akbay
Intel Corporation

2012 BiTS Workshop
March 4 - 7, 2012

Outline

- Introduction
- Pin and SI Modeling
  - Current approach
  - Limitations
- Analyzing SI data
  - New metrics
  - Applying new metrics
- Proposed algorithm
  - Algorithm
  - Example case
- Conclusions
- Discussion



Introduction

- Socket pins are used for HVM test
  - Don't mimic final product requirements
  - Heavy SI penalty (especially IL and crosstalk)
  - Trade-off between mechanical stability and SI
- To improve SI - traditional approach is to shorten pins
  - Initial decreases result in significant SI gains
  - Approach decreases mechanical reliability
- Simulated data suggests that there is a point of diminish returns for SI in shortening pins
  - Desirable to decrease pin length only while significant SI gains are achieved
  - **Goal: Provide an additional evaluation methodology**

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A Quick Word on Power Delivery

- This presentation is about signal integrity – not power delivery!
- Power delivery is most strongly determined by
  - Effects of loop inductance
  - Effects of contact resistance
- Loop inductance
  - Linear dependence on pin length (first order)
  - No diminishing returns on loop inductance with changes in pin length
- Contact resistance
  - Shorter pins will result in shorter springs
  - Shorter springs will likely results in less force
  - Less force will likely result in great contact resistance
  - Likely diminishing returns on contact with changes in pin length
- A dedicate study for PD would be needed to understand if there is a point of diminishing returns for PD with decreases in pin length

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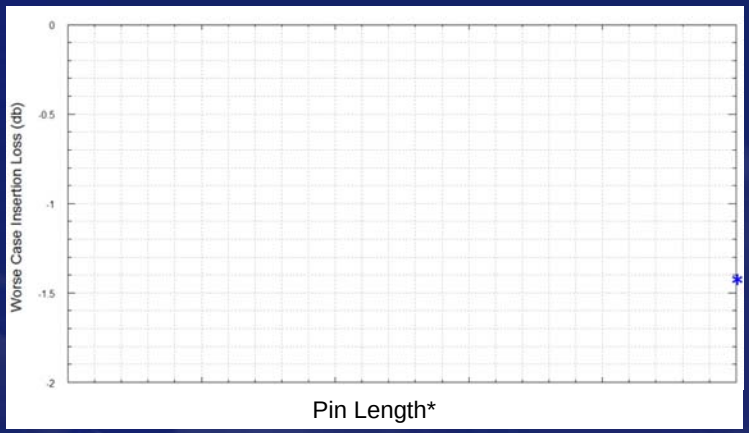
Thinking about our traditional approach

PIN AND SI MODELING

Reducing Pin Length Improves SI



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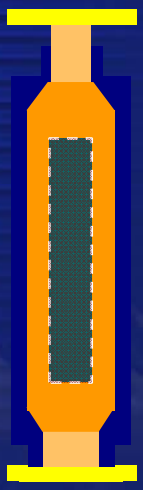
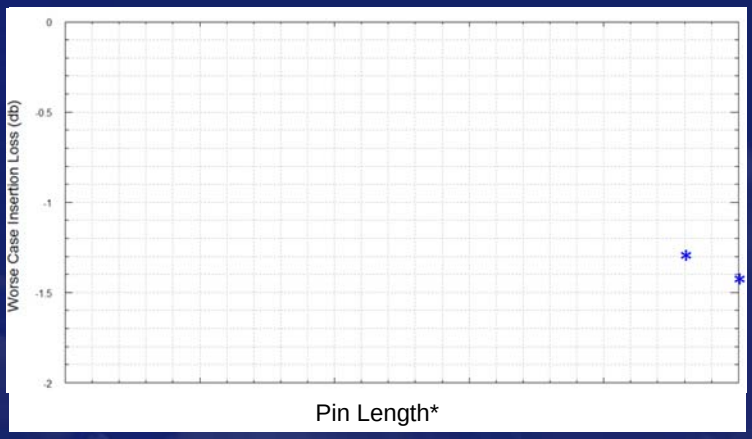
Reducing Pin Length Improves SI





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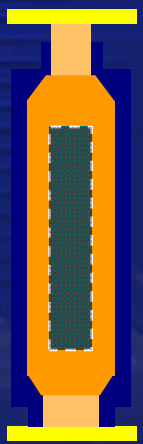
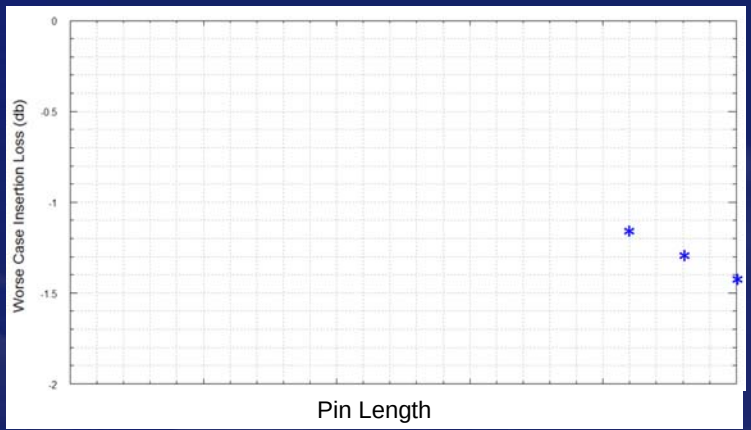
Reducing Pin Length Improves SI





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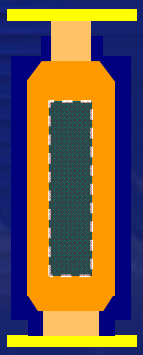
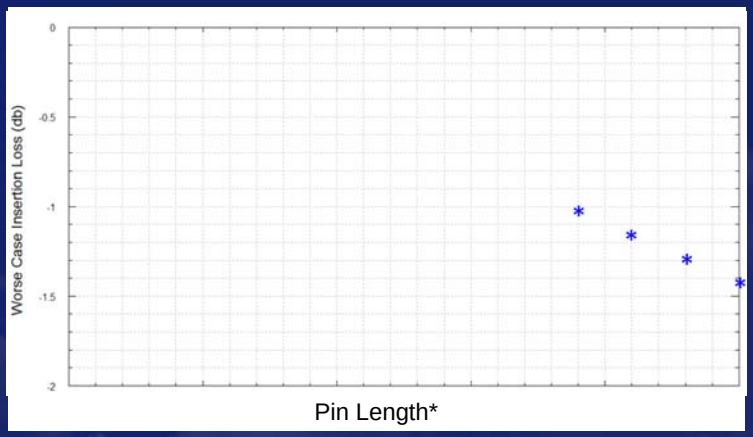
Reducing Pin Length Improves SI





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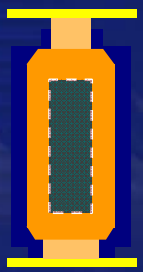
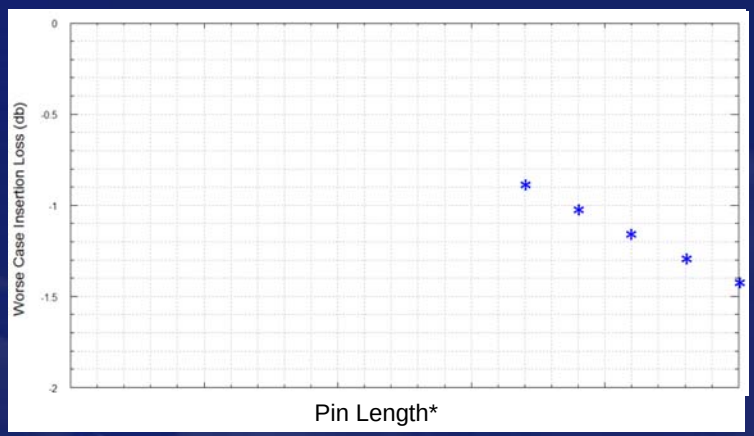
Reducing Pin Length Improves SI





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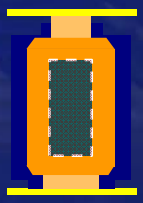
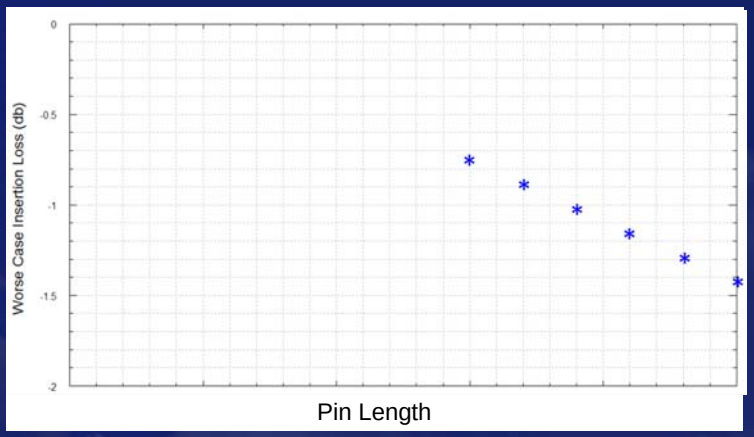
Reducing Pin Length Improves SI





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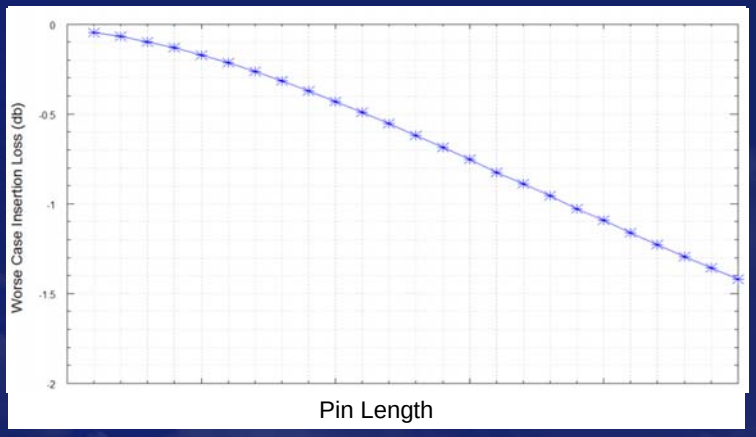
Reducing Pin Length Improves SI

Shorter is better: True, but simplistic



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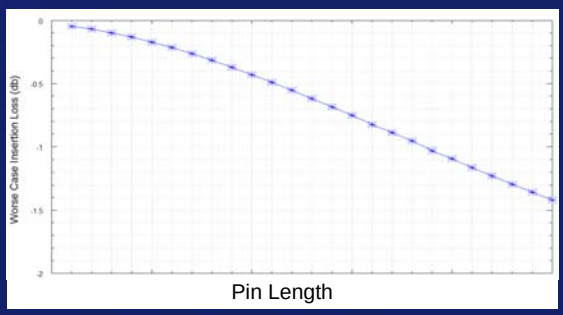
We have a good rule of thumb, but…



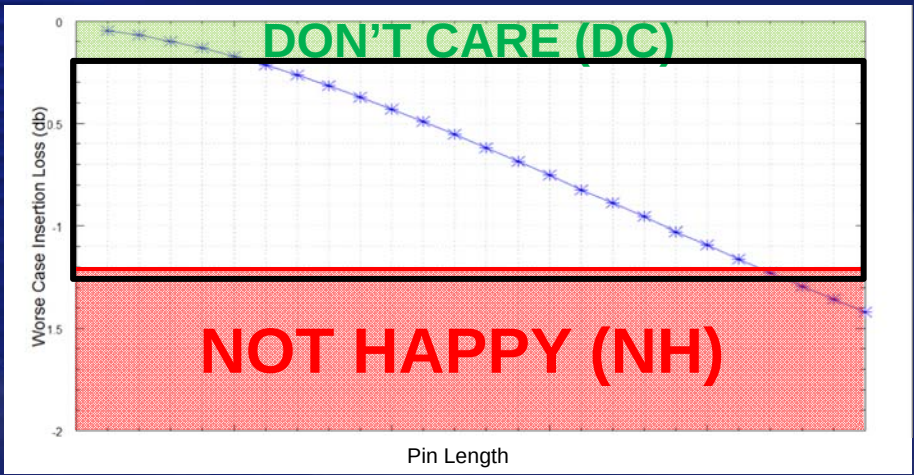
- Represents
  - Single SI parameter (insertion loss)
  - Single frequency
  - Single pitch
  - Single pin pattern
  - Single pin diameter, tapering, etc.

Model and Simulation

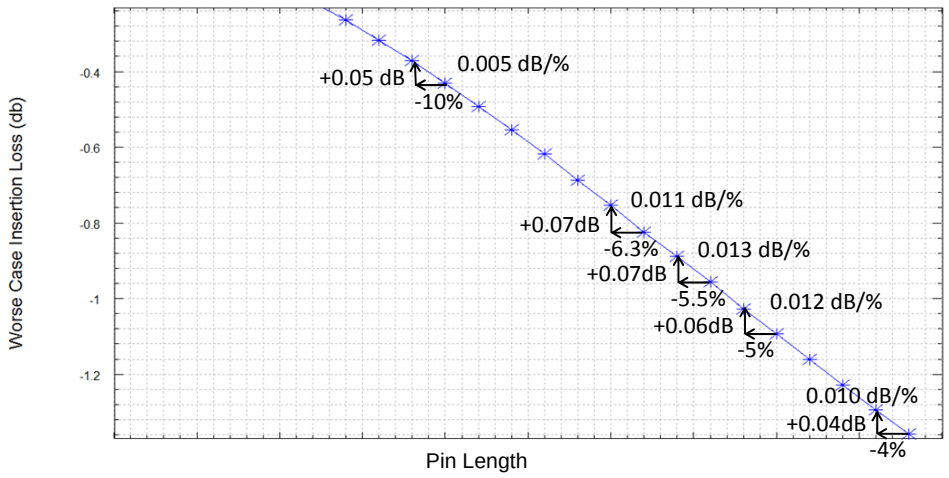
- Model variables
  - Pin geometry
  - Pitch
  - Pin pattern
  - Socket material
  - Solder pad
- Simulation variables
  - Frequency (sweep and step)
  - Meshing options
  - Convergence parameters

ANALYZING SI DATA

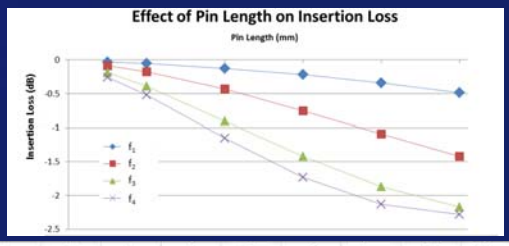
Regions of Interest



Evaluating Returns

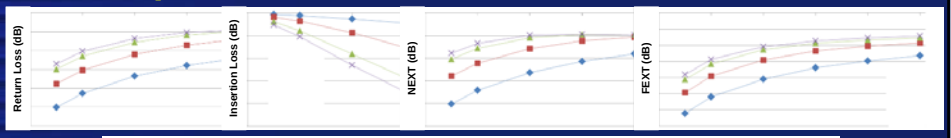


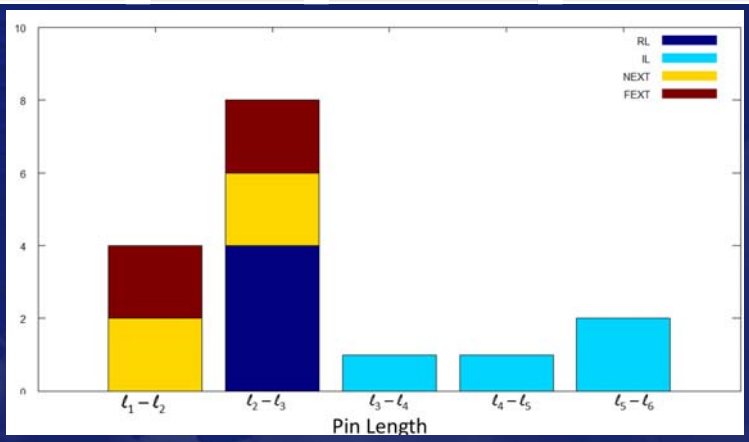
Extending the idea



IL		ℓ_1	Δ	ℓ_2	Δ	ℓ_3	Δ	ℓ_4	Δ	ℓ_5	Δ	ℓ_6
f_1	dB	-0.029		-0.055		-0.126		-0.218		-0.342		-0.489
	dB/%		-5E-04		-0.001		-0.003		-0.005		-0.007	
	dB/mm		-0.052		-0.072		-0.092		-0.124		-0.147	
f_2	dB	-0.084		-0.174		-0.431		-0.753		-1.093		-1.421
	dB/%		-9E-04		-0.005		-0.01		-0.014		-0.016	
	dB/mm		-0.09		-0.257		-0.322		-0.34		-0.328	
f_3	dB	-0.187		-0.387		-0.906		-1.422		-1.87		-2.172
	dB/%		-0.002		-0.01		-0.015		-0.018		-0.015	
	dB/mm		-0.2		-0.519		-0.516		-0.448		-0.302	
f_4	dB	-0.256		-0.522		-1.151		-1.73		-2.13		-2.283
	dB/%		-0.003		-0.013		-0.017		-0.016		-0.008	
	dB/mm		-0.266		-0.629		-0.579		-0.4		-0.153	

Repeat over all SI Parameters

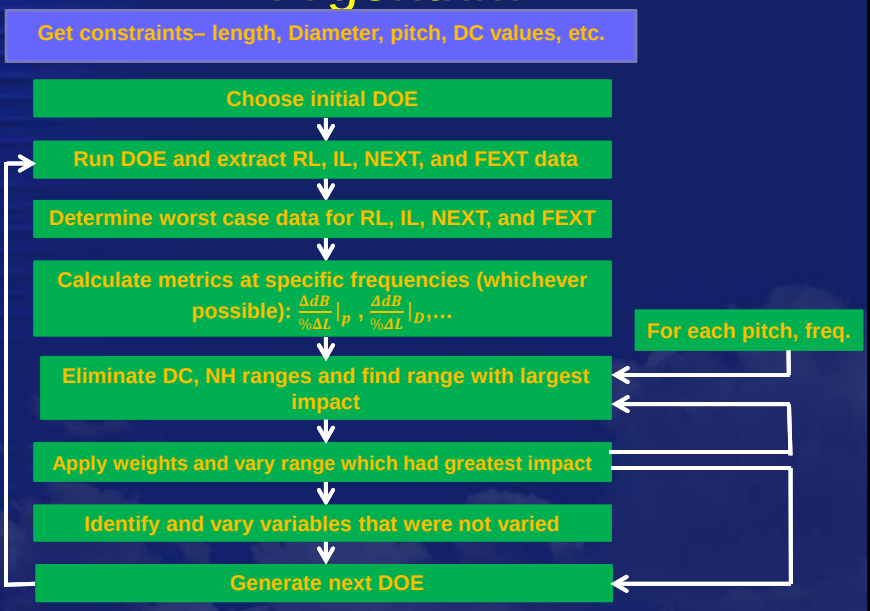




Using the new approach

PROPOSED ALGORITHM

Algorithm



Choose initial DOE

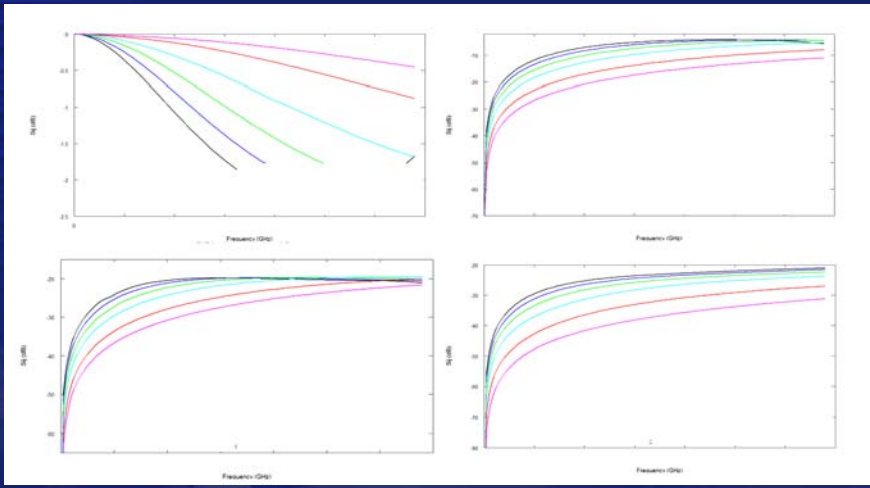
Example DOE

Case Name	length	dim_2	dim_3	dim_4	dim_5	dim_6	dim_7	dim_8	dim_9	dim_{10}
0001	l_1	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0002	l_1	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0003	l_1	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0004	l_2	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0005	l_2	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0006	l_2	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0007	l_3	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0008	l_3	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0009	l_3	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0010	l_4	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0011	l_4	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0012	l_4	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0013	l_5	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0014	l_5	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0015	l_5	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0016	l_6	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0017	l_6	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0018	l_6	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255

Run DOE and extract RL, IL, NEXT, and FEXT data

↓

Determine worst case data for RL, IL, NEXT, and FEXT



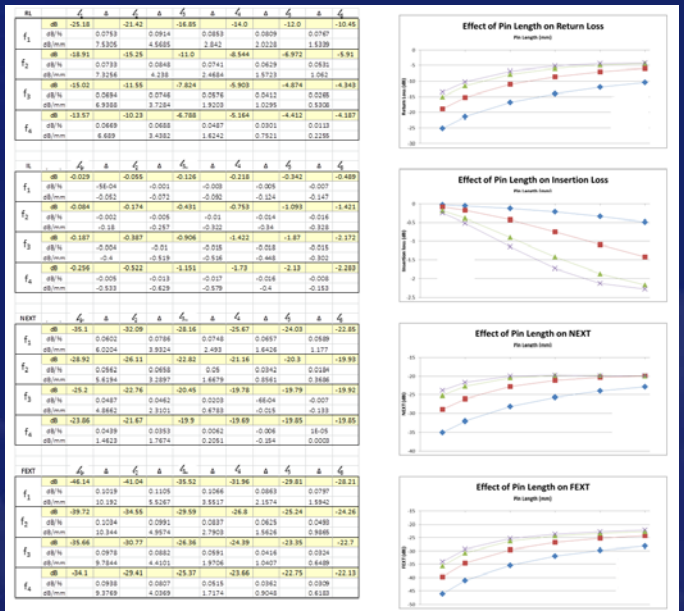
Calculate metrics at specific frequencies (whichever possible): $\frac{\Delta dB}{\%\Delta L}|_p$, $\frac{\Delta dB}{\%\Delta L}|_D$,…

RL

IL

NEXT

FEXT



Eliminate DC, NH ranges and find range with largest impact

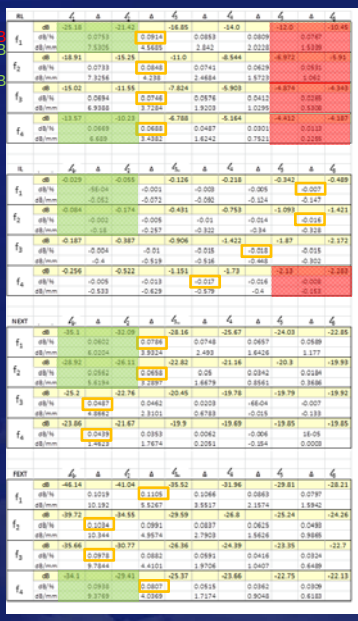
RL

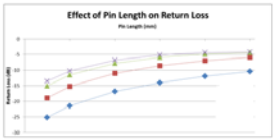
IL

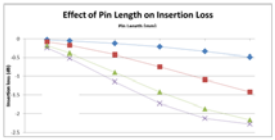
NEXT

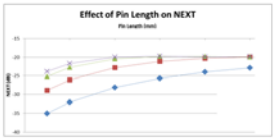
FEXT

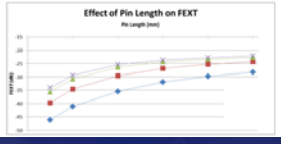
-12.0 dB
-20.0 dB
-7.0 dB
-18.0 dB





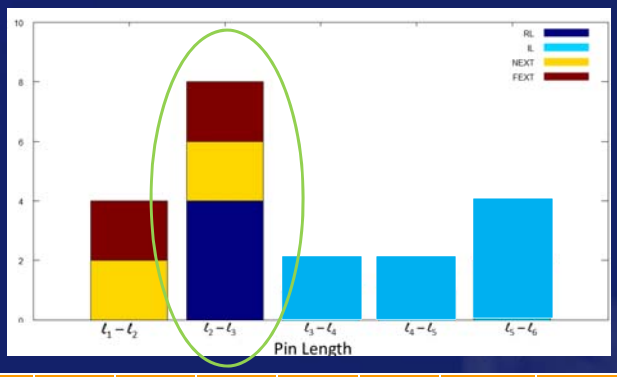






Apply weights and vary range which had greatest impact

Weight:
RL: 1
IL: 2
NEXT: 1
FEXT: 1



Next DOE:

Case Name	length	dim_2	dim_3	dim_4	dim_5	dim_6	dim_7	dim_8	dim_9	dim_{10}
0001	l_7	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0002	l_8	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0003	l_9	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0004	l_{10}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0005	l_{11}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0006	l_{12}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425

Identify and vary variables that were not varied

Original DOE:

Case Name	length	dim_2	dim_3	dim_4	dim_5	dim_6	dim_7	dim_8	dim_9	dim_{10}
0001	l_1	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0002	l_1	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0003	l_1	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0004	l_2	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0005	l_2	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0006	l_2	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0007	l_3	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0008	l_3	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0009	l_3	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0010	l_4	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0011	l_4	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0012	l_4	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0013	l_5	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0014	l_5	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0015	l_5	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255
0016	l_6	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0017	l_6	0.4	0.3	0.18	0.18	0.18	0.18	0.18	0.18	0.34
0018	l_6	0.3	0.225	0.135	0.135	0.135	0.135	0.135	0.135	0.255

3/2012 Point of Diminishing Returns on Socket Pin Length from a Signal Integrity Perspective 27

Generate next DOE

Next DOE:

Case Name	length	dim_2	dim_3	dim_4	dim_5	dim_6	dim_7	dim_8	dim_9	dim_{10}
0001	l_7	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0002	l_8	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0003	l_9	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0004	l_{10}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0005	l_{11}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0006	l_{12}	0.5	0.375	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0007	l_7	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0008	l_8	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0009	l_9	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0010	l_{10}	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0011	l_{11}	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0012	l_{12}	0.5	0.4	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0013	l_7	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0014	l_8	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0015	l_9	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0016	l_{10}	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0017	l_{11}	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425
0018	l_{12}	0.5	0.35	0.225	0.225	0.225	0.225	0.225	0.225	0.425

3/2012 Point of Diminishing Returns on Socket Pin Length from a Signal Integrity Perspective 28

Advantages

- Identifies where effort will produce great result
- Evaluates "goodness"
  - Across multiple SI parameters
  - Across multiple frequencies
  - At each pitch
  - For multiple pin pattern
  - For multiple pin dimensions

Conclusions

- Trade-off between pin-length and SI
- New method which focuses on diminishing returns for SI (not PD!)
- Algorithm which identifies ranges to focus efforts on
- Allow for evaluation across multiple SI parameters, frequencies, pin geometries, and pin patterns

The Anatomy of PCB Vias in Single-ended and Differential Signal Paths

Zaven Tashjian
President, Circuit Spectrum, Inc.

Kevin Chan
Applications Engineer, Circuit Spectrum, Inc.

2012 BiTS Workshop
March 4 - 7, 2012

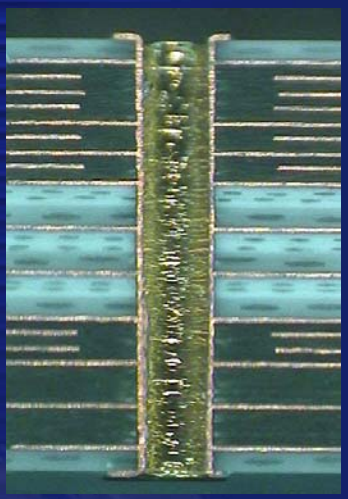
Outline

- Multi-layer PCB as basis for this study
- Variables that determine the behavior of an isolated via
- Via to via crosstalk
- Differential signals and their vias

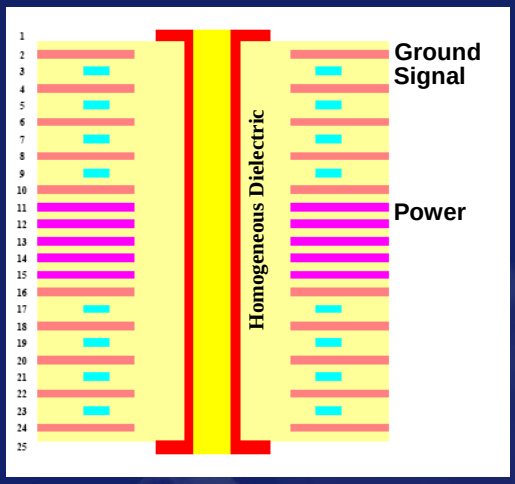
PCB Construction

- Homogeneous dielectric
- Multiple ground plane layers
- Multiple signal layers
- Multiple power plane layers
- All cases in presentation are based on the same stack-up

Via Cross-section



Micro-section



Stack-up

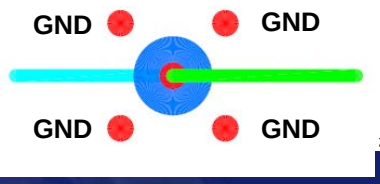
Isolated Via

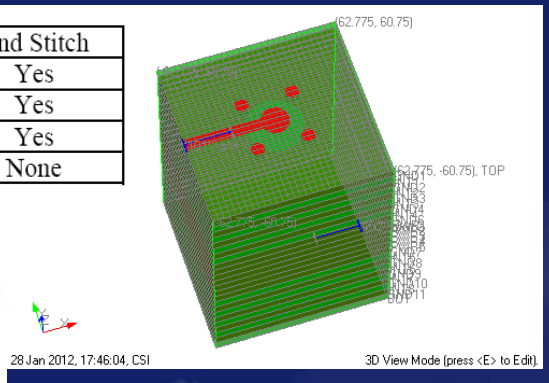
Variables that determine the behavior of an isolated via
- Drill size
- Pad size
- Anti-pad size
- Copper weight on planes
- Dielectric material
- Ground plane stitching
- Transition to trace
- Via stub
- Others

Lumped element model

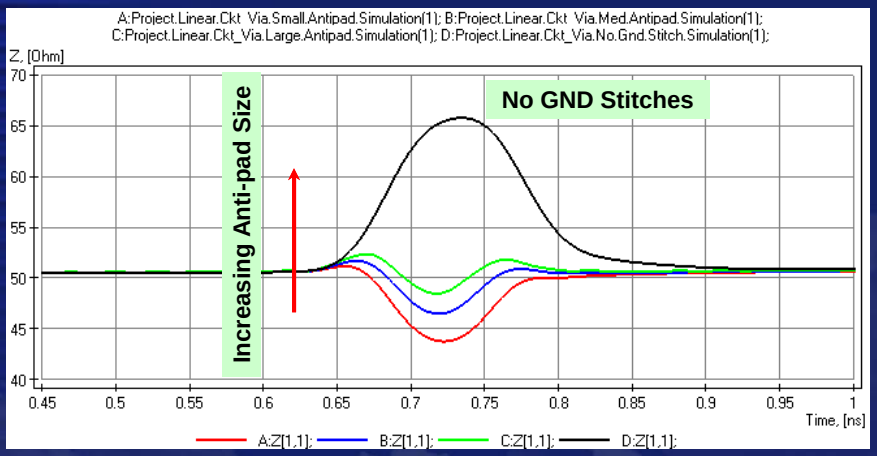
Isolated Via Structure

Case	Signal Anti-pad	Gnd Stitch
1	30 mils	Yes
2	35 mils	Yes
3	40 mils	Yes
4	30 mils	None

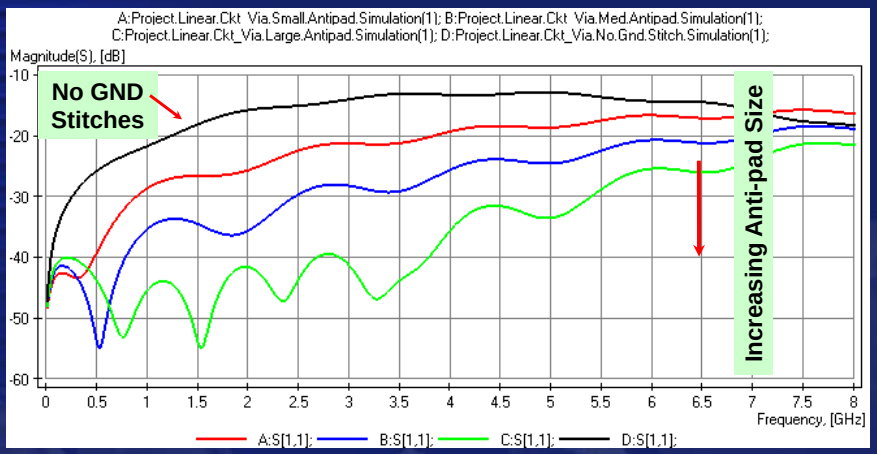




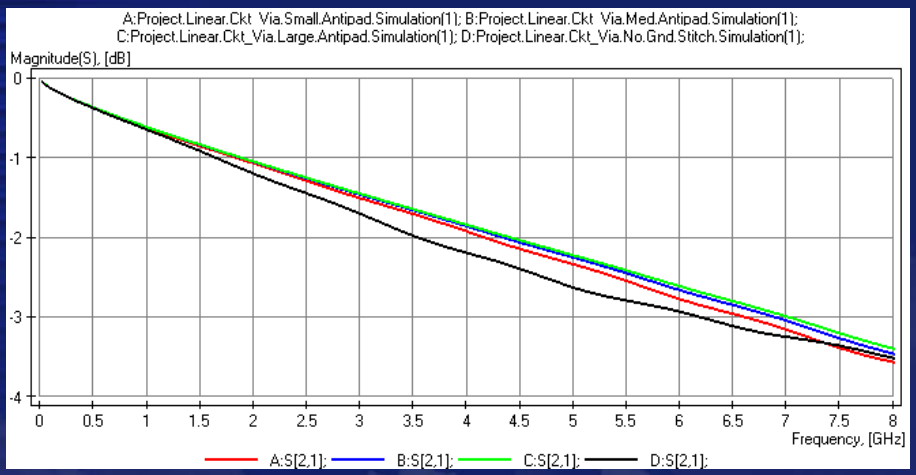
TDR for Isolated Via Structure



Return Loss (S11) for Isolated Via

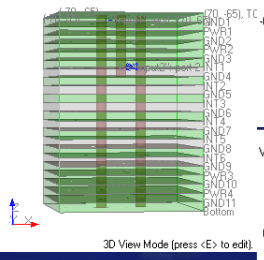


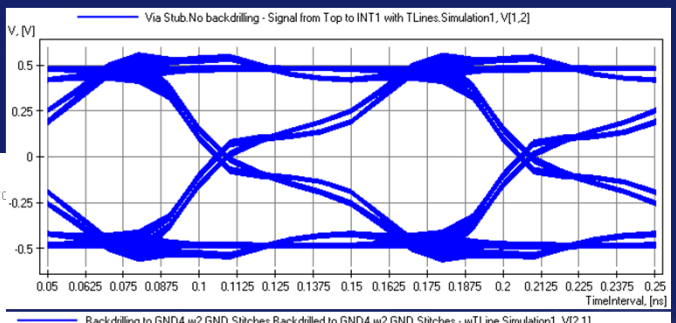
Insertion Loss (S21) for Isolated Via



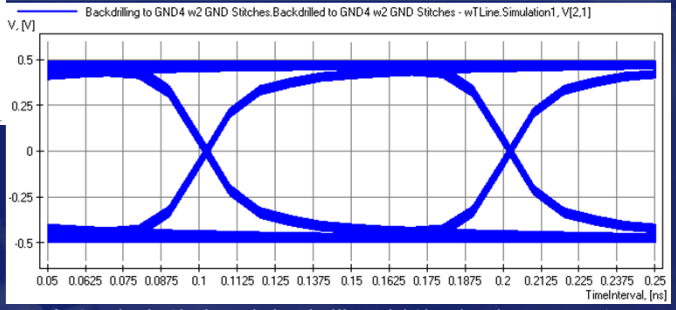
Eye Diagrams for Via with and without Stub

Via with stub

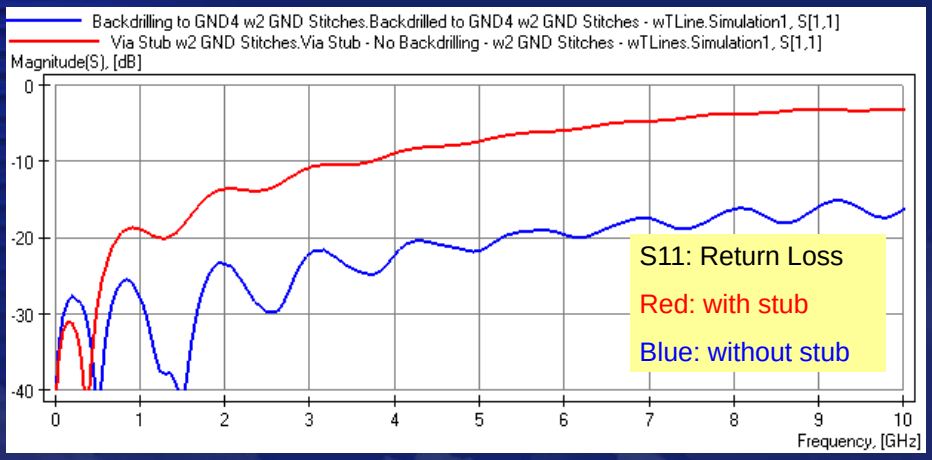




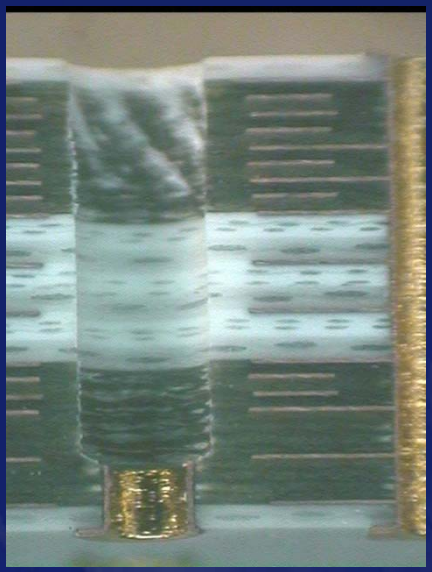
Via with stub removed



Return Loss S11 for Via Example with and without Stub

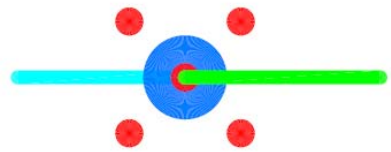


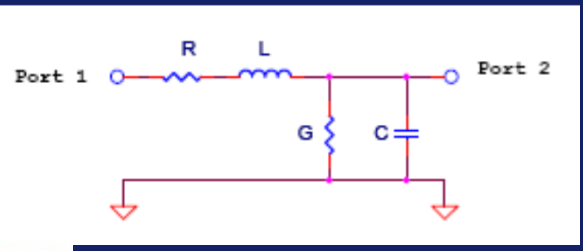
Back-drilled Via



Lumped Element Model

PCB Structure



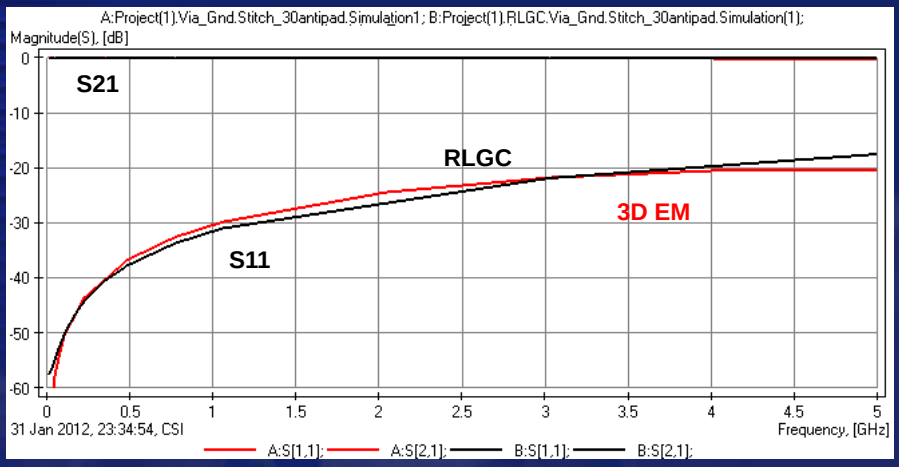


RLGC Elements for Via

Case	Signal Anti-pad	Gnd Stitch	R (Ohm)	L (nH)	G (S)	C (pF)
1	30 mils	Yes	3.56E-03	5.62E-01	5.83E-05	4.84E-02
2	40 mils	Yes	2.02E-02	8.98E-01	1.15E-04	6.41E-02
3	30 mils	None	4.05E-02	1.06E+00	1.64E-04	2.00E-02

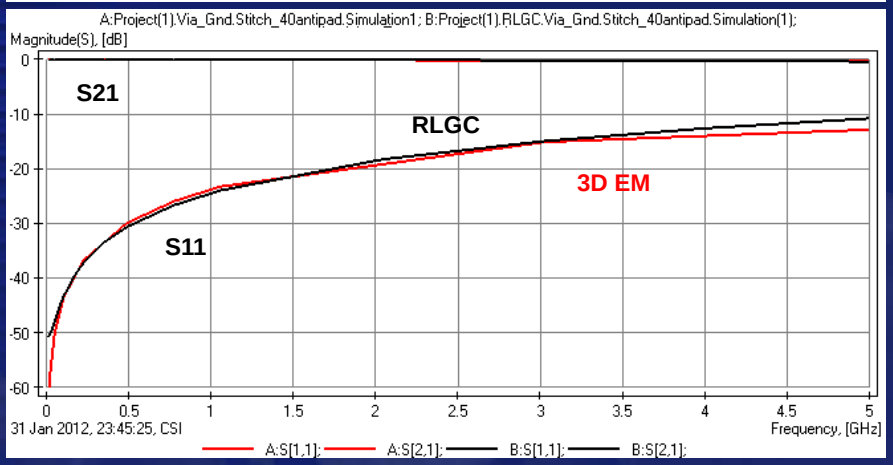
RLGC vs. 3D EM (Case 1)

Case	Signal Anti-pad	Gnd Stitch	R (Ohm)	L (nH)	G (S)	C (pF)
1	30 mils	Yes	3.56E-03	5.62E-01	5.83E-05	4.84E-02



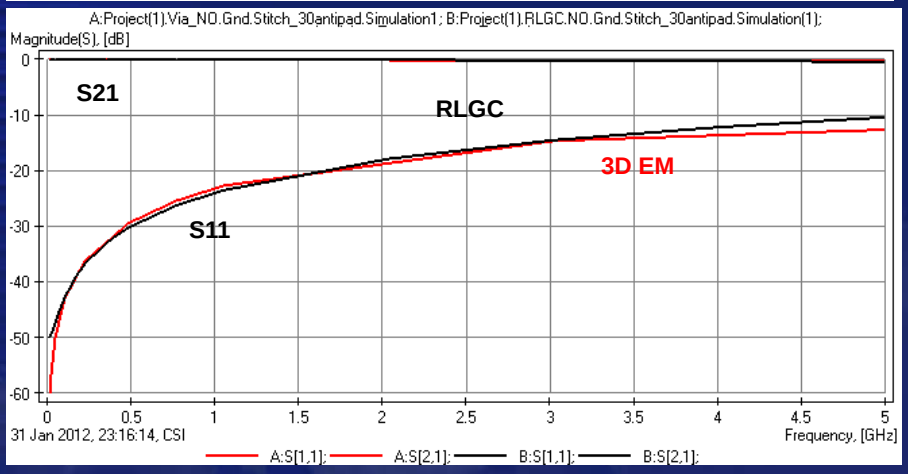
RLGC vs. 3D EM (Case 2)

Case	Signal Anti-pad	Gnd Stitch	R (Ohm)	L (nH)	G (S)	C (pF)
2	40 mils	Yes	2.02E-02	8.98E-01	1.15E-04	6.41E-02



RLGC vs. 3D EM (Case 3)

Case	Signal Anti-pad	Gnd Stitch	R (Ohm)	L (nH)	G (S)	C (pF)
3	30 mils	None	4.05E-02	1.06E+00	1.64E-04	2.00E-02



Via to Via Crosstalk

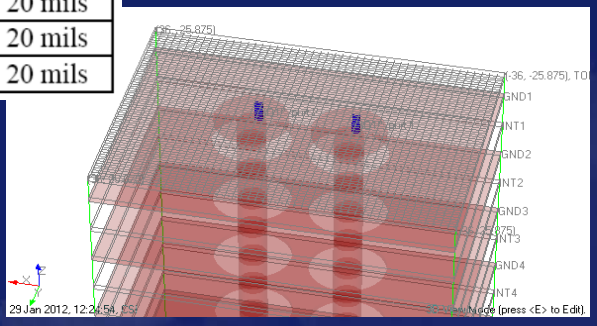
Crosstalk dictated by pitch

- 0.5 mm
- 0.65 mm
- 0.8 mm
- 1.0 mm

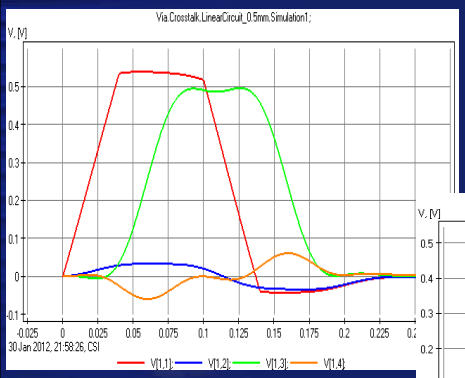
Optimal/practical pitch for negligible crosstalk

Parallel Vias for Crosstalk

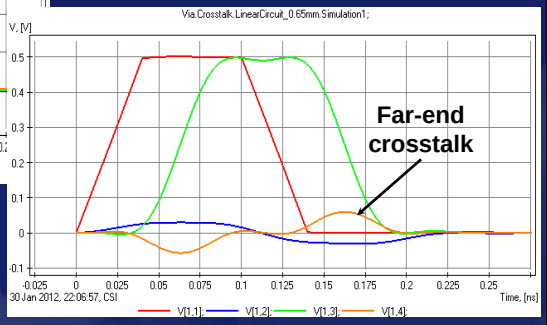
Case	Pitch	Anti-pad
1	0.5 mm	16 mils
2	0.65 mm	18 mils
3	0.8 mm	20 mils
4	1.0 mm	20 mils
5	1.27 mm	20 mils
6	2.54 mm	20 mils



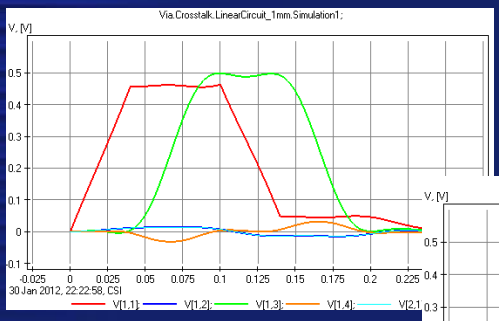
0.5 mm Pitch



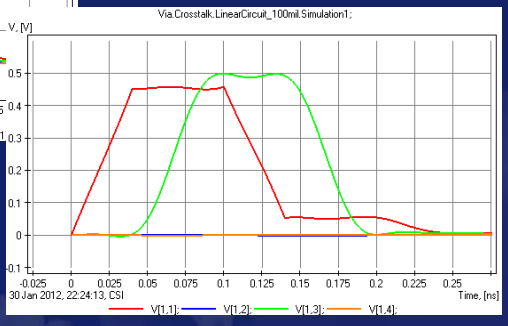
0.65 mm Pitch



1.0 mm Pitch

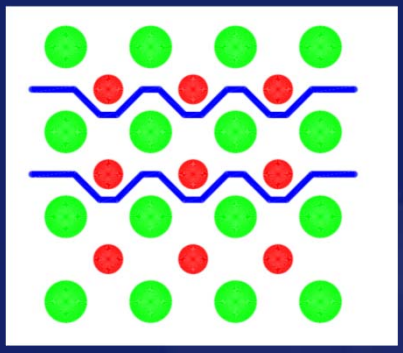


2.54 mm Pitch



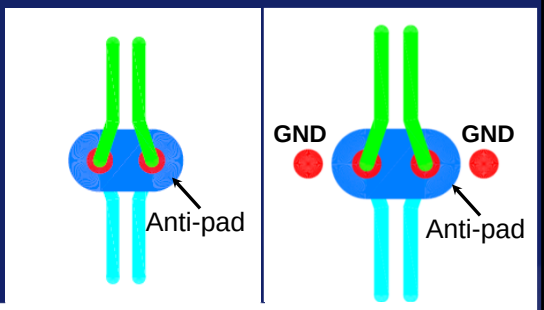
Mitigating Crosstalk

- BGA with interstitial grounds
- New challenges emerge
- Pitch limitation
- Signal trace routing complexity



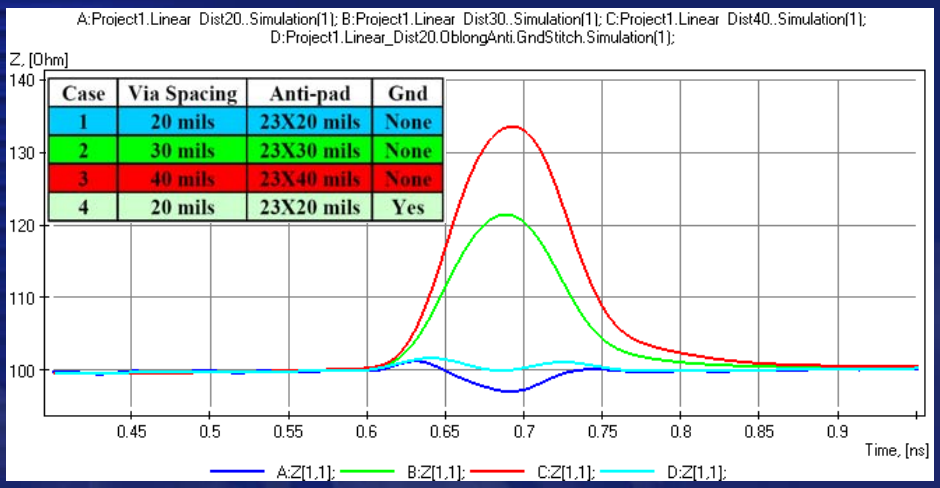
Differential Signals and their Vias

- Via to via spacing
- Anti-pad shape and size
- Ground stitching vias



Case	Signal Via Spacing	Signal Anti-pad	Gnd Stitch
1	20 mils	23X20 mils	None
2	30 mils	23X30 mils	None
3	40 mils	23X40 mils	None
4	20 mils	23X20 mils	Yes

Differential Impedance TDR for Parallel Via Structure



Case	Via Spacing	Anti-pad	Gnd
1	20 mils	23X20 mils	None
2	30 mils	23X30 mils	None
3	40 mils	23X40 mils	None
4	20 mils	23X20 mils	Yes

Conclusion

We have shown that employment of proper and readily available tools and methodologies for the creation of the optimal via structure for a specific objective in a PCB can lead to piece of mind as one commits a design to fabrication. This is particularly important in multi-gigabit digital signal applications. It may require multiple iterations of routines before one achieves the objective, but it is achievable.

Improving Power Delivery in the Test Interface

Ryan Satrom
Multitest

2012 BiTS Workshop
March 4 - 7, 2012

Agenda

- Introduction to Power Integrity
- Optimizing the Interface
- Simulation-Measurement Correlation

Introduction to Power Integrity

My working definition:

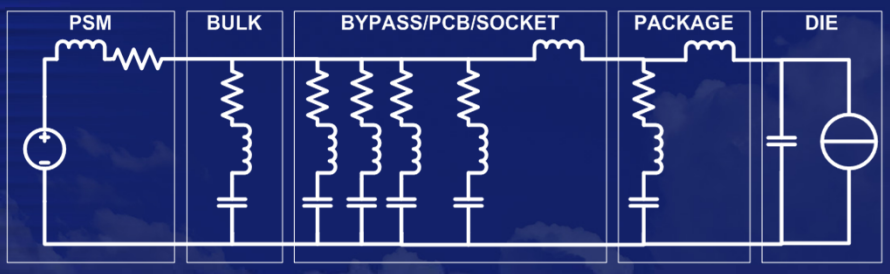
Power Integrity is a measure of the ability of a power and ground network to successfully bypass noise and maintain a constant voltage at the device.

Power Integrity can be problematic in low-voltage, high-current, and high-speed-switching environments.

Introduction to Power Integrity

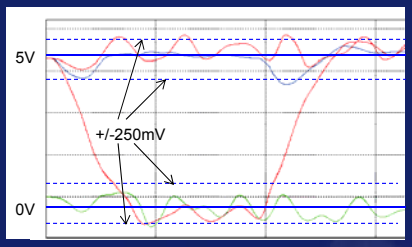
Goal of Power Delivery Network (PDN)

- Provide constant voltage to DUT in high *di/dt* environment by successfully bypassing AC currents from power to ground



Introduction to Power Integrity

- IC Power Supply Voltage
  - Yesterday 5V
  - Today 1V (5x reduction)
- Typical Supply Ripple allowed
  - Yesterday 5-10%
  - Today 0.5% (up to 20x reduction)
- Current Requirements
  - Yesterday 10A
  - Today 150A (15x increase)
- Z_{TARGET} Requirements
  - Yesterday 100mΩ
  - Today 1mΩ (100x reduction)



Year	Power (W)	Vdd (V)	Idd (A)
2010	146	0.97	151
2011	161	0.93	173
2012	158	0.90	176
2013	149	0.87	171
2014	152	0.84	181
2015	143	0.81	177
2016	130	0.78	167

Data courtesy of ITRS 2010

3/2012 Improving Power Delivery in the Test Interface 5

Introduction to Power Integrity

SI Impedance

Ideal Z = 50Ω

Ideal Z → high bandwidth

Instantaneous impedance

Time domain

$$Z = \sqrt{\frac{L}{C}}$$

PDN Impedance

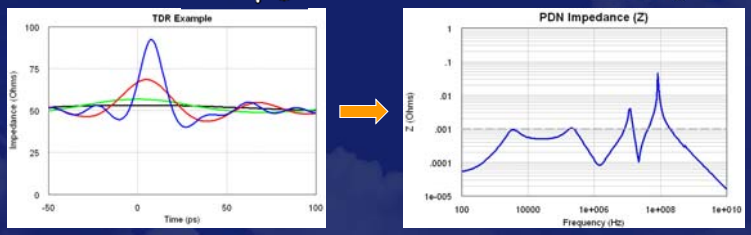
Ideal Z ≈ 0 Ω

Ideal Z → constant voltage

Aggregate impedance response

Frequency domain

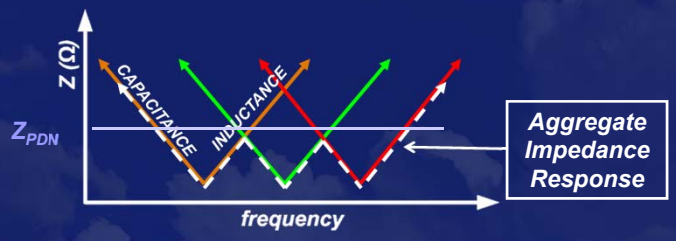
$$Z = R + 2\pi fL + \frac{1}{2\pi fC}$$



3/2012 Improving Power Delivery in the Test Interface 6

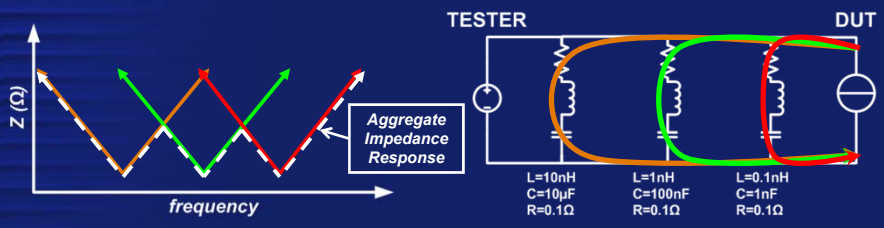
Introduction to Power Integrity

- Quantifying the impedance of the PDN (Z_{PDN})
  - Network comprised of multiple elements – each element has both inductance (L) and capacitance (C)
  - Capacitance determines minimum effective frequency
  - Parasitic inductance determines maximum effective frequency
  - Overall Z_{PDN} is summation of all LC paths
  - Impedance must remain below specified Z_{PDN}



3/2012 Improving Power Delivery in the Test Interface 7

Introduction to Power Integrity



Signal Frequency	Impedance**		
• 30 kHz	***0.5 Ω***	53 Ω	5.3 kΩ
• 80 MHz	5 Ω	***0.5 Ω***	2 Ω
• 250 MHz	15 Ω	2 Ω	***0.5 Ω***

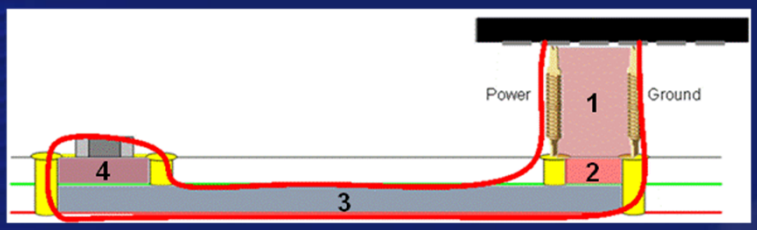
Example Impedance Calculation: f=30kHz; L=10nH; C=10µF; R=0.1Ω
Z = R + 2πfL + 1/2πfC = 0.1 + 2π*30kHz*10nH + 1/(2π*30kHz*10µF) ≈ 0.5Ω

3/2012 Improving Power Delivery in the Test Interface 8

Paper #3
4

Introduction to Power Integrity

Most critical area of the test interface:



1) Contactor
2) DUT Vias
3) Planes
4) Vias/Capacitor

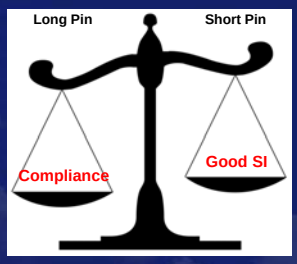
Optimizing the Contactor

Optimal probe length – balancing act

Past Requirements

Excellent Compliance

Good Signal Integrity

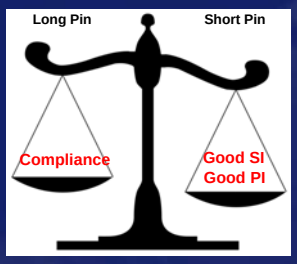


Latest Requirements

Excellent Compliance

Good Signal Integrity

Good Power Integrity



Optimizing the Contactor

- Optimal probe must adequately account for all variables
- Longer probes and shorter probes each have advantages – there is no perfect solution
  - *How much compliance can be sacrificed to improve power delivery?*
  - *How critical is minimal inductance?*
- Example: Large BGAs
  - Increased need for compliance to meet mechanical requirements
  - Increased need for minimized Z_{PDN} due to high-current, low-voltage requirements
  - *What is the optimal probe length?*
- Probe manufacturers must understand the trade-offs to confidently provide the best solution for each application

Optimizing the PCB

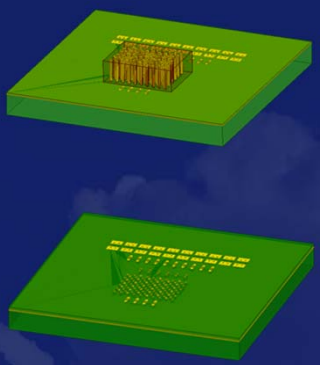
- Optimizing interface board requires tradeoffs among aspects of design
  - Manufacturability
  - Signal Integrity
  - Power Integrity

Optimizing the PCB

- Power integrity in the PCB is dependent upon a combination of several variables:
  - Vias – quantity, length, diameter, power/ground proximity
  - Capacitors – quantity, location, size, type
  - Planes – power/ground proximity, location

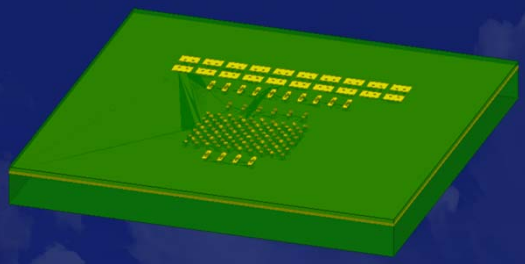
Optimizing the PCB

- Simulation was used to better understand interaction of these variables
- Models were created in HFSS
  - Accurately models small structures
  - Simulates entire critical area
- Examples show the results of varying several parameters
- Each application is different and must be considered individually



Optimizing the PCB

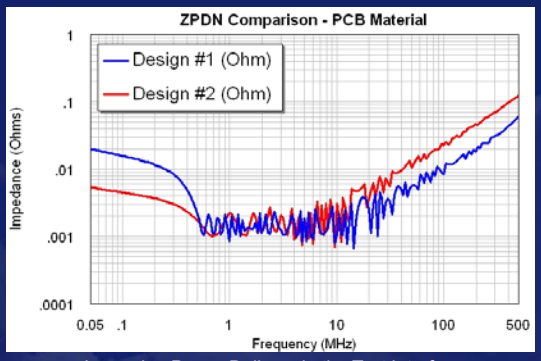
- Parameters Varied:
  - PCB Material
  - Power/ground layer location
  - Capacitor locations
  - Capacitor quantity



Optimizing the PCB – Material

- The PCB material choice impacts the performance of the PDN

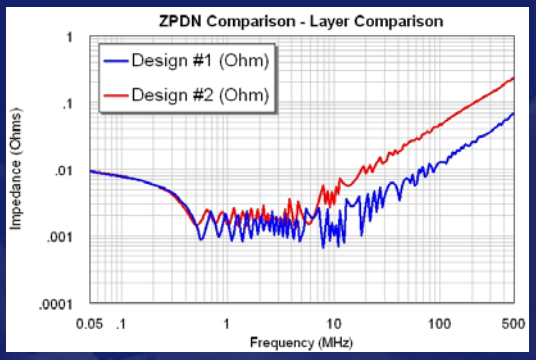
Max Freq (Z_{PDN}=0.01Ω)	
Design #1	85 MHz
Design #2	42 MHz



Optimizing the PCB – Power Layer

- The location of the power layer has a large impact on the performance of the PDN

Max Freq (Z_{PDN}=0.01Ω)	
Design #1	68 MHz
Design #2	18 MHz

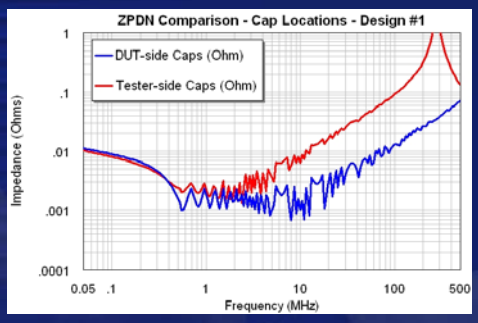


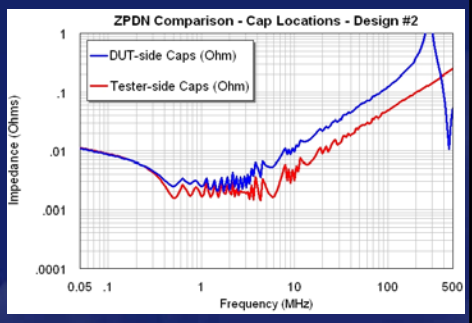
Optimizing the PCB – Cap Locations

- The optimal capacitor location depends on other aspects of the design

Max Freq (Z_{PDN}=0.01Ω)	
DUT-Side Caps	63 MHz
Tester-Side Caps	13 MHz

Max Freq (Z_{PDN}=0.01Ω)	
Tester-Side Caps	18 MHz
DUT-Side Caps	8 MHz

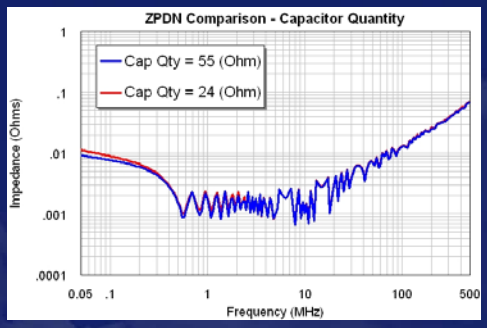




Optimizing the PCB – Cap Quantity

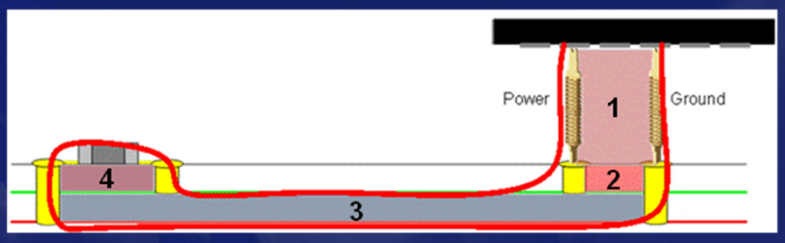
- The quantity of capacitors can be significantly reduced by determining which capacitors are necessary

Max Freq (Z_{PDN}=0.01Ω)	
Cap Qty = 55	63 MHz
Cap Qty = 24	63 MHz



Optimizing the Contactor & PCB

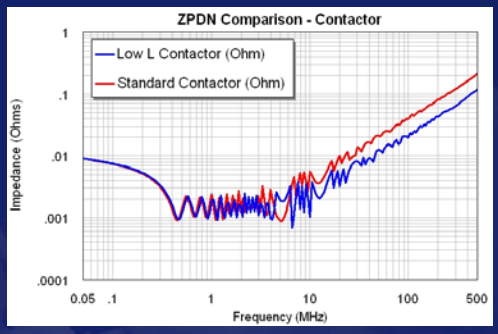
- The contactor has a significant impact on the overall PDN performance
- A highly-inductive socket eliminates any benefits that may be achieved from a good PDN design on the PCB



Optimizing the Contactor & PCB

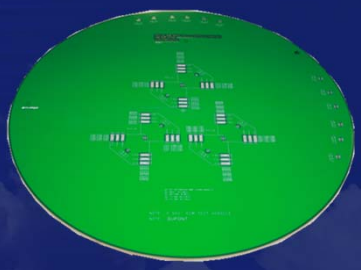
- The contactor has a significant impact on the Z_{PDN}
- Reducing the impedance of the contactor is critical to good PDN performance

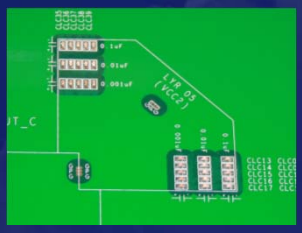
Max Freq (Z_{PDN}=0.01Ω)	
Low L Contactor	45 MHz
Standard Contactor	20 MHz



Simulation-Measurement Correlation

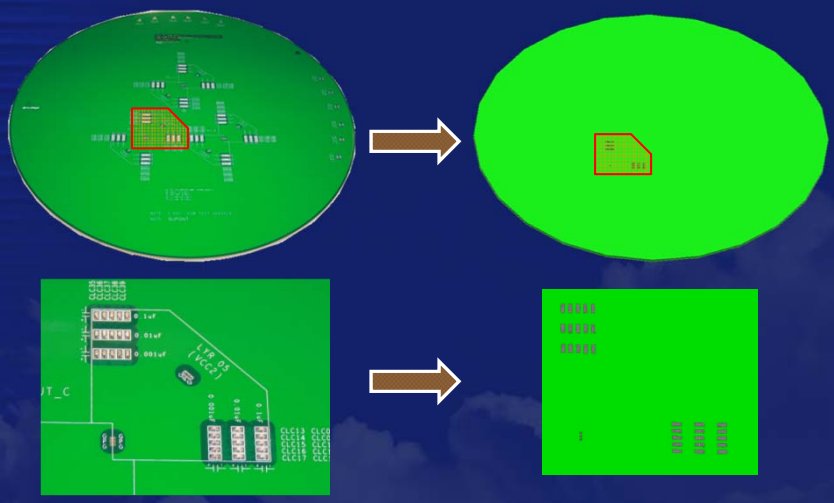
- PCBs were fabricated and measured to validate simulation results
- Main challenge – Probing at DUT
  - BGA has multiple powers/grounds which do not provide place to probe
  - DUT replaced by ground-power-ground via structure in order to provide access for probing





Simulation-Measurement Correlation

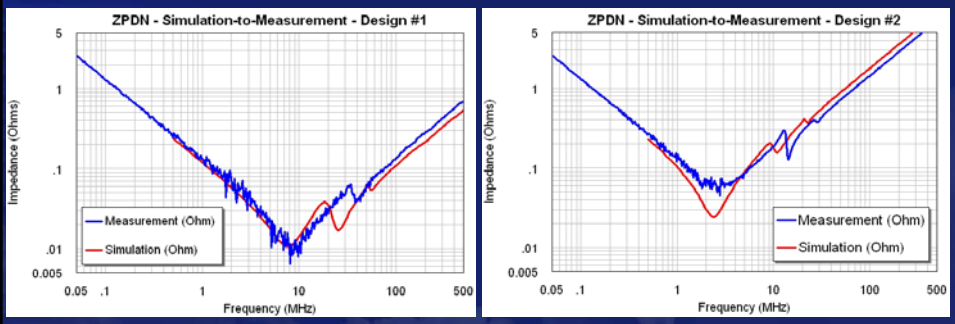
- Simulation models created to exactly match actual PCBs



3/2012 Improving Power Delivery in the Test Interface 23

Simulation-Measurement Correlation

- Simulation results show good correlation to measurement



3/2012 Improving Power Delivery in the Test Interface 24

Conclusion

- Power Delivery Network design is complicated
- PCB and contactor both play a critical role in the PDN
- Simulation can be used to better understand the PDN
- By understanding how each individual part of the design impacts the overall design, the PDN can be improved and optimized
- The focus on power integrity continues to increase

Additional Resources

"Signal and Power Integrity in the Test Interface",
Jason Mroczkowski and Ryan Satrom, BiTS 2011 Tutorial
(http://www.bitsworkshop.org/archive/archive2011/archive2011.htm)

New Interconnect Evaluation Metrics for Design Optimization

Se-Jung Moon
Richard Mellitz, Erkan Acar
Intel Corporation

2012 BiTS Workshop
March 4 - 7, 2012

Outline

- Motivation
- Previous Socket Design Optimization Study
- New Interconnect evaluation metrics
  - Power Spectral Density (PSD) of Random Bit Stream
  - Combination of S parameters and the PSD
- Validation
- Result
- Conclusion

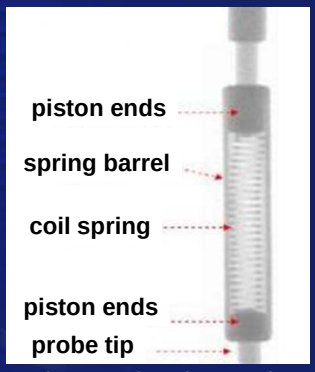
Motivation

There is no simple and clear performance metric for sockets

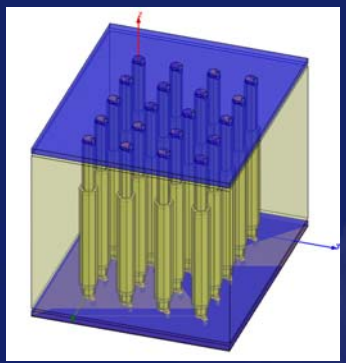
- **Insertion loss (IL), return loss (RL), and crosstalk are frequency dependent values and Single frequency values or frequency masks and are not sufficient criteria for evaluating interconnects.**
- **Computation of high-speed IO eye opening can be used as measure of an interconnect but is complicated and Simulation collateral is not available to 3rd party vendors like socket developers**

Need: Easily obtainable and efficient interconnect evaluation metrics

Spring-Probe Socket



X-ray picture of spring-probe pins

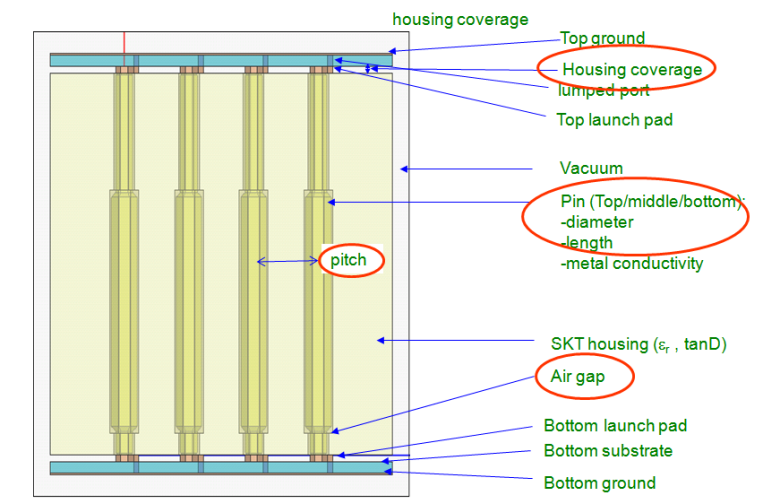


3D EM socket model

- In this numerical model, no cavity and no spring is inside the pins.

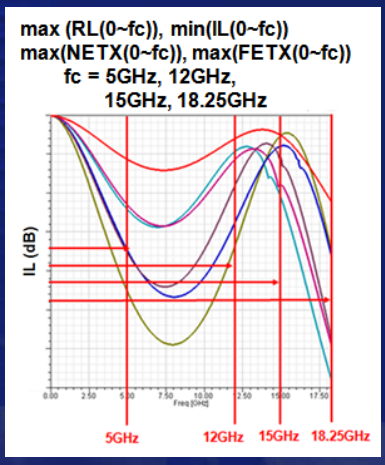
(*) is captured from http://www.ems007.com/pages/zone.cgi?a=60561&artpg=78&topic=0

Socket Parameters

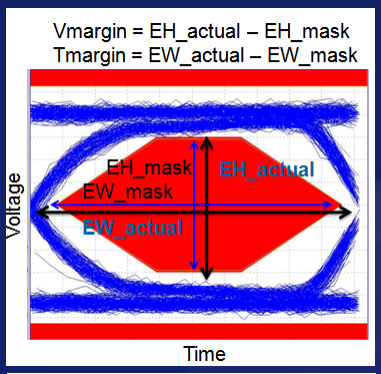


Up-to-now Evaluation Metrics

Frequency-Domain Metrics



Time-Domain Metrics



Findings From Previous Study

- When we optimize socket design using frequency domain metrics, the optimized design structure changes depending on the frequency range of interest.
- Socket design optimization over 0 to 5 GHz range of the fundamental frequency matches with the one in time-domain metric.

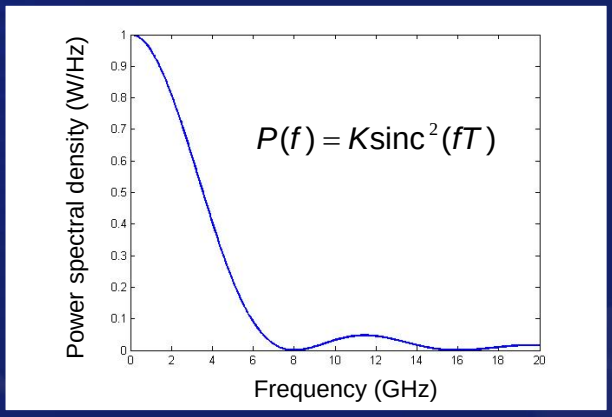
Theory (1) : Power Spectral Density for Random Binary Wave

For a random binary wave that represents binary symbols 1 and 0 through amplitude + A and – A volts respectively with unit interval T, power spectral density can be presented as

$$P(f) = K\,\mathrm{sinc}^2(fT)$$

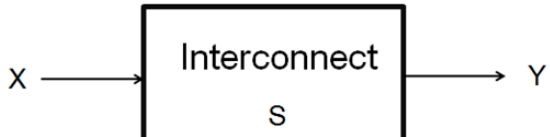
where $K = A^2T$. The unit is W/Hz.

sinc Function



Input PSD for PCIe Gen3 is plotted. Majority of the input power concentrates in lower frequency region.

Theory (2): New Component Evaluation Metrics using PSD



$$Y = SX$$

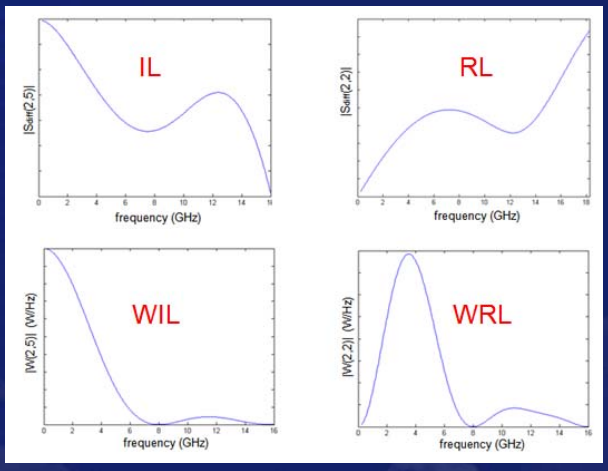
$$|Y| = |S||X|$$

$$|Y|^2 = |S|^2|X|^2$$

$$|Y|^2 = |S|^2 \{K\text{sinc}^2(fT)\}$$

$$IW = \alpha \int_0^{f_{max}} W(f)df = \alpha \int_0^{f\,max} |S(f)|^2 \text{sinc}^2(fT)df$$

IL, RL vs. WIL, WRL



WIL and WRL are actually PSD of output data. Also the output power concentrated in lower frequency region.

Theory (3):New Component Evaluation Metrics

$$IW_{ij} = \alpha \int_0^{f_{max}} W_{ij}(f)df = \alpha \int_0^{f\,max} |S_{ij}(f)|^2 \,\mathrm{sinc}^2(fT)df$$

Integral of weighted IL -> IWIL

Integral of weighted RL -> IWRL

new metrics

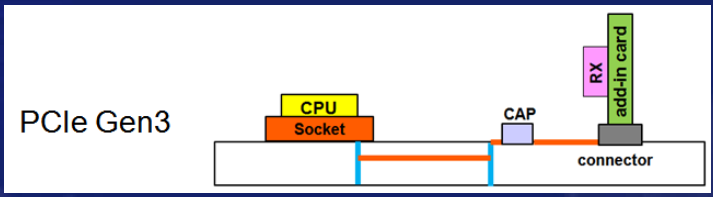
IWIL : overall power which can pass through a socket. Bigger IWIL will be better.
IWRL: overall power which is reflecting back from a socket. Smaller IWRL will be better.

Validation

IWIL
IWRL

Compared to:

Vmargin
Tmargin



A socket design is optimized in terms of IWIL and IWRL and compared to the optimized design which was done in terms of Vmargin and Tmargin.

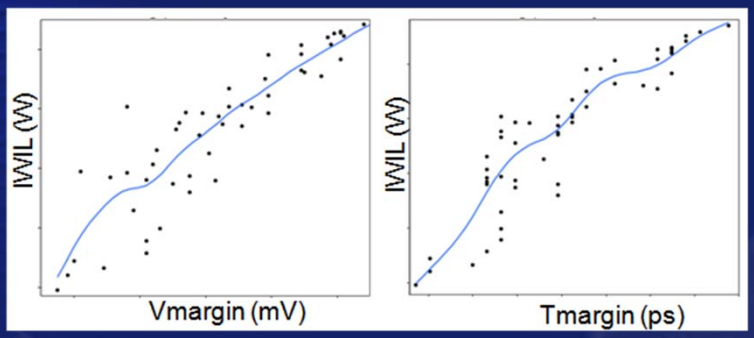
Validation (2): 9 Parameters under Consideration

- **9 parameters from the parameterized socket model are used for DOE screening**
- **4 parameters are selected for impact analysis:**
  1. **Pin Middle length**
  2. **Pin Middle Diameter**
  3. **Airgap**
  4. **Pitch**

Validation (2) : DOE Parameters and Settings

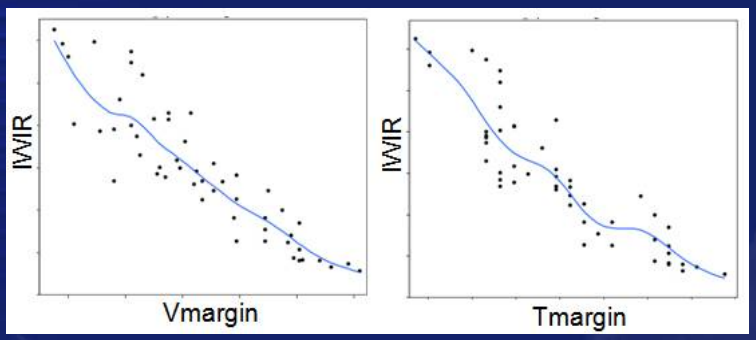
- Take the typical values of 4 parameters and tweak the parameters with 10% of the typical values.
- 10% is small enough for RSM (Response Surface Methodology) and larger than manufacturing tolerance to see design to design variation.

Result (1): IWIL vs. Vmargin/Tmargin



IWIL shows positive correlation with Vmargin and Tmargin, which indicates we can use IWIL as a socket evaluation metric instead of Vmargin and Tmargin.

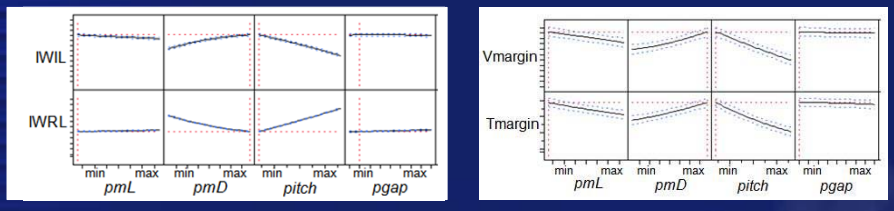
Result (2): IWRL vs. Vmargin/Tmargin



IWRL shows negative correlation with Vmargin and Tmargin, which indicates we can use IWIR as a socket evaluation metric instead of Vmargin and Tmargin.

Result (3):Optimized Socket Design

Frequency-Domain **Time-Domain**



The value at the cross-section of two red dotted lines in each box is the dimension of an optimized socket design. Two optimized designs are matching each other, which validates IWIL and IWRL as new socket evaluation metrics.

Conclusion

- IWIL and IWIR metrics used for socket evaluation and optimization are as good as full channel simulations
- These metrics can be obtained much easily and they can be used to quantify the performance of the sockets effectively
  - Using these metrics instead of single frequency IL& IR is highly recommendable.
  - There is no need to run full channel simulations when these metrics are used

Future Work

- Apply the same method to a Single-ended bus, for example DDR memory bus to validate these new metrics.
- Test the crosstalk parts in the S-parameters.

Acknowledgement

- Xiaoning Ye
- Steven K. Krooswyk