Session 5

ARCHIVE 2012

DESIGNING FOR PERFORMANCE

It just wouldn't be a BiTS Workshop without a session devoted entirely to novel socket designs. Every year, there are new devices on the market and ever critical factors like witness marks on smaller solder balls and minimum contact force that need a socket designed specifically for them. The three papers in this session address three distinctly different socket applications. The first talks to spring probes for fine pitch, then the second paper reviews the heat path for a device mounted in a socket and discusses the important variables in a thermal analysis. Lastly, we'll examine a unique design for a coaxial socket.

Are Spring Contact Probes Valid at Fine Pitch?

Jon Diller, Dr. Jiachun (Frank) Zhou—Interconnect Devices, Inc.

Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application

Nathanaël Loiseau—Presto Engineering
Marco Michi, Dr. James Forster—Wells-CTI

Wall-extended Coaxial Socket

Collins Sun, Justin Liu, Jack Liang—WinWay Technology Co., Ltd.
Kuan-Chung Lu, Tzyy-Sheng Horng—National Sun Yat-Sen University

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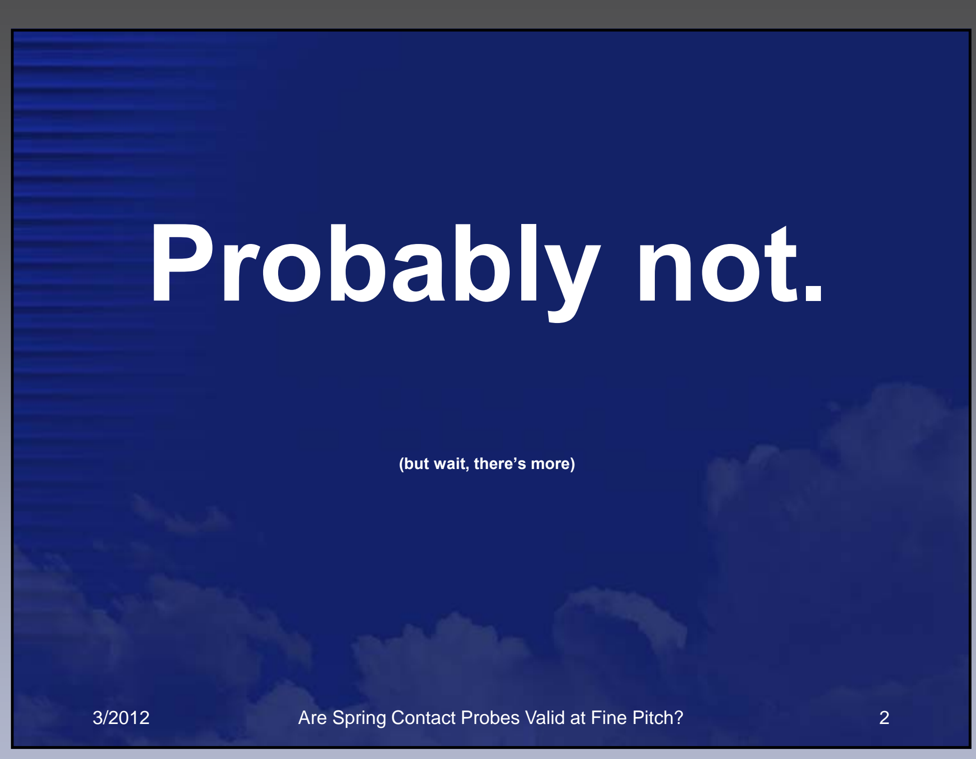
Are Spring Contact Probes Valid at Fine Pitch?
Dr. Jiachun (Frank) Zhou, Jon Diller
Interconnect Devices, Inc.
BiTS
Burn-in & Test Strategies Workshop
2012 BiTS Workshop
March 4 - 7, 2012
IDI
INTERCONNECT DEVICES, INC.
smiths interconnect


Probably not.
(but wait, there's more)
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Are Spring Contact Probes Valid at Fine Pitch?
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Market Requirements

Primarily WLCSP (now) and PoP (pretty soon)

- 0.3 pitch WLCSP bump Ø0.21; 0.2 with Ø0.115 extant
- PoP primarily lands under solder resist or balls

Test Technology Status Quo

- WLCSP on probers, inline cleaning, >200 UPH, expected cycle life >500K
- PoP in pick-and-place applications, offline cleaning, triple-digit UPH, expected cycle life 100-250K

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Current Methodology

Vertical Probe Technology

- Excellent cycle life, SI, reliability, easy to align
- Limited compliance
- Significant initial cost
- Not field serviceable
- Not applicable to PoP

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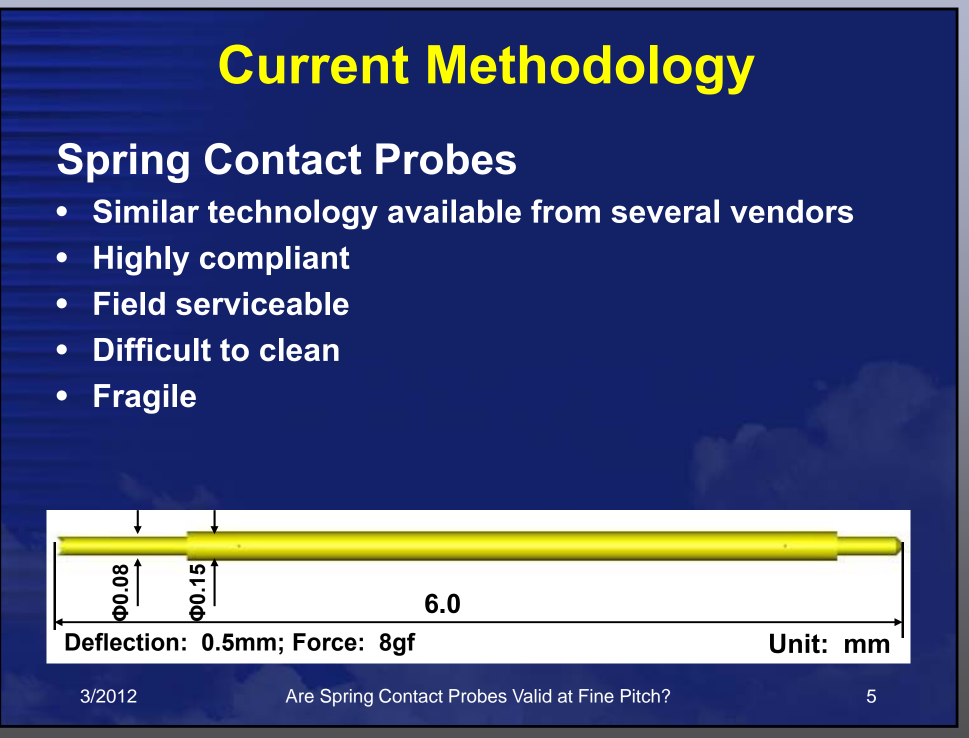
Current Methodology
Spring Contact Probes
• Similar technology available from several vendors
• Highly compliant
• Field serviceable
• Difficult to clean
• Fragile
Φ0.08
Φ0.15
6.0
Deflection: 0.5mm; Force: 8gf
Unit: mm
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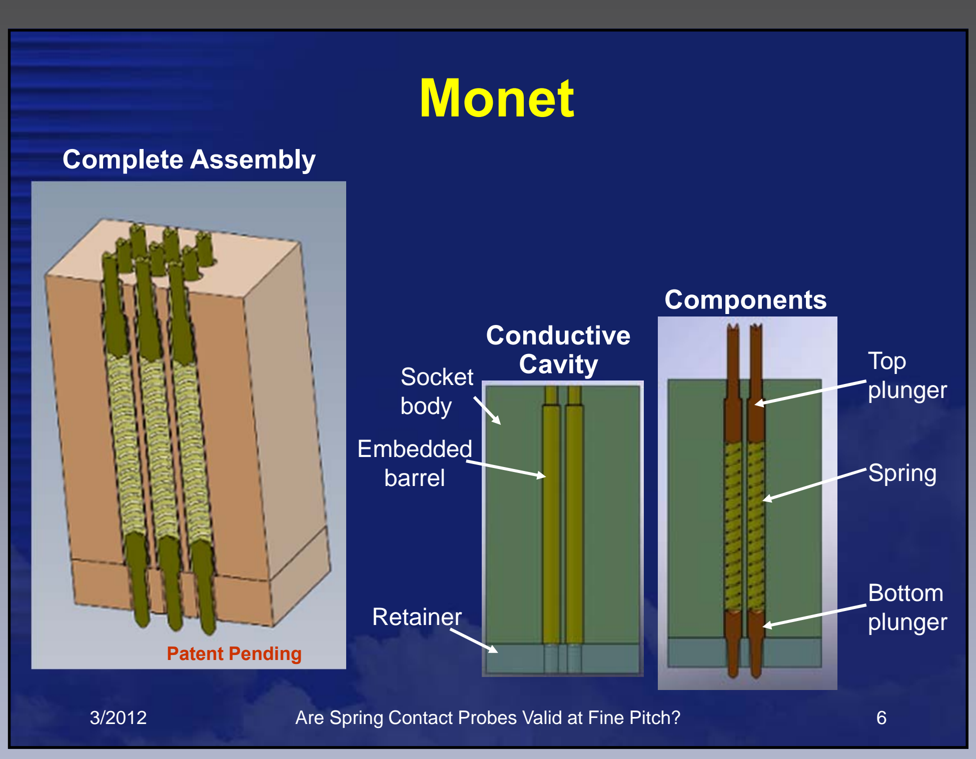
Monet
Complete Assembly
Patent Pending
Conductive Cavity
Components
Socket body
Embedded barrel
Retainer
Top plunger
Spring
Bottom plunger
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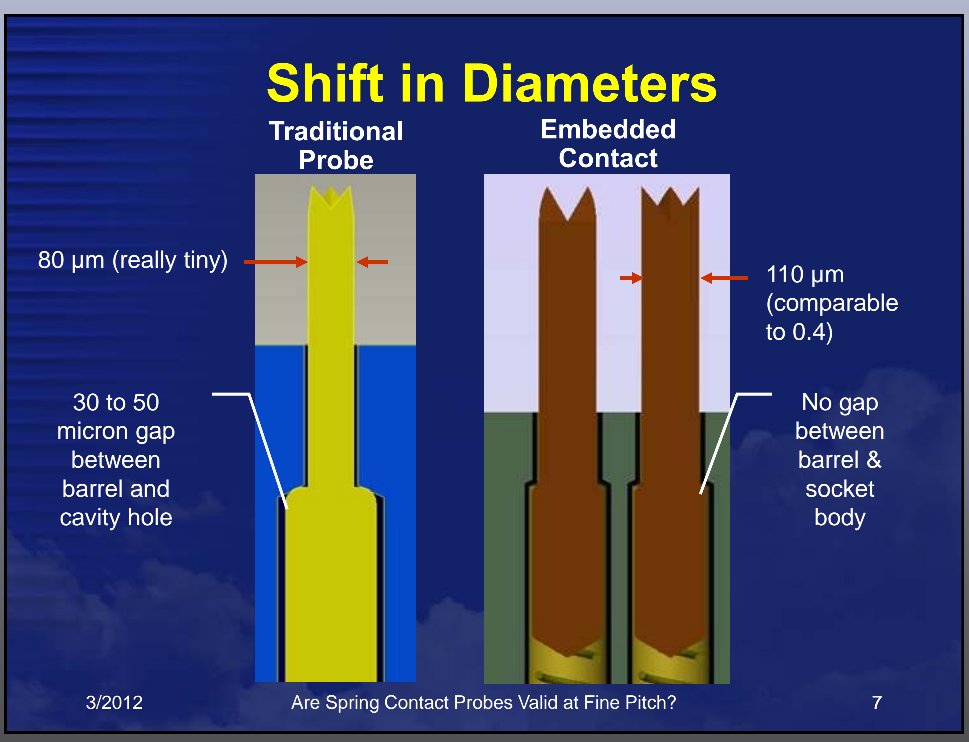

Alignment Improvement

Several Factors

- One less gap
- Improved aspect ratio of hole in plastic
- Larger diameter plunger is more concentric
- Electroforming produces high concentricity of 'barrel'
- Retainer plate true position does not affect top plunger

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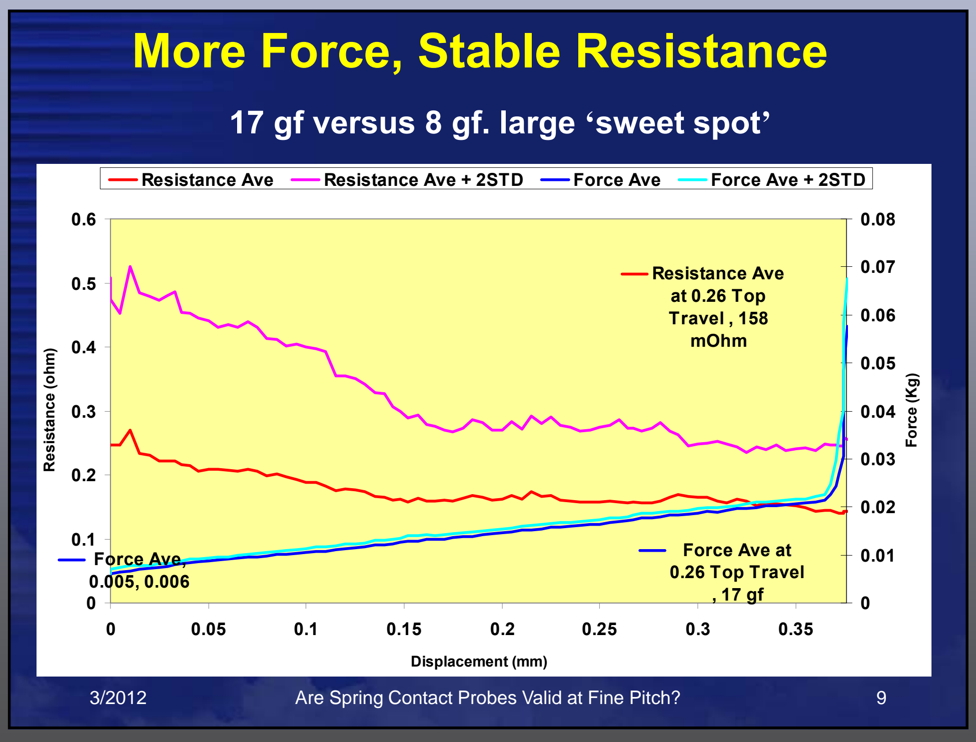

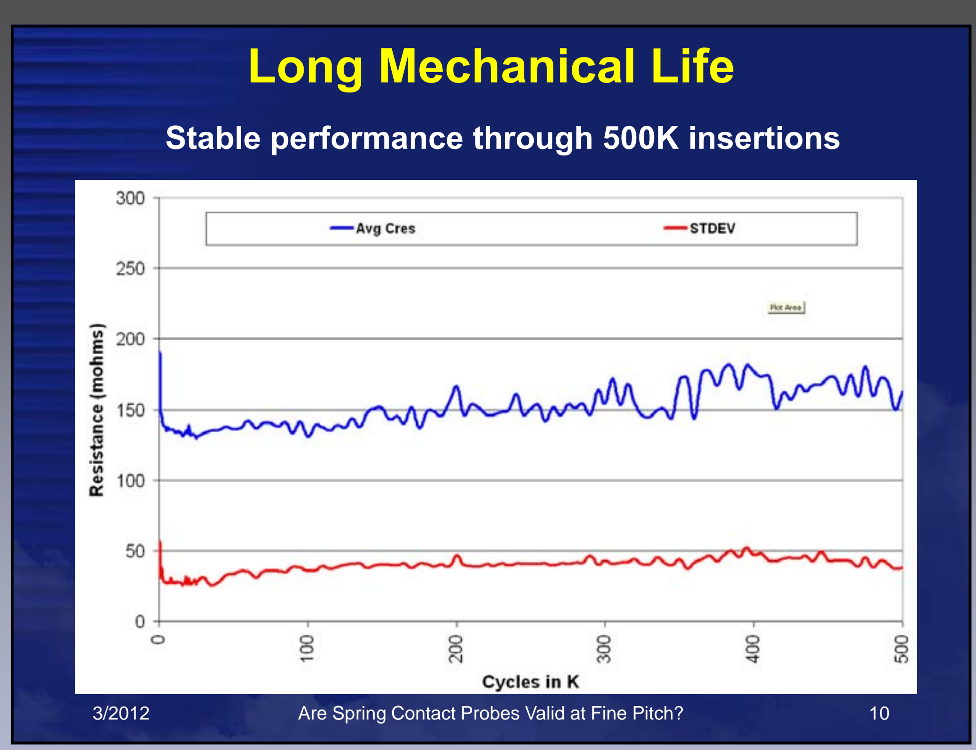

Paper #1
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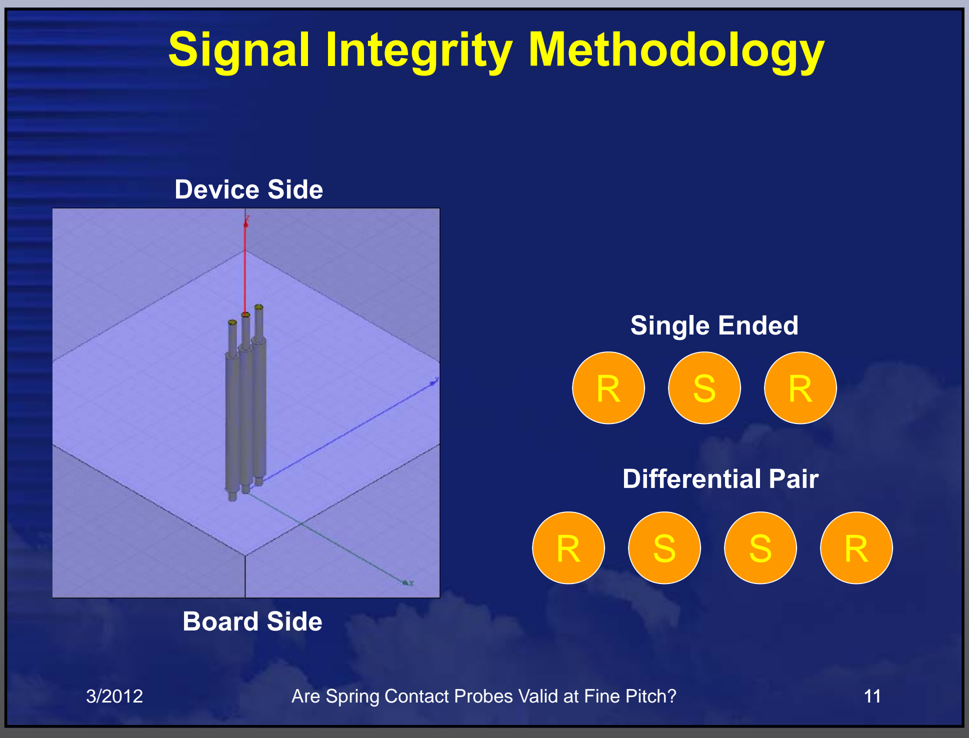
Signal Integrity Methodology
Device Side
Board Side
Single Ended
R S R
Differential Pair
R S S R
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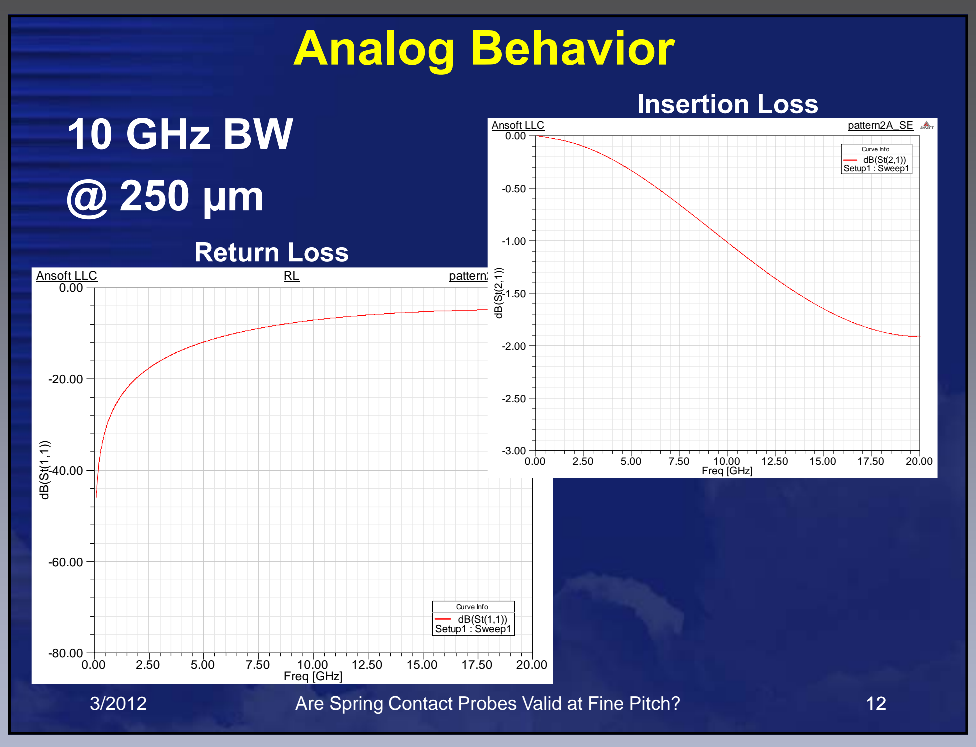
Analog Behavior
10 GHz BW
@ 250 µm
Insertion Loss
Return Loss
Ansoft LLC
pattern2A_SE
dB(St(2,1))
Setup1 : Sweep1
Freq [GHz]
RL
dB(St(1,1))
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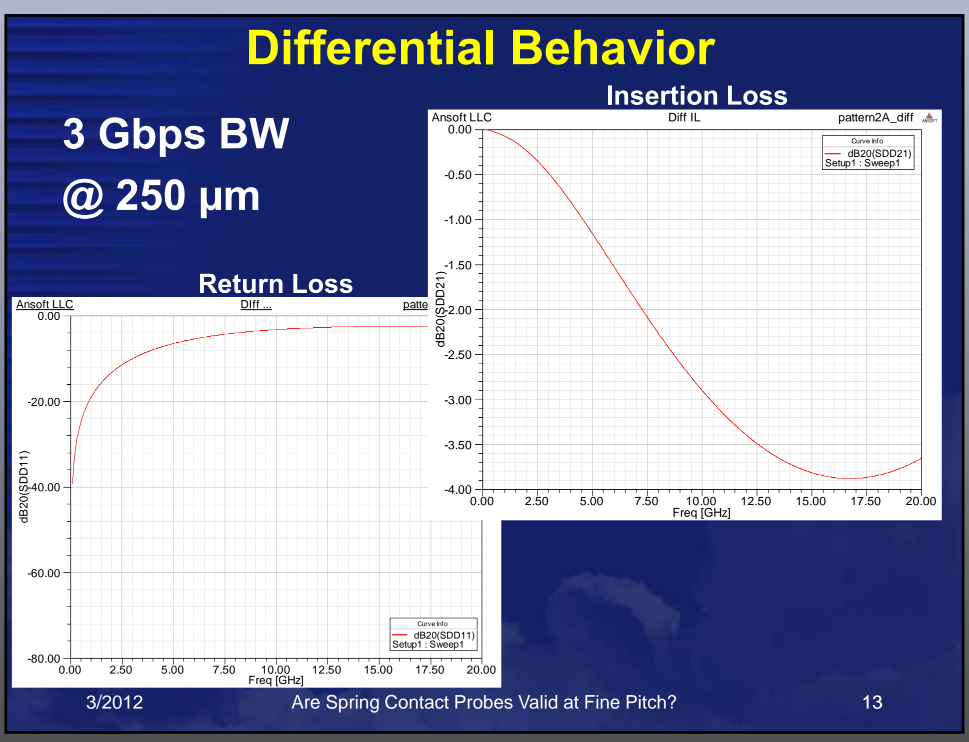
Differential Behavior
3 Gbps BW
@ 250 µm
Insertion Loss
Ansoft LLC
Diff IL
pattern2A_diff
dB20(SDD21)
Setup1 : Sweep1
Freq [GHz]
Return Loss
Ansoft LLC
Diff ...
dB20(SDD11)
Setup1 : Sweep1
Freq [GHz]
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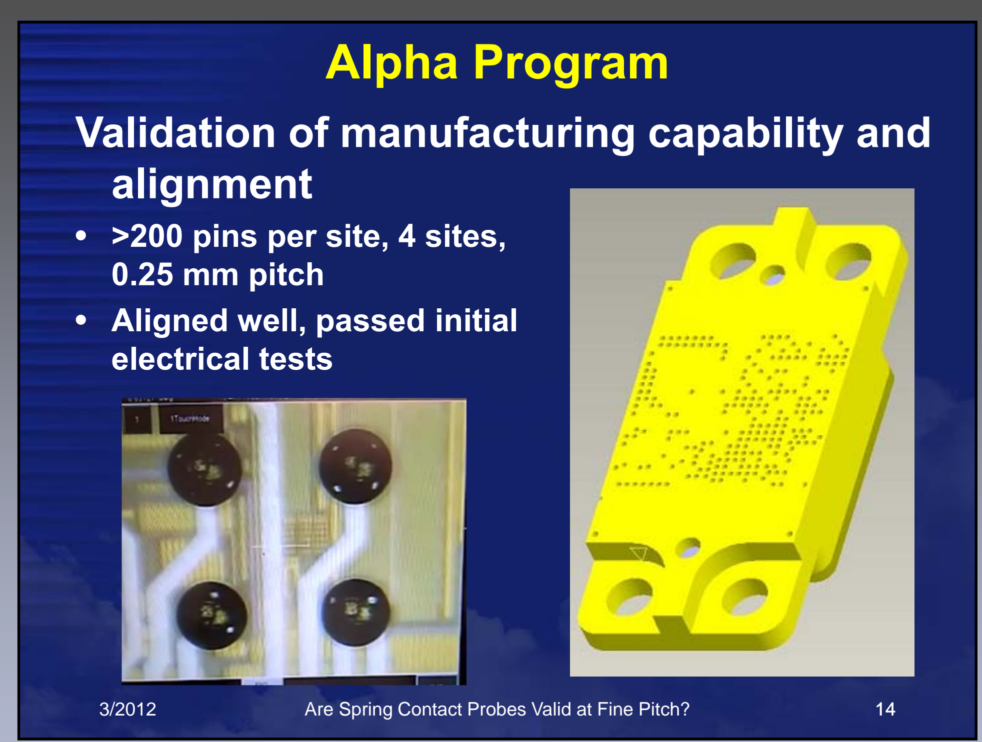
Alpha Program
Validation of manufacturing capability and alignment
• >200 pins per site, 4 sites, 0.25 mm pitch
• Aligned well, passed initial electrical tests
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Summary

Spring contact probes are a preferred technology for ≧0.4mm pitch but are challenged at finer pitches.

By embedding the probe barrel in the contactor body significant gains can be made in robustness, alignment, and signal integrity

This approach has potential for all WLCSP pitches: 250 µm, 200 µm, 180 µm, 150 µm

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Acknowledgements

The following persons and organizations were instrumental in the creation of this paper:

Praba Prabakaran, Khaled Elmadbouly, Brad Henry, Dave Henry, Kevin DeFord, Peter Fitzsimmons, Tim Marshall – Interconnect Devices, Inc.

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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application

Considerations in the selection of a socket for a plastic molded, thermal enhanced package

Nathanaël Loiseau+, Marco Michi* and Dr. James Forster*
+ Presto Engineering, * WELLS-CTI

2012 BiTS Workshop
March 4 - 7, 2012

Introduction

Today's device:
- More functionality
- Higher frequency
- More power / thermal dissipation
- Smaller size

Today's HTOL:
- From static to true application environment simulation
- Higher frequency
- Higher current
- More power / thermal dissipation

DESIGN OFFICE
H.T.O.L. !
No, I don't see that in my design specification

HTOL OFFICE
A.P.P.L.I.C.A.T.I.O.N. !
No, I don't see that in my reference norm

Thermal considerations of socket and test board become more important

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Content

- Technology challenge
- Environment challenge
- Thermal resistance definition
- DUT impact
- PCB impact
- Chamber impact
- Self heating impact
- Socket impact (DOE)
- Conclusion

Definition: HTOL High Temperature Operating Life

Typically 1000 hours at $T_{ambient}$ 125°C or $T_{junction}$ 150°C.

But other times and temps are performed

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Technology Challenge

SOURCE: Semiconductor Industry Association. The International Technology Roadmap for Semiconductors, 2009 Edition. SEMATECH, Austin, TX, 2009.

Package

- Smaller, integration of several functions, dies
- Power dissipation concentrated
- Smaller surface for thermal exchange

Advance process

- Smaller size, higher frequency
- IC Voltage ↘ ➔ IC current ↗ ➔ Current flow ↗ ➔ Socket & board self heating ↗

Customer willingness

- Static HTOL does not always reveal relevant failure mechanism
- Dynamic HTOL closer to real life conditions

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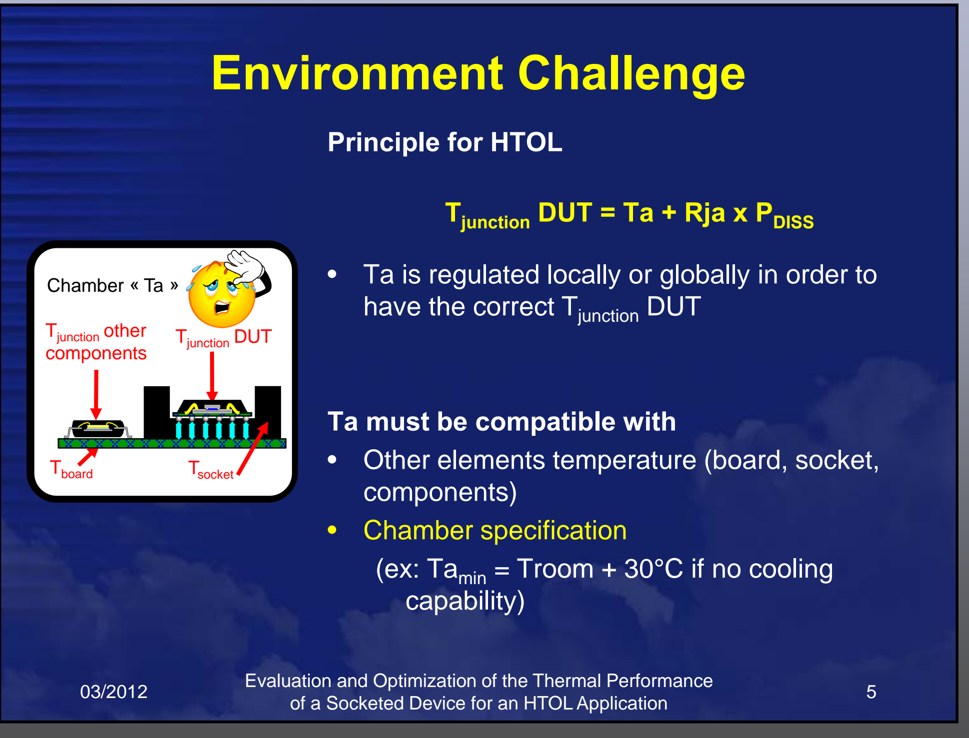
Environment Challenge
Principle for HTOL
T junction DUT = Ta + Rja x PDISS
Chamber « Ta »
T junction other components
T junction DUT
T board
T socket
Ta is regulated locally or globally in order to have the correct T junction DUT
Ta must be compatible with
Other elements temperature (board, socket, components)
Chamber specification
(ex: Ta min = Troom + 30°C if no cooling capability)
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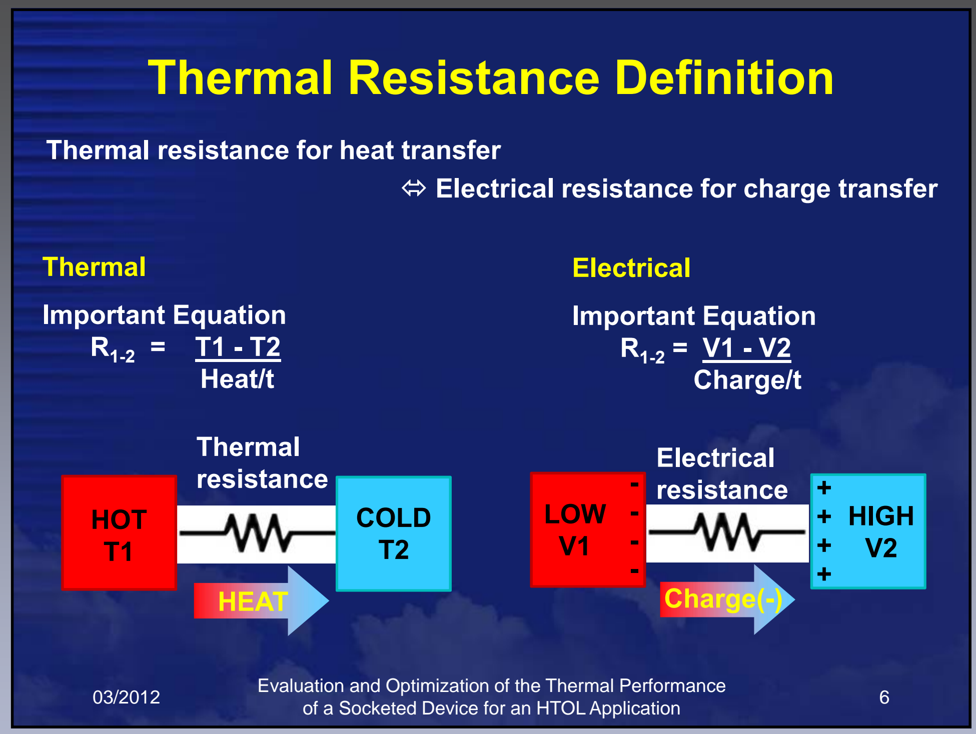
Thermal Resistance Definition
Thermal resistance for heat transfer
⇔ Electrical resistance for charge transfer
Thermal
Important Equation
R1-2 = T1 - T2 / Heat/t
Electrical
Important Equation
R1-2 = V1 - V2 / Charge/t
Thermal resistance
HOT T1
COLD T2
HEAT
Electrical resistance
LOW V1
HIGH V2
Charge(-)
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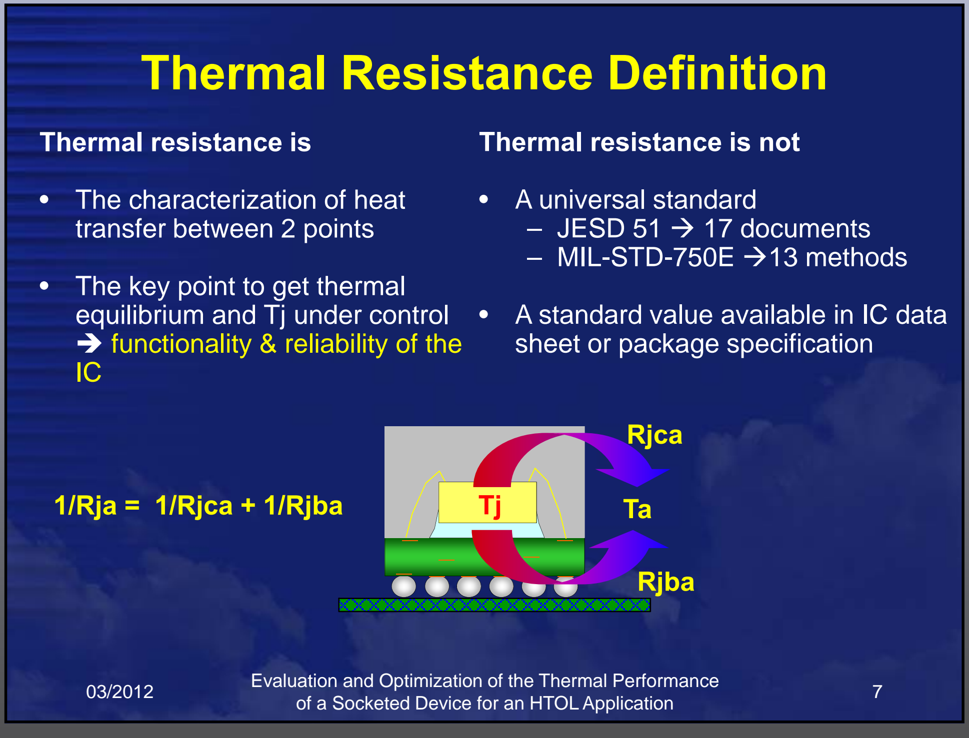
Thermal Resistance Definition
Thermal resistance is
• The characterization of heat transfer between 2 points
• The key point to get thermal equilibrium and Tj under control → functionality & reliability of the IC
Thermal resistance is not
• A universal standard
– JESD 51 → 17 documents
– MIL-STD-750E →13 methods
• A standard value available in IC data sheet or package specification
1/Rja = 1/Rjca + 1/Rjba
Rjca
Tj
Ta
Rjba
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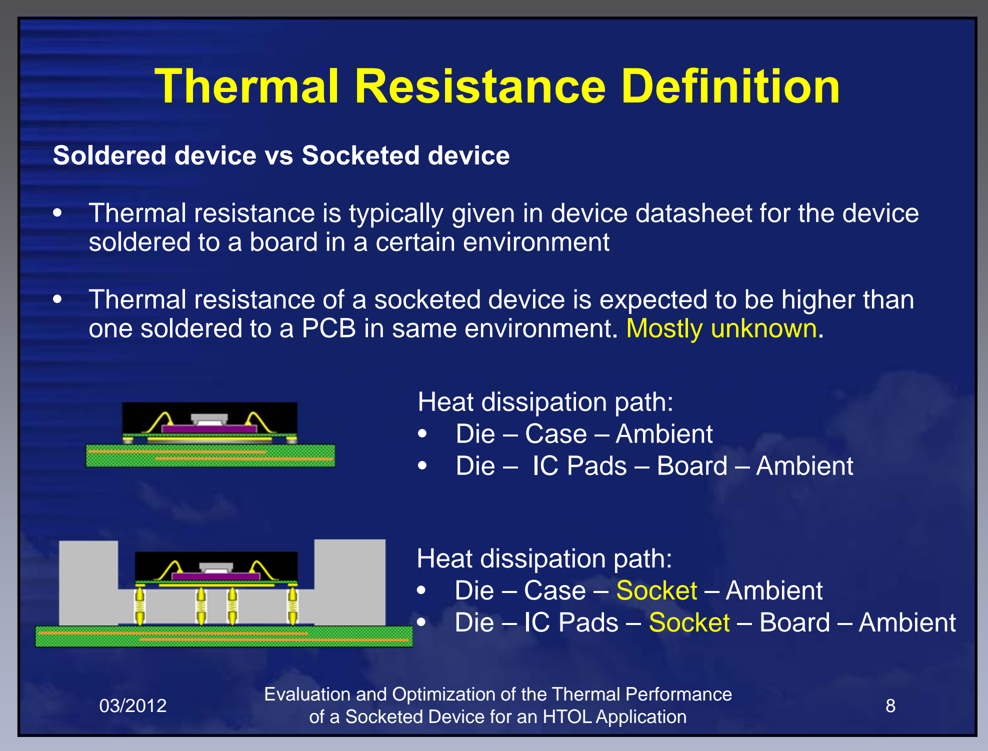
Thermal Resistance Definition
Soldered device vs Socketed device
• Thermal resistance is typically given in device datasheet for the device soldered to a board in a certain environment
• Thermal resistance of a socketed device is expected to be higher than one soldered to a PCB in same environment. Mostly unknown.
Heat dissipation path:
• Die – Case – Ambient
• Die – IC Pads – Board – Ambient
Heat dissipation path:
• Die – Case – Socket – Ambient
• Die – IC Pads – Socket – Board – Ambient
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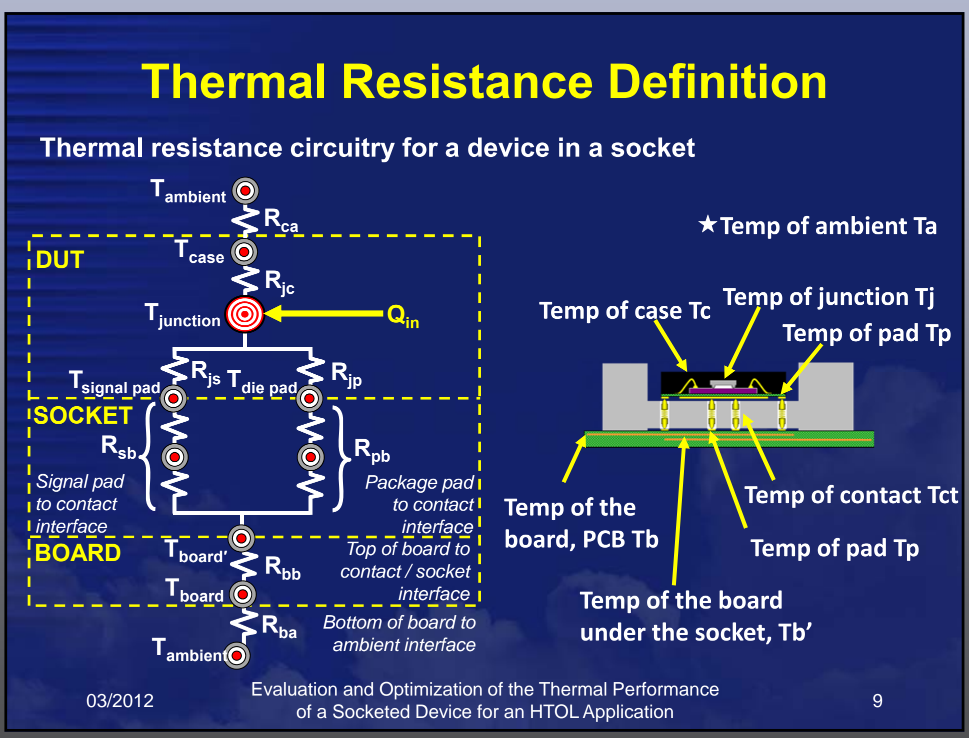
Thermal Resistance Definition
Thermal resistance circuitry for a device in a socket
T ambient
R ca
DUT
T case
R jc
T junction
Q in
T signal pad
R js
T die pad
R jp
SOCKET
R sb
R pb
Signal pad to contact interface
Package pad to contact interface
BOARD
T board'
R bb
Top of board to contact / socket interface
T board
R ba
Bottom of board to ambient interface
T ambient
★Temp of ambient Ta
Temp of case Tc
Temp of junction Tj
Temp of pad Tp
Temp of the board, PCB Tb
Temp of contact Tct
Temp of pad Tp
Temp of the board under the socket, Tb'
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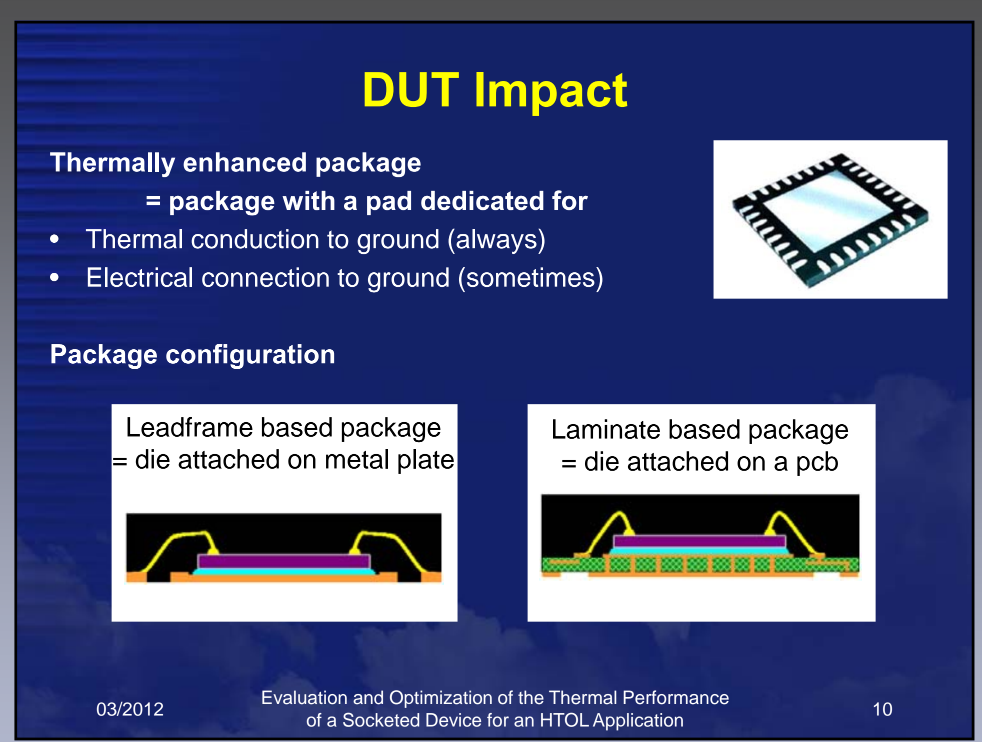
DUT Impact
Thermally enhanced package
= package with a pad dedicated for
• Thermal conduction to ground (always)
• Electrical connection to ground (sometimes)
Package configuration
Leadframe based package
= die attached on metal plate
Laminate based package
= die attached on a pcb
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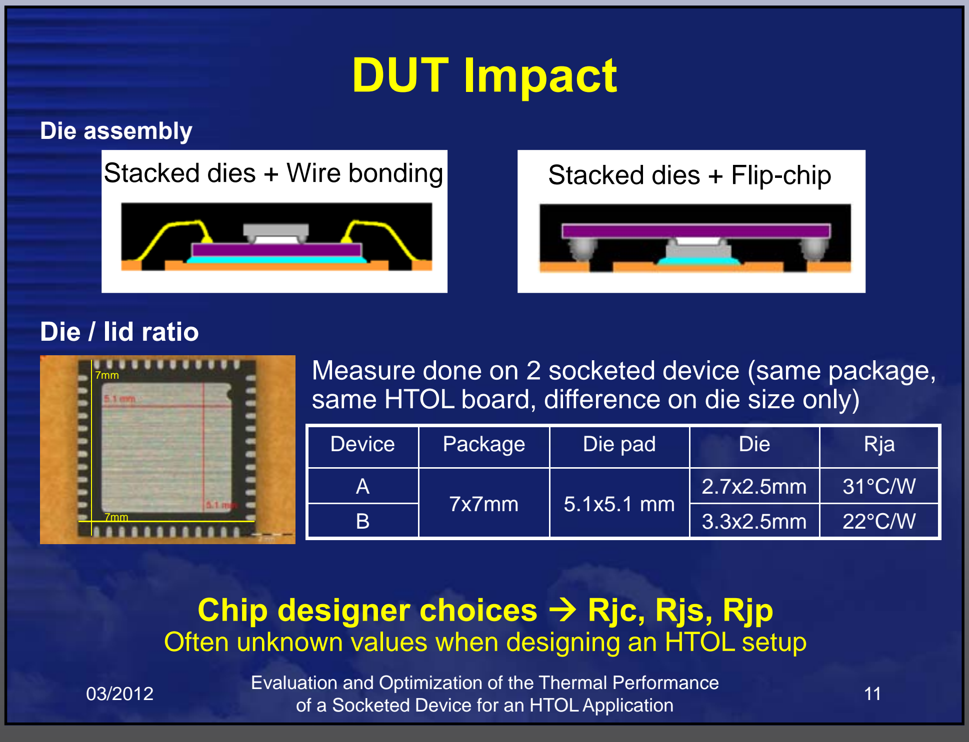

Device	Package	Die pad	Die	Rja
A	7x7mm	5.1x5.1 mm	2.7x2.5mm	31°C/W
B			3.3x2.5mm	22°C/W

PCB Impact

Example of Rja

HVQFN56 soldered on application boards in same environment

Application board #1			Application board #2		
PCB thickness (mm)	Nbr of layer	PCB size (mm)	PCB thickness (mm)	Nbr of layer	PCB size (mm)
1.17	10	30x60	1.43	10	35x80
Rja = 36.4 °C/W			**Rja = 31.6 °C/W**		

Material, size, thickness, stack up → Rbb, Rba

In HTOL, depend of chamber size and DUT requirements

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Chamber Impact

From previous BiTS presentations, HTOL chamber often seen like:

- A simple box
- A "tunnel" between BIB's
- "Fresh" air at one side
- Inconsistent air flow between boards
- Extraction of heat capability

For HTOL, JESD22-A108D:

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered.

For test cost reduction, most often:

- Maximize the number of BIB's in chamber
- Maximize the number of site per BIB

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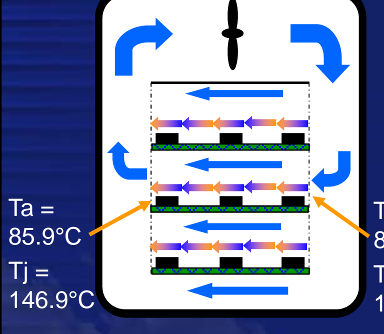
Chamber Impact

Experimental results with a 1.3W DUT

- Chamber and BIB populated in order to keep maximum air flow around sockets
- Air flow modified on a BIB position by adding a « box » on the socket



Chamber & Life-test Engineer choices → Rba, Rca

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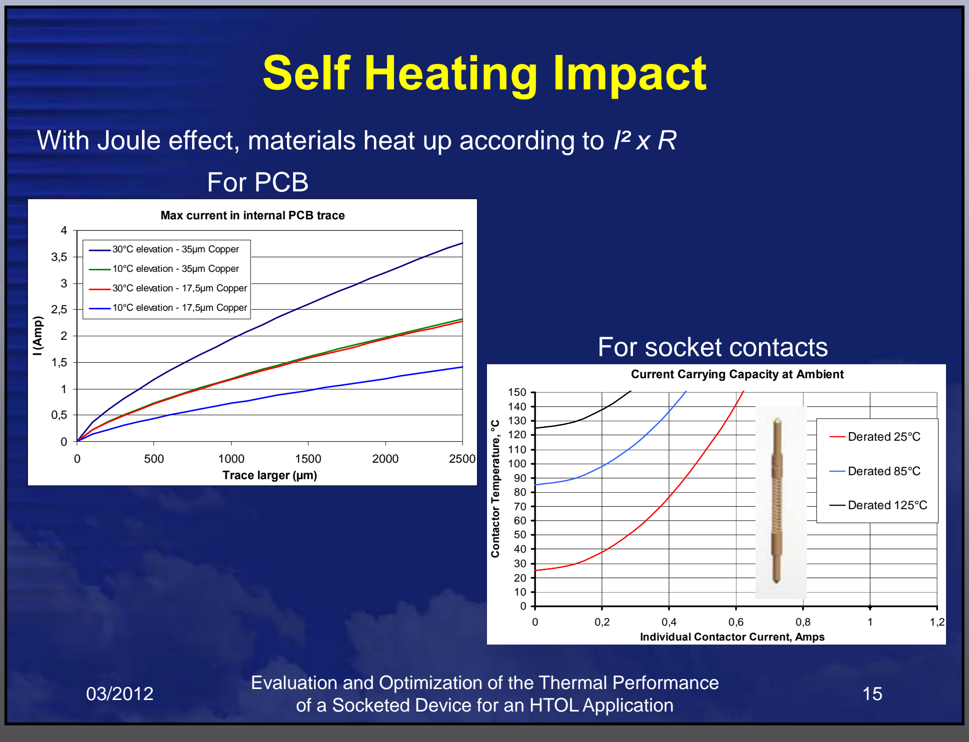
Self Heating Impact
With Joule effect, materials heat up according to I² x R
For PCB
Max current in internal PCB trace
30°C elevation - 35µm Copper
10°C elevation - 35µm Copper
30°C elevation - 17,5µm Copper
10°C elevation - 17,5µm Copper
I (Amp)
Trace larger (µm)
For socket contacts
Current Carrying Capacity at Ambient
Derated 25°C
Derated 85°C
Derated 125°C
Contactor Temperature, °C
Individual Contactor Current, Amps
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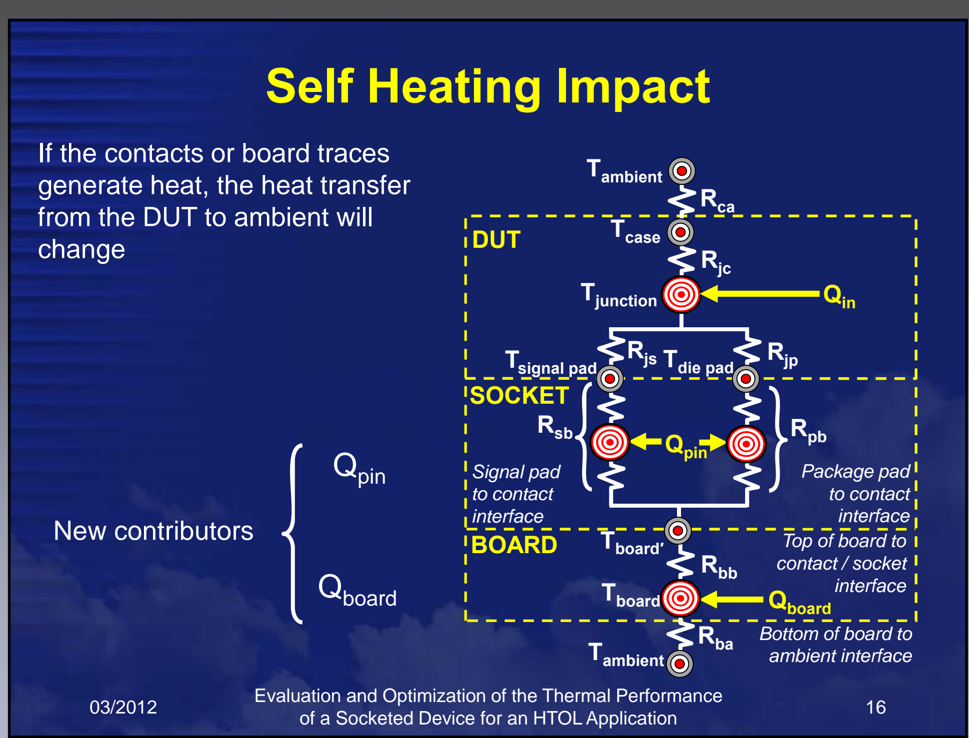
Self Heating Impact
If the contacts or board traces generate heat, the heat transfer from the DUT to ambient will change
New contributors
Qpin
Qboard
Tambient
Rca
DUT
Tcase
Rjc
Tjunction
Qin
Tsignal pad
Rjs
Tdie pad
Rjp
SOCKET
Rsb
Qpin
Rpb
Signal pad to contact interface
Package pad to contact interface
BOARD
Tboard'
Rbb
Top of board to contact / socket interface
Tboard
Qboard
Rba
Bottom of board to ambient interface
Tambient
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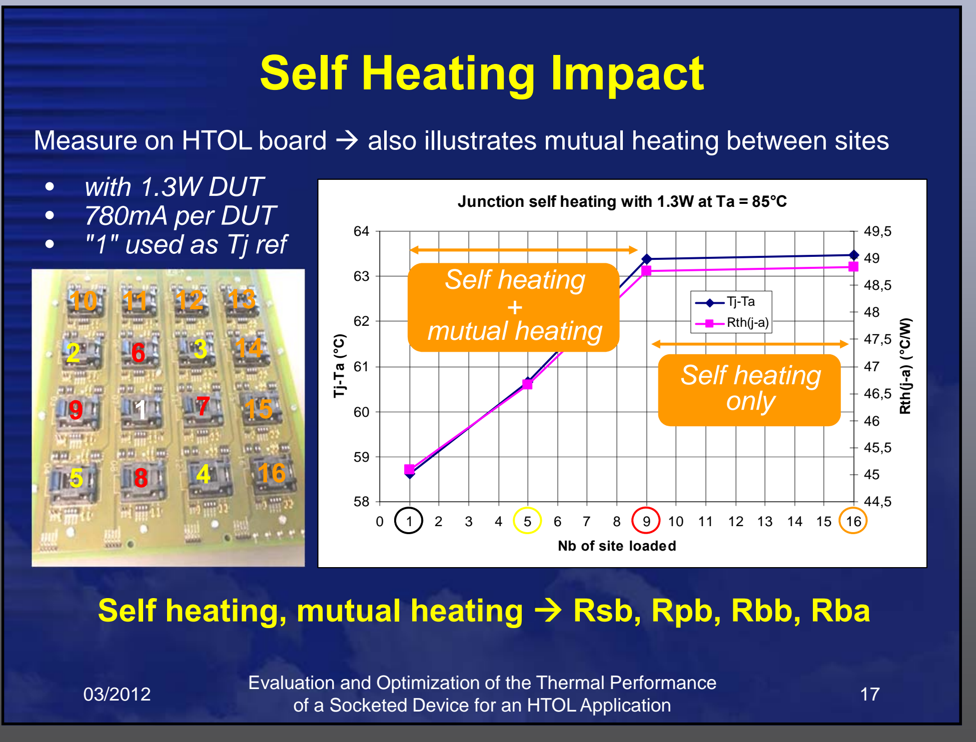

Socket Impact

DOE in order to evaluate impact of socket design on global Rja

DUT Vehicle :

- Thermal enhanced HVQFN56 8x8mm
- Laminate based
- 1.3W dissipation
- Always the same IC used

Socket Vehicle :

- Clamshell,
- Surface mount
- 10 different thermal designs

Board Vehicle :

- HTOL board 540x245mm,
- Full application mode simulated (800MHz signals in),
- 16 sites available
- 1 site loaded (always the same)

HTOL chamber Vehicle :

- 16 BIB position available,
- Board vehicle always loaded in same position
- Measure of Tj / Rja at minimum 3 temperatures (only 1 reported in this document)

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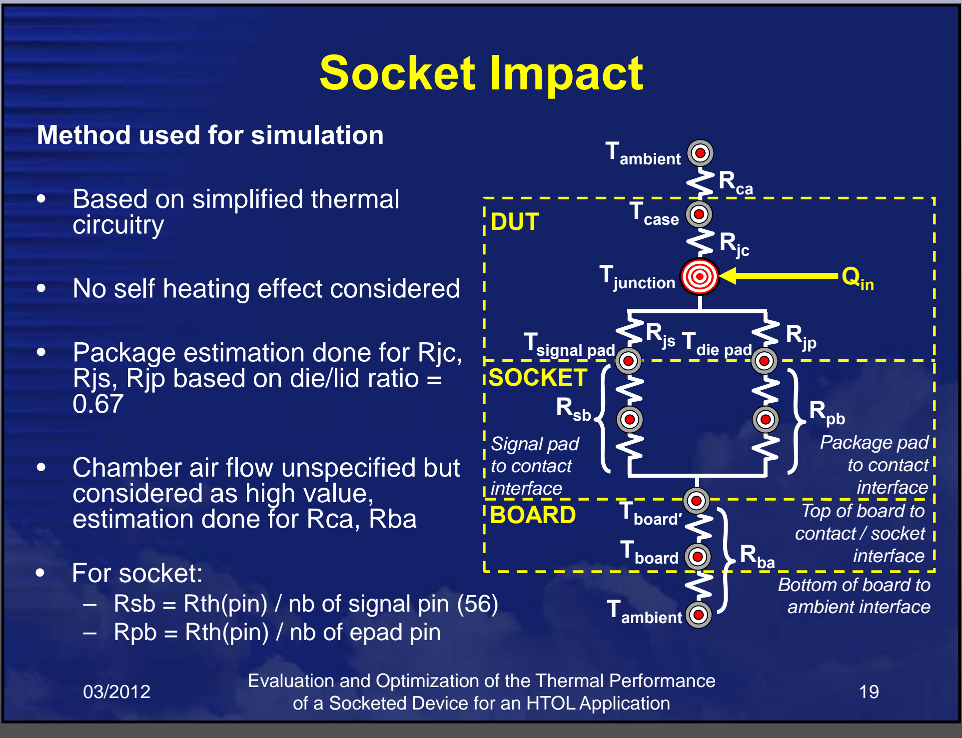
Socket Impact
Method used for simulation
Based on simplified thermal circuitry
No self heating effect considered
Package estimation done for Rjc, Rjs, Rjp based on die/lid ratio = 0.67
Chamber air flow unspecified but considered as high value, estimation done for Rca, Rba
For socket:
Rsb = Rth(pin) / nb of signal pin (56)
Rpb = Rth(pin) / nb of epad pin
T ambient
R ca
DUT
T case
R jc
T junction
Q in
T signal pad
R js
T die pad
R jp
SOCKET
R sb
R pb
Signal pad to contact interface
Package pad to contact interface
BOARD
T board'
T board
R ba
Top of board to contact / socket interface
Bottom of board to ambient interface
T ambient
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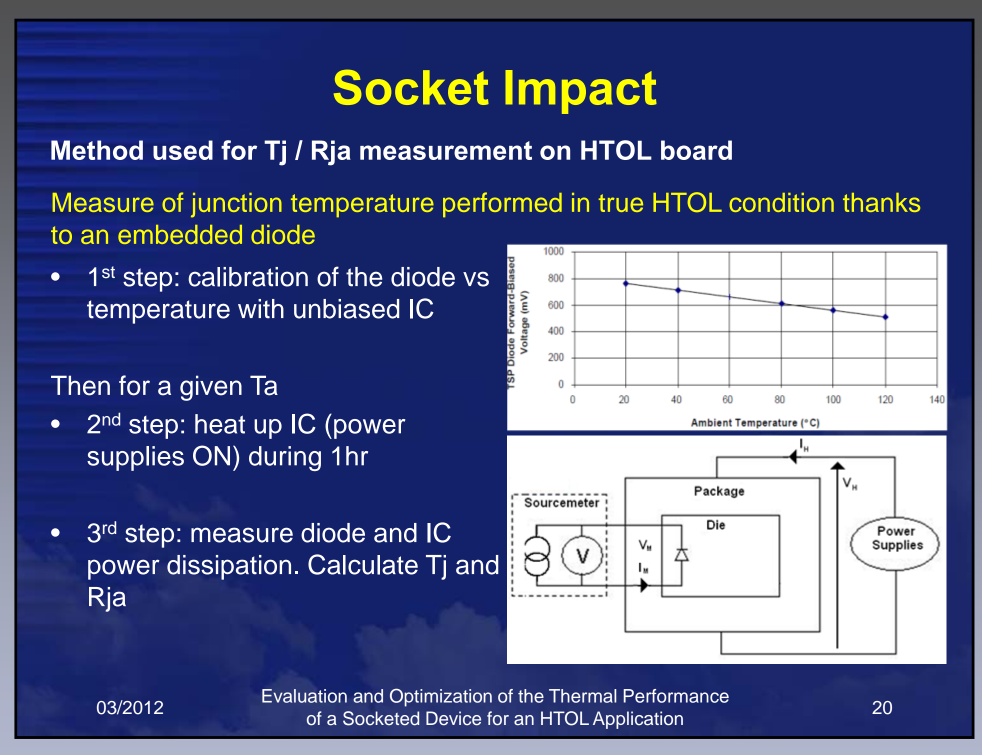
Socket Impact
Method used for Tj / Rja measurement on HTOL board
Measure of junction temperature performed in true HTOL condition thanks to an embedded diode
1st step: calibration of the diode vs temperature with unbiased IC
Then for a given Ta
2nd step: heat up IC (power supplies ON) during 1hr
3rd step: measure diode and IC power dissipation. Calculate Tj and Rja
TSP Diode Forward-Biased Voltage (mV)
Ambient Temperature (°C)
Sourcemeter
Package
Die
Power Supplies
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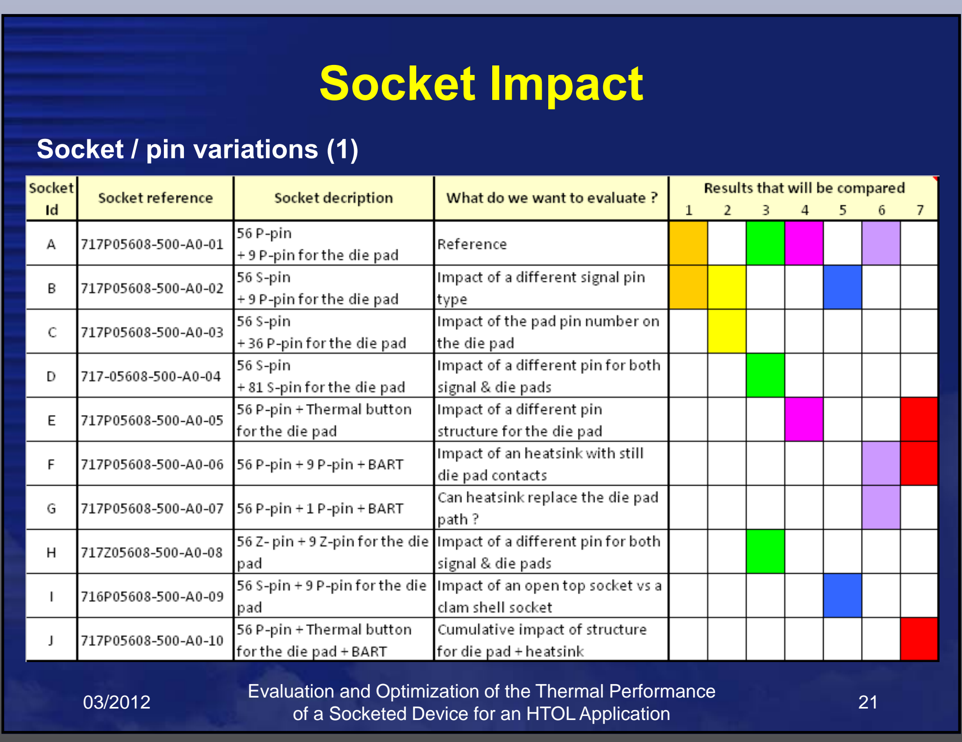
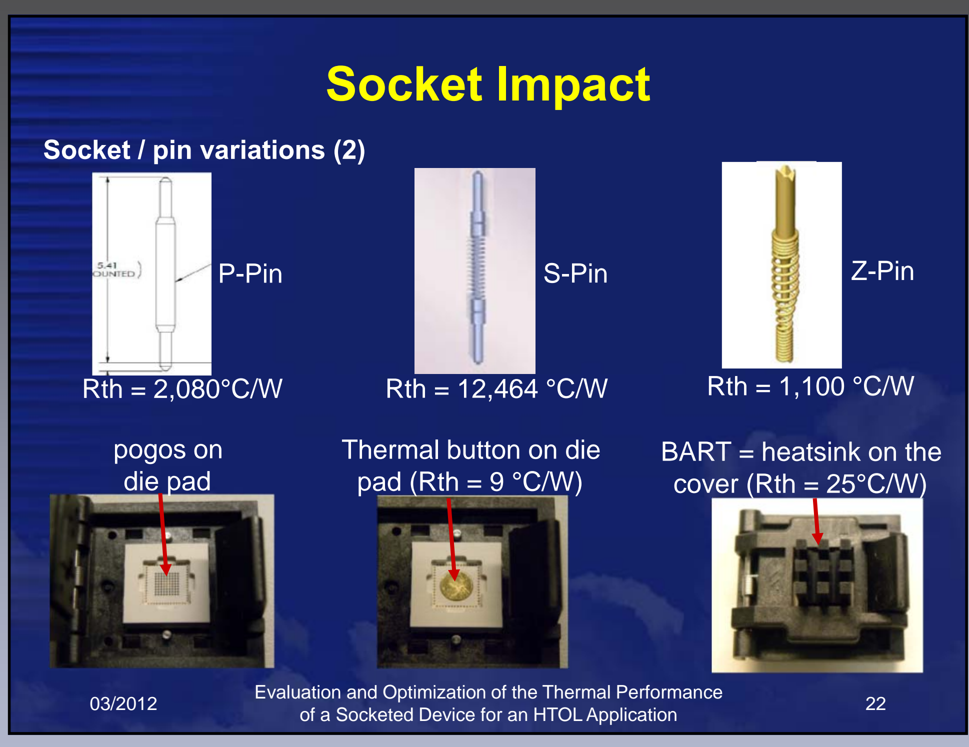
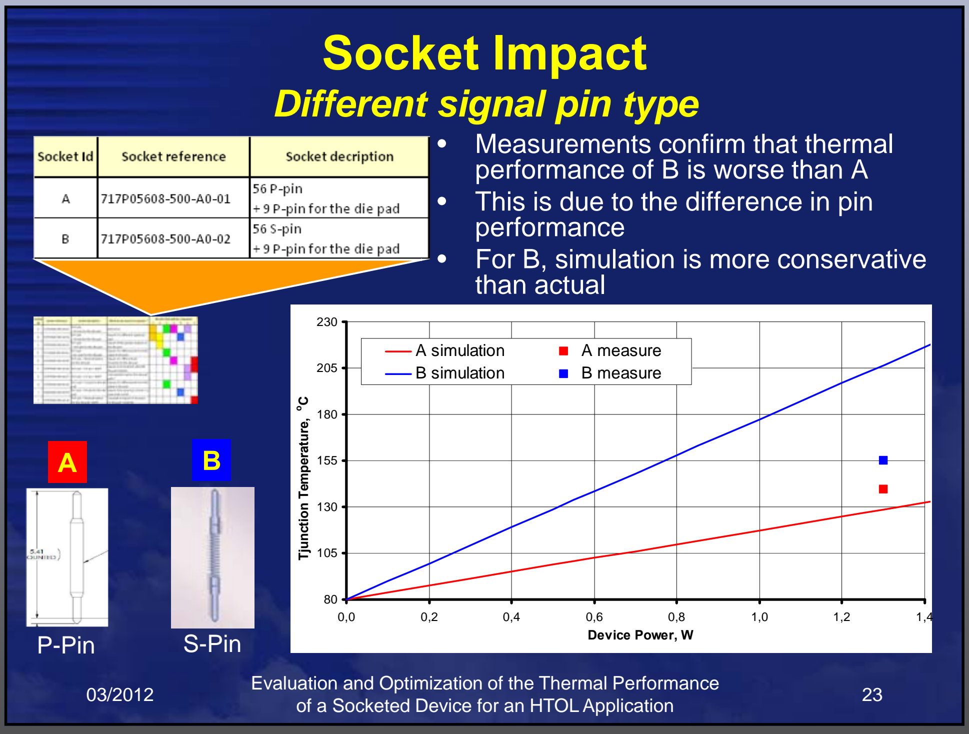


Socket Id	Socket reference	Socket decription	What do we want to evaluate ?	Results that will be compared 1	2	3	4	5	6	7
A	717P05608-500-A0-01	56 P-pin + 9 P-pin for the die pad	Reference							
B	717P05608-500-A0-02	56 S-pin + 9 P-pin for the die pad	Impact of a different signal pin type							
C	717P05608-500-A0-03	56 S-pin + 36 P-pin for the die pad	Impact of the pad pin number on the die pad							
D	717-05608-500-A0-04	56 S-pin + 81 S-pin for the die pad	Impact of a different pin for both signal & die pads							
E	717P05608-500-A0-05	56 P-pin + Thermal button for the die pad	Impact of a different pin structure for the die pad							
F	717P05608-500-A0-06	56 P-pin + 9 P-pin + BART	Impact of an heatsink with still die pad contacts							
G	717P05608-500-A0-07	56 P-pin + 1 P-pin + BART	Can heatsink replace the die pad path ?							
H	717Z05608-500-A0-08	56 Z- pin + 9 Z-pin for the die pad	Impact of a different pin for both signal & die pads							
I	716P05608-500-A0-09	56 S-pin + 9 P-pin for the die pad	Impact of an open top socket vs a clam shell socket							
J	717P05608-500-A0-10	56 P-pin + Thermal button for the die pad + BART	Cumulative impact of structure for die pad + heatsink							




Socket Impact
Different signal pin type
Socket Id | Socket reference | Socket decription
A | 717P05608-500-A0-01 | 56 P-pin + 9 P-pin for the die pad
B | 717P05608-500-A0-02 | 56 S-pin + 9 P-pin for the die pad
• Measurements confirm that thermal performance of B is worse than A
• This is due to the difference in pin performance
• For B, simulation is more conservative than actual
A
B
P-Pin
S-Pin
A simulation
B simulation
A measure
B measure
Tjunction Temperature, °C
Device Power, W
230
205
180
155
130
105
80
0,0
0,2
0,4
0,6
0,8
1,0
1,2
1,4
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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application
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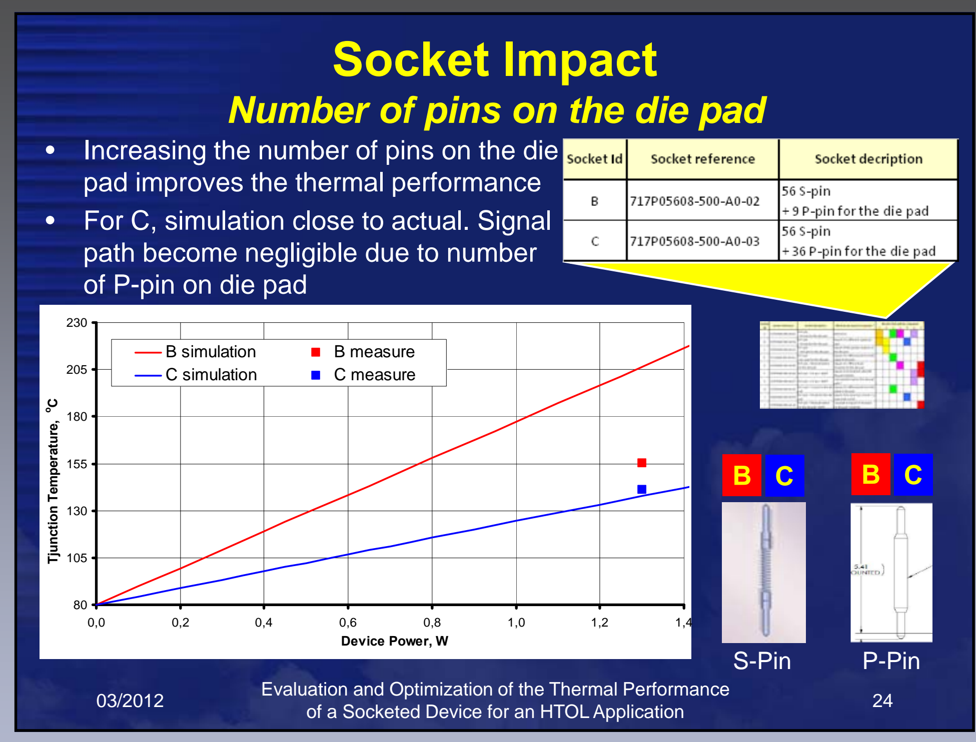
Socket Impact
Number of pins on the die pad
• Increasing the number of pins on the die pad improves the thermal performance
• For C, simulation close to actual. Signal path become negligible due to number of P-pin on die pad
Socket Id | Socket reference | Socket decription
B | 717P05608-500-A0-02 | 56 S-pin + 9 P-pin for the die pad
C | 717P05608-500-A0-03 | 56 S-pin + 36 P-pin for the die pad
B simulation
C simulation
B measure
C measure
Tjunction Temperature, °C
Device Power, W
230
205
180
155
130
105
80
0,0
0,2
0,4
0,6
0,8
1,0
1,2
1,4
B C
S-Pin
P-Pin
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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application
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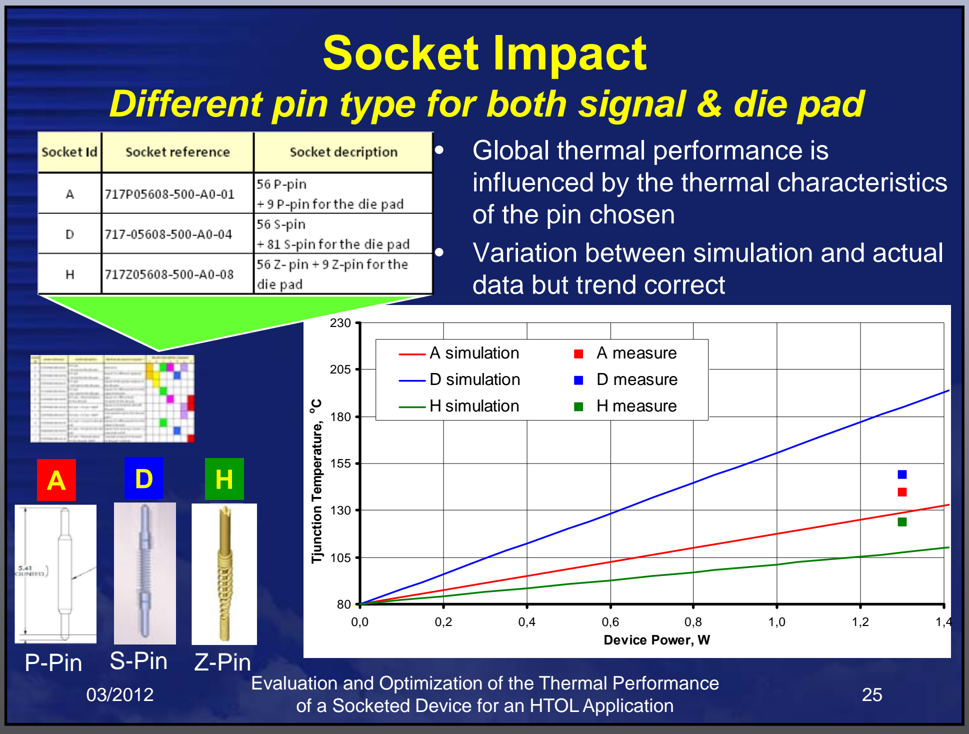
Socket Impact
Different pin type for both signal & die pad
Socket Id | Socket reference | Socket decription
A | 717P05608-500-A0-01 | 56 P-pin + 9 P-pin for the die pad
D | 717-05608-500-A0-04 | 56 S-pin + 81 S-pin for the die pad
H | 717Z05608-500-A0-08 | 56 Z- pin + 9 Z-pin for the die pad
Global thermal performance is influenced by the thermal characteristics of the pin chosen
Variation between simulation and actual data but trend correct
A simulation
D simulation
H simulation
A measure
D measure
H measure
Tjunction Temperature, °C
Device Power, W
A
D
H
P-Pin
S-Pin
Z-Pin
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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application
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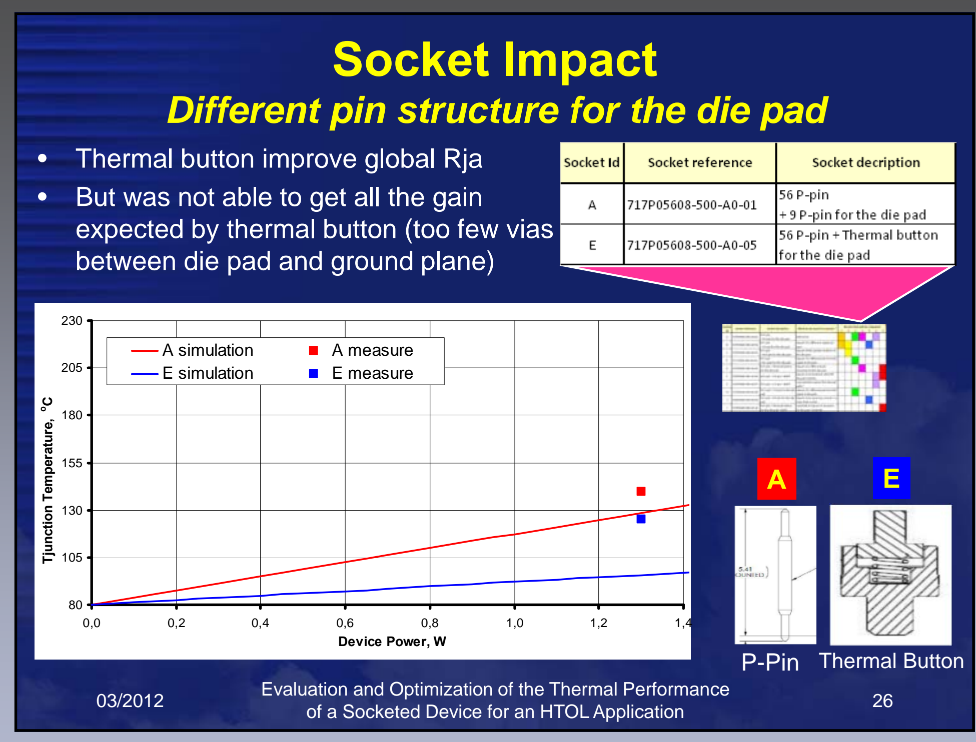
Socket Impact
Different pin structure for the die pad
Thermal button improve global Rja
But was not able to get all the gain expected by thermal button (too few vias between die pad and ground plane)
Socket Id | Socket reference | Socket decription
A | 717P05608-500-A0-01 | 56 P-pin + 9 P-pin for the die pad
E | 717P05608-500-A0-05 | 56 P-pin + Thermal button for the die pad
A simulation
E simulation
A measure
E measure
Tjunction Temperature, °C
Device Power, W
A
E
P-Pin
Thermal Button
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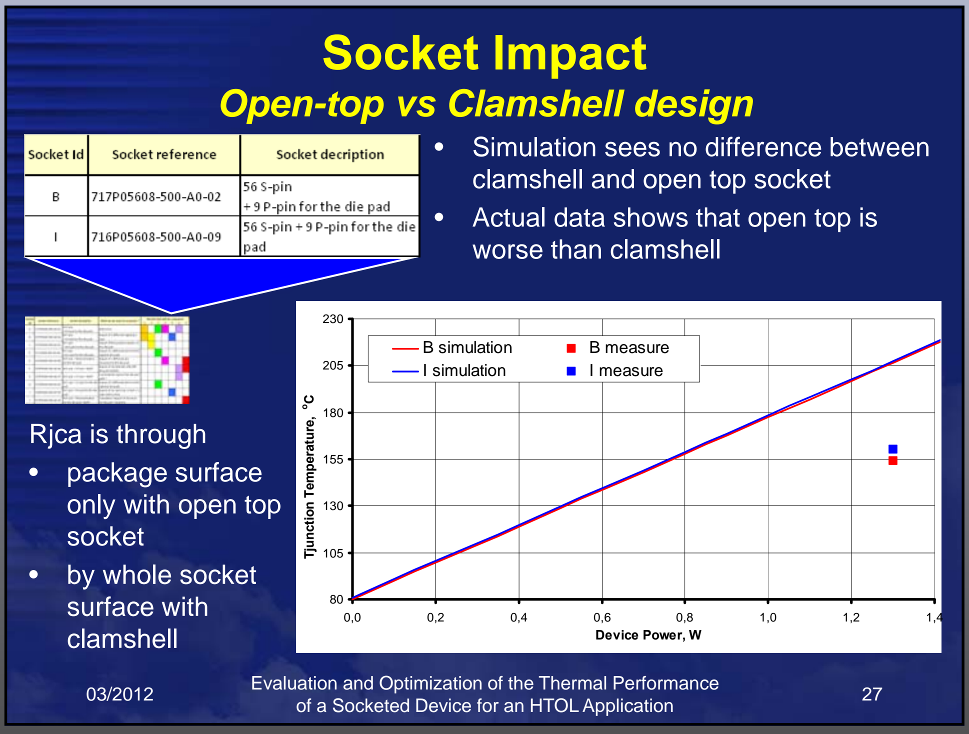
Socket Impact
Open-top vs Clamshell design
Socket Id | Socket reference | Socket decription
B | 717P05608-500-A0-02 | 56 S-pin + 9 P-pin for the die pad
I | 716P05608-500-A0-09 | 56 S-pin + 9 P-pin for the die pad
Simulation sees no difference between clamshell and open top socket
Actual data shows that open top is worse than clamshell
Rjca is through
package surface only with open top socket
by whole socket surface with clamshell
B simulation
I simulation
B measure
I measure
Tjunction Temperature, °C
Device Power, W
230
205
180
155
130
105
80
0,0
0,2
0,4
0,6
0,8
1,0
1,2
1,4
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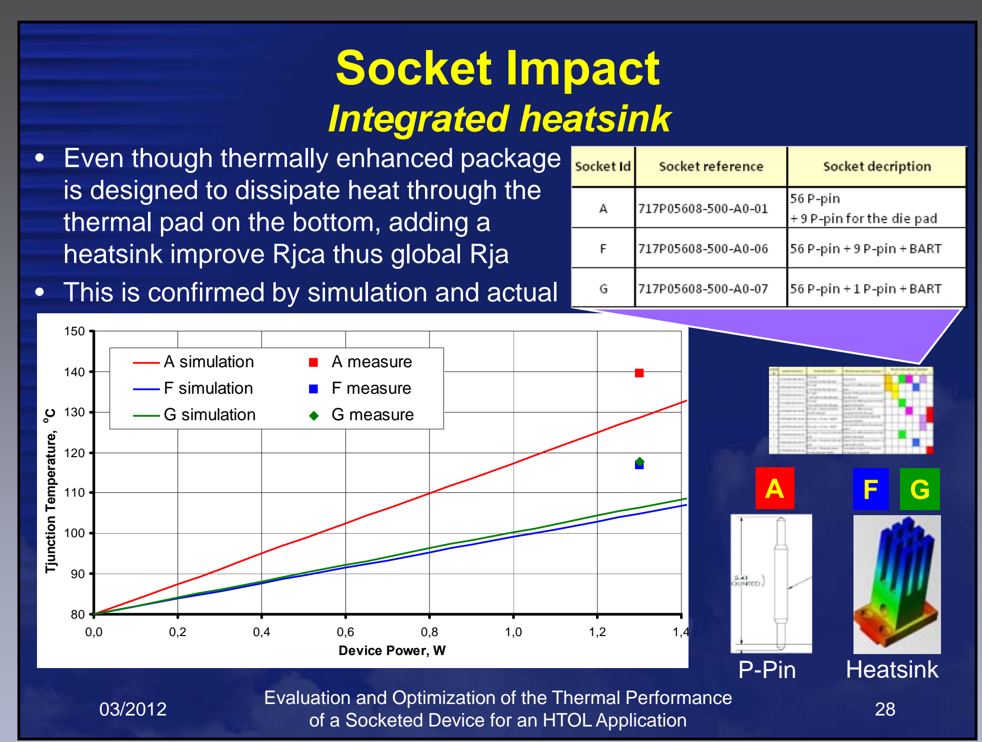
Socket Impact
Integrated heatsink
Even though thermally enhanced package is designed to dissipate heat through the thermal pad on the bottom, adding a heatsink improve Rjca thus global Rja
This is confirmed by simulation and actual
Socket Id | Socket reference | Socket decription
A | 717P05608-500-A0-01 | 56 P-pin + 9 P-pin for the die pad
F | 717P05608-500-A0-06 | 56 P-pin + 9 P-pin + BART
G | 717P05608-500-A0-07 | 56 P-pin + 1 P-pin + BART
A simulation
F simulation
G simulation
A measure
F measure
G measure
Tjunction Temperature, °C
Device Power, W
150
140
130
120
110
100
90
80
0,0
0,2
0,4
0,6
0,8
1,0
1,2
1,4
A
F
G
P-Pin
Heatsink
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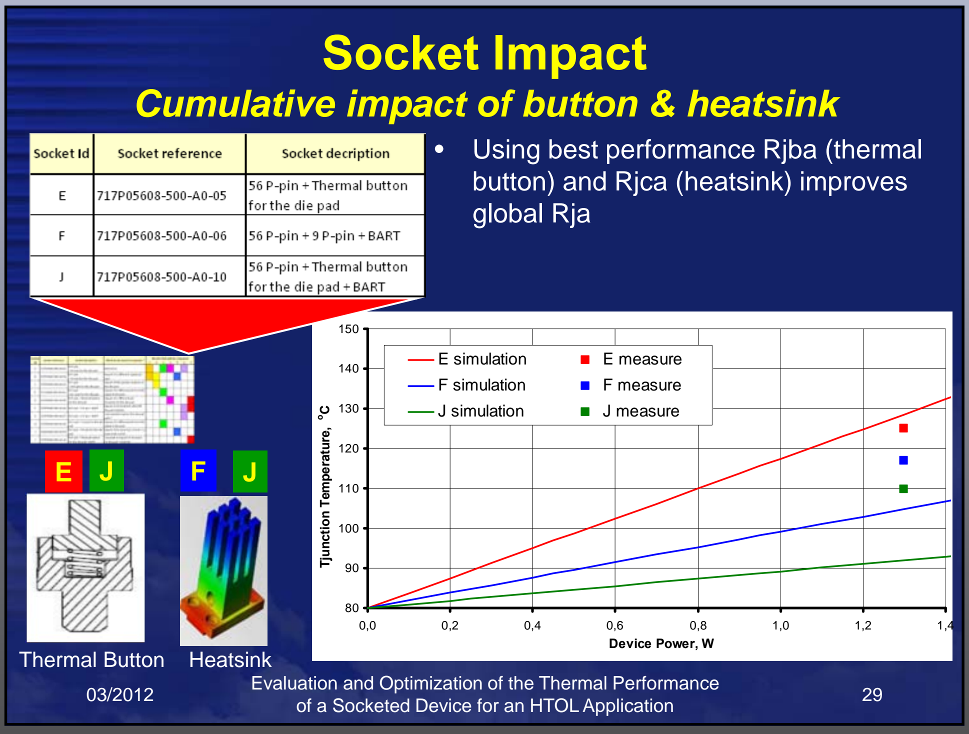
Socket Impact
Cumulative impact of button & heatsink
Socket Id | Socket reference | Socket decription
E | 717P05608-500-A0-05 | 56 P-pin + Thermal button for the die pad
F | 717P05608-500-A0-06 | 56 P-pin + 9 P-pin + BART
J | 717P05608-500-A0-10 | 56 P-pin + Thermal button for the die pad + BART
Using best performance Rjba (thermal button) and Rjca (heatsink) improves global Rja
E J
F J
Thermal Button
Heatsink
E simulation
F simulation
J simulation
E measure
F measure
J measure
Tjunction Temperature, °C
Device Power, W
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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application
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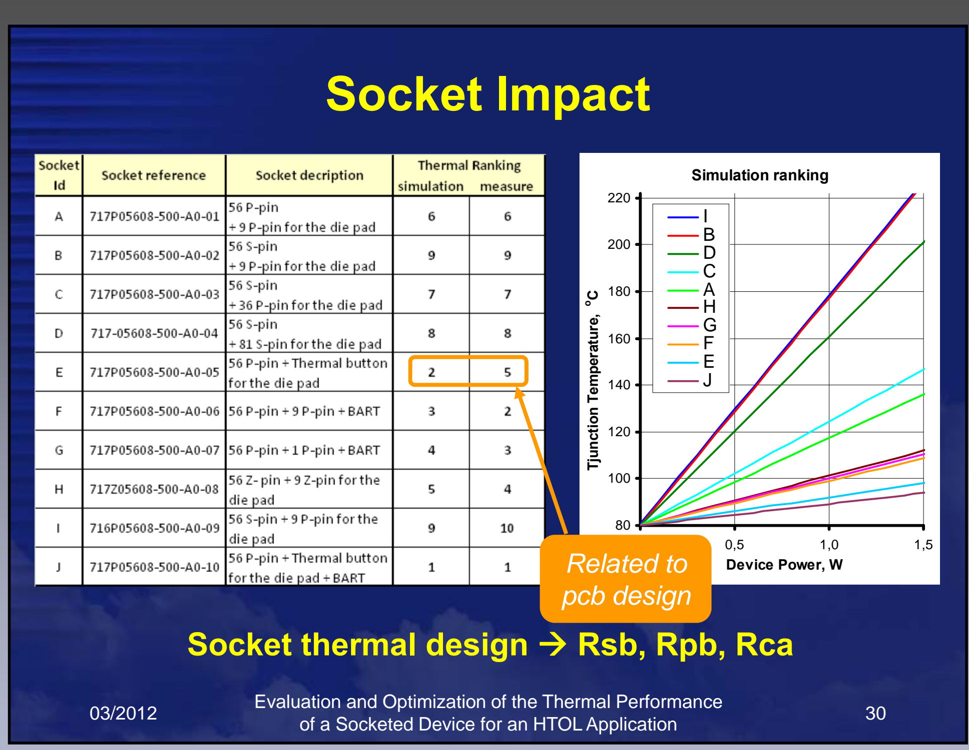
Socket Impact
Socket Id | Socket reference | Socket decription | Thermal Ranking simulation | measure
A | 717P05608-500-A0-01 | 56 P-pin + 9 P-pin for the die pad | 6 | 6
B | 717P05608-500-A0-02 | 56 S-pin + 9 P-pin for the die pad | 9 | 9
C | 717P05608-500-A0-03 | 56 S-pin + 36 P-pin for the die pad | 7 | 7
D | 717-05608-500-A0-04 | 56 S-pin + 81 S-pin for the die pad | 8 | 8
E | 717P05608-500-A0-05 | 56 P-pin + Thermal button for the die pad | 2 | 5
F | 717P05608-500-A0-06 | 56 P-pin + 9 P-pin + BART | 3 | 2
G | 717P05608-500-A0-07 | 56 P-pin + 1 P-pin + BART | 4 | 3
H | 717Z05608-500-A0-08 | 56 Z-pin + 9 Z-pin for the die pad | 5 | 4
I | 716P05608-500-A0-09 | 56 S-pin + 9 P-pin for the die pad | 9 | 10
J | 717P05608-500-A0-10 | 56 P-pin + Thermal button for the die pad + BART | 1 | 1
Simulation ranking
Tjunction Temperature, °C
Device Power, W
Related to pcb design
Socket thermal design → Rsb, Rpb, Rca
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Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application
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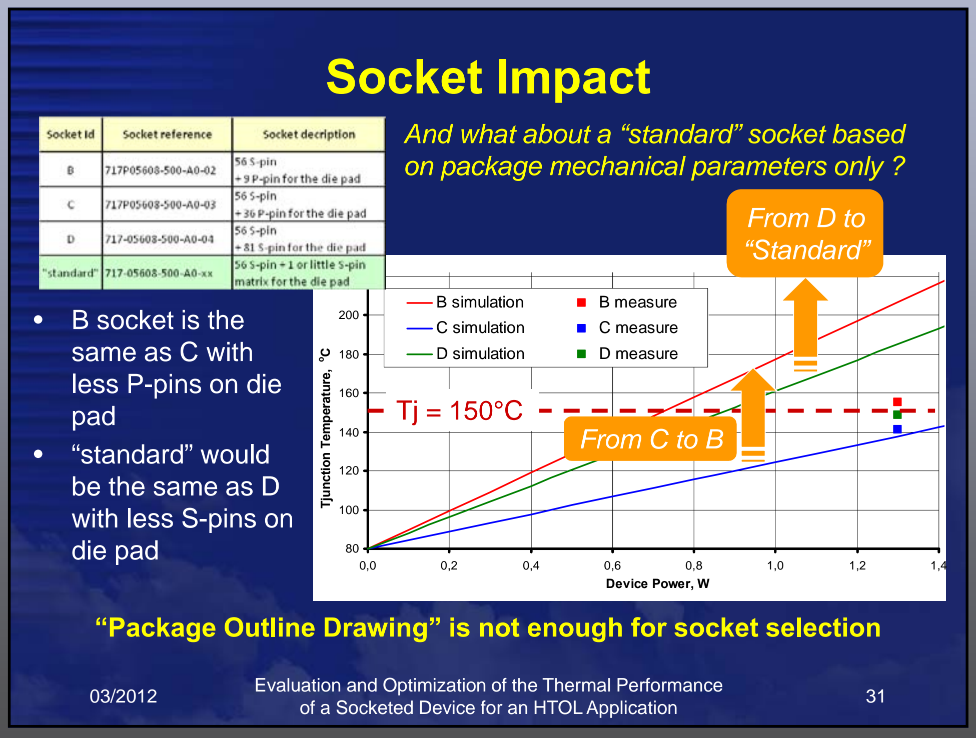

Socket Id	Socket reference	Socket decription
B	717P05608-500-A0-02	56 S-pin +9 P-pin for the die pad
C	717P05608-500-A0-03	56 S-pin +36 P-pin for the die pad
D	717-05608-500-A0-04	56 S-pin +81 S-pin for the die pad
"standard"	717-05608-500-A0-xx	56 S-pin + 1 or little S-pin matrix for the die pad

Conclusion

- DOE shows that *simulations and actual data follow the same tendency*. But amplitudes appear different due to incomplete/unknown information such as accurate design/package information or considering self heating of the contacts.
- In fact, *the real simulation « fine-tuning » is all in the details* i.e. the more detailed the information which is considered (such as precise package structure, die/lid ratio, lid material, precise socket/pcb setup…) always improves the accuracy of the simulation data
- Since device and chamber contribution in thermal performance can not be modified, *socket thermal design becomes an increasingly important factor* to consider and optimize the overall thermal performance (Rja) of the device-socket-board structure during an HTOL test.
- **But** … even with an « *optimal socket design* » the benefit of this upfront accurate design *will be lost if other aspects* such as board design and population, chamber population and *ventilation…are not taken into account by the lifetest engineers.*

Content

- Introduction to wall-extended coaxial socket
- How to achieve the design concept?
- Socket test performance
- Summary

Coaxial socket
=Performance oriented product!!

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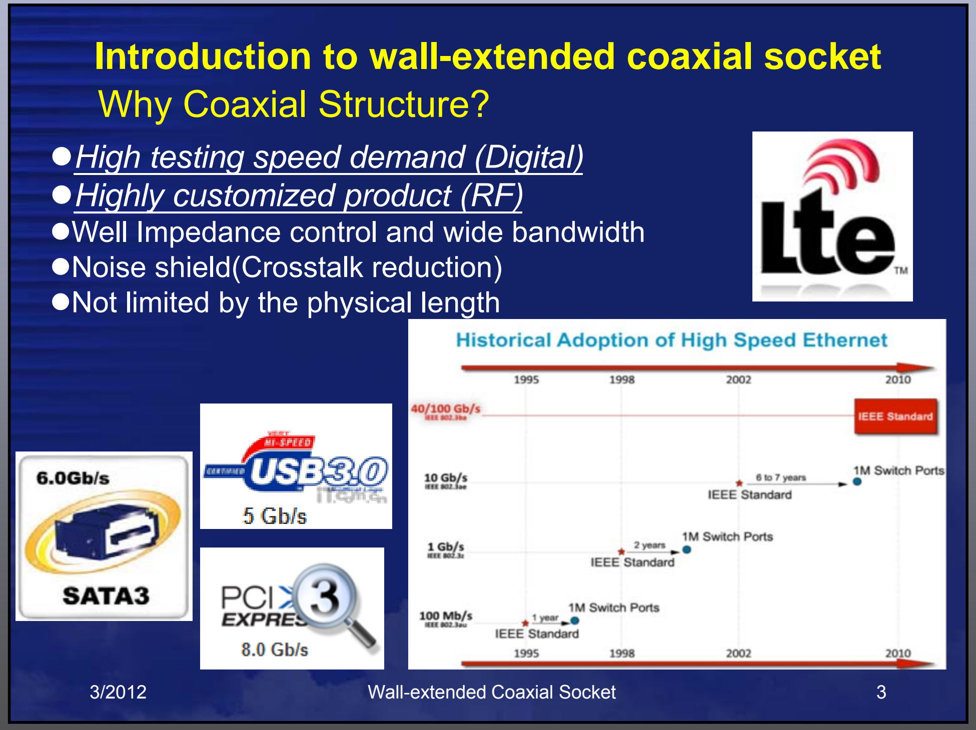
Introduction to wall-extended coaxial socket
Why Coaxial Structure?
High testing speed demand (Digital)
Highly customized product (RF)
Well Impedance control and wide bandwidth
Noise shield(Crosstalk reduction)
Not limited by the physical length
Historical Adoption of High Speed Ethernet
40/100 Gb/s
IEEE Standard
10 Gb/s
6 to 7 years
1M Switch Ports
1 Gb/s
2 years
1M Switch Ports
100 Mb/s
1 year
1995
1998
2002
2010
6.0Gb/s
SATA3
USB 3.0
5 Gb/s
PCI EXPRESS 3
8.0 Gb/s
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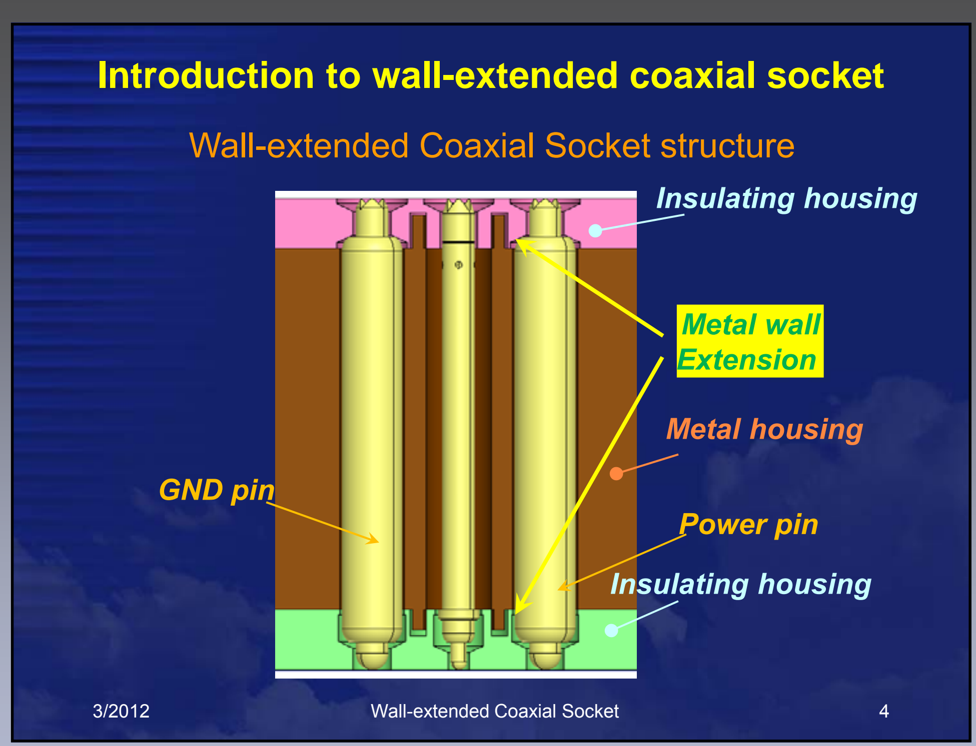
Introduction to wall-extended coaxial socket
Wall-extended Coaxial Socket structure
Insulating housing
Metal wall Extension
Metal housing
GND pin
Power pin
Insulating housing
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Wall-extended Coaxial Socket
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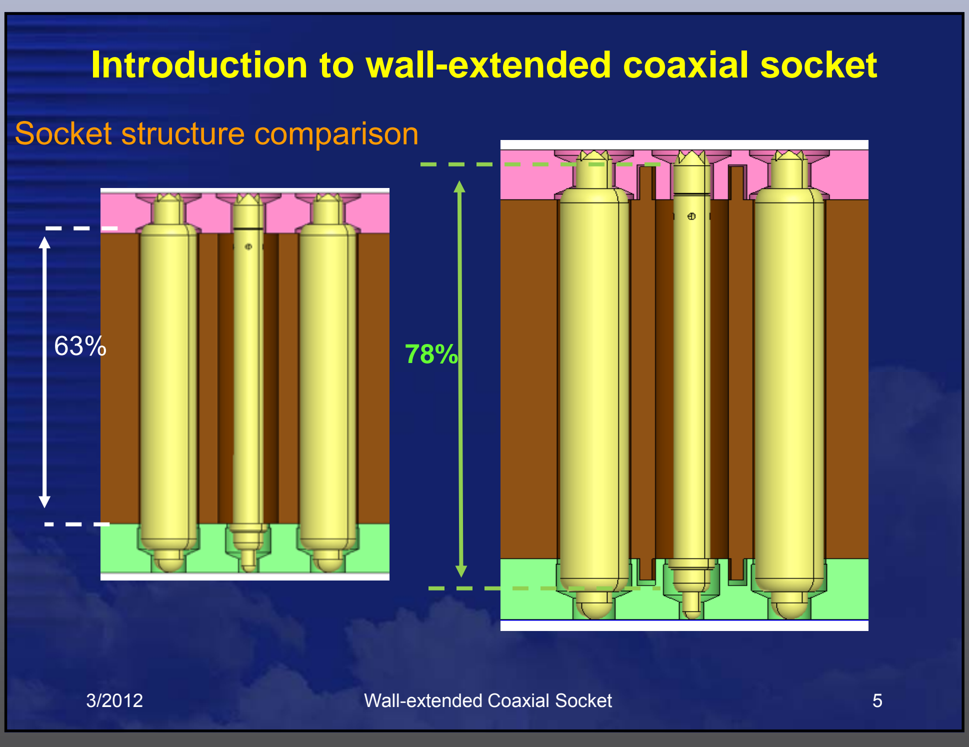
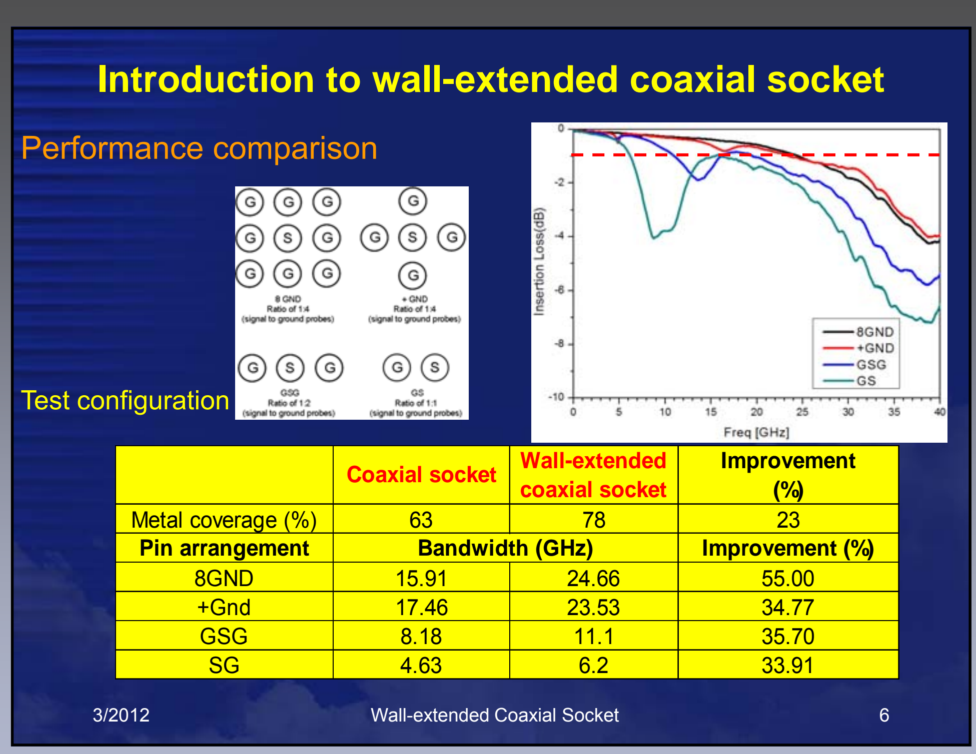
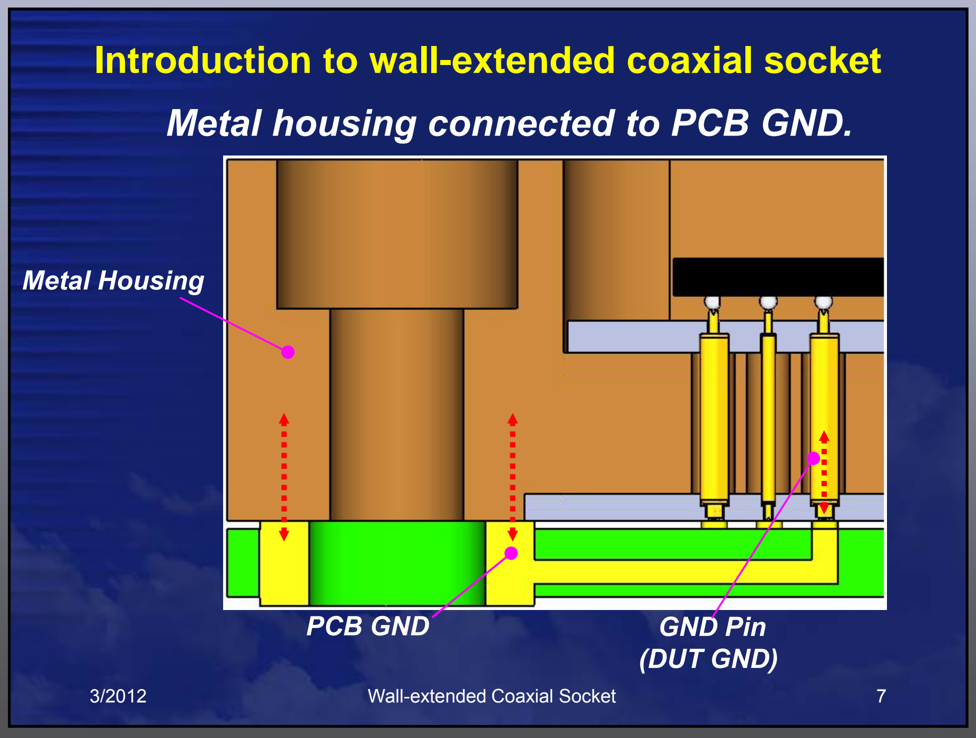




	Coaxial socket	Wall-extended coaxial socket	Improvement (%)
Metal coverage (%)	63	78	23
Pin arrangement	**Bandwidth (GHz)**		**Improvement (%)**
8GND	15.91	24.66	55.00
+Gnd	17.46	23.53	34.77
GSG	8.18	11.1	35.70
SG	4.63	6.2	33.91


Introduction to wall-extended coaxial socket
Metal housing connected to PCB GND.
Metal Housing
PCB GND
GND Pin
(DUT GND)
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Wall-extended Coaxial Socket
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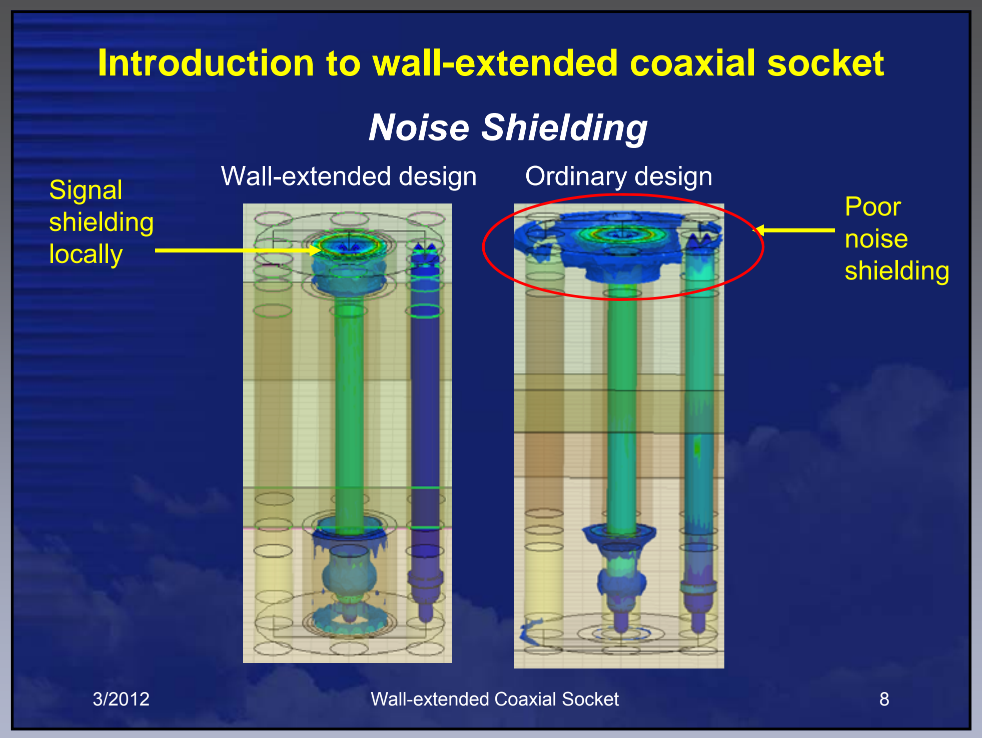
Introduction to wall-extended coaxial socket
Noise Shielding
Wall-extended design
Ordinary design
Signal shielding locally
Poor noise shielding
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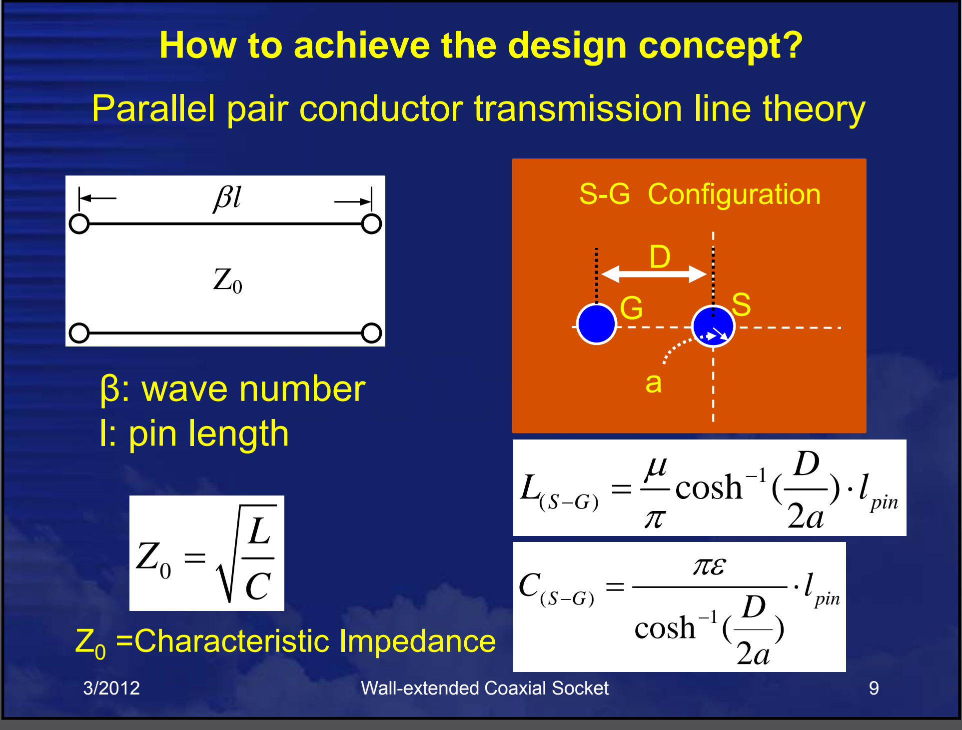
How to achieve the design concept?
Parallel pair conductor transmission line theory
βl
Z_0
β: wave number
l: pin length
$Z_0 = \sqrt{\frac{L}{C}}$
Z_0 =Characteristic Impedance
S-G Configuration
D
G
S
a
$L_{(S-G)} = \frac{\mu}{\pi}\cosh^{-1}(\frac{D}{2a})\cdot l_{pin}$
$C_{(S-G)} = \frac{\pi\varepsilon}{\cosh^{-1}(\frac{D}{2a})}\cdot l_{pin}$
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Wall-extended Coaxial Socket
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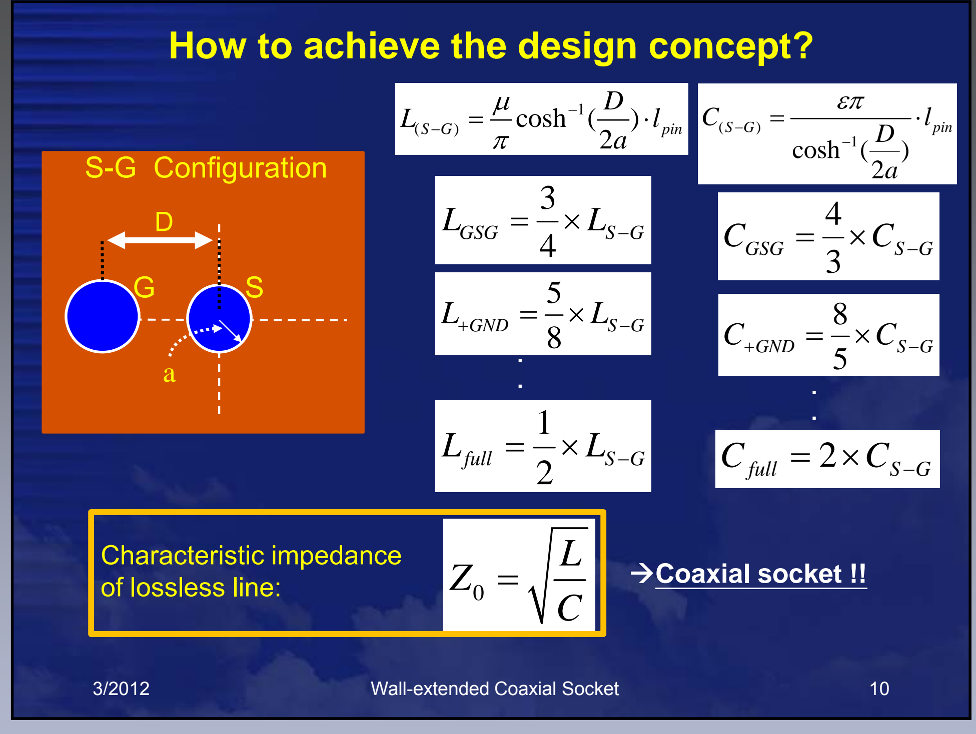
How to achieve the design concept?
S-G Configuration
D
G
S
a
$L_{(S-G)} = \frac{\mu}{\pi}\cosh^{-1}(\frac{D}{2a})\cdot l_{pin}$
$C_{(S-G)} = \frac{\varepsilon\pi}{\cosh^{-1}(\frac{D}{2a})}\cdot l_{pin}$
$L_{GSG} = \frac{3}{4}\times L_{S-G}$
$L_{+GND} = \frac{5}{8}\times L_{S-G}$
$L_{full} = \frac{1}{2}\times L_{S-G}$
$C_{GSG} = \frac{4}{3}\times C_{S-G}$
$C_{+GND} = \frac{8}{5}\times C_{S-G}$
$C_{full} = 2\times C_{S-G}$
Characteristic impedance of lossless line:
$Z_0 = \sqrt{\frac{L}{C}}$
→Coaxial socket !!
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Wall-extended Coaxial Socket
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How to achieve the design concept?

Consider coaxial socket as the **multi-stage transmission line**

$$L = \frac{\mu}{2\pi} \ln\left(\frac{b}{a}\right) \cdot l_{pin}$$

$$C = \frac{2\pi\varepsilon}{\ln\left(\frac{b}{a}\right)} \cdot l_{pin}$$

Coaxial region

$$L_{(S-G)} = \frac{\mu}{\pi} \cosh^{-1}\left(\frac{D}{2a}\right) \cdot l_{pin}$$

$$C_{(S-G)} = \frac{\pi\varepsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)} \cdot l_{pin}$$

Insulating region

Parameter Definition:
a: Pin diameter; **b**: Pin hole ; **D**: signal to ground distance

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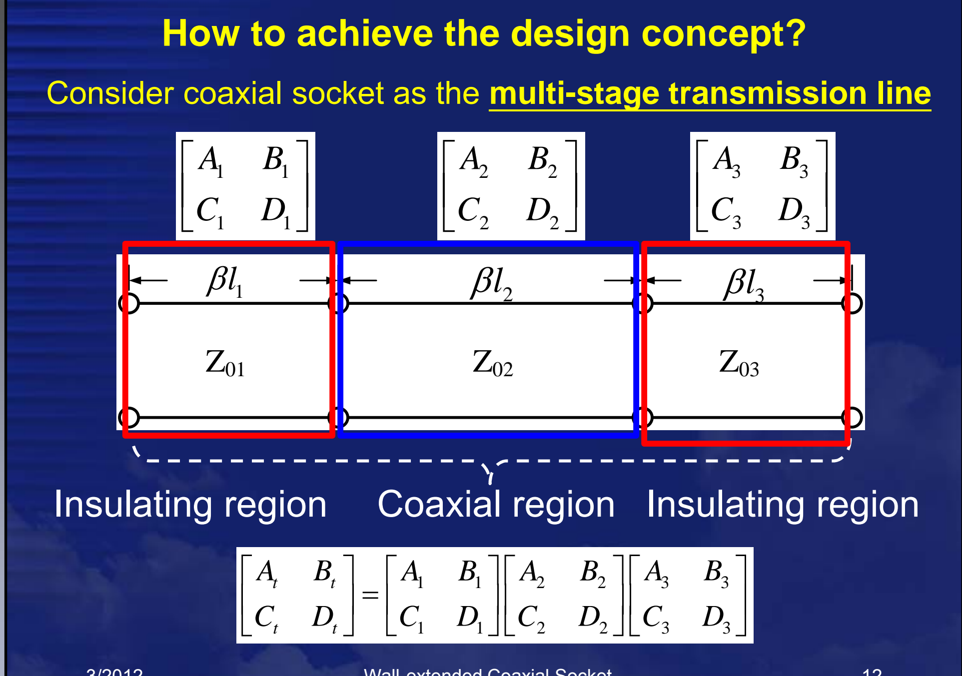

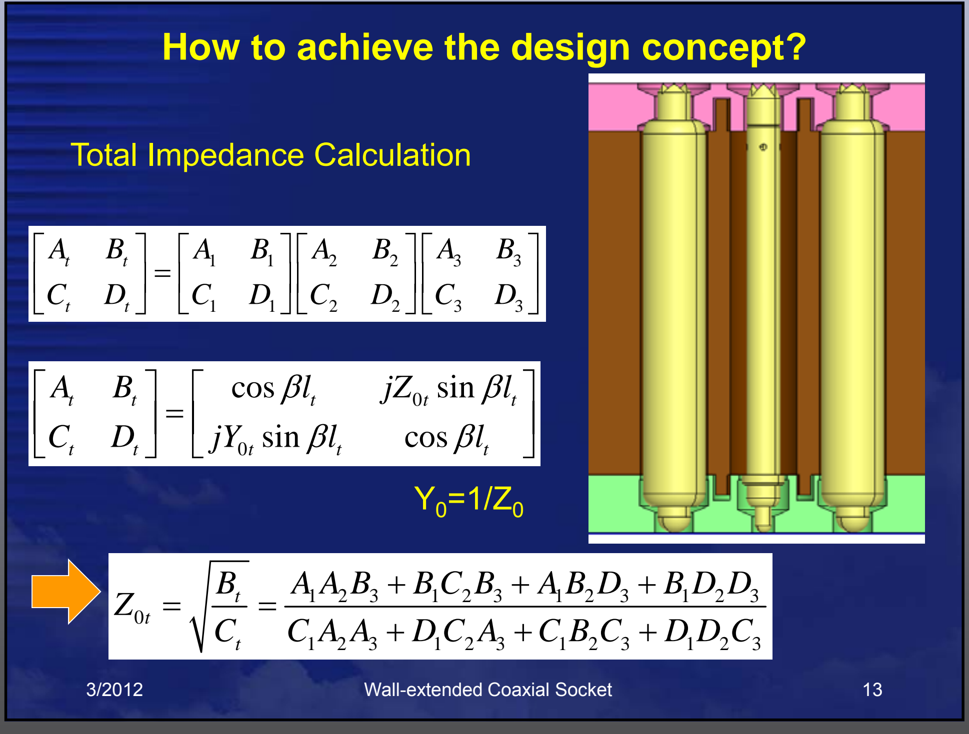
How to achieve the design concept?
Total Impedance Calculation
$\begin{bmatrix} A_t & B_t \\ C_t & D_t \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}\begin{bmatrix} A_3 & B_3 \\ C_3 & D_3 \end{bmatrix}$
$\begin{bmatrix} A_t & B_t \\ C_t & D_t \end{bmatrix} = \begin{bmatrix} \cos\beta l_t & jZ_{0t}\sin\beta l_t \\ jY_{0t}\sin\beta l_t & \cos\beta l_t \end{bmatrix}$
$Y_0=1/Z_0$
$Z_{0t} = \sqrt{\frac{B_t}{C_t}} = \frac{A_1A_2B_3 + B_1C_2B_3 + A_1B_2D_3 + B_1D_2D_3}{C_1A_2A_3 + D_1C_2A_3 + C_1B_2C_3 + D_1D_2C_3}$
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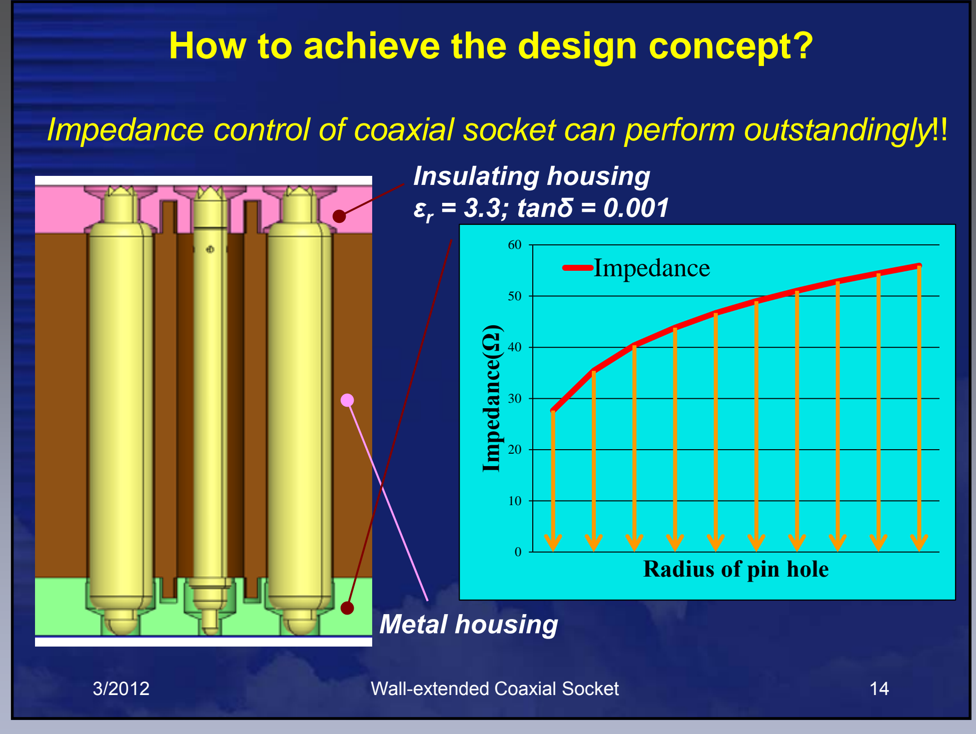
How to achieve the design concept?
Impedance control of coaxial socket can perform outstandingly!!
Insulating housing
$\varepsilon_r = 3.3; \tan\delta = 0.001$
Impedance
Impedance(Ω)
0
10
20
30
40
50
60
Radius of pin hole
Metal housing
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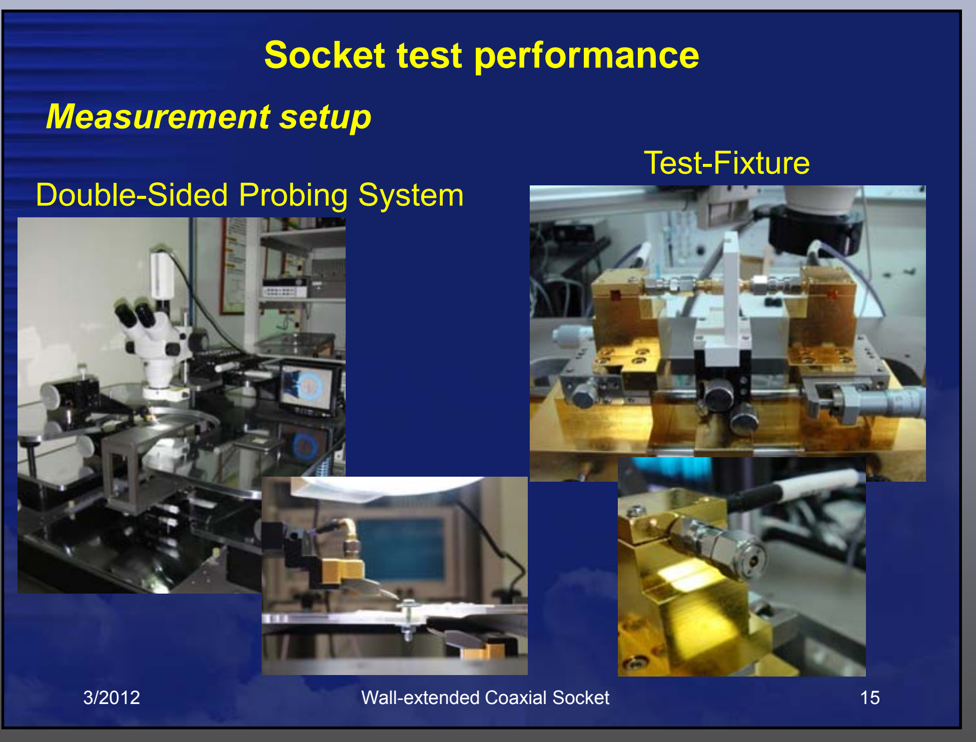
Socket test performance
Measurement setup
Double-Sided Probing System
Test-Fixture
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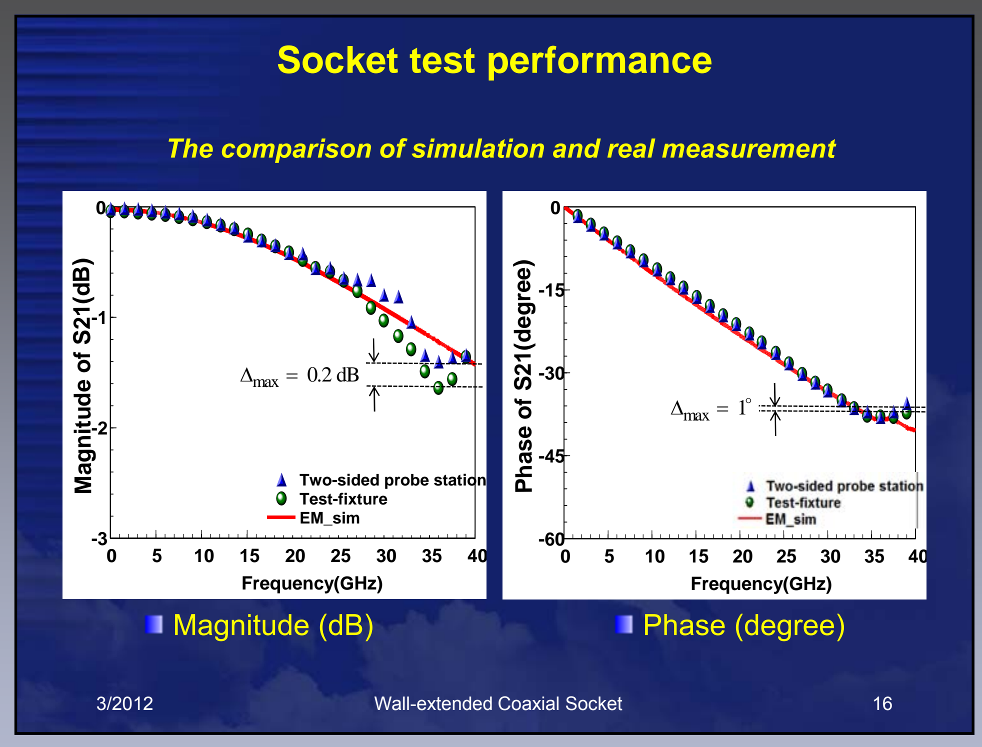
Socket test performance
The comparison of simulation and real measurement
Magnitude of S21(dB)
Δmax = 0.2 dB
Two-sided probe station
Test-fixture
EM_sim
Frequency(GHz)
Phase of S21(degree)
Δmax = 1°
Magnitude (dB)
Phase (degree)
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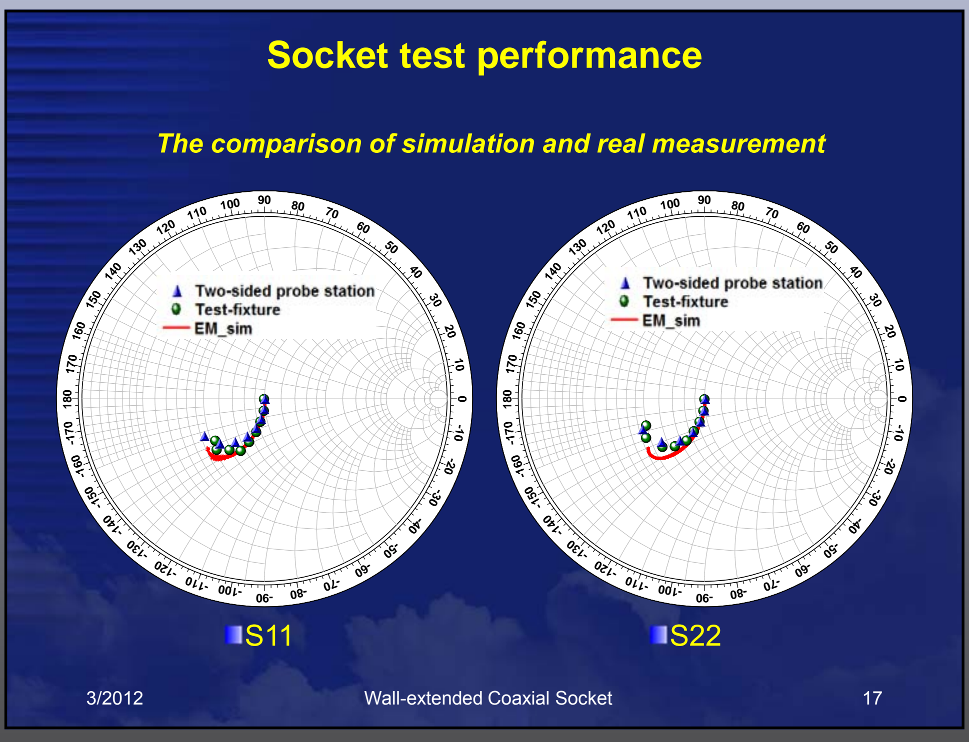
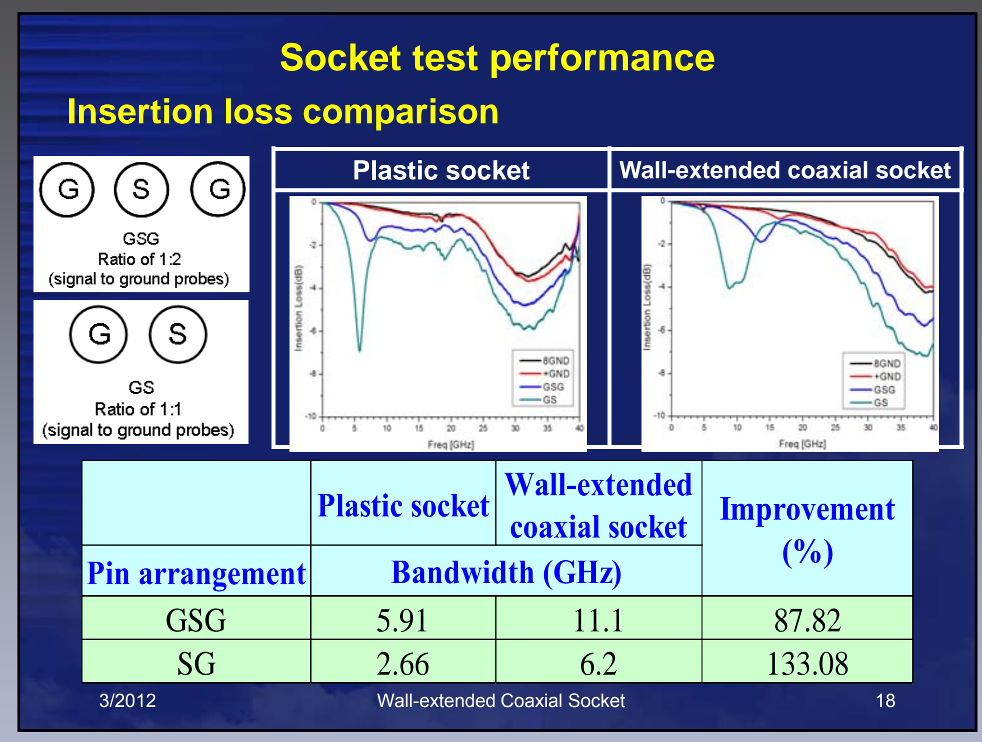
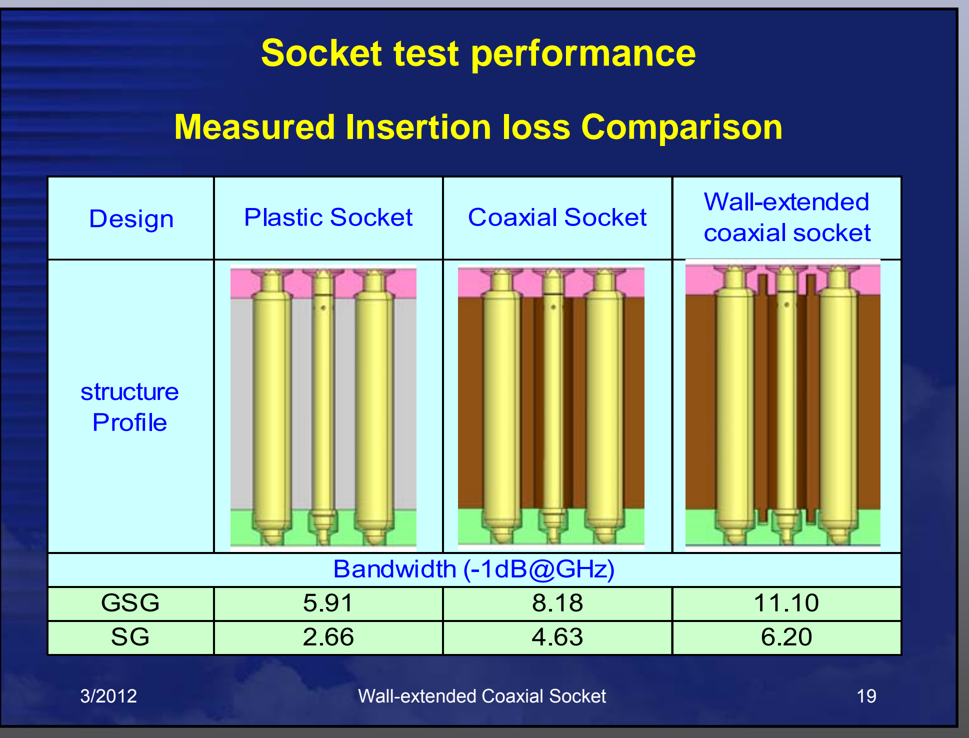
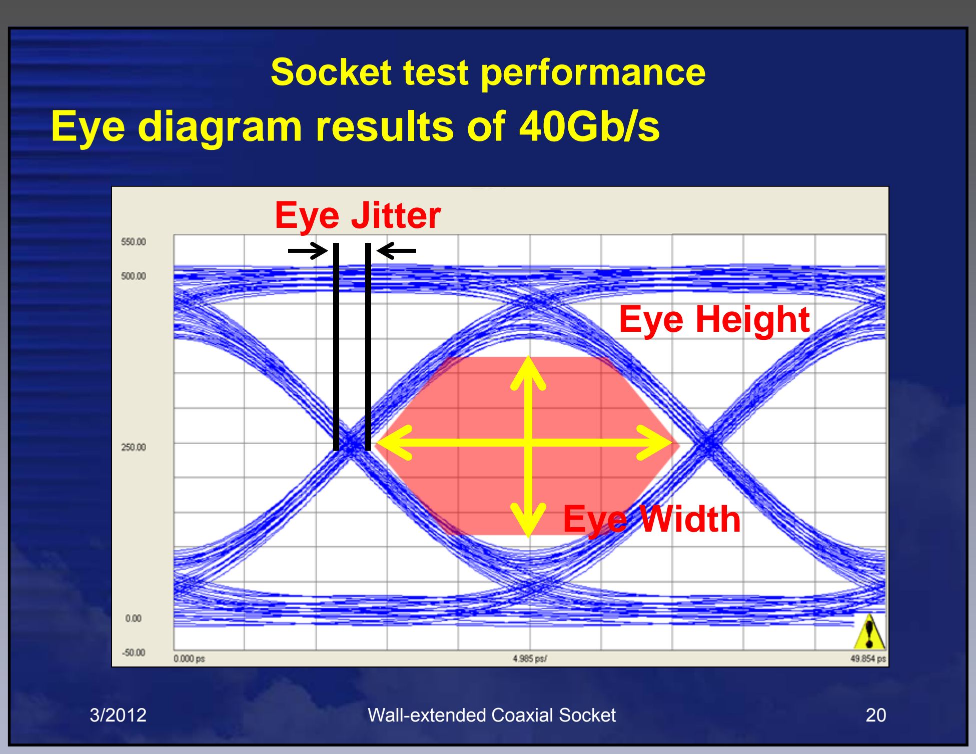


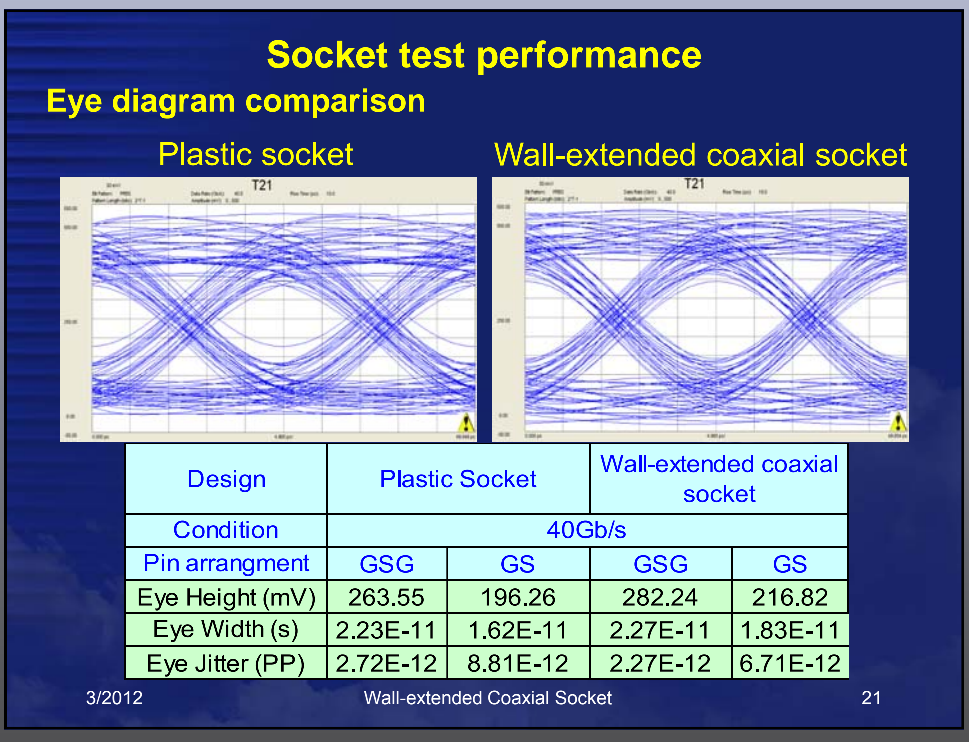


Pin arrangement	Plastic socket	Wall-extended coaxial socket	Improvement (%)
	Bandwidth (GHz)		
GSG	5.91	11.1	87.82
SG	2.66	6.2	133.08

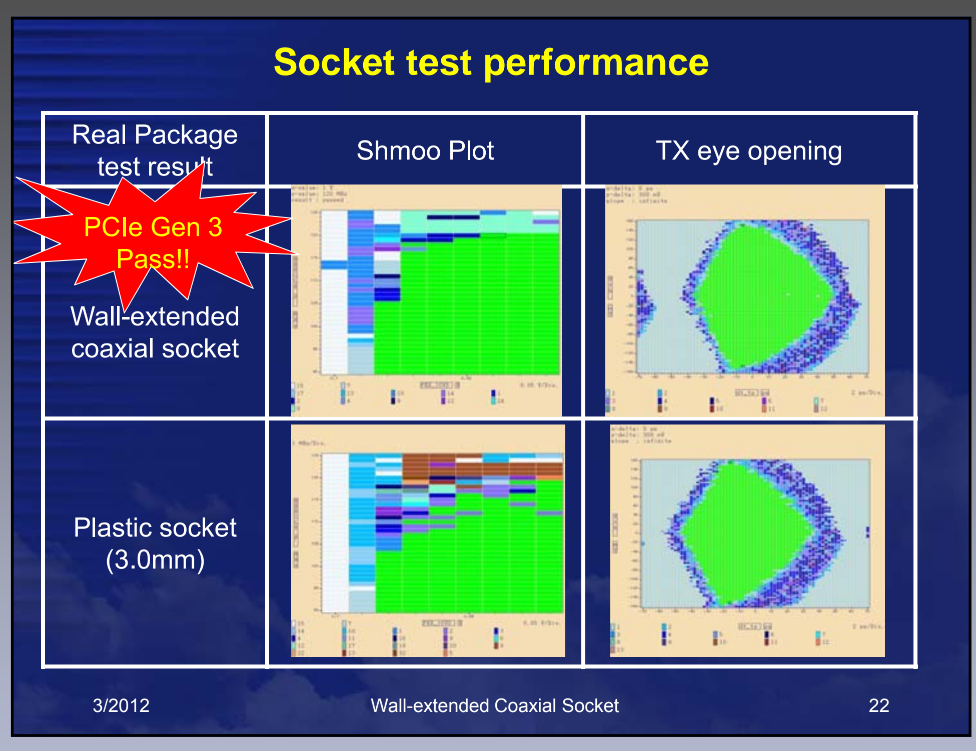


Design	Plastic Socket	Coaxial Socket	Wall-extended coaxial socket
structure Profile			
Bandwidth (-1dB@GHz)			
GSG	5.91	8.18	11.10
SG	2.66	4.63	6.20





Design	Plastic Socket		Wall-extended coaxial socket	
Condition	40Gb/s			
Pin arrangment	GSG	GS	GSG	GS
Eye Height (mV)	263.55	196.26	282.24	216.82
Eye Width (s)	2.23E-11	1.62E-11	2.27E-11	1.83E-11
Eye Jitter (PP)	2.72E-12	8.81E-12	2.27E-12	6.71E-12



Summary

- Wall-extended coaxial design could effectively improve the RF performance compared with ordinary coaxial design and plastic socket.
- The highly customized techniques were necessary to meet the various application.

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Acknowledgment

•Special thanks to Prof. Horng and his outstanding group of NSYSU, Kaohsiung, Taiwan for the cooperation and reviewing the presentation.

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