It just wouldn't be a BiTS Workshop without a session devoted entirely to novel socket designs. Every year, there are new devices on the market and ever critical factors like witness marks on smaller solder balls and minimum contact force that need a socket designed specifically for them. The three papers in this session address three distinctly different socket applications. The first talks to spring probes for fine pitch, then the second paper reviews the heat path for a device mounted in a socket and discusses the important variables in a thermal analysis. Lastly, we'll examine a unique design for a coaxial socket.

**Are Spring Contact Probes Valid at Fine Pitch?**
Jon Diller, Dr. Jiachun (Frank) Zhou—Interconnect Devices, Inc.

**Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application**
Nathanaël Loiseau—Presto Engineering
Marco Michi, Dr. James Forster—Wells-CTI

**Wall-extended Coaxial Socket**
Collins Sun, Justin Liu, Jack Liang—WinWay Technology Co., Ltd.
Kuan-Chung Lu, Tzyy-Sheng Horng—National Sun Yat-Sen University

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Are Spring Contact Probes Valid at Fine Pitch?

Dr. Jiachun (Frank) Zhou, Jon Diller
Interconnect Devices, Inc.

2012 BiTS Workshop
March 4 - 7, 2012

Probably not.

(but wait, there’s more)
Market Requirements

Primarily WLCSP (now) and PoP (pretty soon)
- 0.3 pitch WLCSP bump Ø0.21; 0.2 with Ø0.115 extant
- PoP primarily lands under solder resist or balls

Test Technology Status Quo
- WLCSP on probers, inline cleaning, >200 UPH, expected cycle life >500K
- PoP in pick-and-place applications, offline cleaning, triple-digit UPH, expected cycle life 100-250K

Current Methodology

Vertical Probe Technology
- Excellent cycle life, SI, reliability, easy to align
- Limited compliance
- Significant initial cost
- Not field serviceable
- Not applicable to PoP
Current Methodology

Spring Contact Probes
- Similar technology available from several vendors
- Highly compliant
- Field serviceable
- Difficult to clean
- Fragile

Deflection: 0.5mm; Force: 8gf

Unit: mm

Monet

Complete Assembly

Conductive Cavity
- Socket body
- Embedded barrel
- Retainer

Components
- Top plunger
- Spring
- Bottom plunger

Patent Pending
### Shift in Diameters

#### Traditional Probe
- 80 µm (really tiny)
- 30 to 50 micron gap between barrel and cavity hole

#### Embedded Contact
- 110 µm (comparable to 0.4)
- No gap between barrel & socket body

### Alignment Improvement

**Several Factors**
- One less gap
- Improved aspect ratio of hole in plastic
- Larger diameter plunger is more concentric
- Electroforming produces high concentricity of ‘barrel’
- Retainer plate true position does not affect top plunger
More Force, Stable Resistance

17 gf versus 8 gf. large ‘sweet spot’

- Resistance Ave
- Resistance Ave + 2STD
- Force Ave
- Force Ave + 2STD

Resistance Ave at 0.26 Top Travel, 158 mOhm

Force Ave at 0.26 Top Travel, 17 gf

Long Mechanical Life

Stable performance through 500K insertions
Signal Integrity Methodology

Device Side

Single Ended

Single Ended

Differential Pair

Board Side

Analog Behavior

10 GHz BW
@ 250 μm

Return Loss

Insertion Loss

3/2012

Are Spring Contact Probes Valid at Fine Pitch?

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Are Spring Contact Probes Valid at Fine Pitch?

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### Differential Behavior

3 Gbps BW
@ 250 µm

### Insertion Loss

- 0.00 dB
- 2.50 dB
- 5.00 dB
- 7.50 dB
- 10.00 dB
- 12.50 dB
- 15.00 dB
- 17.50 dB
- 20.00 dB

### Alpha Program

Validation of manufacturing capability and alignment

- >200 pins per site, 4 sites, 0.25 mm pitch
- Aligned well, passed initial electrical tests
Summary

Spring contact probes are a preferred technology for \( \geq 0.4 \text{mm} \) pitch but are challenged at finer pitches.

By embedding the probe barrel in the contactor body significant gains can be made in robustness, alignment, and signal integrity.

This approach has potential for all WLCSP pitches: 250 \( \mu \text{m} \), 200 \( \mu \text{m} \), 180 \( \mu \text{m} \), 150 \( \mu \text{m} \).

Acknowledgements

The following persons and organizations were instrumental in the creation of this paper:

Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application

Considerations in the selection of a socket for a plastic molded, thermal enhanced package

Nathanaël Loiseau+, Marco Michi* and Dr. James Forster*
+ Presto Engineering, * WELLS-CTI

Introduction

Today’s device:
- More functionality
- Higher frequency
- More power / thermal dissipation
- Smaller size

Today’s HTOL:
- From static to true application environment simulation
- Higher frequency
- Higher current
- More power / thermal dissipation

Thermal considerations of socket and test board become more important
Content

- Technology challenge
- Environment challenge
- Thermal resistance definition
- DUT impact
- PCB impact
- Chamber impact
- Self heating impact
- Socket impact (DOE)
- Conclusion

**Definition: HTOL High Temperature Operating Life**

Typically 1000 hours at $T_{ambient} \ 125^\circ C$ or $T_{junction} \ 150^\circ C$.

*But other times and temps are performed*

**Technology Challenge**

**Package**

- Smaller, integration of several functions, dies
- Power dissipation concentrated
- Smaller surface for thermal exchange

**Advance process**

- Smaller size, higher frequency
- IC Voltage $\downarrow$ IC current $\uparrow$ Current flow $\uparrow$
  $\Rightarrow$ Socket & board self heating $\uparrow$

**Customer willingness**

- Static HTOL does not always reveal relevant failure mechanism
- Dynamic HTOL closer to real life conditions

**Environment Challenge**

**Principle for HTOL**

\[ T_{\text{junction DUT}} = T_a + R_{ja} \times P_{\text{Diss}} \]

- Ta is regulated locally or globally in order to have the correct \( T_{\text{junction DUT}} \)

Ta must be compatible with
- Other elements temperature (board, socket, components)
- Chamber specification
  (ex: \( T_{\text{min}} = T_{\text{room}} + 30^\circ\text{C} \) if no cooling capability)

**Thermal Resistance Definition**

Thermal resistance for heat transfer

\[ R_{1-2} = \frac{T_1 - T_2}{\text{Heat/t}} \]

Electrical resistance for charge transfer

\[ R_{1-2} = \frac{V_1 - V_2}{\text{Charge/t}} \]
Thermal Resistance Definition

Thermal resistance is

- The characterization of heat transfer between 2 points
- The key point to get thermal equilibrium and $T_j$ under control to ensure functionality & reliability of the IC

$\frac{1}{R_{ja}} = \frac{1}{R_{jca}} + \frac{1}{R_{jba}}$

Thermal resistance is not

- A universal standard
  - JESD 51 → 17 documents
  - MIL-STD-750E → 13 methods
- A standard value available in IC data sheet or package specification

Soldered device vs Socketed device

- Thermal resistance is typically given in device datasheet for the device soldered to a board in a certain environment
- Thermal resistance of a socketed device is expected to be higher than one soldered to a PCB in same environment. Mostly unknown.

Heat dissipation path:
- Die – Case – Ambient
- Die – IC Pads – Board – Ambient

Heat dissipation path:
- Die – Case – Socket – Ambient
- Die – IC Pads – Socket – Board – Ambient
Thermal Resistance Definition

Thermal resistance circuitry for a device in a socket

\[ R_{ja} \]

\[ R_{ca} \]

\[ R_{jc} \]

\[ R_{bj} \]

\[ R_{bb} \]

\[ R_{sb} \]

\[ R_{bp} \]

\[ R_{pp} \]

\[ Q_{in} \]

DUT Impact

Thermally enhanced package = package with a pad dedicated for
- Thermal conduction to ground (always)
- Electrical connection to ground (sometimes)

Package configuration

Leadframe based package = die attached on metal plate
Laminate based package = die attached on a pcb
DUT Impact

Die assembly

- Stacked dies + Wire bonding
- Stacked dies + Flip-chip

Die / lid ratio

Measure done on 2 socketed device (same package, same HTOL board, difference on die size only)

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Die pad</th>
<th>Die</th>
<th>Rja</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7x7mm</td>
<td>5.1x5.1 mm</td>
<td>2.7x2.5mm</td>
<td>31°C/W</td>
</tr>
<tr>
<td>B</td>
<td>3.3x2.5mm</td>
<td></td>
<td>3.3x2.5mm</td>
<td>22°C/W</td>
</tr>
</tbody>
</table>

Chip designer choices \( \rightarrow \) Rjc, Rjs, Rjp

Often unknown values when designing an HTOL setup

PCB Impact

Example of Rja

HVQFN56 soldered on application boards in same environment

<table>
<thead>
<tr>
<th>Application board #1</th>
<th>Application board #2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB thickness (mm)</td>
<td>PCB thickness (mm)</td>
</tr>
<tr>
<td>1.17</td>
<td>1.43</td>
</tr>
<tr>
<td>Nbr of layer</td>
<td>Nbr of layer</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>PCB size (mm)</td>
<td>PCB size (mm)</td>
</tr>
<tr>
<td>30x60</td>
<td>35x80</td>
</tr>
</tbody>
</table>

Rja = 36.4 °C/W
Rja = 31.6 °C/W

Material, size, thickness, stack up \( \rightarrow \) Rbb, Rba

In HTOL, depend of chamber size and DUT requirements
Chamber Impact

From previous BiTS presentations, HTOL chamber often seen like:
- A simple box
- A “tunnel” between BIB’s
- “Fresh” air at one side
- Inconsistent air flow between boards
- Extraction of heat capability

For HTOL, JESD22-A108D:
The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered.

For test cost reduction, most often:
- Maximize the number of BIB’s in chamber
- Maximize the number of site per BIB

Experimental results with a 1.3W DUT
- Chamber and BIB populated in order to keep maximum air flow around sockets
- Air flow modified on a BIB position by adding a « box » on the socket

Chamber & Life-test Engineer choices → Rba, Rca
Self Heating Impact

With Joule effect, materials heat up according to $I^2 x R$

For PCB

For socket contacts

If the contacts or board traces generate heat, the heat transfer from the DUT to ambient will change

New contributors

\[ \{ Q_{pin}, Q_{board} \} \]

Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application

03/2012
**Self Heating Impact**

Measure on HTOL board → also illustrates mutual heating between sites

- with 1.3W DUT
- 780mA per DUT
- "1" used as Tj ref

![Graph showing self heating and mutual heating](image)

**Self heating, mutual heating → Rs, Rpb, Rbb, Rba**

**Socket Impact**

DOE in order to evaluate impact of socket design on global Rja

**DUT Vehicle:**
- Thermal enhanced HVQFN56
  8x8mm
- Laminate based
- 1.3W dissipation
- Always the same IC used

**Board Vehicle:**
- HTOL board 540x245mm,
- Full application mode simulated (800MHz signals in),
- 16 sites available
- 1 site loaded (always the same)

**Socket Vehicle:**
- Clamshell,
- Surface mount
- 10 different thermal designs

**HTOL chamber Vehicle:**
- 16 BIB position available,
- Board vehicle always loaded in same position
- Measure of Tj / Rja at minimum 3 temperatures (only 1 reported in this document)
**Socket Impact**

**Method used for simulation**

- Based on simplified thermal circuitry
- No self heating effect considered
- Package estimation done for Rjc, Rjs, Rjp based on die/lid ratio = 0.67
- Chamber air flow unspecified but considered as high value, estimation done for Rca, Rba
- For socket:
  - Rsb = Rth(pin) / nb of signal pin (56)
  - Rpb = Rth(pin) / nb of epad pin

---

**Socket Impact**

**Method used for Tj / Rj measurement on HTOL board**

Measure of junction temperature performed in true HTOL condition thanks to an embedded diode

- 1st step: calibration of the diode vs temperature with unbiased IC

Then for a given Ta

- 2nd step: heat up IC (power supplies ON) during 1hr
- 3rd step: measure diode and IC power dissipation. Calculate Tj and Rja
### Socket Impact

#### Socket / pin variations (1)

<table>
<thead>
<tr>
<th>Socket ID</th>
<th>Socket reference</th>
<th>Socket description</th>
<th>What do we want to evaluate?</th>
<th>Results that will be compared</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>717P00608-560-60-05</td>
<td>S-Pin + 9-Pin for the die pad</td>
<td>Reference</td>
<td>1 2 3 4 5 6 7</td>
</tr>
<tr>
<td>B</td>
<td>717P00608-560-60-02</td>
<td>S-Pin + 9-Pin for the die pad</td>
<td>Impact of a different signal pin type</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>717P00509-860-60-02</td>
<td>S-Pin + 36-Pin for the die pad</td>
<td>Impact of the pad pin number on the die pad</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>717-05008-500-60-04</td>
<td>S-Pin + 31-Pin for the die pad</td>
<td>Impact of a different pin for both signal &amp; die pads</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>717P00509-860-60-05</td>
<td>S-Pin + Thermal button for the die pad</td>
<td>Impact of a different pin structure for the die pad</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>717P00509-860-60-06</td>
<td>S-Pin + S-Pin + BART</td>
<td>Impact of an heatsink with still die pad contacts</td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>717P00508-560-60-07</td>
<td>S-Pin + 3-Pin + BART</td>
<td>Can heatsink replace the die pad path?</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>717P00508-560-60-08</td>
<td>S-Pin + 3-Pin + BART</td>
<td>Impact of a different pin for both signal &amp; die pads</td>
<td></td>
</tr>
<tr>
<td>I</td>
<td>717P00508-500-60-09</td>
<td>S-Pin + 3-Pin for the die pad</td>
<td>Impact of an open top socket vs a dam shell socket</td>
<td></td>
</tr>
<tr>
<td>J</td>
<td>717P00508-600-60-10</td>
<td>S-Pin + Thermal button for the die pad + BART</td>
<td>Cumulative impact of structure for die pad + heatsink</td>
<td></td>
</tr>
</tbody>
</table>

#### Evaluation and Optimization of the Thermal Performance of a Socketed Device for an HTOL Application

- **Socket Impact**
  - **P-Pin**
    - $R_{th} = 2,080$ °C/W
  - **S-Pin**
    - $R_{th} = 12,464$ °C/W
  - **Z-Pin**
    - $R_{th} = 1,100$ °C/W

- Pogos on die pad
- Thermal button on die pad ($R_{th} = 9$ °C/W)
- BART = heatsink on the cover ($R_{th} = 25$ °C/W)
**Socket Impact**

**Different signal pin type**

- Measurements confirm that thermal performance of B is worse than A.
- This is due to the difference in pin performance.
- For B, simulation is more conservative than actual.

<table>
<thead>
<tr>
<th>Socket Id</th>
<th>Socket reference</th>
<th>Socket description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>777905000-500-A0-01</td>
<td>54 P-pin + 9 P-pin for the die pad</td>
</tr>
<tr>
<td>B</td>
<td>777905000-500-A0-02</td>
<td>54 S-pin + 9 P-pin for the die pad</td>
</tr>
</tbody>
</table>

**Socket Impact**

**Number of pins on the die pad**

- Increasing the number of pins on the die pad improves the thermal performance.
- For C, simulation close to actual. Signal path become negligible due to number of P-pin on die pad.

<table>
<thead>
<tr>
<th>Socket Id</th>
<th>Socket reference</th>
<th>Socket description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>777905000-500-A0-02</td>
<td>54 S-pin + 9 P-pin for the die pad</td>
</tr>
<tr>
<td>C</td>
<td>777905000-500-A0-03</td>
<td>54 S-pin + 9 P-pin for the die pad</td>
</tr>
</tbody>
</table>
Socket Impact

**Different pin type for both signal & die pad**

- Global thermal performance is influenced by the thermal characteristics of the pin chosen
- Variation between simulation and actual data but trend correct

### Socket Impact

**Different pin structure for the die pad**

- Thermal button improve global Rja
- But was not able to get all the gain expected by thermal button (too few vias between die pad and ground plane)

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Paper #2

13
**Socket Impact**

*Open-top vs Clamshell design*

- Simulation sees no difference between clamshell and open top socket
- Actual data shows that open top is worse than clamshell

Rjca is through:
- package surface only with open top socket
- by whole socket surface with clamshell

---

**Socket Impact**

*Integrated heatsink*

- Even though thermally enhanced package is designed to dissipate heat through the thermal pad on the bottom, adding a heatsink improve Rjca thus global Rja
- This is confirmed by simulation and actual
Socket Impact

Cumulative impact of button & heatsink

- Using best performance Rjba (thermal button) and Rjca (heatsink) improves global Rja

<table>
<thead>
<tr>
<th>Socket Id</th>
<th>Socket reference</th>
<th>Socket description</th>
<th>Thermal Ranking</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>7172P5650-500-A0-00</td>
<td>56-pin + Thermal button for the die pad</td>
<td>6 6</td>
</tr>
<tr>
<td>F</td>
<td>7172P5650-500-A0-06</td>
<td>56-pin + 9-pin + BART</td>
<td>9 9</td>
</tr>
<tr>
<td>J</td>
<td>7172P5650-500-A0-10</td>
<td>56-pin + Thermal button for the die pad + BART</td>
<td></td>
</tr>
</tbody>
</table>
**Socket Impact**

And what about a “standard” socket based on package mechanical parameters only?

<table>
<thead>
<tr>
<th>Socket Id</th>
<th>Socket Reference</th>
<th>Socket Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>27106015-590-adj</td>
<td>88 P-pin, 89 S-pin for the die pad</td>
</tr>
<tr>
<td>C</td>
<td>27106015-590-adj</td>
<td>88 P-pin, 89 S-pin for the die pad</td>
</tr>
<tr>
<td>D</td>
<td>27106015-590-adj</td>
<td>88 P-pin, 89 S-pin for the die pad</td>
</tr>
<tr>
<td>&quot;Standard&quot;</td>
<td>27106015-590-adj</td>
<td>88 P-pin, 89 S-pin for the die pad</td>
</tr>
</tbody>
</table>

- B socket is the same as C with less P-pins on die pad
- “standard” would be the same as D with less S-pins on die pad

**“Package Outline Drawing” is not enough for socket selection**

**Conclusion**

- DOE shows that *simulations and actual data follow the same tendency*. But amplitudes appear different due to incomplete/unknown information such as accurate design/package information or considering self-heating of the contacts.

- In fact, *the real simulation « fine-tuning » is all in the details* i.e. the more detailed the information which is considered (such as precise package structure, die/lid ratio, lid material, precise socket/pcb setup…) always improves the accuracy of the simulation data

- Since device and chamber contribution in thermal performance can not be modified, *socket thermal design becomes an increasingly important factor* to consider and optimize the overall thermal performance (Rja) of the device-socket-board structure during an HTOL test.

- But … even with an « optimal socket design » the benefit of this upfront accurate design will be lost if other aspects such as board design and population, chamber population and Ventilation…are not taken into account by the lifetest engineers.

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2012 BiTS Workshop ~ March 4 - 7, 2012
Wall-extended Coaxial Socket

Collins Sun, Justin Liu, Jack Liang  
WinWay Technology Co., Ltd.  
Kuan-Chung Lu; Tzyy-Sheng Horng  
National Sun Yat-Sen University

Content

• Introduction to wall-extended coaxial socket  
• How to achieve the design concept?  
• Socket test performance  
• Summary

Coaxial socket  
=Performance oriented product!!
Introduction to wall-extended coaxial socket

Why Coaxial Structure?

- High testing speed demand (Digital)
- Highly customized product (RF)
- Well impedance control and wide bandwidth
- Noise shield (Crosstalk reduction)
- Not limited by the physical length

Introduction to wall-extended coaxial socket

Wall-extended Coaxial Socket structure
**Introduction to wall-extended coaxial socket**

**Socket structure comparison**

- **63%**
- **78%**

---

**Test configuration**

**Introduction to wall-extended coaxial socket**

**Performance comparison**

<table>
<thead>
<tr>
<th>Metal coverage (%)</th>
<th>Coaxial socket</th>
<th>Wall-extended coaxial socket</th>
<th>Improvement (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>78</td>
<td>23</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin arrangement</th>
<th>Bandwidth (GHz)</th>
<th>Improvement (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8GND</td>
<td>15.91</td>
<td>24.66</td>
</tr>
<tr>
<td>+Gnd</td>
<td>17.46</td>
<td>23.53</td>
</tr>
<tr>
<td>GSG</td>
<td>8.18</td>
<td>11.1</td>
</tr>
<tr>
<td>SG</td>
<td>4.63</td>
<td>6.2</td>
</tr>
</tbody>
</table>

---

2012 BiTS Workshop ~ March 4 - 7, 2012
**Introduction to wall-extended coaxial socket**

*Metal housing connected to PCB GND.*

**Metal Housing**

- **PCB GND**
- **GND Pin (DUT GND)**

---

**Noise Shielding**

- Signal shielding locally
- Wall-extended design
- Ordinary design
- Poor noise shielding
How to achieve the design concept?

Parallel pair conductor transmission line theory

$\beta l$  
$Z_0$

$Z_0 = \sqrt{\frac{L}{C}}$

$\beta$: wave number  
$l$: pin length

$L_{(S-G)} = \frac{\mu}{\pi} \cosh^{-1}\left(\frac{D}{2a}\right) \cdot l_{pin}$

$C_{(S-G)} = \frac{\pi \varepsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)} \cdot l_{pin}$

How to achieve the design concept?

$L_{(S-G)} = \frac{\mu}{\pi} \cosh^{-1}\left(\frac{D}{2a}\right) \cdot l_{pin}$

$C_{(S-G)} = \frac{\pi \varepsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)} \cdot l_{pin}$

$L_{GS} = \frac{3}{4} \times L_{S-G}$

$L_{GND} = \frac{5}{8} \times L_{S-G}$

$L_{full} = \frac{1}{2} \times L_{S-G}$

$C_{GS} = \frac{4}{3} \times C_{S-G}$

$C_{GND} = \frac{8}{5} \times C_{S-G}$

$C_{full} = 2 \times C_{S-G}$

Characteristic impedance of lossless line:

$Z_0 = \sqrt{\frac{L}{C}}$

Coaxial socket!!
How to achieve the design concept?

Consider coaxial socket as the **multi-stage transmission line**

\[
L = \frac{\mu}{2\pi} \ln\left(\frac{b}{a}\right) \cdot l_{\text{pin}}
\]

\[
C = \frac{2\pi \varepsilon}{\ln\left(\frac{b}{a}\right)} \cdot l_{\text{pin}}
\]

Coaxial region

Parameter Definition:
- \(a\): Pin diameter;
- \(b\): Pin hole;
- \(D\): Signal to ground distance

\[
L_{(S-G)} = \frac{\mu}{\pi} \cosh^{-1}\left(\frac{D}{2a}\right) \cdot l_{\text{pin}}
\]

\[
C_{(S-G)} = \frac{\pi \varepsilon}{\cosh^{-1}\left(\frac{D}{2a}\right)} \cdot l_{\text{pin}}
\]

Insulating region

---

How to achieve the design concept?

Consider coaxial socket as the **multi-stage transmission line**

\[
\begin{bmatrix}
A_1 & B_1 \\
C_1 & D_1
\end{bmatrix} = \begin{bmatrix}
A_2 & B_2 \\
C_2 & D_2
\end{bmatrix} = \begin{bmatrix}
A_3 & B_3 \\
C_3 & D_3
\end{bmatrix}
\]

\[
\begin{aligned}
\beta l_1 & \quad Z_{01} \\
\beta l_2 & \quad Z_{02} \\
\beta l_3 & \quad Z_{03}
\end{aligned}
\]

Insulating region  Coaxial region  Insulating region

---
How to achieve the design concept?

Total Impedance Calculation

\[
\begin{bmatrix}
A_1 & B_1 \\
C_1 & D_1
\end{bmatrix} = \begin{bmatrix}
A_2 & B_2 \\
C_2 & D_2
\end{bmatrix} \begin{bmatrix}
A_3 & B_3 \\
C_3 & D_3
\end{bmatrix}
\]

\[
\begin{bmatrix}
A_t & B_t \\
C_t & D_t
\end{bmatrix} = \begin{bmatrix}
\cos \beta l_t & jZ_{0t} \sin \beta l_t \\
-jY_{0t} \sin \beta l_t & \cos \beta l_t
\end{bmatrix}
\]

\[Z_{0t} = \frac{B_t}{C_t} = \frac{A_1 A_2 B_3 + B_1 C_1 B_3 + A_2 B_2 D_3 + B_2 D_2 D_3}{C_1 A_2 A_3 + D_1 C_2 A_3 + C_1 B_2 C_3 + D_1 D_2 D_3}
\]

How to achieve the design concept?

**Impedance control of coaxial socket can perform outstandingly!!**

*Insulating housing*

\( \varepsilon_r = 3.3; \tan \delta = 0.001\)

*Metal housing*

Impedance vs Radius of pin hole

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Socket test performance

Measurement setup

Double-Sided Probing System

Test-Fixture

The comparison of simulation and real measurement

Magnitude (dB) Phase (degree)

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Socket test performance

The comparison of simulation and real measurement

- **S11**
- **S22**

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---

**Insertion loss comparison**

<table>
<thead>
<tr>
<th>GSG Ratio of 1:2 (signal to ground probes)</th>
<th>Plastic socket</th>
<th>Wall-extended coaxial socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSG</td>
<td>5.91</td>
<td>11.1</td>
</tr>
<tr>
<td>SG</td>
<td>2.66</td>
<td>6.2</td>
</tr>
</tbody>
</table>

Improvement (%)

<table>
<thead>
<tr>
<th>Pin arrangement</th>
<th>Plastic socket</th>
<th>Wall-extended coaxial socket</th>
<th>Improvement (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GSG</td>
<td>5.91</td>
<td>11.1</td>
<td>87.82</td>
</tr>
<tr>
<td>SG</td>
<td>2.66</td>
<td>6.2</td>
<td>133.08</td>
</tr>
</tbody>
</table>

3/2012 Wall-extended Coaxial Socket
### Socket test performance

#### Measured Insertion loss Comparison

<table>
<thead>
<tr>
<th>Design</th>
<th>Plastic Socket</th>
<th>Coaxial Socket</th>
<th>Wall-extended coaxial socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>structure</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Profile</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bandwidth (-1dB@GHz)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GSG</td>
<td>5.91</td>
<td>8.18</td>
<td>11.10</td>
</tr>
<tr>
<td>SG</td>
<td>2.66</td>
<td>4.63</td>
<td>6.20</td>
</tr>
</tbody>
</table>

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### Socket test performance

#### Eye diagram results of 40Gb/s

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### Socket test performance

#### Eye diagram comparison

**Plastic socket** vs **Wall-extended coaxial socket**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Plastic Socket</th>
<th>Wall-extended coaxial socket</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin arrangement</td>
<td>GSG</td>
<td>GSG</td>
</tr>
<tr>
<td>Eye Height (mV)</td>
<td>263.55</td>
<td>196.26</td>
</tr>
<tr>
<td>Eye Width (s)</td>
<td>2.23E-11</td>
<td>1.62E-11</td>
</tr>
<tr>
<td>Eye Jitter (PP)</td>
<td>2.72E-12</td>
<td>8.81E-12</td>
</tr>
</tbody>
</table>

#### Rock Package test result

- **Shmoo Plot**: PCIe Gen 3 Pass!!
- **TX eye opening**: Wall-extended coaxial socket

**Plastic socket (3.0mm)**

3/2012 Wall-extended Coaxial Socket
Summary

- Wall-extended coaxial design could effectively improve the RF performance compared with ordinary coaxial design and plastic socket.
- The highly customized techniques were necessary to meet the various application.

Acknowledgment

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