What good is it to have optimized test devices if the characterization and analysis processes aren't up to speed as well? This session focuses on the whole picture. We open with methods for taking device specifications and translating them into test contactor requirements to reduce the impact of testing the device in the contactor. Next we'll move on to the challenges of balancing signal integrity with power integrity through the socket and PC board. The session wraps up with two presentations investigating parameters; the first discusses key parameters of pulse current testing and their significance and the second shares some crucial parameters in thermal simulations.

**Understanding Specs to Better Simulate Solder-to-Board Performance**  
Jeff Sherry—Johnstech International

**Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices**  
Thomas P. Warwick, Al Seier—R&D Circuits, Inc.

**Pulse Current Testing: Parameters and Their Significance**  
Gert Hohenwarter—GateWave Northern, Inc.

**Key Parameters in Thermal Simulations**  
Larry Furman, Joseph Ortega—Plastronics Sockets & Connectors

***COPYRIGHT NOTICE***

The papers in this publication comprise the Proceedings of the 2012 BiTS Workshop. They reflect the authors’ opinions and are reproduced here as they were presented at the 2012 BiTS Workshop. This version of the papers may differ from the version that was distributed in hardcopy & softcopy form at the 2012 BiTS Workshop. The inclusion of the papers in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.

There is NO copyright protection claimed by this publication (occasionally a Tutorial and/or TechTalk may be copyrighted by the author). However, each presentation is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.
Understanding Specs to Better Simulate Solder-to-Board Performance

Jeff Sherry
Johnstech International

2012 BiTS Workshop
March 4 - 7, 2012

Agenda

- Changes in Contactor performance
  - Inductance effects
  - Thermal or current carrying effects
  - Cres and repeatability
- Importance of design margins
- Effects of device configurations
- Mechanical considerations
- Test methods
- Conclusion
Causes of Changes in Performance

- Variations in signal path
- Variations in insertion position
- Variations in oxides and debris buildup
- Variations in package platings
- Variations in I/O pitch
- Variations in location of ground or return path
- Variations in insertion forces and speed

High Gain Amplifier Spec Sheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-GHz Transmit Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Compliance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Nominal Conditions</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Specifications must be met across VDD, VSS, and temperature unless otherwise specified</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.4</td>
<td>2.5</td>
<td></td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>Power Supply</td>
<td>3.0</td>
<td>3.3</td>
<td>4.2</td>
<td></td>
<td>V</td>
<td>Rw x nominal voltage supply (VDD)</td>
</tr>
<tr>
<td>VDD Voltage</td>
<td>ON</td>
<td>3.0</td>
<td>5.1</td>
<td>3.6</td>
<td>V</td>
<td>Rw x &quot;ON&quot; state</td>
</tr>
<tr>
<td></td>
<td>OFF</td>
<td>0.50</td>
<td>0.26</td>
<td>0.40</td>
<td>V</td>
<td>Rw x &quot;OFF&quot; state</td>
</tr>
<tr>
<td>Output Power</td>
<td>1.1</td>
<td>1.8</td>
<td>1.9</td>
<td>dBm</td>
<td></td>
<td>S4.5kHz 54MHz 54MHz 5V</td>
</tr>
<tr>
<td></td>
<td>1.9</td>
<td>1.9</td>
<td>1.9</td>
<td>dBm</td>
<td></td>
<td>S4.5kHz 54MHz 54MHz 5V</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>1.2</td>
<td>1.2</td>
<td>dBm</td>
<td></td>
<td>1.1kHz 51kHz 5V</td>
</tr>
<tr>
<td></td>
<td>1.1</td>
<td>1.2</td>
<td>1.2</td>
<td>dBm</td>
<td></td>
<td>1.1kHz 51kHz 5V</td>
</tr>
<tr>
<td>EVM</td>
<td>5.5</td>
<td>4.6</td>
<td></td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Adjacent Channel Power</td>
<td>3.6</td>
<td>-33</td>
<td>dBm</td>
<td></td>
<td></td>
<td>Pout = 1MHz 1.1kHz 51kHz 5V, note 2</td>
</tr>
<tr>
<td></td>
<td>-33</td>
<td>-33</td>
<td>dBm</td>
<td></td>
<td></td>
<td>VDD = 2.5V, meeting 11u spectral mask</td>
</tr>
<tr>
<td></td>
<td>-95</td>
<td>-95</td>
<td>dBm</td>
<td></td>
<td></td>
<td>requirements</td>
</tr>
<tr>
<td>Gain</td>
<td>20</td>
<td>24</td>
<td></td>
<td></td>
<td>dB</td>
<td>At rated power and a given supply voltage, room temp</td>
</tr>
<tr>
<td>Gain Variation Steps</td>
<td>3.0</td>
<td>4.2</td>
<td></td>
<td></td>
<td>V</td>
<td>2.45Hz to 2.5Hz</td>
</tr>
</tbody>
</table>

Testing at hot will stress device if die temperature is exceeded!
Effects of Inductance

Gain ($S_{21}$) With Different Grounding vs. Soldered Down

- Amplifier gains above 20 dB more sensitive to ground inductance

Higher amplifier gains require lower ground inductance!!

High Power Amplifier Spec Sheet

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical Conditions</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>2.5</td>
<td>GHz</td>
<td>Tune A</td>
</tr>
<tr>
<td></td>
<td>2.7</td>
<td>GHz</td>
<td>Tune B</td>
</tr>
<tr>
<td></td>
<td>3.3</td>
<td>GHz</td>
<td>Tune C</td>
</tr>
<tr>
<td>Output Power</td>
<td>30</td>
<td></td>
<td>Tune A, B, C, D</td>
</tr>
<tr>
<td>Voltage (V)</td>
<td>3.3</td>
<td>V</td>
<td>10% 10% Mod 50% 50%</td>
</tr>
<tr>
<td>Stability</td>
<td>33</td>
<td>dBi</td>
<td>RF should be measured from 0 dBm to 30 dBm</td>
</tr>
<tr>
<td>Gain</td>
<td>11</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>3</td>
<td>dB</td>
<td>Peak PEP over 300 MHz bandwidth</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Operating Current</td>
<td>1.3</td>
<td>Amp</td>
<td>RF $P_{out} = 100$ dBm</td>
</tr>
<tr>
<td>Backoff Current</td>
<td>200</td>
<td>mA</td>
<td>Non-Linear</td>
</tr>
<tr>
<td>LO Current</td>
<td>10</td>
<td>mA</td>
<td>for RF</td>
</tr>
<tr>
<td>Leakage Current</td>
<td>100</td>
<td>uA</td>
<td></td>
</tr>
<tr>
<td>Turn on Time From Setting F</td>
<td>400</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>-10</td>
<td>dB</td>
<td>In linear band</td>
</tr>
<tr>
<td>Isolation Loss</td>
<td>-10</td>
<td>dB</td>
<td>In linear band</td>
</tr>
<tr>
<td>Stable Into Deadband SWR</td>
<td>-31</td>
<td>dB</td>
<td>(outside 47 dBm)</td>
</tr>
</tbody>
</table>

Amplifiers have large bandwidths so it is difficult to optimize performance! Large DC power, 1W RF out -> rest is heat!!
Material Softening/Melting Voltages

<table>
<thead>
<tr>
<th>Material</th>
<th>Softening Volts (V)</th>
<th>Melting Volts (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>0.10</td>
<td>0.30</td>
</tr>
<tr>
<td>Iron</td>
<td>0.19</td>
<td>0.19</td>
</tr>
<tr>
<td>Nickel</td>
<td>0.16</td>
<td>0.16</td>
</tr>
<tr>
<td>Copper</td>
<td>0.12</td>
<td>0.43</td>
</tr>
<tr>
<td>Zinc</td>
<td>0.10</td>
<td>0.17</td>
</tr>
<tr>
<td>Silver</td>
<td>0.09</td>
<td>0.37</td>
</tr>
<tr>
<td>Cadmium</td>
<td>0.15</td>
<td>0.16</td>
</tr>
<tr>
<td>Tin</td>
<td>0.07</td>
<td>0.13</td>
</tr>
<tr>
<td>Gold</td>
<td>0.08</td>
<td>0.43</td>
</tr>
<tr>
<td>Palladium</td>
<td>0.57</td>
<td>0.57</td>
</tr>
<tr>
<td>Lead</td>
<td>0.12</td>
<td>0.19</td>
</tr>
<tr>
<td>60Cu-40Zn</td>
<td>0.20</td>
<td>0.25</td>
</tr>
</tbody>
</table>

Source: Tinuron Scientific Inc., Electrical Contacts And Electroplating In Separable Connectors

The low melting voltage of Matte Tin can cause test problems!!

Current Carrying Example Calculations

<table>
<thead>
<tr>
<th>Contact Resistance</th>
<th>Current to Soften</th>
<th>Current to Melt</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 mOhms</td>
<td>3.5 A</td>
<td>6.5 A</td>
</tr>
<tr>
<td>50 mOhms</td>
<td>1.4 A</td>
<td>2.6 A</td>
</tr>
<tr>
<td>100 mOhms</td>
<td>0.7 A</td>
<td>1.3 A</td>
</tr>
<tr>
<td>150 mOhms</td>
<td>0.47 A</td>
<td>0.87 A</td>
</tr>
<tr>
<td>200 mOhms</td>
<td>0.35 A</td>
<td>0.65 A</td>
</tr>
<tr>
<td>250 mOhms</td>
<td>0.28 A</td>
<td>0.52 A</td>
</tr>
<tr>
<td>500 mOhms</td>
<td>140 mA</td>
<td>260 mA</td>
</tr>
</tbody>
</table>

Lower $C_{\text{res}}$ solutions enable higher current carrying capability!!
0.5mm Pitch Socket Contacts Current Carrying Capacity

Test times can be longer with less current carrying capability!!

Socket With Too Much $C_{res}$

Customer later switched to Contactor using solid contacts to dissipate heat required to achieve desired test times.

Oops!! Excessive heat caused by normal increases in $C_{res}$ and not considering required production duty cycles can melt sockets!!
RDSon Measurements Needs Low $C_{res}$

Wide variations in Contact $C_{res}$ cause excessive false failures!!

ROL™ Technology $C_{res}$
With NiPdAu Plated Device @ 175 °C

Solid contacts provide low and stable $C_{res}$!
Contact Resistance Repeatability – Solid Contact vs. Spring Pin

Actual production data shows $C_{\text{res}}$ variability causing false failures!

Contactor RF Repeatability – Solid ROL™ Technology

Contact and elastomer were not replaced during test

Solid contact has very good RF repeatability!
Contactor Digital Repeatability – Solid ROL™ Technology

Solid contact has consistent repeatable delay!

3/2012 Understanding Specs to Better Simulate Solder-to-Board Performance 15

0.8mm Pitch Verticon® 100 BGA Insertion Loss vs. Compression – S21

Shorter Contact lengths improve RF performance!

3/2012 Understanding Specs to Better Simulate Solder-to-Board Performance 16
0.8mm Pitch Verticon® 100 BGA Return Loss vs. Compression – $S_{11}$

Increasing contact interfaces increases variation in RF performance during compression!

Importance of Design Margin

- Contact resistance will increase over time
- Debris or oxides may impact $C_{res}$ or ground inductance path
- IR drop across interfaces could cause softening or melting of device plating
- Variation in signal path and ground location will vary electrical performance

All of these will affect Guard Bands and Test Limits

NOTE: The contactor will always add more ground inductance and resistance to the path than solder-to-board performance!
Proximity of grounds affects performance at higher frequencies!

Both pitch and contact design impacts characteristic impedance!
Verticon® 100 BGA Modeled Data
For Different Pitches – S_{41}

Return loss is correlated to Crosstalk!

Signal Transition Comparison
RF Signal Launch vs. Airplane Take Off

RF performance degrades with every right angle connection!!
Mechanical Considerations

- Wiping action vs. no wiping action effects MTBA and cleaning intervals
- One piece vs. multiple parts: more parts = more variability
- Handler interface issues – insertion speed
- Maintenance of parts
- Test conditions affect performance

Mechanical features also affect RF performance!

Solid Contact Shows Minimal Wear After 500K Insertions
C<sub>res</sub> Test Method Differences

- Testing with correct device plating
  - Gold on gold gives best results. Majority of package use other platings (i.e. Matte Tin and NiPdAu)
  - Hardness of plating affects performance
  - Oxide level affects performance
  - Wear and contaminants affect life
  - Wiping or self cleaning action affect MTBA
- Testing at correct forces and insertion speeds
  - Higher the force the lower the C<sub>res</sub>
  - Higher the force the shorter the contact life and MTBA

Conclusion

- Ground inductance is extremely important when measuring high frequency signals and devices with high gain
- Shorter paths result in better electrical performance (hypotenuse shorter than sum of legs)
- Solid contacts have current carrying advantages over contacts with multiple parts
- Fewer contact interfaces result in lower Cres
- Repeatability improves both electrical and mechanical data accuracy resulting in higher yields
- Not all specifications are created equal
Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

Thomas P. Warwick, Al Seier
R&D Circuits, Inc.

Purpose and Content

This Presentation discusses ATE-Specific Interface Issues for >25GB/s Devices

• Comparing ATE to the “Real World”
• Signal and Power Integrity Conflicts
• Compromises
• Concluding Comments
Comparing ATE to the “Real World”

Real World

Transmission Path

Path Response = F(x) => \( S_{21} \)

(ideal)

\( 1/f(x) \)

TX

RX

Data

Path

Correction

Data

S21

S21

S21

S21

Comparing ATE to the “Real World”

Real World

ATE

socket

Relay or other circuit

Longer vias

2 levels of Discontinuity
Package + Via

Full Adaptive Training

4 levels of Discontinuity
Package + Socket + Via + Relay

DFT Modified Training

Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

3/2012

3/2012

3/2012
Comparing ATE to the “Real World”

A reminder: Digital Pre-emphasis / equalization cannot correct for discontinuities, just monotonic loss.

Signal and Power Integrity Conflicts

Key Signal Integrity Requirements:

1. Minimize Discontinuities
   a) Socket + Entry Via
   b) Via + Relay or circuitry
   c) Impedance Controlled or Coaxial Vias

2. Improve Isolation / Reduce Crosstalk
   a) Increased Spacing
   b) Better Ground Plane Coverage
   c) Increased Quantity Ground Vias
Signal and Power Integrity Conflicts

Key Signal Integrity Design:

- High Performing S11 in surrounded ground designs
- Short impedance controlled via under socket desired
- Impedance Controlled Via

Materials Adjusted

Metal Probes Can still Work! (Elastomer is better.)
Signal and Power Integrity Conflicts

Key Power Integrity Requirements:

1. High Current Power Delivery
   a) Via Size, Plane Thickness, and Plane Redundancy
   b) “Web” or “Swiss Cheese” Effect
   c) Power Dissipation in the Socket pin

2. Transient Suppression
   a) Via and Socket Inductance
   b) Cres and ESR

Signal and Power Integrity Design:
Signal and Power Integrity Conflicts

Key Power Delivery Design: (Power Web Issues)

- Soft Shorted vias
- Remains of power trace
- Normal web width
- Conductive Carbonization (burning)

Thermal Image of 174 amps in 0.4mm pitch @ 115°C

Key Power Delivery Design: (Redesign for Fine Pitch)

- Package
- Socket
- PC board

Thermal Image of 174 amps in 0.4mm pitch @ 115°C

2012 BiTS Workshop ~ March 4 - 7, 2012
Signal and Power Integrity Conflicts

Key Power Integrity Design for Transients:

- **Vdd**
- **Droop**

### Summary of Critical Conflicts:

- Both PI and SI requirements want respective routing stacked high in the board.
- Fine pitch and back-drilling cause power delivery issues ("Web" or "Swiss cheese" effect).
- PI is far more sensitive to ESR – "equivalent series resistance"; C_res is a component of ESR.
- SI can survive longer socket pins; PI cannot.
Compromises

Load board Construction:
Signal and Power Delivery In Fine Pitch

- Solid Planes
- No web effect
- But higher inductance
- Embedded capacitor

Compromises

Improved Power Delivery with Embedded Cap:

- Vdd
- Socket causes droop

Design pattern still fails

Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

3/2012
Compromises

Improved Power Delivery with Elastomer Socket And Embedded Capacitor:

- Vdd → Socket still causes droop

Concluding Comments

- Test will likely always compromise relative to any “real world” environment.
- Attention to Signal integrity issues over the past few years make ultra high data rates possible in pinned sockets.
- Power remains a challenge both for the PC board, especially in high power and fine pitch.
- Elastomer contactors, while not “production worthy”, remain the best choice for transient power management.
Background

- Pulse testing of contacts can generate a wide variety of responses and results for critical parameters like:
  - Current handling capability
  - Contact temperature rise
- Interpretation of measurements depends on:
  - Test parameters
  - Test environment
  - Instrumentation
  - Test methods
Objective

• Identify potential pitfalls in pulse current testing
• Instrumentation
• Measurement techniques
• Test specimen

• Provide some guidelines for performance assessment

• Highlight impact of pulse current exposure of contacts on measured performance

Approach

• Provide overview of basic parameters

• Utilize test results to demonstrate significance of full understanding required for pulse test models and procedures

• Engage computer simulations to demonstrate impact of test environment and parameters
• SPICE circuit simulator
• ANSYS HFSS field modeler
• 2.5D modeler for thermal problems
Contact design

- Important parameters
  - Electrical resistance
  - Thermal resistance
  - Thermal mass

- Cooling mechanisms
  - Conduction
  - Convection
  - Radiation

Operating parameters

- What a contact may be subjected to:
  - DC (steady state) current
  - AC (alternating / RF) current
  - Short term loads
  - Spikes from malfunctions
  - Ambient temperature

- Consequences of exceeding design envelope
  - Parameter changes
  - Bulk
  - Surface
  - Premature (longer term) wear/failure
  - Immediate failure
Current with a particular time dependency is applied and temperature is monitored along the length of the contact.

**Pulse Operation**

- Measurement points

**Simulated short pulse response**

- A short pulse causes only a slight temperature rise in the contact center since propagation of heat requires potentially significant amount of time.
- Temperature rise will be much larger in narrow sections of contact that are not as well cooled.

**Graphs:**

- Simulated short pulse response graph showing temperature rise over time.
- Current pulse graph showing current versus time.
Impact of long pulse

- After a short time contact temperature reaches steady state
- There is little difference in response time for different test point locations

Impact of shorter pulse

- Contact temperature does not reach steady state
- Temperature in the center peaks after the end of the pulse

Instrumentation timing becomes an issue.
**Impact of very short pulse**

- Contact temperature does not reach steady state
- Temperature in the center peaks long after the end of the pulse

**High duty cycle short pulses**

- Contact temperature does not reach steady state
- Temperature levels ramp up due to gradual warming of environment
Effect of averaging and long acquisition times on overall results: Error is largest in the narrow portions of the contact near the ends.

This shows a sequence of readings on TC meter. Clearly, timing determines the outcome of the measurement.
DC and pulse test

This shows R and V across contact in a succession of tests conducted after applying pulse current as specified.

I max changes after I pulse

This shows $I_{max}$ for 20C Trise after applying pulse current and a last data point after dis/reassembly.
DC and pulse test

This shows R and V across contact in a succession of tests conducted after applying pulse current as specified.

I max changes after I pulse

This shows $I_{\text{max}}$ for 20C Trise after applying pulse current.
After dis- and re-assembly resistance has gone up noticeably even when touching on Au (orange curve).

Matte Sn (1 large area tip)

This shows $I_{max}$ for 20C Trise after applying pulse current and a last data point after dis/reassembly.

Matte Sn (1 large area tip)
This shows $T_{\text{rise}}$ as a function of pulse current level.

This shows $T_{\text{rise}}$ as a function of pulse current duty cycle.
Performance after mechanical actuation

Significant noise development is evident after 10k cycles but disappeared after high pulse current was applied.

Performance after mechanical actuation

Significant reduction in Imax is evident after 10k cycles but disappeared after high pulse current was applied.
Conclusion

- Pulse test requires accurate knowledge of system time constants
  - Source
  - Load
  - Thermal time constants of specimen
  - Instrumentation
- Assessment of maximum current capability is not straightforward
  - Measurement point for highest temperature rise may not be accessible
  - A force based criterion may be more descriptive measure
Key Parameters in Thermal Simulations

Joseph Ortega, Larry Furman
Plastronics Sockets & Connectors

2012 BiTS Workshop
March 4 - 7, 2012

Outline

• Device Power Dissipation
• DUT Heat Variance is Increasing
• BIB Active Control Parameters Challenge
• CFD Conjunctive Heat Transfer Simulation
• Modeling The System
• Establishing Target Guidelines
• Tuning Parameters / Heat Sink Size
• Summary / Conclusion
Some of the power consumed by IC devices gets dissipated as heat loss. This energy loss is equal to the resistance of a circuit times the square of current flowing through it.

\[ P = I^2R. \]

Industry rule of thumb is to budget 15-20% of IC power draw to thermo-electric heat loss.

\[ \text{20 Watts Thermal Loss} \]
\[ \text{100 Watt (Power in)} \]
\[ \text{80 Watts (productive output)} \]

Power Dissipation Variances are Increasing

As circuit density and frequencies get higher, and voltages drop, process variations impacting resistance could have a bigger influence.

* (i.e., a 30 m-ohm resistance change in a 500 m-Ω circuit is only a 6% change, but it’s a 30% variation for a 100 m-Ω circuit.) This % change also correlates to heat loss variability.
Power Dissipation Variances are Increasing (cont’d)

• At Higher frequencies -> current travels increasingly near conductor surface (“skin effect”), contributing to increased circuit resistance.

• Other internal die effects contributing to increased heat loss variability, (i.e., leakage currents, gate switching) and also tend to have a cumulative effect in heat loss variance\(^{(1)}\).

\(^{(1)}\) ref. Freescale Semi BitS 2008 Session 4, paper #2

+/- 50% Variance In Same Lot?

• Really ??
• Need Higher Precision Inputs / Verification
• What is the sample distribution, std. deviation, etc. ?
• Can we get lot sample measurement data and stats ?
**What About Sample Size & Confidence Values?**

* WHAT ABOUT SAMPLE SIZE?

What if we sampled 4 parts and measured 30W, 40W, 50W, and 65W of heat dissipation, what is the 95% confidence interval for the mean of the population?

Ans: 46.25W +/- 23.75 W = [22.5 W – 70W]*

Conclusion: With a limited data set which also has a large standard deviation, we can’t really predict much about a population, so Burn In Test Engineer is forced to evaluate “worse case” extremes.


---

**Power Density Trend and Higher Dissipation Variances = Burn-in Test Engineer Migraine**

![DUT Power Density Roadmap](image)
Determining Optimum Active BIB Control Parameters

Can CFD SIMS Help Me Get Near the Ballpark?

Conjugate Heat Transfer CFD

The combination of convection and conduction heat exchange, is known as conjugate heat transfer. Conjugate simulations are referred to coupled fluid-solid temperature calculations.
Fortunately, today’s software technology assists greatly in modeling most of the thermal challenges of burn-in. A good checklist for modeling is as follows:

- Thermal resistance of the die and case (or package)
- Wattage range of the device
- Die size
- Size of the case or heat spreader
- Ambient oven temperature
- Inlet air temperature
- Box or envelop size of the system
- Air velocity and direction or cross-flow, and or inlet valve size if directly over the heat sink

With this information, a proper heat sink can be constructed, as well as determining if the heater cartridges imbedded in the heat sink will properly bring the device to temperature quickly enough within the recommend working duty cycle of the cartridge. If there is a controller on the fan speed or valve, a calculation can also be performed to ensure it’s not overworked as well.

An added benefit to the model also includes a finite element analysis (FEA) on the heat sink force to ensure there is not an excessive load on the die.
Model Preparation

- Outlet: standard pressure
- Ambient Air @ 25°C
- 60 & 18 W heat sources

3.2 ft/s (cross-flow)
TOP 6 ft²/min (inlet area = 0.55 in²)

Simulation Output

Heat input
- 60 W (embedded cartridge heater rod)
- 18 W (at bottom surface of heat sink)

Temp (°C)

The heat sink must also be optimized to be the "correct" efficiency – too efficient and the lower wattage parts will not heat to temperature, and not efficient enough and the package will go into thermal runaway.
Simulation Output

DUT & Heat Sink - Temp Distribution

1.8 ft³/min top inlet
3 ft/s cross-flow
65W from Device
60W cartridge heater
~50% duty cycle
Simulation Output

Top Inlet volume flow 1.8 ft/min
[9mm (0.3543 in) x 40 mm (1.5748 in)]
Opening (0.5580 sq. in)

BIB Crossflow
Inlet velocity 3.33 ft/s

Input Parameter Consideration 1

• DIE VS. CASE TEMP - Where is control location, internal IC circuit or external couple? This location is the feedback loop to control heater cartridge activation in the simulation model. Depending on location, setpoint value changes.

Die (internal circuit sensor)

Case surface thermo-couple sensor location

$\Delta T = \text{Between die vs. case ?}$
Input Parameter Consideration 2

- What is acceptable setpoint target Temp Tolerance band? (125°C target, but +/- ?)

50 W DUT
60 W Cartridge Heater
(turn off when DUT > 125°C)

Input Parameter Consideration 3

- What is considered optimal time to setpoint TEST TEMP? (i.e., with 125°C target, what is acceptable +/- time window?)
Input Parameter Consideration 4

• Cartridge Heater Output vs. Rating Consideration

• Input voltage drives cartridge heat power output (Voltage supply can be on lower end of rated +/- 15% nominal value).

• Since output Power relative to input voltage is $P = V^2/R$, a 15% lower voltage results in >25% less Power output from the cartridge heater.

Input Parameter Consideration 5

• Top air Inlet Orientation vs. Heat Sink Fins length-wise arrangement vs. cross-flow direction
• Orientation impacts Heat Sink efficiency
• (orthogonal -> better efficiency vs. parallel)

Heat Sink Fins orthogonal to x-flow and top air inlet = more cooling efficiency
Input Parameter Consideration 6

- Test OVEN AIR TEMP "AMBIENT" (what's the process variation, how well is it controlled?)

Summary / Conclusions

- Industry trending towards higher variances with DUT heat dissipation

- Increases in Circuit Density and resulting power draw in combination with larger variances in heat dissipation result in greater (max., min.) test conditions.

- A "one size fits all" solution with nominal heat sink & active Burn-in oven control parameters may not always be adequate, tuning of control parameters and/or heat sink could be necessary.

- Pro-active CFD simulations of set up parameters and heat sink adjustments can help Test Engineers better prepare for various “game time” situations (i.e., plan “a”, “b”, etc.)
Summary / Conclusions (cont’d)

With growing thermal concerns, using modeling tools can assist in solving issues. Diligence is needed in the selection of capital equipment on the front end in to make sure it can handle the range of devices that need to be tested, but once selected, additional hardware that includes boards, heat sink and sockets can be accurately modeled to achieve the goal – burn-in at the exact temperature needed.

Better inputs -> More accurate CFD simulations -> Less time spent “tuning” BIB parameters = Faster product 
time to market!

Appendix


If $\bar{x}$ and $s^2$ are the mean and variance of a sample of size $n$ from a normal distribution $N(\mu, \sigma^2)$, where $\mu$ and $\sigma^2$ are unknown, then:

$$\bar{x} \pm [(t_{n-1; \alpha/2}) \times (s) \div (\text{sq. root (n)})]$$

Is a $100(1 – \alpha)$% confidence interval for $\mu$.

Ref. $t$ = Student $t$ distribution (approaches normal distribution $\sim z$ when (n -1) is large

For sample parts measuring 30, 40, 50, 65 Watts. Then:

$\overline{x} = 46.25$, n = 4, and $s = 14.9$ ; therefore $(s) \div (\text{sq. root (n)}) = 14.9 / 2 = 7.45$

For confidence interval: $1 – \alpha = 0.95$, then $\alpha = .05$ and $\alpha \div 2 = 0.025$ and $n – 1 = 3$, we then find from t distribution reference table for $t_{3; 0.025} = 3.182$

So confidence interval = $46.25 \pm (3.182) \times (7.45) = 46.25 \pm 23.7 = [22.5 – 70]$