THIRTEENTH ANNUAL BiTS 2012 Burn-in & Test Strategies Workshop

Session 3

ARCHIVE 2012

ANALYZE THIS

What good is it to have optimized test devices if the characterization and analysis processes aren't up to speed as well? This session focuses on the whole picture. We open with methods for taking device specifications and translating them into test contactor requirements to reduce the impact of testing the device in the contactor. Next we'll move on to the challenges of balancing signal integrity with power integrity through the socket and PC board. The session wraps up with two presentations investigating parameters; the first discusses key parameters of pulse current testing and their significance and the second shares some crucial parameters in thermal simulations.

Understanding Specs to Better Simulate Solder-to-Board Performance

Jeff Sherry—Johnstech International

Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

Thomas P. Warwick, Al Seier—R&D Circuits, Inc.

Pulse Current Testing: Parameters and Their Significance

Gert Hohenwarter—GateWave Northern, Inc.

Key Parameters in Thermal Simulations

Larry Furman, Joseph Ortega—Plastronics Sockets & Connectors

Understanding Specs to Better Simulate Solder-to-Board Performance

Jeff Sherry
Johnstech International

2012 BiTS Workshop
March 4 - 7, 2012

Agenda

- Changes in Contactor performance
  - Inductance effects
  - Thermal or current carrying effects
  - Cres and repeatability
- Importance of design margins
- Effects of device configurations
- Mechanical considerations
- Test methods
- Conclusion

Causes of Changes in Performance

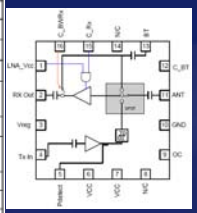
- Variations in signal path
- Variations in insertion position
- Variations in oxides and debris buildup
- Variations in package platings
- Variations in I/O pitch
- Variations in location of ground or return path
- Variations in insertion forces and speed

High Gain Amplifier Spec Sheet

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
2.4 GHz Transmit Parameters					**Front End Module**
Compliance					IEEE802.11b, IEEE802.11g, FCC CFG 15.247, .205, .209, EN, and JDEC
Nominal Conditions					Specifications must be met across V_{CC}, V_{REG}, and Temperature; unless otherwise specified.
Frequency	2.4		2.5	GHz	
Power Supply	3.0	3.3	4.2	V	PA nominal voltage supply (V_{CC})
V_{REG} Voltage					
ON	3.0	3.1	3.2	V	PA in "ON" state
OFF		0.00	0.20	V	PA in "OFF" state
Output Power					
11g	18	18.5		dBm	54 Mbps, OFDM 54 Mbps, $V_{CC} \geq 3.0V$
	19	19.5		dBm	54 Mbps, OFDM 54 Mbps, $V_{CC} \geq 3.3V$
11b	20	22		dBm	11 Mbps, CCK, $V_{CC} \geq 3.0V$
EVM		3.3	4.0	%	$P_{OUT(g)}$ = Rated Output Power, 54 Mbps OFDM, 50Ω, see note 1
Adjacent Channel Power					$P_{OUT(b)}$ = 20 dBm 1 Mbps CCK, note 2
ACP1		-36	-33	dBc	$V_{CC} \geq 3.3V$, meeting 11b spectral mask requirements
ACP2		-56	-51	dBc	
Gain	26	30	34	dB	
Gain Variation Slope					At rated power and a given supply voltage, room temp
Range	3.0		4.2	V	
Frequency	-0.5		+0.5	dB	2.4 GHz to 2.5 GHz

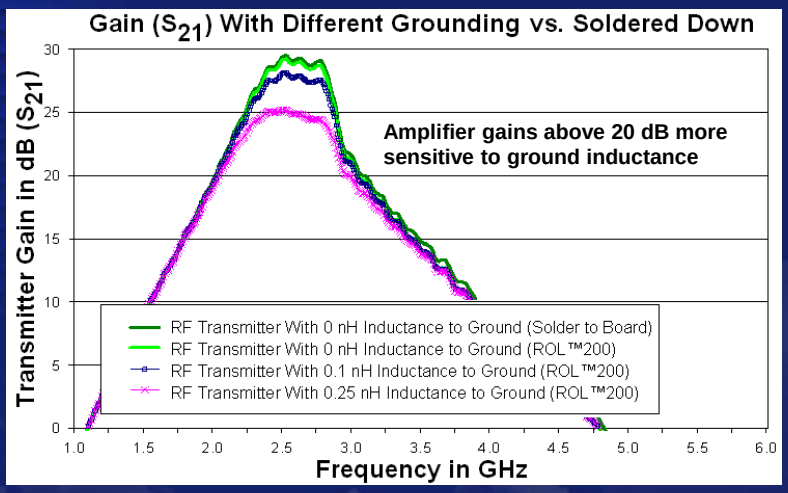
http://www.rfmd.com/CS/Documents/RF5758D5.pdf

Schematic



Testing at hot will stress device if die temperature is exceeded!

Effects of Inductance



Higher amplifier gains require lower ground inductance!!

High Power Amplifier Spec Sheet

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Typical Conditions					Temp=25°C, Frequency=2.3GHz to 3.8GHz depending on the evaluation board tune, V_{CC}=V_{PC}=6.0V unless otherwise specified
Frequency	2.3		2.5	GHz	Tune A
	2.5		2.7	GHz	Tune B
	2.7		2.9	GHz	Tune C
	3.3		3.8	GHz	Tune D
Output Power		30			Tune A, B, C, D
EVM		3.0		%	802.16e 16QAM 3/4 modulation, P_{OUT}=+30dBm
Stability	0		33	dBm	PA should be stable when P_{OUT} is measured from 0dBm to 33dBm
Gain		11		dB	
Gain Flatness			3	dB	Peak-Peak over any 300MHz bandwidth
Noise Figure		5		dB	
Operating Current		1.3		Amp	RF P_{OUT}=+30dBm, V_{CC}=6V
Quiescent Current		900		mA	
I_VPC Current		10		mA	No RF
Leakage Current		100		uA	
Turn-on Time from Setting of V_{BIAS}			400	ns	Output stable within 90% of final gain
Input Return Loss		-15	-10	dB	In tune band
Output Return Loss		-10	-7	dB	In tune band
Stable into Output VSWR			4:1		No spurs above -47dBm

http://www.rfmd.com/CS/Documents/RFS643DS.pdf

Amplifiers have large bandwidths so it is difficult to optimize performance! Large DC power, 1W RF out -> rest is heat!!

Material Softening/Melting Voltages

Material	Softening Volts (V)	Melting Volts (V)
Aluminum	0.10	0.30
Iron	0.19	0.19
Nickel	0.16	0.16
Copper	0.12	0.43
Zinc	0.10	0.17
Silver	0.09	0.37
Cadmium	0.15	0.16
Tin	0.07	0.13
Gold	0.08	0.43
Palladium	0.57	0.57
Lead	0.12	0.19
60Cu,40Zn	0.20	0.25

Source: Timron Scientific Inc., *Electrical Contacts And Electroplates In Separable Connectors*

The low melting voltage of Matte Tin can cause test problems!!

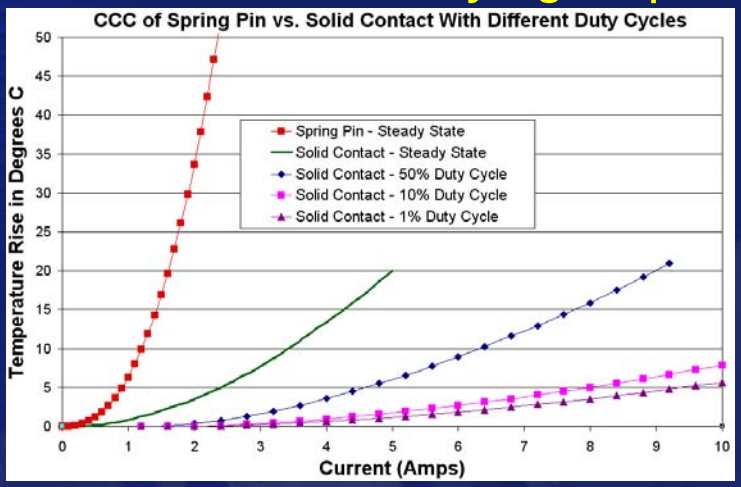
Current Carrying Example Calculations

For Matte Tin Plated Device

Contact Resistance	Current to Soften	Current to Melt
20 mOhms	3.5 A	6.5A
50 mOhms	1.4 A	2.6 A
100 mOhms	0.7 A	1.3 A
150 mOhms	0.47 A	0.87 A
200 mOhms	0.35 A	0.65 A
250 mOhms	0.28 A	0.52 A
500 mOhms	140 mA	260 mA

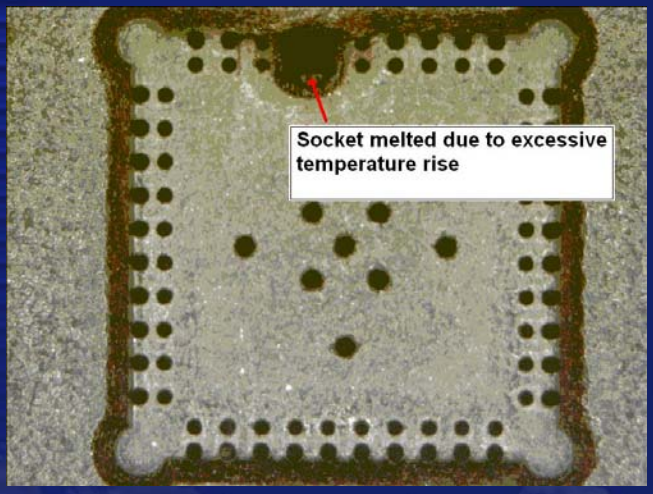
Lower C_{res} solutions enable higher current carrying capability!!

0.5mm Pitch Socket Contacts Current Carrying Capacity



Test times can be longer with less current carrying capability!!

Socket With Too Much C_{res}



Customer later switched to Contactor using solid contacts to dissipate heat required to achieve desired test times.

Oops!! Excessive heat caused by normal increases in C_{res} and not considering required production duty cycles can melt sockets!!

RDSon Measurements Needs Low C_{res}

FEATURES

- SON 2-mm × 2-mm Plastic Package

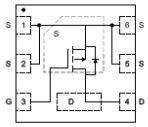
APPLICATIONS

- Battery Management
- Load Management
- Battery Protection

DESCRIPTION

The device has been designed to deliver the lowest on resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra low profile for space constrained applications.

Top View

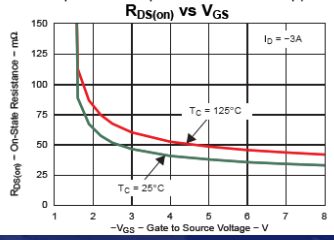


P-Channel NexFET™ Power MOSFET

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	–20	V
Q_g	Gate Charge Total (–4.5V)	2.6	nC
Q_{gd}	Gate Charge Gate to Drain	0.5	nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = –1.8V: 71	mΩ
		V_{GS} = –2.5V: 56	mΩ
		V_{GS} = –4.5V: 39	mΩ
$V_{GS(th)}$	Threshold Voltage	–0.65	V

$R_{DS(on)}$ vs V_{GS}



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Continuous Drain Current, T_C = 25°C	–5	A
	Continuous Drain Current(1)	–5	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	–20	A
P_D	Power Dissipation	2.4	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C

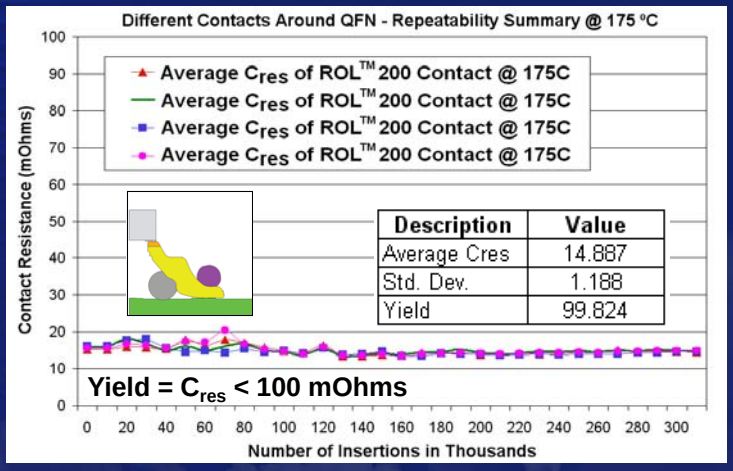
(1) Package Limited

(2) Pulse duration 10 µs, duty cycle ≤2%

http://www.ti.com/lit/ds/symlink/csd25302q2.pdf

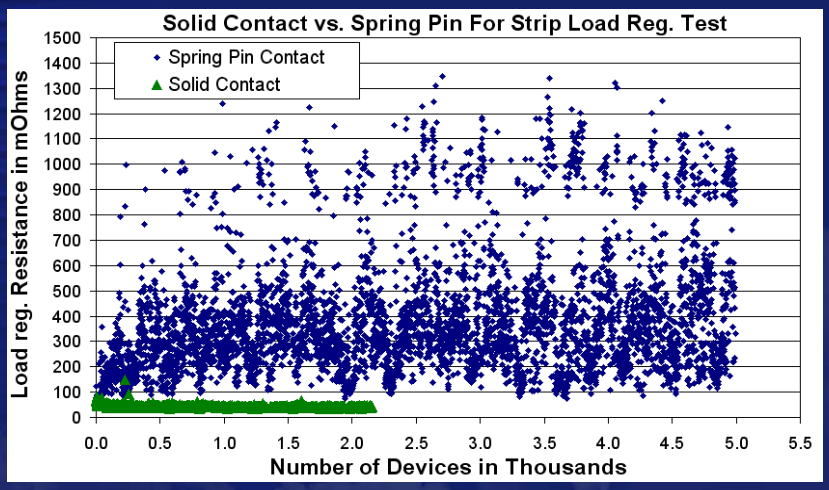
Wide variations in Contact C_{res} cause excessive false failures!!

ROL™ Technology C_{res} With NiPdAu Plated Device @ 175 ºC



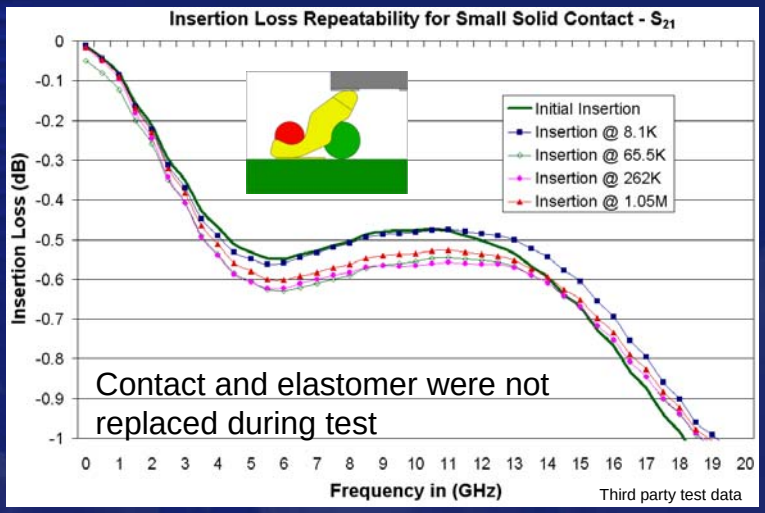
Solid contacts provide low and stable C_{res}!

Contact Resistance Repeatability – Solid Contact vs. Spring Pin



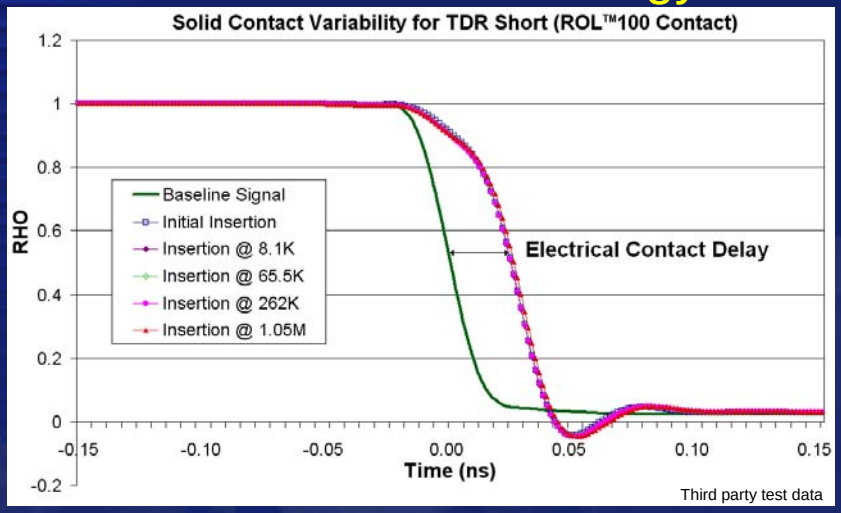
Actual production data shows C_{res} variability causing false failures!

Contactor RF Repeatability – Solid ROL™ Technology



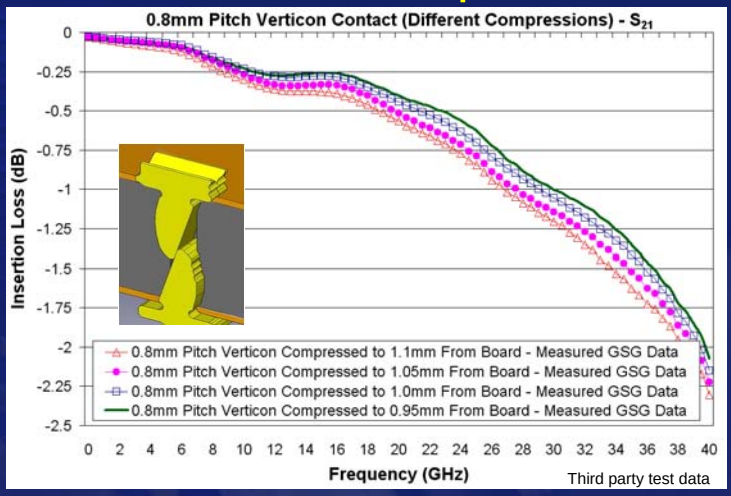
Solid contact has very good RF repeatability!

Contactor Digital Repeatability – Solid ROL™ Technology



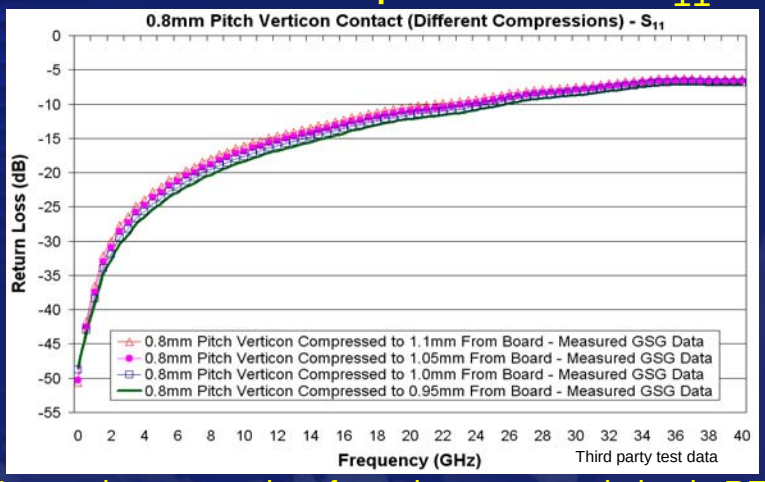
Solid contact has consistent repeatable delay!

0.8mm Pitch Verticon® 100 BGA Insertion Loss vs. Compression – S_{21}



Shorter Contact lengths improve RF performance!

0.8mm Pitch Verticon® 100 BGA Return Loss vs. Compression – S_{11}



Increasing contact interfaces increases variation in RF performance during compression!

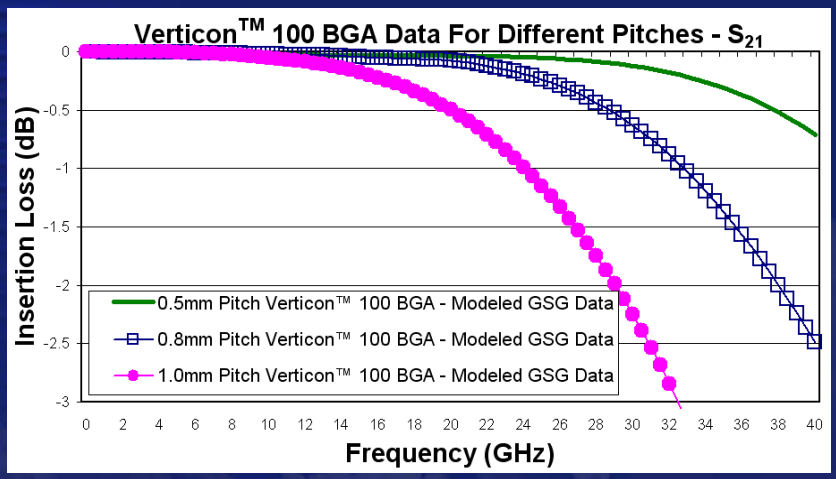
Importance of Design Margin

- Contact resistance will increase over time
- Debris or oxides may impact C_{res} or ground inductance path
- IR drop across interfaces could cause softening or melting of device plating
- Variation in signal path and ground location will vary electrical performance

All of these will affect Guard Bands and Test Limits

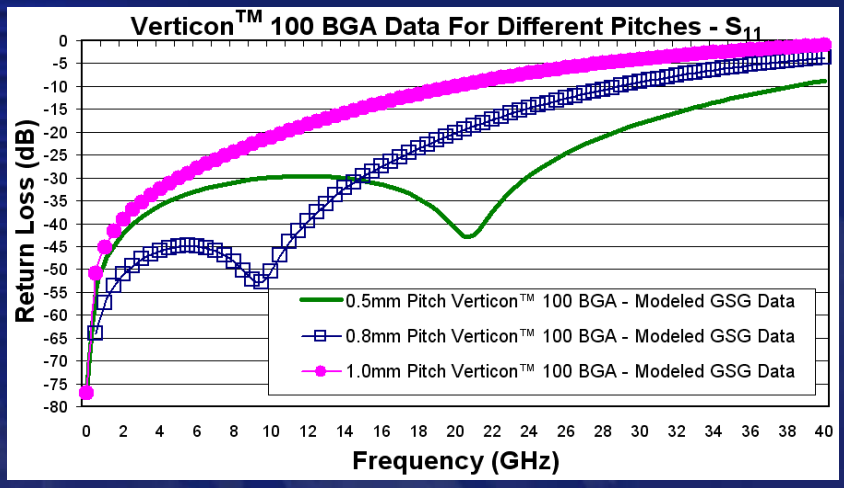
NOTE: The contactor will always add more ground inductance and resistance to the path than solder-to-board performance!

Verticon® 100 BGA Modeled Data For Different Pitches – S_{21}



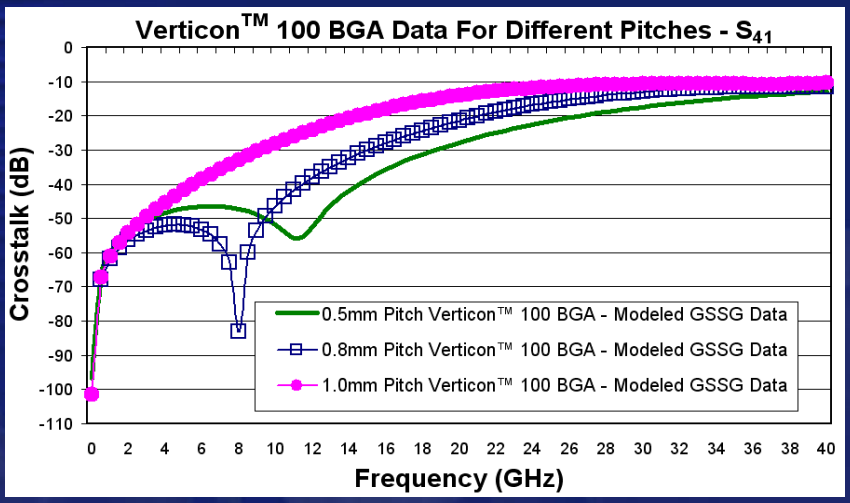
Proximity of grounds affects performance at higher frequencies!

Verticon® 100 BGA Modeled Data For Different Pitches – S_{11}



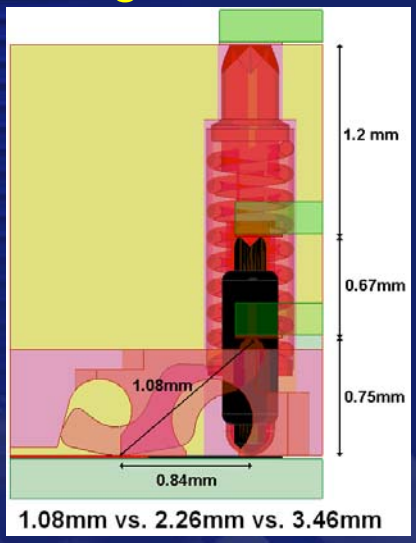
Both pitch and contact design impacts characteristic impedance!

Verticon® 100 BGA Modeled Data For Different Pitches – S_{41}



Return loss is correlated to Crosstalk!

Signal Transition Comparison RF Signal Launch vs. Airplane Take Off



1.08mm vs. 2.26mm vs. 3.46mm

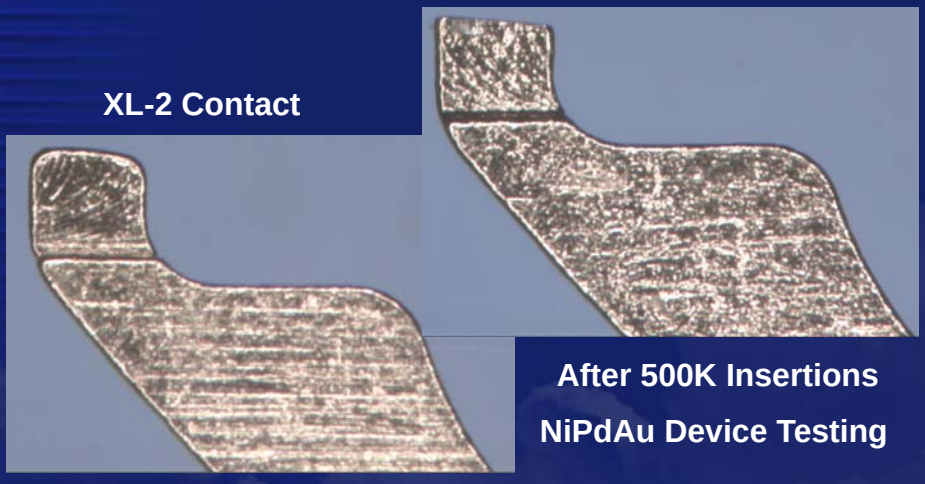
RF performance degrades with every right angle connection!!

Mechanical Considerations

- Wiping action vs. no wiping action effects MTBA and cleaning intervals
- One piece vs. multiple parts : more parts = more variability
- Handler interface issues – insertion speed
- Maintenance of parts
- Test conditions affect performance

Mechanical features also affect RF performance!

Solid Contact Shows Minimal Wear After 500K Insertions



C_{res} Test Method Differences

- Testing with correct device plating
  - Gold on gold gives best results. Majority of package use other platings (i.e. Matte Tin and NiPdAu)
  - Hardness of plating affects performance
  - Oxide level affects performance
  - Wear and contaminants affect life
  - Wiping or self cleaning action affect MTBA
- Testing at correct forces and insertion speeds
  - Higher the force the lower the C_{res}
  - Higher the force the shorter the contact life and MTBA

Conclusion

- Ground inductance is extremely important when measuring high frequency signals and devices with high gain
- Shorter paths result in better electrical performance (hypotenuse shorter than sum of legs)
- Solid contacts have current carrying advantages over contacts with multiple parts
- Fewer contact interfaces result in lower Cres
- Repeatability improves both electrical and mechanical data accuracy resulting in higher yields
- Not all specifications are created equal

Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

Thomas P. Warwick, Al Seier
R&D Circuits, Inc.

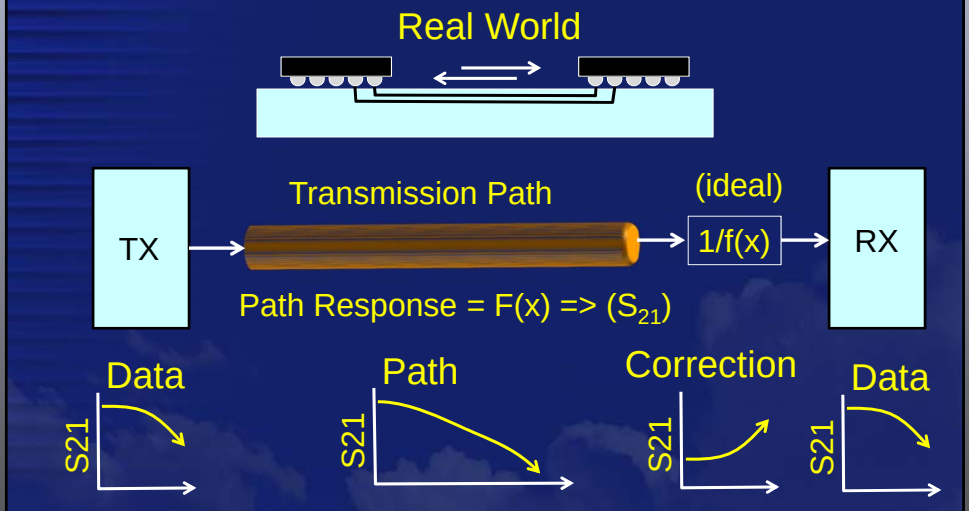
2012 BiTS Workshop
March 4 - 7, 2012

Purpose and Content

This Presentation discusses ATE-Specific Interface Issues for >25GB/s Devices

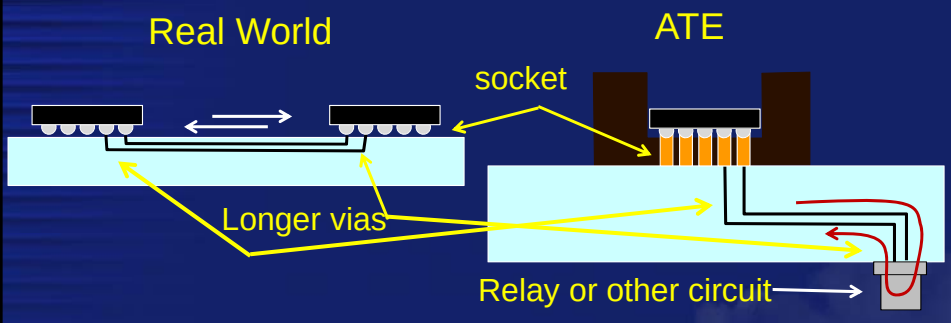
- Comparing ATE to the "Real World"
- Signal and Power Integrity Conflicts
- Compromises
- Concluding Comments

Comparing ATE to the "Real World"



3/2012 Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices 3

Comparing ATE to the "Real World"



2 levels of Discontinuity
Package + Via

Full Adaptive Training

4 levels of Discontinuity
Package + Socket + Via + Relay

DFT Modified Training

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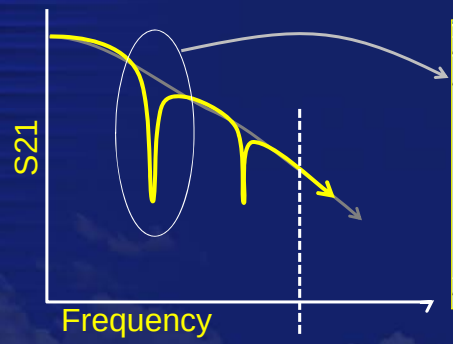
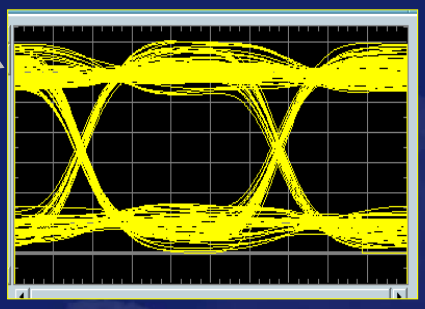
Comparing ATE to the "Real World"

A reminder: Digital Pre-emphasis / equalization cannot correct for discontinuities, just monotonic loss.





Low Loss Material Data Eye, Via Discontinuity

Signal and Power Integrity Conflicts

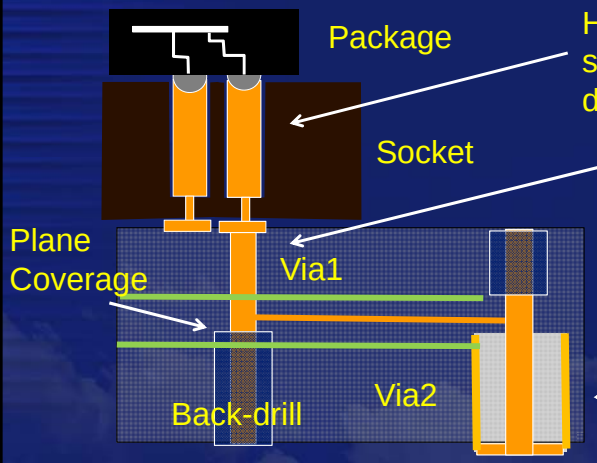
Key Signal Integrity Requirements:

1. Minimize Discontinuities
   a) Socket + Entry Via
   b) Via + Relay or circuitry
   c) Impedance Controlled or Coaxial Vias

2. Improve Isolation / Reduce Crosstalk
   a) Increased Spacing
   b) Better Ground Plane Coverage
   c) Increased Quantity Ground Vias

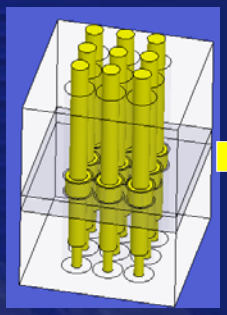
Signal and Power Integrity Conflicts

Key Signal Integrity Design:

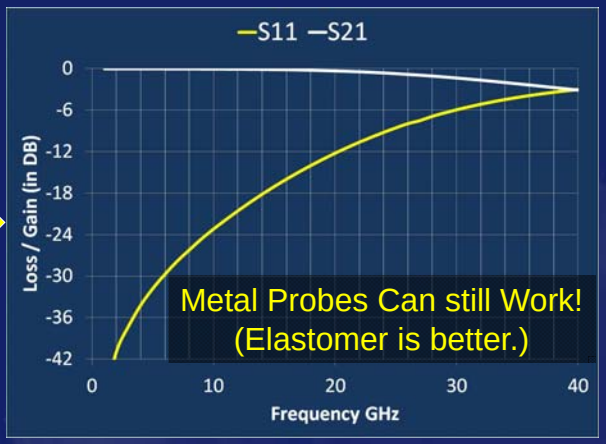


Signal and Power Integrity Conflicts

Key Signal Integrity Design:



Materials Adjusted



Signal and Power Integrity Conflicts

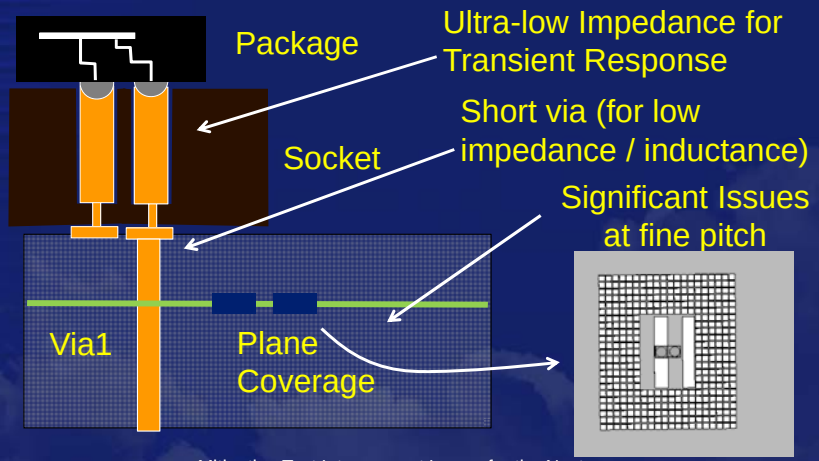
Key Power Integrity Requirements:

1. High Current Power Delivery
   a) Via Size, Plane Thickness, and Plane Redundancy
   b) "Web" or "Swiss Cheese" Effect
   c) Power Dissipation in the Socket pin

2. Transient Suppression
   a) Via and Socket Inductance
   b) Cres and ESR

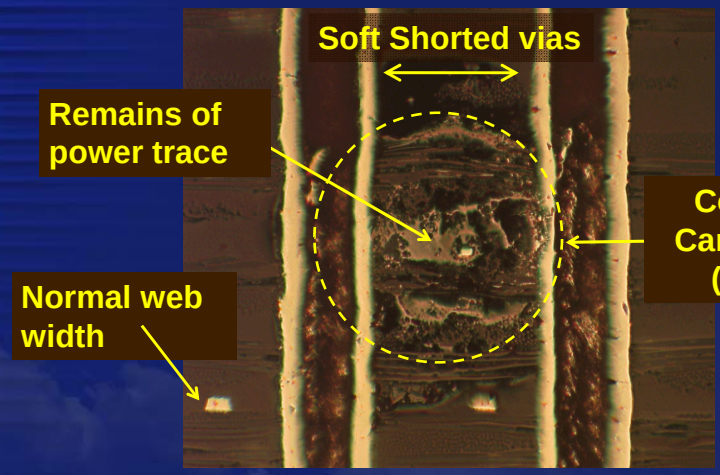
Signal and Power Integrity Conflicts

Key Power Integrity Design:



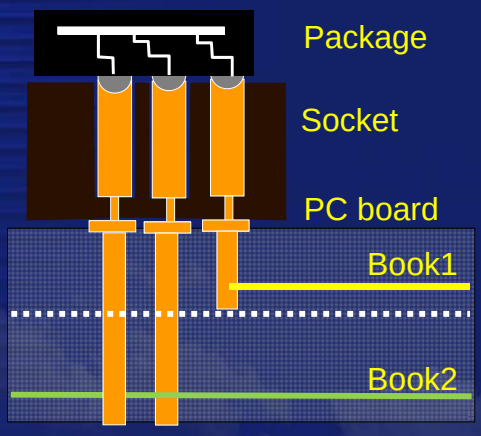
Signal and Power Integrity Conflicts

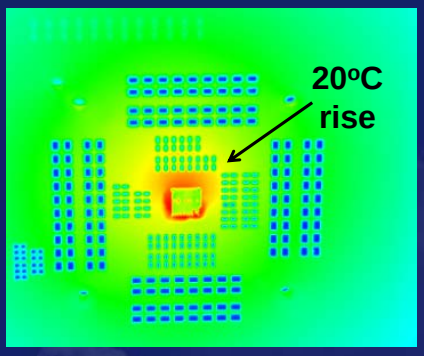
Key Power Delivery Design: (Power Web Issues)



Signal and Power Integrity Conflicts

Key Power Delivery Design: (Redesign for Fine Pitch)

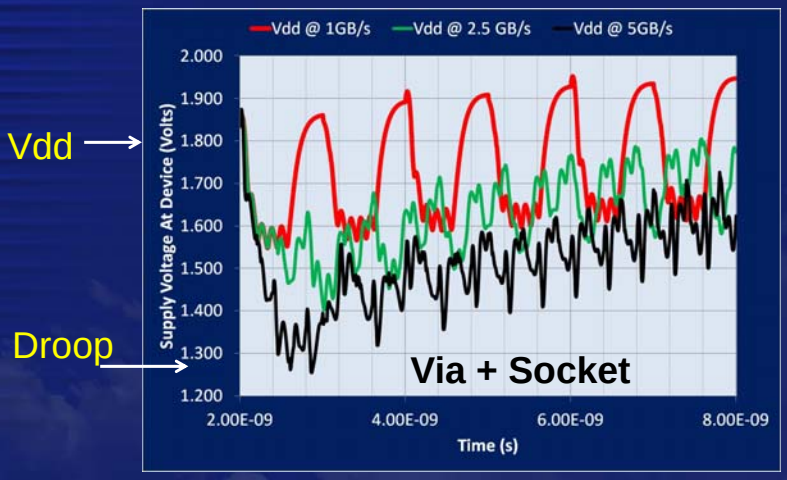




Thermal Image of 174 amps in 0.4mm pitch @ 115°C

Signal and Power Integrity Conflicts

Key Power Integrity Design for Transients:



Vdd →

Droop →

Signal and Power Integrity Conflicts

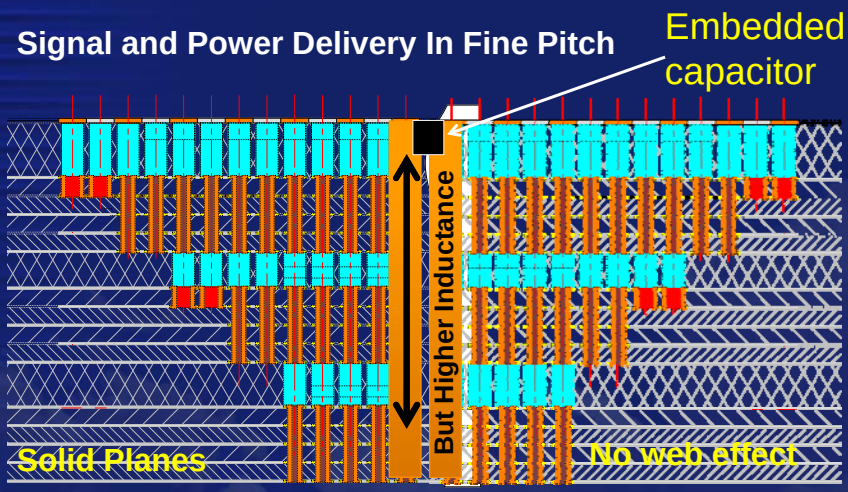
Summary of Critical Conflicts:

- Both PI and SI requirements want respective routing stacked high in the board.
- Fine pitch and back-drilling cause power delivery issues ("Web" or "Swiss cheese" effect).
- PI is far more sensitive to ESR – "equivalent series resistance"; Cres is a component of ESR.
- SI can survive longer socket pins; PI cannot.

Compromises

Load board Construction:

Signal and Power Delivery In Fine Pitch

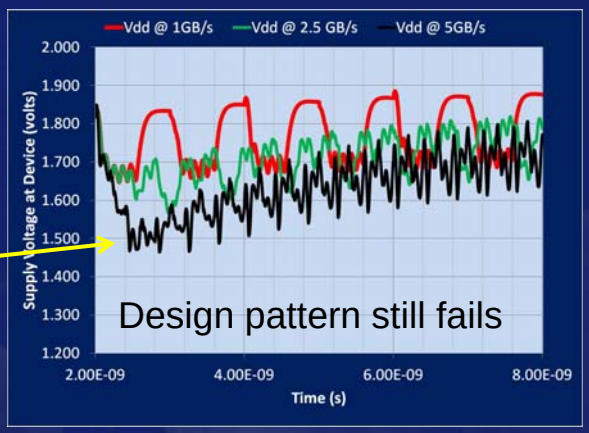


Compromises

Improved Power Delivery with Embedded Cap:

Vdd →

Socket causes droop →

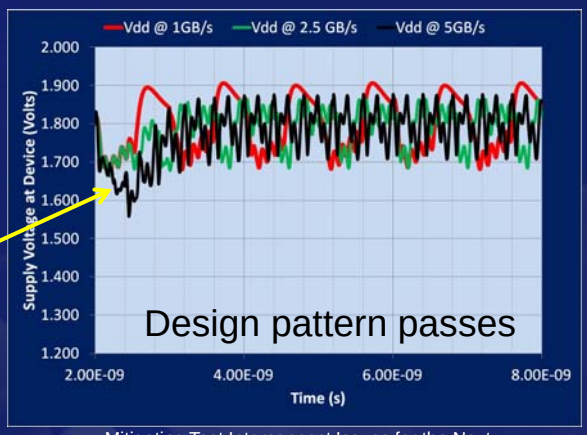


Compromises

Improved Power Delivery with Elastomer Socket And Embedded Capacitor:

Vdd →

Socket still causes droop



Concluding Comments

- **Test will likely always compromise relative to any "real world" environment.**
- **Attention to Signal integrity issues over the past few years make ultra high data rates possible in pinned sockets.**
- **Power remains a challenge both for the PC board, especially in high power and fine pitch.**
- **Elastomer contactors, while not "production worthy", remain the best choice for transient power management.**

Pulse Current Testing: Parameters and Their Significance

Gert Hohenwarter
GateWave Northern, Inc.

2012 BiTS Workshop
March 4 - 7, 2012

Background

- Pulse testing of contacts can generate a wide variety of responses and results for critical parameters like
- Current handling capability
- Contact temperature rise

- Interpretation of measurements depends on
- Test parameters
- Test environment
- Instrumentation
- Test methods

Objective

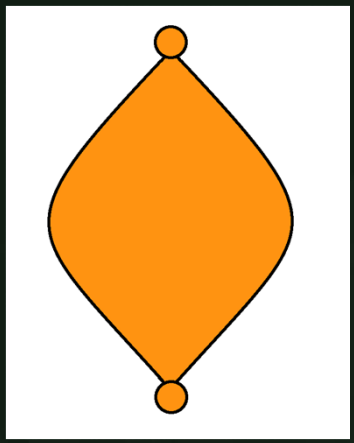
- Identify potential pitfalls in pulse current testing
- Instrumentation
- Measurement techniques
- Test specimen
- Provide some guidelines for performance assessment
- Highlight impact of pulse current exposure of contacts on measured performance

Approach

- Provide overview of basic parameters
- Utilize test results to demonstrate significance of full understanding required for pulse test models and procedures
- Engage computer simulations to demonstrate impact of test environment and parameters
- SPICE circuit simulator
- ANSYS HFSS field modeler
- 2.5D modeler for thermal problems

Contact design

- Important parameters
  - Electrical resistance
  - Thermal resistance
  - Thermal mass
- Cooling mechanisms
  - Conduction
  - Convection
  - Radiation

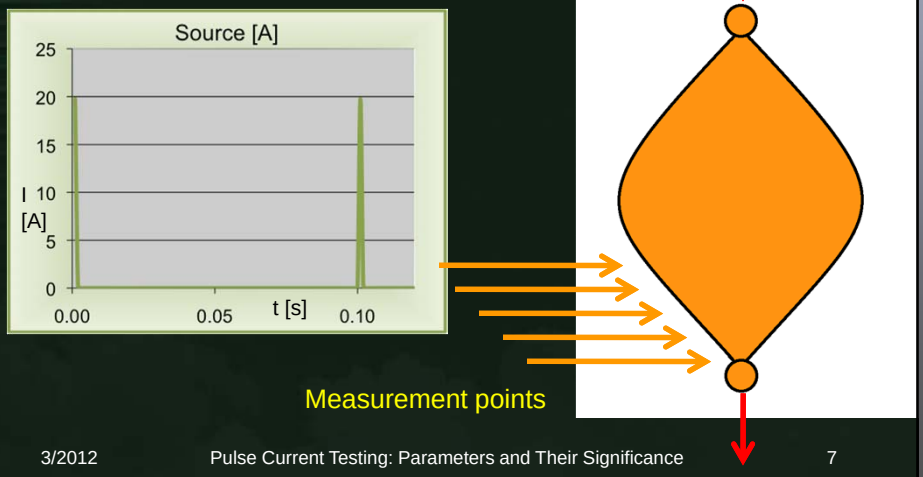


Operating parameters

- What a contact may be subjected to:
  - DC (steady state) current
  - AC (alternating / RF) current
  - Short term loads
  - Spikes from malfunctions
  - Ambient temperature
- Consequences of exceeding design envelope
  - Parameter changes
  - Bulk
  - Surface
  - Premature (longer term) wear/failure
  - Immediate failure

Pulse Operation

- Current with a particular time dependency is applied and temperature is monitored along the length of the contact



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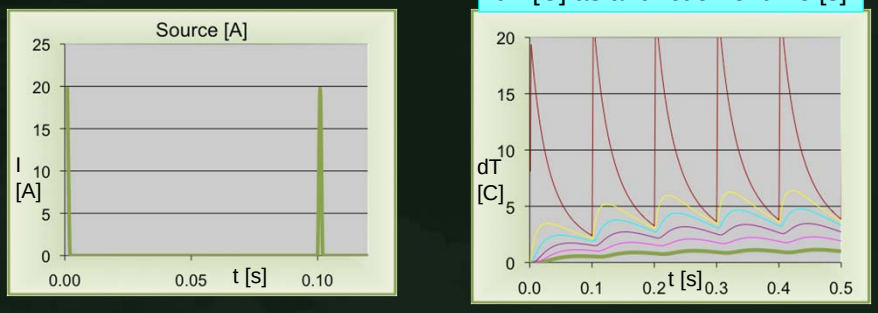
Simulated short pulse response

- A short pulse causes only a slight temperature rise in the contact center since propagation of heat requires potentially significant amount of time
- Temperature rise will be much larger in narrow sections of contact that are not as well cooled

20A 100 ms 1% duty cycle
dT [C] as a function of time [s]



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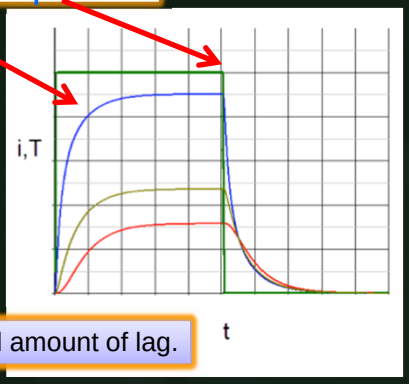
Paper #3
4

Impact of long pulse

$\tau_{th} << \tau_{pulse}$

- After a short time contact temperature reaches steady state
- There is little difference in response time for different test point locations



There is a small amount of lag.

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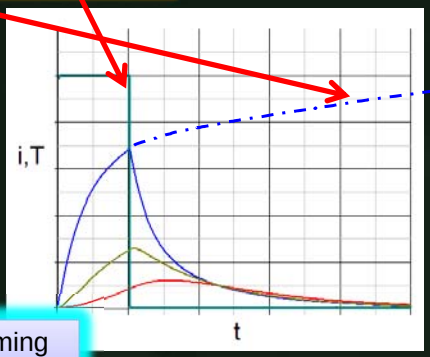
Impact of shorter pulse

$\tau_{th} > \tau_{pulse}$

- Contact temperature does not reach steady state
- Temperature in the center peaks after the end of the pulse



Instrumentation timing becomes an issue.

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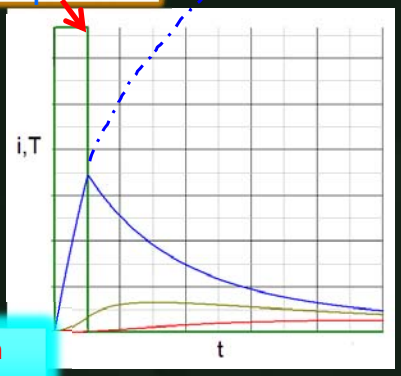
Impact of very short pulse

$\tau_{th} >> \tau_{pulse}$

- Contact temperature does not reach steady state
- Temperature in the center peaks long after the end of the pulse

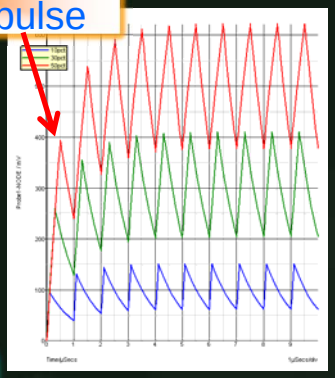


Instrumentation timing is critical.

High duty cycle short pulses

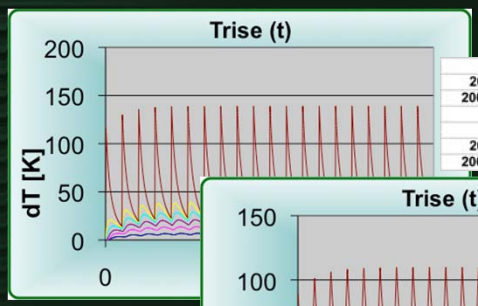
$\tau_{th} >> \tau_{pulse}$

- Contact temperature does not reach steady state
- Temperature levels ramp up due to gradual warming of environment



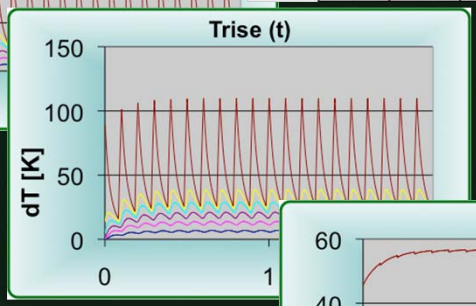
Instrumentation timing is critical.

Averaging



Temperature error						
20 ms	0.0	0.1	0.1	0.2	0.4	29.2
200 ms	0.6	1.2	2.1	3.7	7.3	82.0

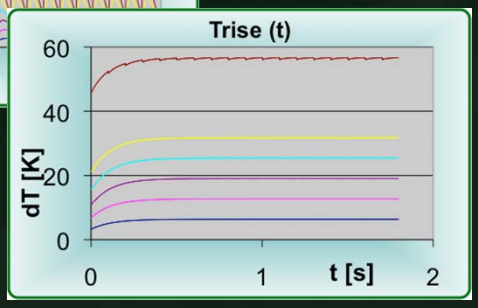
Percent error						
20 ms	0.4	0.4	0.4	0.6	1.1	21.1
200 ms	8.6	8.8	9.9	12.7	18.6	59.1



0 ms

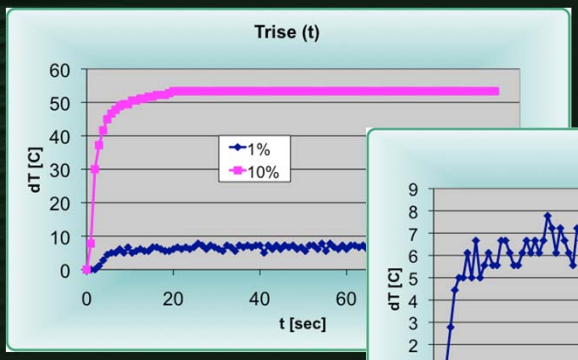
20 ms

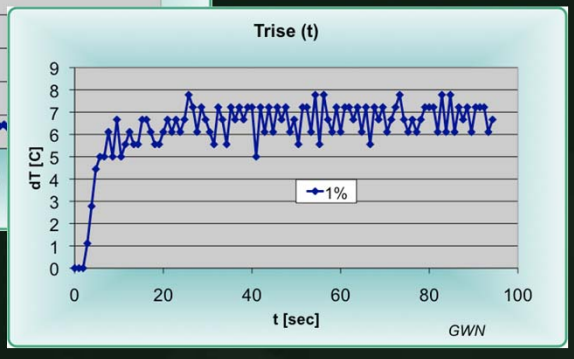
200 ms



Effect of averaging and long acquisition times on overall results: Error is largest in the narrow portions of the contact near the ends

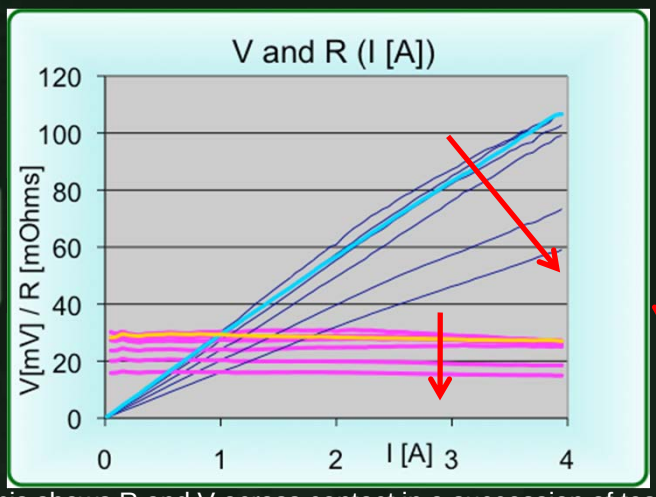
Trise during pulse test





This shows a sequence of readings on TC meter. Clearly, timing determines the outcome of the measurement

DC and pulse test



Au (pointed tips)

10% duty cycle

[A]
4.6
6.9
9.8
16.5
25.0

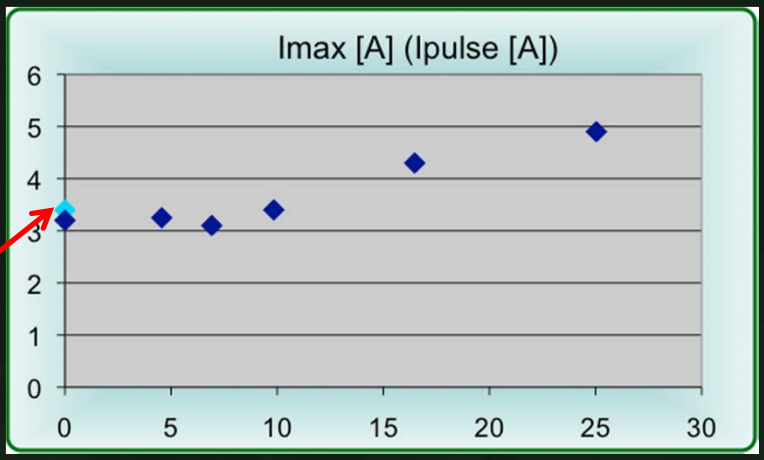
This shows R and V across contact in a succession of tests conducted after applying pulse current as specified

I max changes after I pulse

Au (pointed tips)

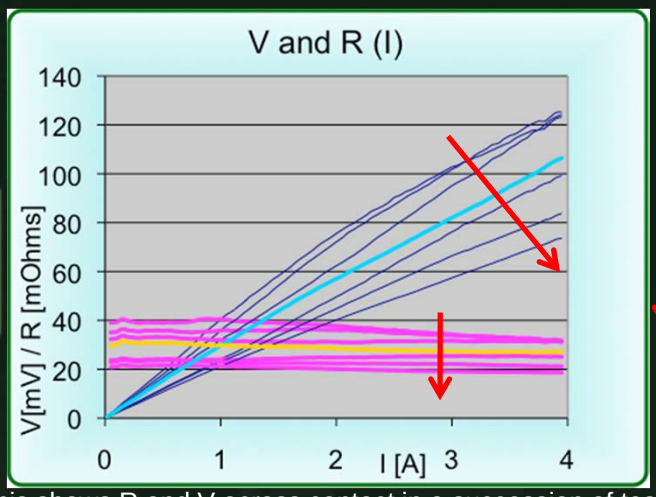
10% duty cycle

After dis/re-assembly



This shows I_{max} for 20C Trise after applying pulse current and a last data point after dis/reassembly

DC and pulse test



Matte Sn (pointed tips)

10% duty cycle

[A]
4.6
6.9
9.8
16.5
25.0

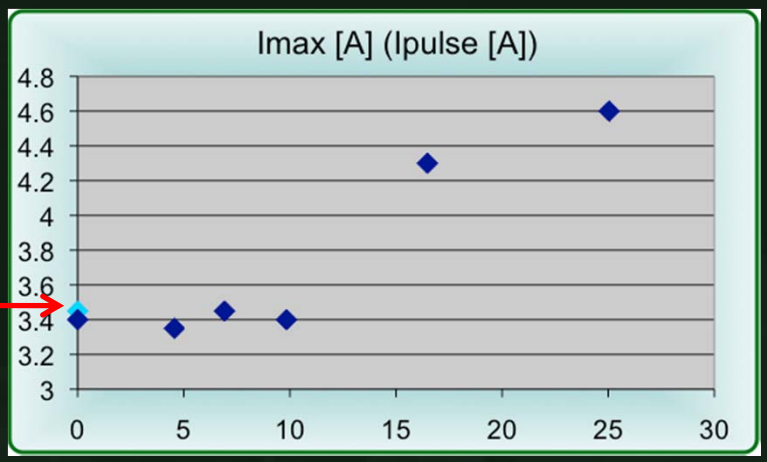
This shows R and V across contact in a succession of tests conducted after applying pulse current as specified

I max changes after I pulse

Matte Sn (pointed tips)

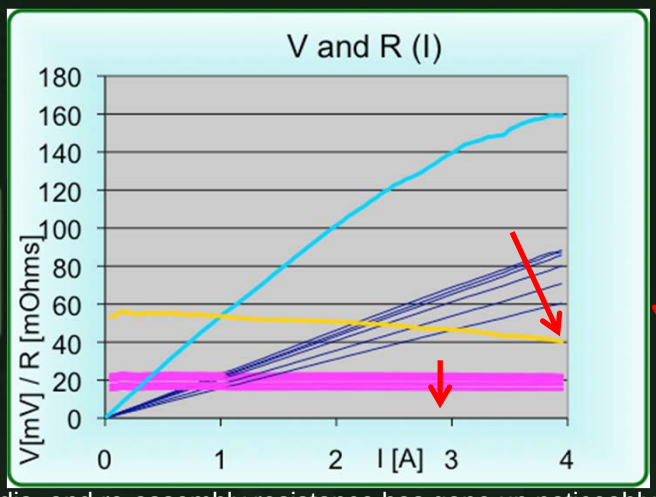
10% duty cycle

After dis/re-assembly



This shows I_{max} for 20C Trise after applying pulse current

DC and pulse test



Matte Sn (1 large area tip)

10% duty cycle

[A]
4.6
6.9
9.8
16.5
25.0

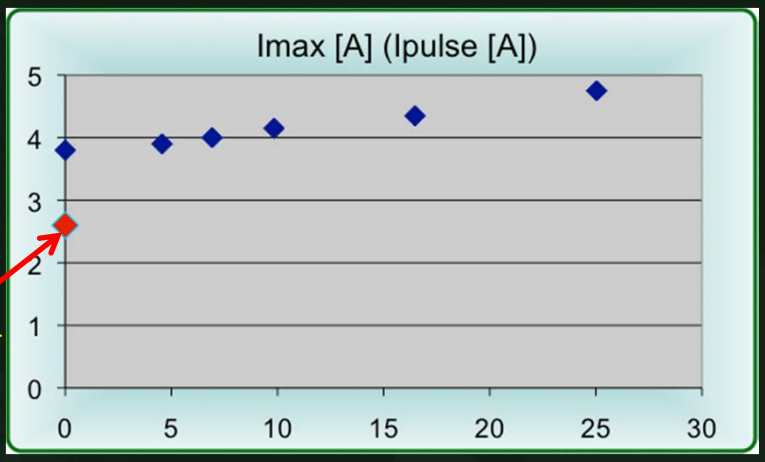
After dis- and re-assembly resistance has gone up noticeably even when touching on Au (orange curve)

I max changes after I pulse

Matte Sn (1 large area tip)

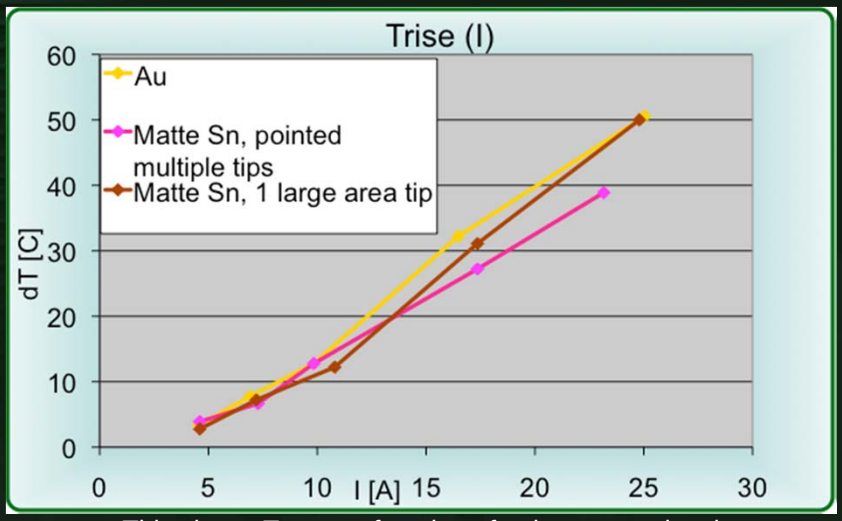
10% duty cycle

After dis/re-assembly



This shows I_{max} for 20C Trise after applying pulse current and a last data point after dis/reassembly

Pulse test

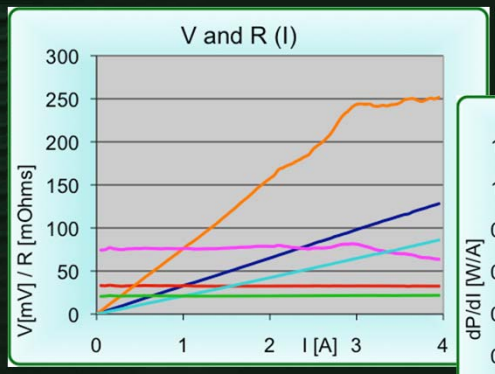


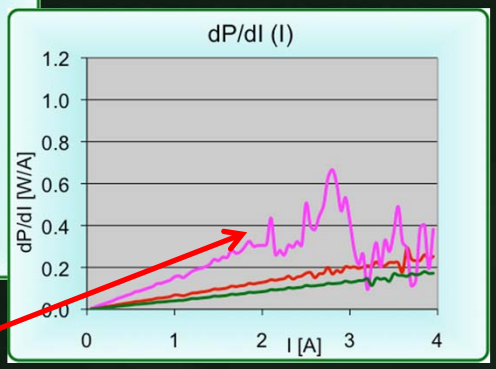
This shows T_{rise} as a function of pulse current level

Pulse test

This shows T_{rise} as a function of pulse current duty cycle

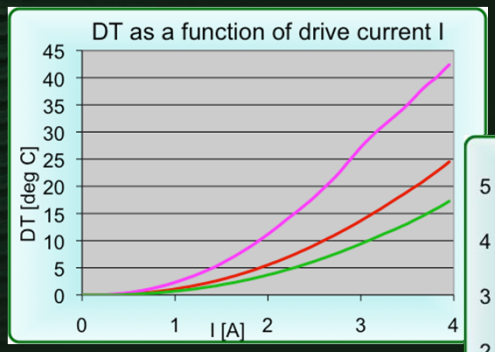
Performance after mechanical actuation

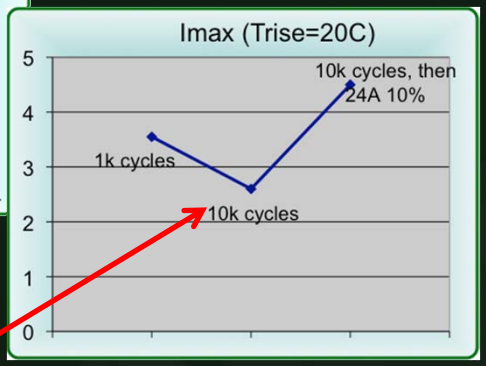




Significant noise development is evident after 10k cycles but disappeared after high pulse current was applied

Performance after mechanical actuation





Significant reduction in Imax is evident after 10k cycles but disappeared after high pulse current was applied

Conclusion

- Pulse test requires accurate knowledge of system time constants
  - Source
  - Load
  - Thermal time constants of specimen
  - Instrumentation
- Assessment of maximum current capability is not straightforward
  - Measurement point for highest temperature rise may not be accessible
  - A force based criterion may be more descriptive measure

Key Parameters in Thermal Simulations

Joseph Ortega, Larry Furman

Plastronics Sockets & Connectors

2012 BiTS Workshop
March 4 - 7, 2012

Outline

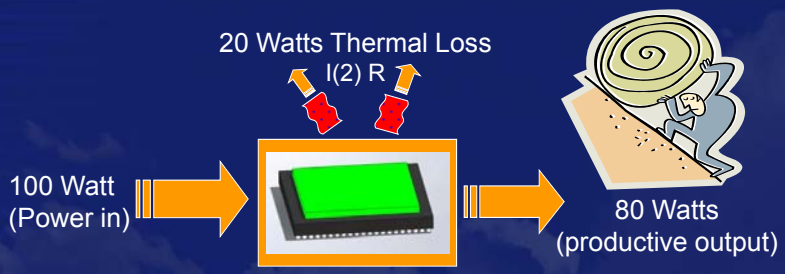
- Device Power Dissipation
- DUT Heat Variance is Increasing
- BIB Active Control Parameters Challenge
- CFD Conjunctive Heat Transfer Simulation
- Modeling The System
- Establishing Target Guidelines
- Tuning Parameters / Heat Sink Size
- Summary / Conclusion

Device Power Dissipation

Some of the power consumed by IC devices gets dissipated as heat loss. This energy loss is equal to the resistance of a circuit times the square of current flowing thru it.

$P = I^2R$.

Industry rule of thumb is to budget 15-20% of IC power draw to thermo-electric heat loss.

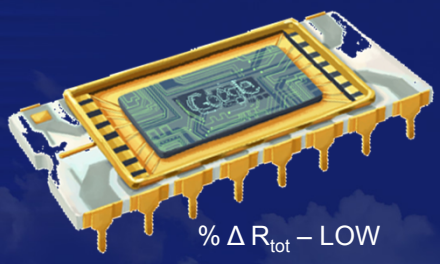


3/2012 Key Parameters in Thermal Simulations 3

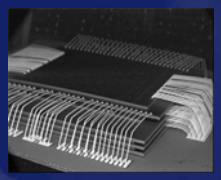
Power Dissipation Variances are Increasing

As circuit density and frequencies get higher, and voltages drop, process variations impacting resistance could have a bigger influence.

* (I.e., a 30 m-ohm resistance change in a 500 m-Ω circuit is only a 6% change, but it's a 30% variation for a 100 m-Ω circuit.) This % change also correlates to heat loss variability.



$\% \Delta R_{tot}$ – LOW



$\% \Delta R_{tot}$ – HIGH

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Power Dissipation Variances are Increasing (cont'd)

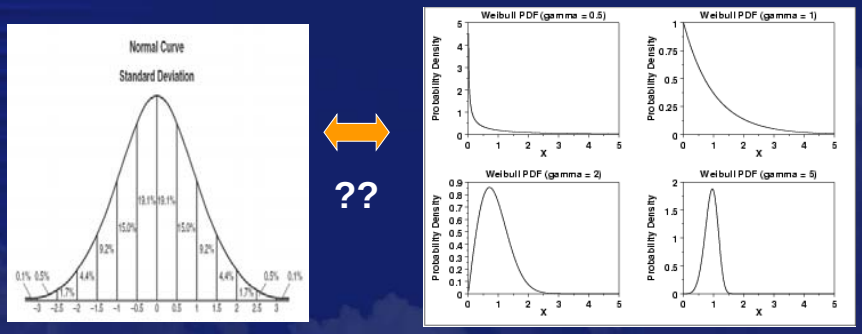
• At Higher frequencies -> current travels increasingly near conductor surface ("skin effect"), contributing to increased to circuit resistance.

• Other internal die effects contributing to increased heat loss variability, (i.e., leakage currents, gate switching) and also tend to have a cumulative effect In heat loss variance(1).

(1) ref. Freescale Semi BiTS 2008 Session 4, paper #2

+/- 50% Variance In Same Lot?

- Really ??
- Need Higher Precision Inputs / Verification
- What is the sample distribution, std. deviation, etc. ?
- Can we get lot sample measurement data and stats ?



What About Sample Size & Confidence Values?

* WHAT ABOUT SAMPLE SIZE?

What if we sampled 4 parts and measured 30W, 40W, 50W, and 65W of heat dissipation, what is the 95% confidence interval for the mean of the population?

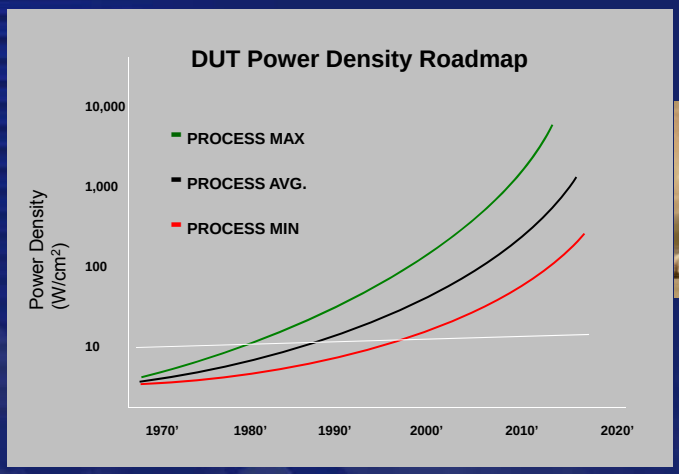
Ans: 46.25W +/- 23.75 W = [22.5 W – 70W]*

Conclusion: With a limited data set which also has a large standard deviation, we can't really predict much about a population, so Burn In Test Engineer is forced to evaluate "worse case" extremes.

* Normal Distribution, theorem 9.3.2 Introduction Eng. Stat., Wiley, 2nd Ed. Ref. Appendix

3/2012 Key Parameters in Thermal Simulations 7

Power Density Trend *and* Higher Dissipation Variances = Burn-in Test Engineer Migraine



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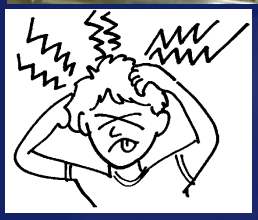
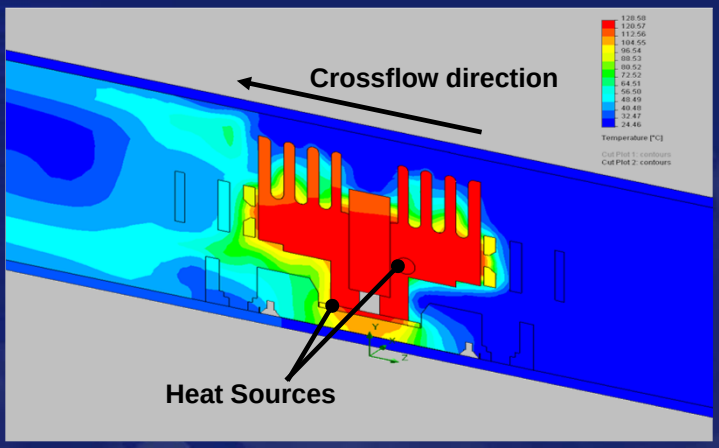
Determining Optimum Active BIB Control Parameters



CAN CFD SIMS HELP ME GET NEAR THE BALLPARK?

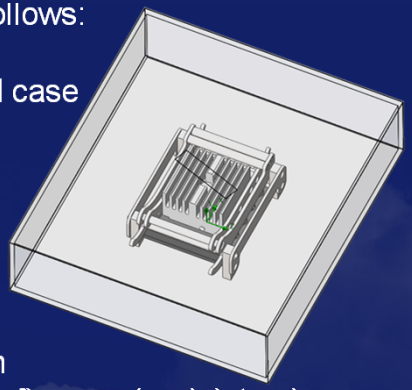
Conjugate Heat Transfer CFD

The combination of convection and conduction heat exchange, is known as **conjugate heat transfer.** Conjugate simulations are referred to coupled fluid-solid temperature calculations.



Model The System

Fortunately, today's software technology assists greatly in modeling most of the thermal challenges of burn-in. A good checklist for modeling is as follows:



- Thermal resistance of the die and case (or package)
- Wattage range of the device
- Die size
- Size of the case or heat spreader
- Ambient oven temperature
- Inlet air temperature
- Box or envelop size of the system
- Air velocity and direction or cross-flow, and or inlet valve size if directly over the heat sink

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Model The System (cont'd)

With this information, a proper heat sink can be constructed, as well as determining if the heater cartridges imbedded in the heat sink will properly bring the device to temperature quickly enough within the recommend working duty cycle of the cartridge. If there is a controller on the fan speed or valve, a calculation can also be performed to ensure it's not overworked as well.

An added benefit to the model also includes a finite element analysis (FEA) on the heat sink force to ensure there is not an excessive load on the die

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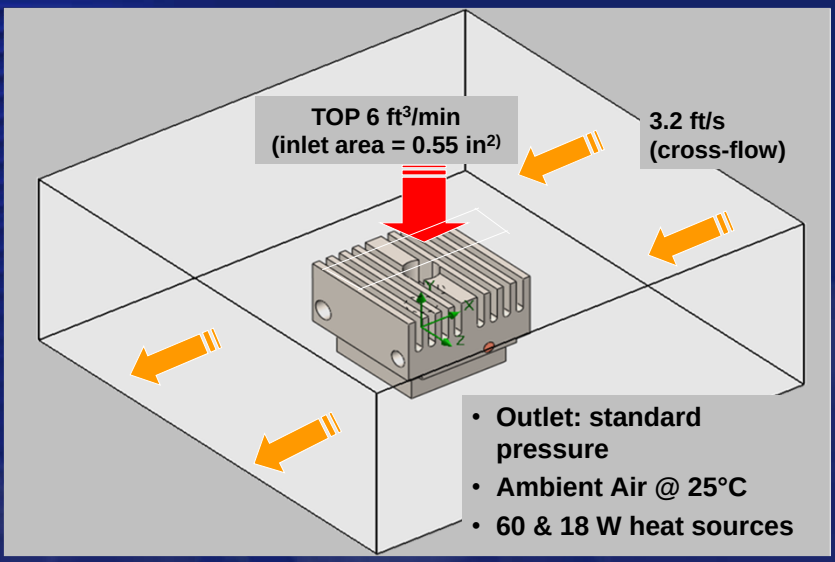
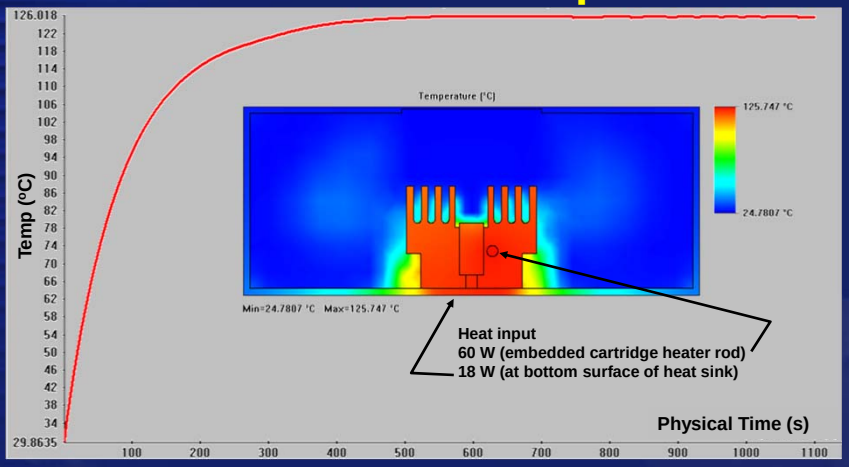
Model Preparation

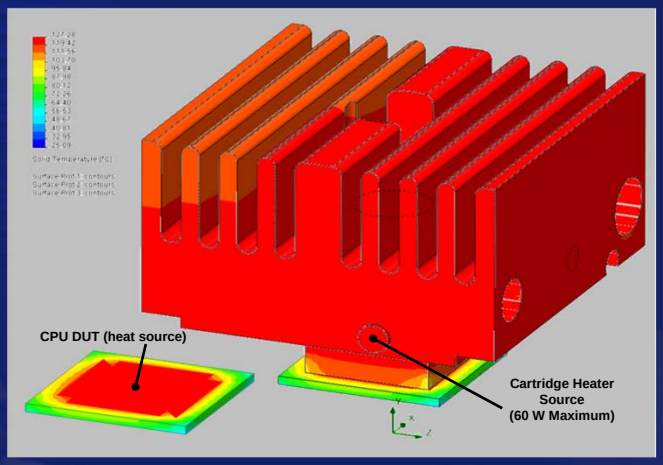


Simulation Output



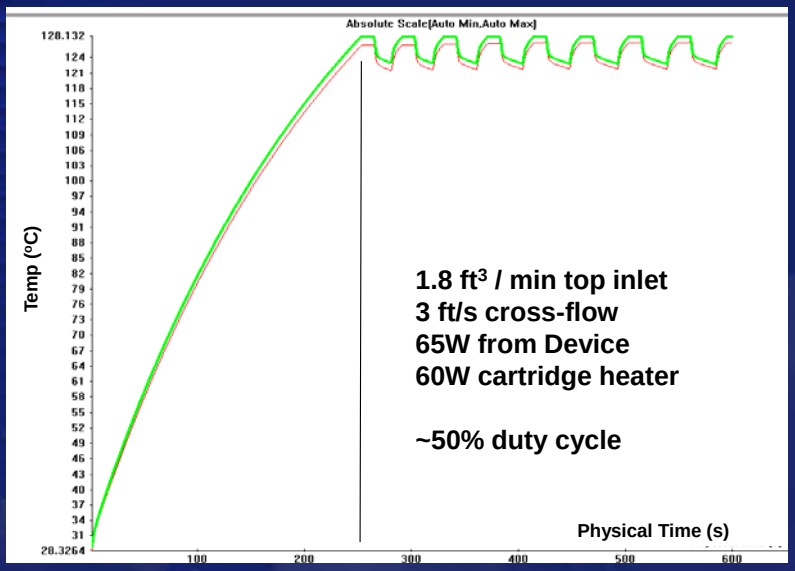
The heat sink must also be optimized to be the "correct" efficiency – too efficient and the lower wattage parts will not heat to temperature, and not efficient enough and the package will go into thermal runaway

Simulation Output

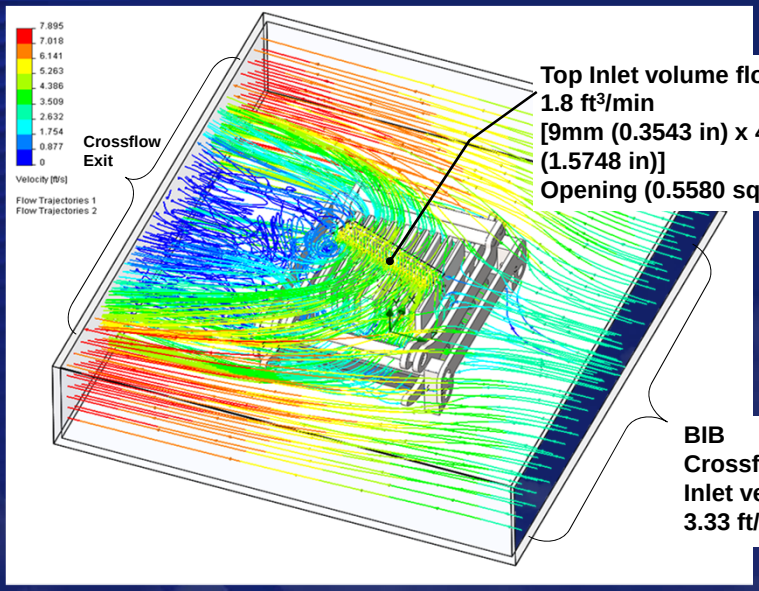


DUT & Heat Sink - Temp Distribution

Simulation Output

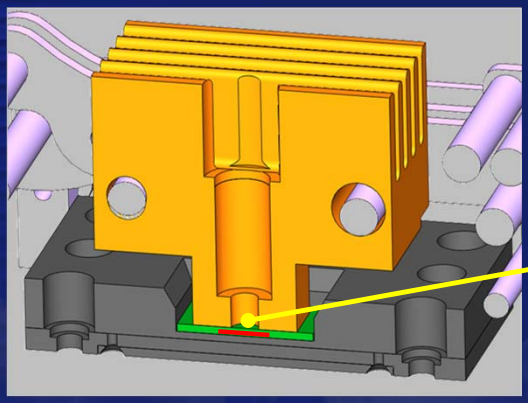


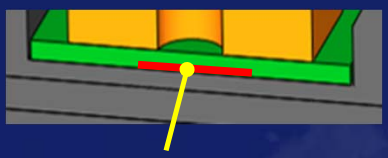
Simulation Output



Input Parameter Consideration 1

- DIE VS. CASE TEMP - Where is control location, internal IC circuit or external couple? This location is the feedback loop to control heater cartridge activation in the simulation model. Depending on location, setpoint value changes.





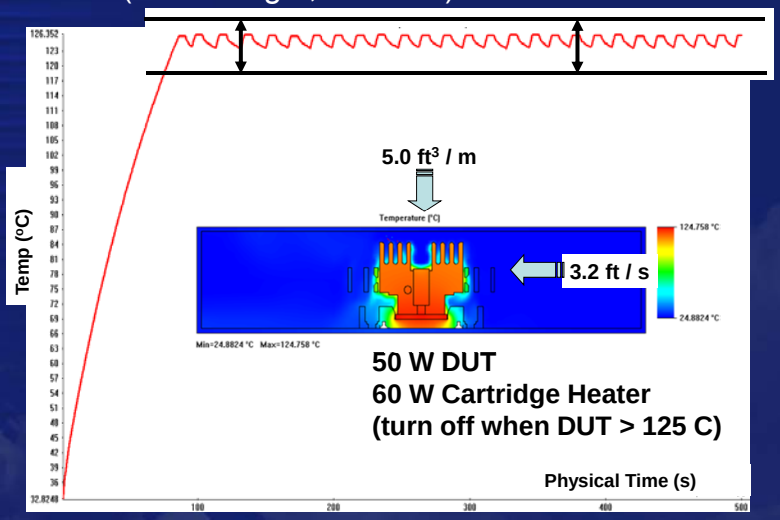
Die (internal circuit sensor)

Case surface thermo-couple sensor location

ΔT = Between die vs. case ?

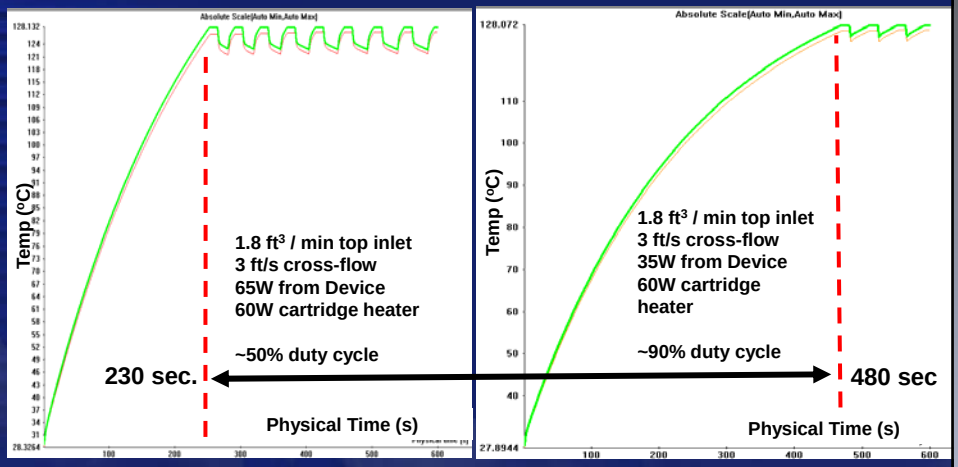
Input Parameter Consideration 2

- What is acceptable setpoint target Temp Tolerance band? (125 C target, but +/- ?)



Input Parameter Consideration 3

- What is considered optimal time to setpoint TEST TEMP ? (i.e., with 125° C target, what is acceptable +/- time window?)



Input Parameter Consideration 4

- Cartridge Heater Output vs. Rating Consideration
- Input voltage drives cartridge heat power output (Voltage supply can be on lower end of rated +/- 15% nominal value).
- Since output Power relative to input voltage is $P=V^2/R$ a 15% lower voltage results in >25% less Power output from the cartridge heater.

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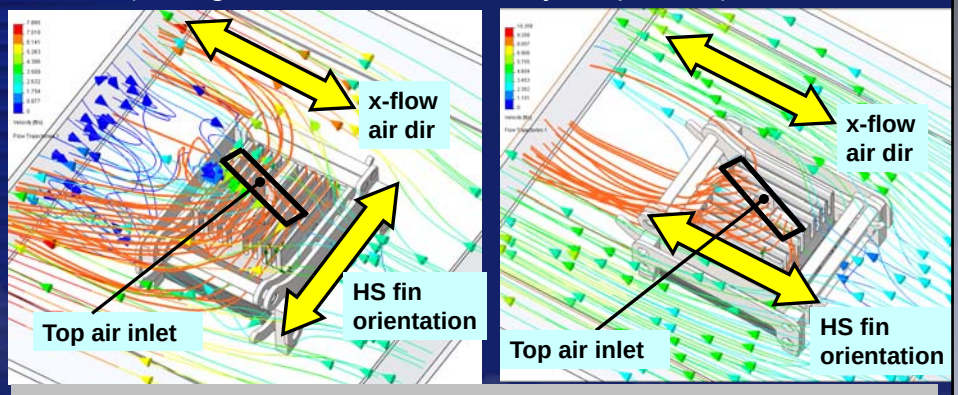
Input Parameter Consideration 5

- Top air Inlet Orientation vs. Heat Sink Fins length-wise arrangement vs. cross-flow direction
- Orientation impacts Heat Sink efficiency
- (orthogonal -> better efficiency vs. parallel)



Heat Sink Fins orthogonal to x-flow and top air inlet = more cooling efficiency

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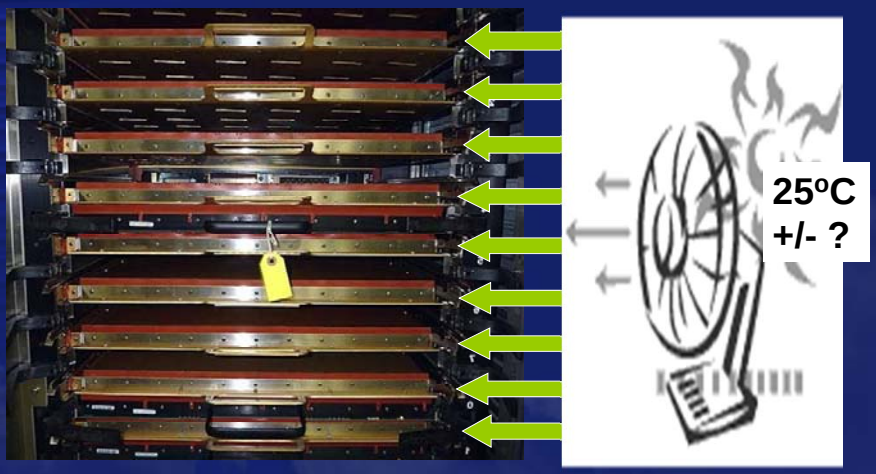
Input Parameter Consideration 6

• Test OVEN AIR TEMP "AMBIENT" (what's the process variation, how well is it controlled?)



Summary / Conclusions

• Industry trending towards higher variances with DUT heat dissipation

• Increases in Circuit Density and resulting power draw in combination with larger variances in heat dissipation result in greater (max., min) test conditions.

• A "one size fits all" solution with nominal heat sink & active Burn-in oven control parameters may not always be adequate, tuning of control parameters and/or heat sink could be necessary.

• Pro-active CFD simulations of set up parameters and heat sink adjustments can help Test Engineers better prepare for various "game time" situations (i.e., plan "a", "b", etc.)

Summary / Conclusions (cont'd)

With growing thermal concerns, using modeling tools can assist in solving issues. Diligence is needed in the selection of capital equipment on the front end in to make sure it can handle the range of devices that need to be tested, but once selected, additional hardware that includes boards, heat sink and sockets can be accurately modeled to achieve the goal – burn-in at the exact temperature needed.

Better inputs -> More accurate CFD simulations -> Less time spent "tuning" BIB parameters = Faster product time to market!

Appendix

* Normal Distribution, theorem 9.3.2 Introduction Eng. Stat., Wiley, 2nd Ed.

If $\bar{x}$ and s^2 are the mean and variance of a sample of size n from a normal distribution $N(\mu, \sigma^2)$, where μ and σ^2 are unknown, then:

$$\bar{x} \pm [(t_{n-1;\, \alpha/2}) * (s) \div (\text{sq. root } (n))]$$

Is a $100(1 - \alpha)\%$ confidence interval for μ.

Ref. *t* = Student *t* distribution (approaches normal distribution ~z when (n -1) is large

For sample parts measuring 30, 40, 50, 65 Watts. Then:
$\bar{x}$ = **46.25**, *n =4, and s* = 14.9 ; therefore (*s*) ÷ (sq. root (*n*))] = 14.9 / 2 = **7.45**
For confidence interval: 1 – α = 0.95, then α = .05 and α ÷ 2 = 0.025 and n – 1 = 3, we then find from t distribution reference table for $t_{3;\, 0.025}$ = **3.182**

So confidence interval = **46.25** ± (**3.182**) * (**7.45**) = 46.25 ± 23.7 = [22.5 – 70]