BiTS™ Burn-in & Test Socket Workshop 2011

Tutorial

ARCHIVE 2011

SIGNAL AND POWER INTEGRITY IN THE TEST INTERFACE

by

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ABSTRACT

The instructors for the Tutorial are Jason Mroczkowski & Ryan Satrom of Multitest Electronic Systems, Inc. Both are well known in the socket industry for their high frequency modeling, analysis and design expertise. In this tutorial they'll deliver a comprehensive Tutorial focused specifically on ATE hardware.

This tutorial will expose the audience to the real world implications of designing test hardware to meet various signal integrity and power integrity needs. The tutorial will start by defining the terminology for analog and digital products. The tutorial will move on to present a range of past problematic designs showing real examples of signal and power integrity failures. Armed with a common terminology and previous experience, the tutorial then moves into its main section of providing the attendees with methods to design hardware to meet both the power and signal integrity specifications. Topics ranging from S-parameters, impedance targets, crosstalk, capacitor and inductor fundamentals, measurement equipment, modeling equipment and hardware selection will all be presented during the tutorial.

Signal and Power Integrity in the Test Interface

Jason Mroczkowski, Ryan Satrom
Multitest

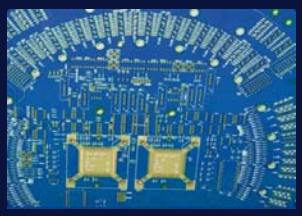
2011 BiTS Workshop
March 6 - 9, 2011

About Multitest
economy through technology

- Multitest is a global one-stop supplier for leading test equipment at best cost of test.
- The Dover group and Multitest's financial strength assure a long-term partnership.
- Decades of experience result in comprehensive understanding of the industry.

Innovative Solutions

- test handlers for
  - small packages down to 2x2 mm
  - high parallel test
  - MEMS test
  - tri-temp test
- contactors for
  - RF to 40GHz
  - Kelvin testing incl.BGAs /WLCSP
  - for pitches down to 0.25 mm / wafer-level packages
- boards for
  - RF test applications
  - fine pitch IC test
  - burn-in test



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Semiconductor Industry

- Semiconductor market led by:
  - Consumer products
    - iPad, smartphones, netbooks, convenience products
  - Green Energy
    - communications, appliances, transportation, industrial
- "More than Moore"
  - SOP, SIP, 3D packaging
  - Parallelism has allowed faster processing than Moore's Law
- 8% annual frequency growth rate
- 4% annual supply voltage reduction rate

Data courtesy of New Venture Research 2010 and ITRS 2010

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Semiconductor Device Trends

- Microprocessors (MPU)
  - Highest revenue semiconductor device
  - Flip-Chip BGA moving toward FBGA
  - Most technological advancements
  - Up to 3.5GHz
  - High Power (~150A)
- Memory
  - Second highest revenue device
  - DDR3 up to 2Ghz
  - DDR4, XDR up to 4GHz
  - FBGA's shifting toward WLP
- Logic
  - FPGA, ASIC, PLDs (largest dies)
  - Flip-Chip BGA (up to ~2000)
  - 25-32 Gbps next Gen
  - Analog
  - Wireless, 4G, 802n, GSM, etc.
  - Smaller packaging QFN, WLP
  - High electrical performance
  - Consumer up to 6GHz
  - Satellite ~30GHz
  - Automotive up to 77GHz

Data courtesy of New Venture Research 2010 and ITRS 2010

Semiconductor Packaging Trends

- 0.4mm pitch FBGA's to increase to 20% BGA market by 2015
- Leaded Devices falling from 50% to %40 market by 2015
- FBGA has largest increase and SO largest decrease through 2015
- Drive toward smaller more integrated devices with similar to or better electrical performance creates both signal integrity and power delivery concerns

Data courtesy of New Venture Research 2010 and ITRS 2010

Agenda

- Signal Integrity Concepts
- Signal Integrity in the Test Interface
- Power Integrity in the Test Interface

Signal Integrity Concepts

Signal Integrity Concepts Overview

- What is Signal Integrity?
- Inductance and Capacitance
- Insertion Loss and Return Loss
- S-Parameters
- Impedance
- TDR
- Differential Signals
- Analog-to-Digital Conversions
- Eye Diagrams
- Simulation Techniques

What is Signal Integrity?

My working definition:

Signal Integrity is the quality of an electrical signal when the wavelength approaches the size of the signal path

Inductance and Capacitance

- Inductance defines the amount of voltage induced when an AC current travels through a component

Time Domain

$$V = L\frac{di}{dt}$$

Frequency Domain

$$Z_L = 2\pi fL$$

- Capacitance is the ability to store charge between two conductors

Time Domain

$$i = C\frac{dv}{dt}$$

Frequency Domain

$$Z_C = \frac{1}{2\pi fC}$$

Insertion Loss and Return Loss

Insertion Loss

- Measures Signal Transmission
- Ratio: Transmitted/Input
- S-Parameters: S_{12}, S_{21}
- Specified at -1dB, -3dB

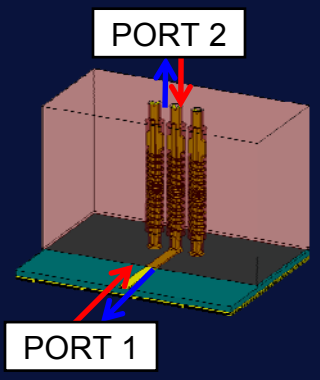
Return Loss

- Measures Signal Reflection
- Ratio: Reflected/Input
- S-Parameters: S_{11}, S_{22}
- Specified at -10dB, -20dB

S-Parameters

The incident signal:

- Transmits through structure (S_{12}, S_{21})
  - Insertion Loss
- Reflects back to source (S_{11}, S_{22})
  - Return Loss
  - Impedance
- Absorbs within structure
  - Conductor Loss, Dielectric Loss



S-Parameters models include:

- Information on transmission and reflection for all relevant frequencies
- All necessary information to describe performance

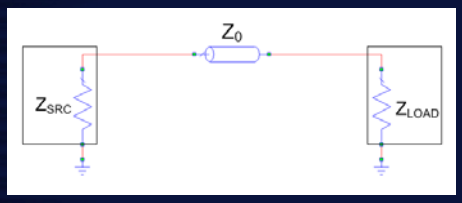
Impedance

- Impedance:
  - The relationship between the inductance and the capacitance of a signal path
  - Describes the amount of reflections seen throughout an interface
  - Matched impedance throughout the interface minimizes loss and reflections
  - Focus for signal integrity is instantaneous impedance
- Equation for instantaneous impedance:

$$Z = \sqrt{\frac{L}{C}}$$

Impedance

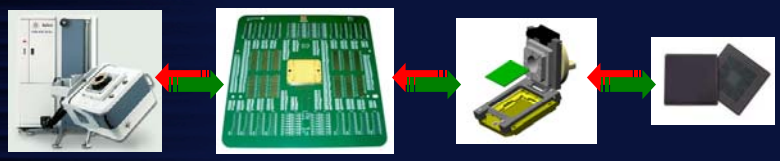
- Two cases: $Z_{SRC}=Z_{LOAD}$, $Z_{SRC}\neq Z_{LOAD}$
- For $Z_{SRC}=Z_{LOAD}$:
  - Interface designed to match impedance throughout interface
  - Most common impedance is 50Ω single-ended (100Ω differential)
- For $Z_{SRC}\neq Z_{LOAD}$:
  - Optimal performance requires interface tuning
  - Tuning optimizes performance within specific frequency band
  - Tuning is achieved by placing inductors and/or capacitors in path**

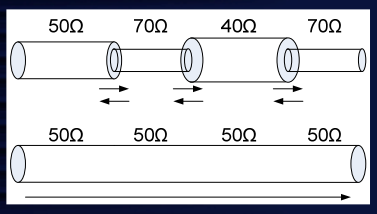


****See "Tuning a PCB/Contactor to Your Device", Ryan Satrom, BiTS 2009.**

Fluid Flow Analogy

- Impedance change similar to pipe diameter changing
- Optimal design occurs when pipe diameter/impedance remains constant throughout system



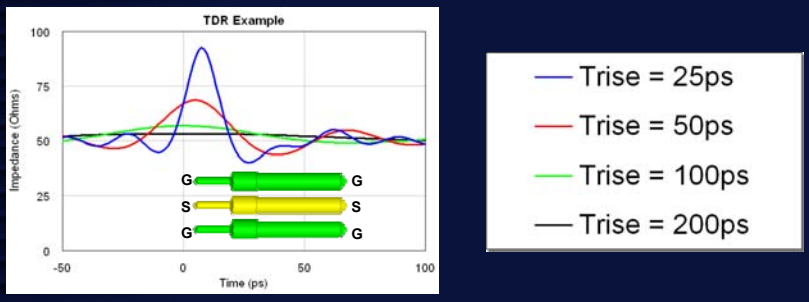


Non-Ideal

Ideal

Time Domain Reflectometry (TDR)

- A method for measuring the impedance through an interface
- Can be mathematically derived from S-Parameters
- Used to see inside the structure
- Magnitude of discontinuities depends on rise time of signal
  - Faster rise-time → Larger impact from discontinuity
  - Slower rise-time → Smaller impact from discontinuity



Differential Signaling

- Method for data transfer of two complementary signals

- Result is the voltage difference between signals:

$$V_{OUT(DIFF)} = V_{OUT1} - V_{OUT2}$$

- Simplified equation for differential impedance:

$$Z_{DIFF} = Z_{11} + Z_{22} - 2 \times Z_{12}$$

$$Z_{DIFF} = 2 \times Z_0 - 2 \times Z_{12}$$

Differential Signals

Advantages

- Reduces Simultaneous Switching Output (SSO) Noise
  - SSO is caused by multiple signals changing the same direction simultaneously
  - Complementary signal changes cancel out, reducing total noise
- Noise Immunity
  - Noise reaching both lines is cancelled out
  - Noise seen on one line has half the impact:
  - Example: 0.1V noise on 1V line
    - Single-Ended: V_{NOISE} = 0.1V / 1V = 10%
    - Differential: V_{NOISE} = 2.1V / 2V = 5%

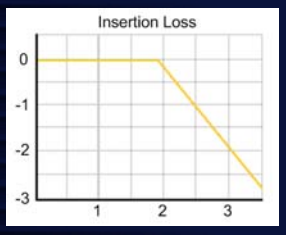
Disadvantages

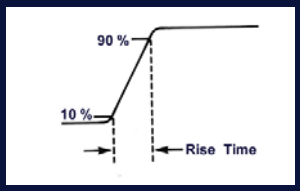
- Requires twice the number of signal lines
- Can add EMI if not properly balanced

Analog-to-Digital Conversions

Conversions are good as 1st-order assumptions

1) Bandwidth-to-Rise Time
   - 10%-90%: Bandwidth(-3dB) ≈ $0.35/TR_{10\text{-}90}$
   - 20%-80%: Bandwidth(-3dB) ≈ $0.227/TR_{20\text{-}80}$
2) Data Rate-to-Rise Time
   - Rise Time ≈ Period/7 ≈ 1/(7 x Frequency)**





**Use fundamental frequency, which equals Data Rate / 2

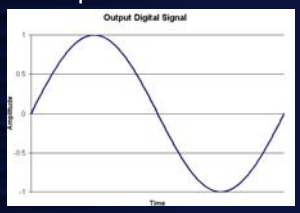
Analog-to-Digital Conversions

3) Bandwidth-to-Data Rate

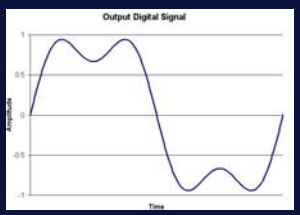
- Slower data rates require higher harmonic content
- Higher data rates unable to use higher harmonic content
  - a) 0 – 1 Gb/s:
    Bandwidth = 5 x Data Rate = 2.5 * Frequency
  - b) 1 – 5 Gb/s:
    Bandwidth = 3 x Data Rate = 1.5 * Frequency
  - c) 5+ Gb/s:
    Bandwidth = 1 x Data Rate = 0.5 * Frequency
- High data rate designs often assume only 1st harmonic
- Trade-offs made in other areas of design

Harmonics of Digital Signals

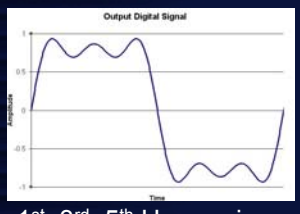
- Signal output of square wave input based on an interface that passes specific harmonics



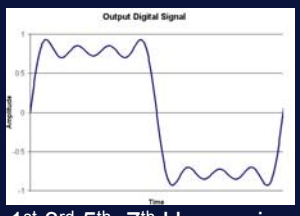
1st-Harmonic Only



1st, 3rd Harmonics



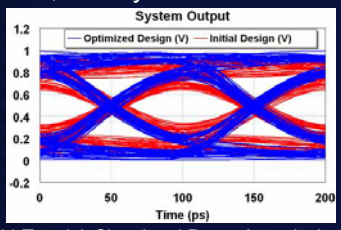
1st, 3rd, 5th Harmonics



1st,3rd,5th ,7th Harmonics

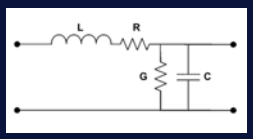
Eye Diagrams

- Eye Diagrams are graphical displays of data that overlay repeating periods of the same data
- Used to analyze digital signals
- Depicts signal fidelity in time domain
- Become increasingly useful with increased speeds
- Several aspects used to describe performance
  - Eye Height, Eye Width, Jitter, Overshoot, Rise-Time, Fall-Time, Crossing-Time, Intersymbol Interference (ISI)



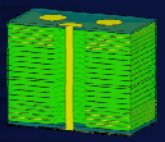
Simulation Techniques

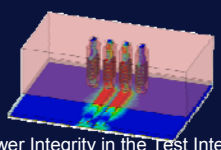
1) Lumped Element Models (SPICE)
   - Appropriate below ~1 GHz



2) Distributed Element Models
   - Highly accurate; only valid for constant cross-section

3) Full 3D Electromagnetic Simulation
- Required for complex structures such as vias, contactors
- Most resource intensive, but also most accurate

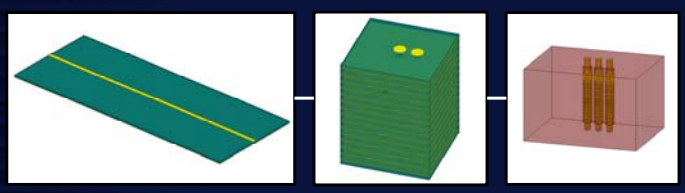




Signal Integrity in the Test Interface

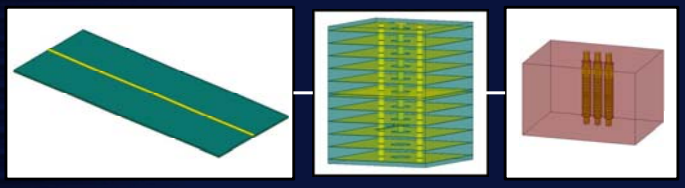
SI in the Test Interface Agenda

- PCB Traces
- Vias
- Contactor
- System



Signal Integrity in the Test Interface

PCB Traces



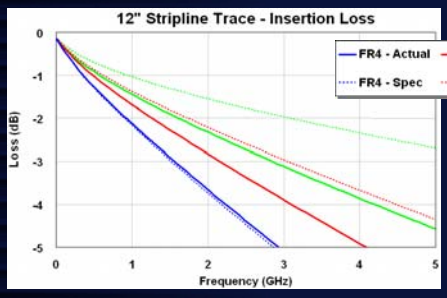
General PCB Guidelines

1) In general, most loss in test interface is due to the PCB
   - PCB trace length ≈ 4”-16”
   - Contactor probe length ≈ 0.05”-0.3”
   - PCB trace length >> contactor probe length
2) PCB loss mainly due to length, not reflections
   - Impedance typically controlled within ±10%
   - Reflections are minimized

	PCB	Contactor
Length	Long	Short
Impedance Control	Easy	Difficult

General PCB Guidelines

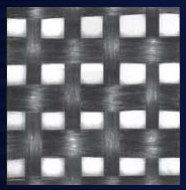
3) Expect more loss in PCB than specifications suggests
   - Expect up to 50% more loss in actual PCB
   - Tan δ values
     - Typical specifications: 0.002-0.02
     - More representative: 0.008-0.025



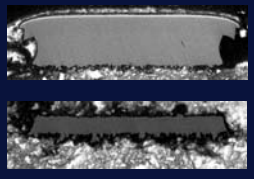
	Loss @ 2 GHz	
	Spec	Actual
FR4	-3.7 dB	-3.7 dB
Mid-Level Mat'l	-2.2 dB	-2.8 dB
Exotic Mat'l	-1.5 dB	-2.3 dB

General PCB Guidelines

- Reasons for discrepancy in performance
  - Vendor specifications do not reflect PCB environment
  - Some PCB materials require harder copper for adhesion which increases roughness and loss
  - Etch/material tolerances
  - Dielectric/weave variation



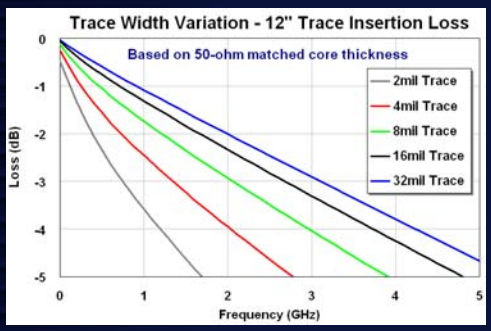
PCB Weave



Copper Roughness

General PCB Guidelines

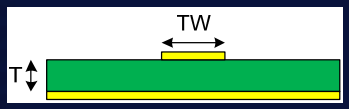
4) Doubling trace width improves performance about 30%



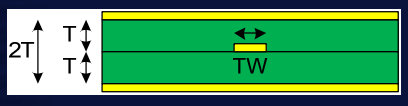
	Loss @ 2 GHz
2mil Wide	-5.6 dB
4mil Wide	-4.0 dB
8mil Wide	-2.9 dB
16mil Wide	-2.3 dB
32mil Wide	-2.0 dB

General PCB Guidelines

5) Trace width for 50Ω microstrip is roughly 2X core thickness
- Example: Core thickness = 8mil → Trace width = 16mil



6) Trace width for 50Ω stripline is roughly 1X core thickness
- Example: Core thickness = 8mil → Trace width = 8mil

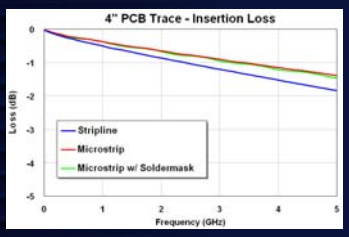


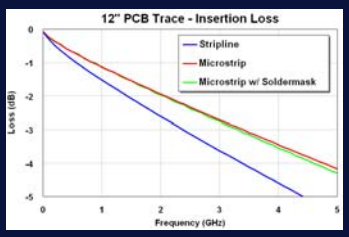
***See Appendix 1 to see how different variables impact impedance**

General PCB Guidelines

7) Microstrip performance about 30% better than stripline
8) Soldermask has a negligible impact on signal integrity

	Loss @ 2 GHz	
	4"	12"
Stripline	-0.9 dB	-2.6 dB
Microstrip	-0.7 dB	-2.0 dB
Microstrip w/ Soldermask	-0.7 dB	-2.0 dB





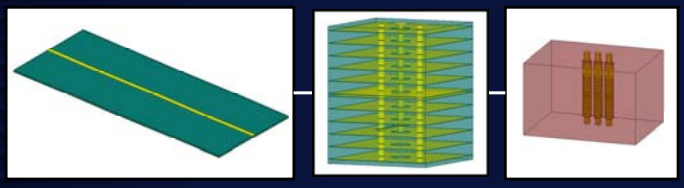
***Assumes core thickness is modified to maintain 50Ω impedance**

Typical PCB Insertion Loss Values

	(-1dB) **Stripline**	(-1dB) **Microstrip**
• 2" Trace	3-7 GHz	4-10 GHz
• 4" Trace	1-3 GHz	1.5-4.5 GHz
• 8" Trace	0.4-1.2 GHz	0.6-1.8 GHz
• 16" Trace	0.1-0.4 GHz	0.2-0.7 GHz

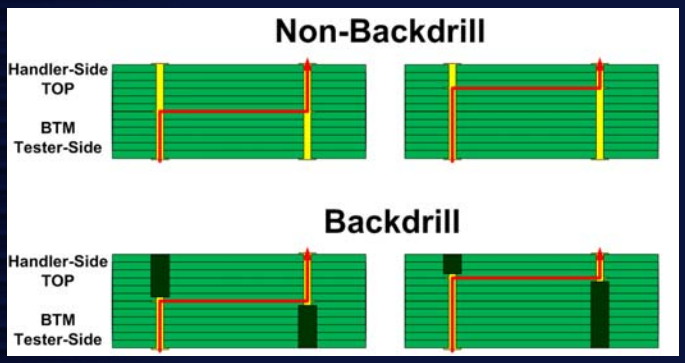
Signal Integrity in the Test Interface

Vias



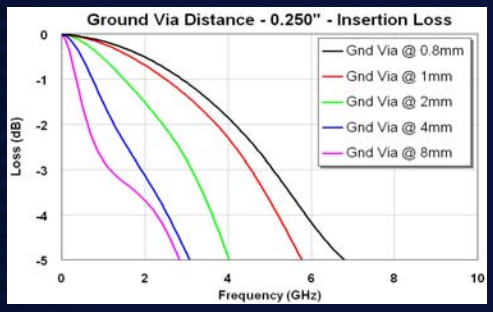
General Via Design Guidelines

1) Place critical signals close to center of the PCB stackup
   - Two medium-sized vias/stubs are better than one small and one large via/stub



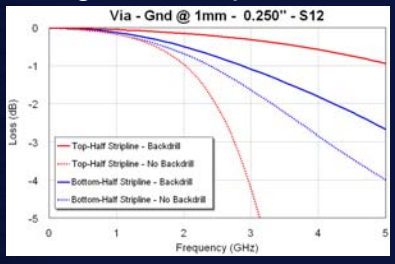
General Via Design Guidelines

2) Place ground via within 1mm of every signal via
   - Example:
     - 0.250” PCB
     - Signal on bottom stripline layer



General Via Design Guidelines

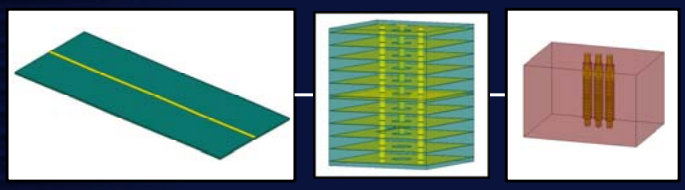
3) Backdrill signals above 1GHz
   - Signal layer location, via stub are not issues < 1 GHz**
   - Example:
     - 0.250” PCB
     - Compares signals on top-half, bottom-half of PCB



****Assumes ground via within 1mm**

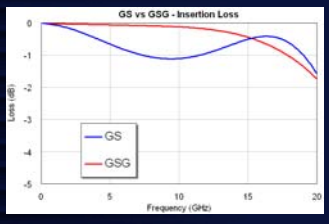
Signal Integrity in the Test Interface

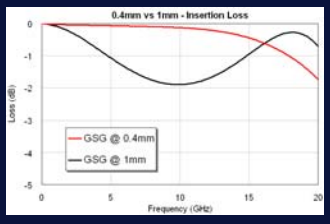
Contactors



General Contactor Guidelines

1) Most contactors are adequate for sub-1GHz signals
2) Performance for differential signals is typically much better than performance of single-ended signals
   - $Z_{CONTACTOR}$ (Single-Ended) >> 50Ω
   - $Z_{CONTACTOR}$ (Differential) ≈ 100Ω
   - Z_{DIFF} typically a much closer match than Z_{SE}
3) Ground proximity critical for determining performance





Also see Appendix 3 to see how different variables impact contactor impedance

General Contactor Guidelines

4) Performance is not *Black Magic*
   - Two probes with similar length/diameter will have similar performance
   - Beware of specifications that don't seem to make sense
5) Shorter probes are better because they minimize the mismatch
   - If impedance is matched, length is only a very minor issue
6) Tuning applications are the exception to the rule
   - Shorter, higher bandwidth probe not always best solution
   - Requires component tuning on PCB to optimize performance**

****Tuning is required when $Z_{SOURCE} \neq Z_{TERM}$; See "Tuning a PCB/Contactor to Your Device", Ryan Satrom, BiTS 2009.**

Typical Contactor Insertion Loss (-1dB)

SINGLE-ENDED (Z_0=50Ω)

- **G-S-G (GND SIG GND)**** — **20-40 GHz**
- **G-S (GND SIG)** — **3-12 GHz**
- **G-S (DIAG) (FLOAT SIG / GND FLOAT)** — **2-7 GHz**
- **G-X-S (GND FLOAT SIG)** — **1.5-5 GHz**
- **G-X-X-S (GND FLOAT FLOAT SIG)** — **1-3 GHz**

DIFFERENTIAL (Z_0=100Ω)

- **S-S (SIG SIG)** — **15-20 GHz**
- **G-S-S (GND SIG SIG)** — **15-20 GHz**
- **G-S-S-G (GND SIG SIG GND)** — **15-20 GHz**

****GSG is standard datasheet specification, also see Appendix 2 for Return Loss Comparison**

Typical Contactor Impedance (Ω)

SINGLE-ENDED (Z_0=50Ω)

• G-S-G (GND SIG GND)**	55-65 Ω
• G-S (GND SIG)	70-90 Ω
• G-S (DIAG) (FLOAT SIG / GND FLOAT)	75-100 Ω
• G-X-S (GND FLOAT SIG)	85-170 Ω
• G-X-X-S (GND FLOAT FLOAT SIG)	110-220 Ω

DIFFERENTIAL (Z_0=100Ω)

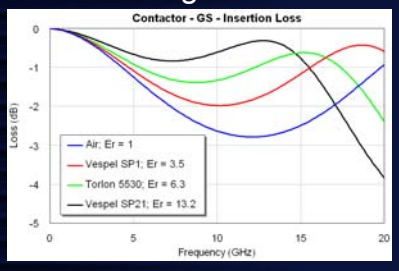
• S-S (SIG SIG)	100-110 Ω
• G-S-S (GND SIG SIG)	95-105 Ω
• G-S-S-G (GND SIG SIG GND)	85-100 Ω

Contactor Designs – Changing Dielectric

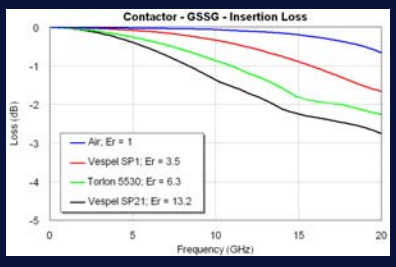
- The contactor body can be changed to modify the dielectric constant of material

Performance Comparison

Single-Ended



Differential



Contactor Designs – Changing Dielectric

Is it worth modifying dielectric for RF performance?

- ***Sometimes*** for High-speed single-ended signals
  - Depends on pitch, ground configuration, frequency
  - Difference may be seen above ~2 GHz
  - Choose on case-by-case basis – Performance will just as often degrade as it will improve
- ***Rarely*** for high-speed differential signals
  - Differential signals typically have good impedance match through contactor

Contactor Designs – Coaxial

Strengths

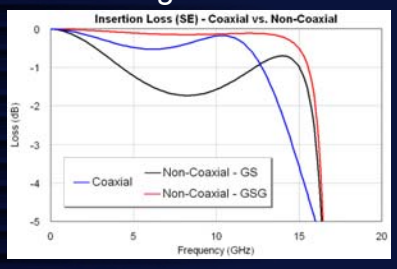
- Optimized impedance
- Improve bandwidth
- Improve crosstalk

Weaknesses

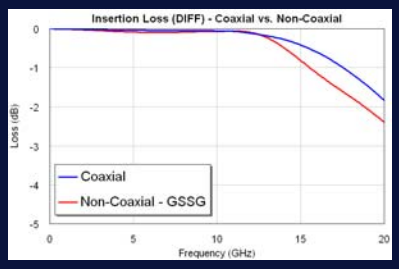
- Mechanical challenges
- Low force probes
- Expense

Performance Comparison

Single-Ended



Differential



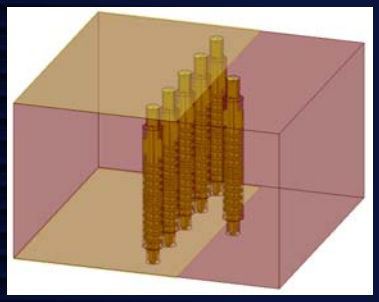
Contactor Designs – Coaxial

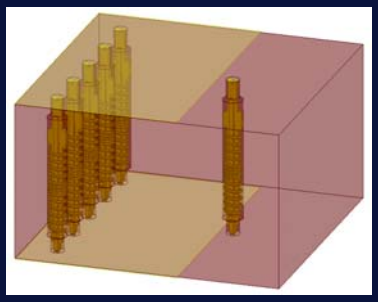
Is it worth using a coaxial contactor?

- ***Sometimes*** for High-speed single-ended signals
  - Depends on pitch, ground configuration, frequency
  - Potential benefit may be seen above ~2 GHz
- ***Never*** for High-speed differential signals
  - Differential signals typically have good impedance match through contactor without coax
  - Differential signals benefit from coupling between complementary signals – Coax removes this benefit

Contactor Designs – QFN Grounding

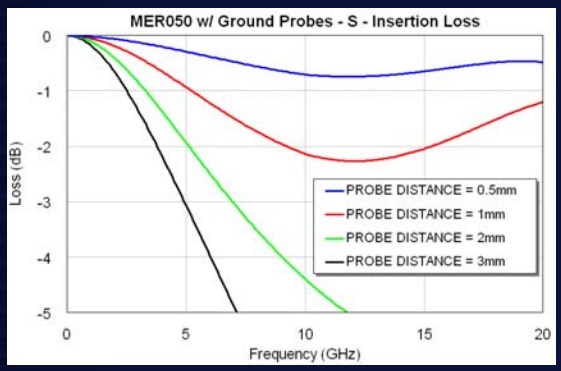
- Where should ground probes be placed?
- Simulation compares performance as ground probes move further away from signal probe





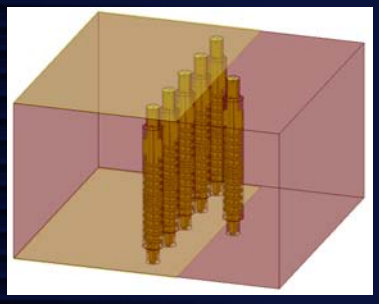
Contactor Designs – QFN Grounding

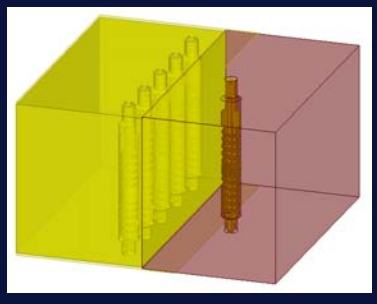
- Results show ground probes need to be place as close to periphery as possible



Contactor Designs – QFN Grounding

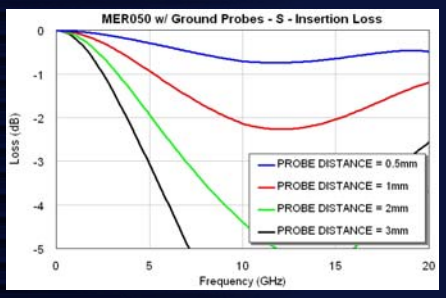
- Are ground slugs better than ground probes?
- Simulation compares performance with and without ground slug

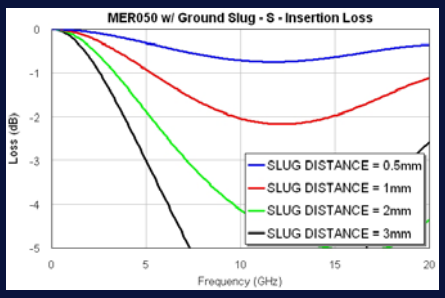




Contactor Designs – QFN Grounding

- Performance between slug and probes with same spacing is very similar

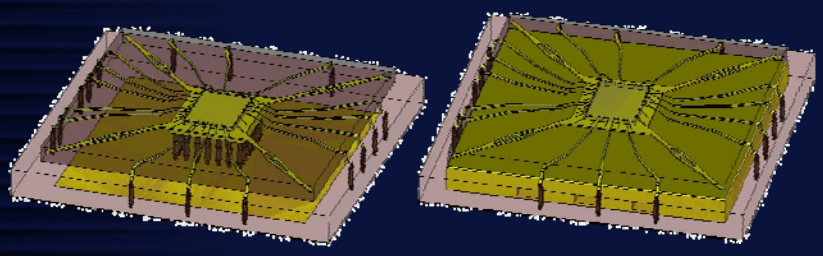




- However, there are cases where ground slug will provide benefit

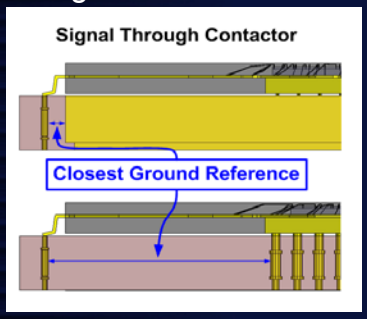
Contactor Designs – QFP Grounding

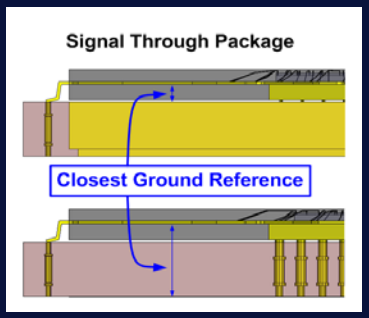
- If device has small ground pad, ground slug can improve performance
  - Ground probe locations will be limited by size of ground pad
  - Ground slugs can get much closer to signal pins



Contactor Designs – QFP Grounding

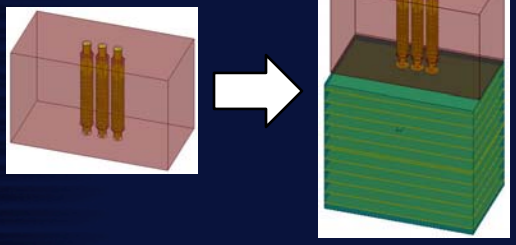
- Ground slugs
  - Can improve performance through contactor AND through package
  - Brings contactor/package ground reference closer to signals





Contactor Performance w/ PCB Launch

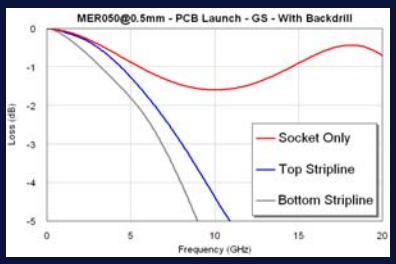
- Launch reduces bandwidth due to three variables:
  - 90° transition
  - Via length
  - Stub length (if not backdrilled)



- Example
  - Compare different layers, ground configurations on 0.187” PCB

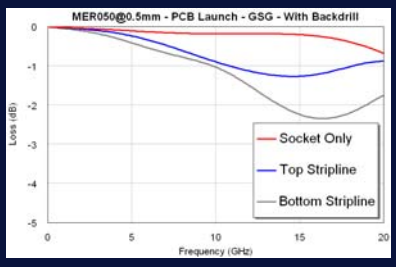
Contactor Performance w/ PCB Launch
G-S (GND SIG) Configuration

	-1dB	-3dB
Contactor Only	5.5 GHz	24 GHz
Contactor/Launch (Backdrill)	3-4.5 GHz	7-8 GHz
Contactor/Launch (No Backdrill)	2.7 GHz	3.5-5.5 GHz



Contactor Performance w/ PCB Launch
G-S-G (GND SIG GND) Configuration

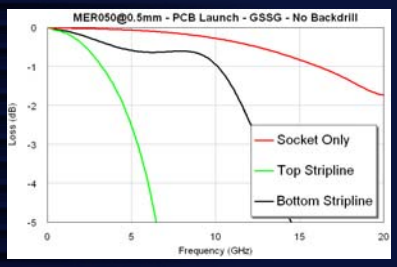
	-1dB	-3dB
Contactor Only	21.5 GHz	27 GHz
Contactor/Launch (Backdrill)	10 GHz	25 GHz
Contactor/Launch (No Backdrill)	3.5-6 GHz	5-12 GHz

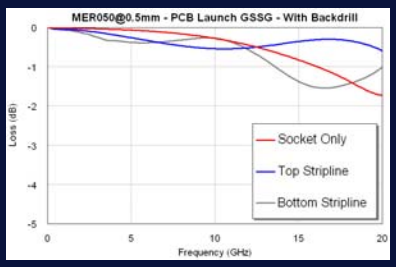


Contactor Performance w/ PCB Launch

G-S-S-G (GND SIG SIG GND) Configuration

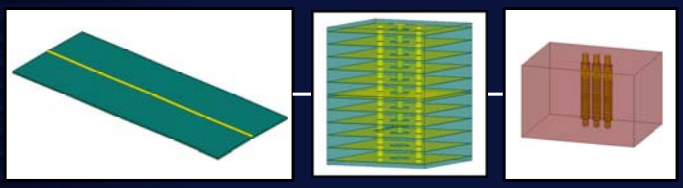
	-1dB	-3dB
Contactor Only	16 GHz	28 GHz
Contactor/Launch (Backdrill)	13-21 GHz	26-28 GHz
Contactor/Launch (No Backdrill)	3-10 GHz	5-13 GHz





Signal Integrity in the Test Interface

System



System Rules of Thumb

- What is the loss budget for a typical system?
- Industry rule of thumb is -3dB:

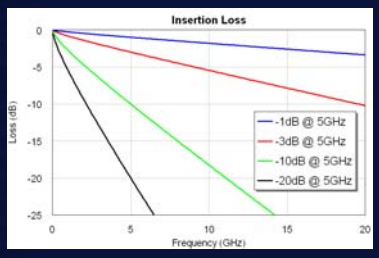
	-1dB	→ Contactor
+	-1dB	→ PCB
+	-1dB	→ Everything else**
	-3dB	→ System

- -3dB is a VERY rough approximation
- Actual loss can be much more, up to -20dB
- Several variables dictate actual requirements

**includes connectors, cabling, launches

Digital Applications

- -3dB rule of thumb is insufficient
- Some applications can handle up to -20dB
- Example:
  - View 10GB/s eye diagrams for different interfaces
  - Compare 1dB, 3dB, 10dB, 20dB at fundamental

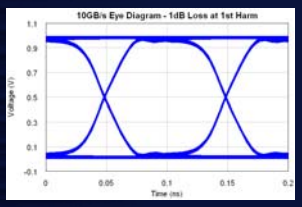


Digital Applications

- Results

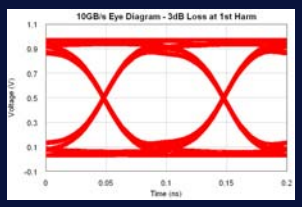
-1dB

EYE_{HEIGHT}	865 mV
EYE_{WIDTH}	99 ps
$JITTER_{P-P}$	1 ps
$T_{RISE-OUT}$	26 ps



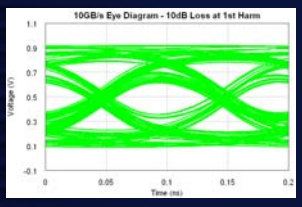
-3dB

EYE_{HEIGHT}	624 mV
EYE_{WIDTH}	95 ps
$JITTER_{P-P}$	3 ps
$T_{RISE-OUT}$	33 ps



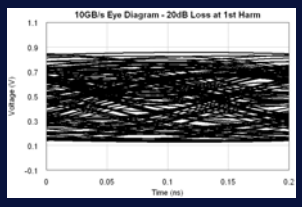
-10dB

EYE_{HEIGHT}	41 mV
EYE_{WIDTH}	57 ps
$JITTER_{P-P}$	26 ps
$T_{RISE-OUT}$	59 ps



-20dB

EYE_{HEIGHT}	N/A
EYE_{WIDTH}	N/A
$JITTER_{P-P}$	N/A
$T_{RISE-OUT}$	N/A

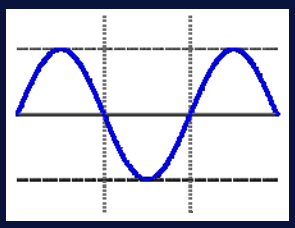


Digital Applications

- Recovering data
  - It is possible to recover data with significant loss
  - Data often recovered using pre-emphasis or equalization
  - Pre-emphasis → Modifies content at the output
  - Equalization → Modifies content at the input
- Linear loss (due to PCB length) is much easier to offset than non-linear loss (due to discontinuities)
  - Return loss quantifies reflections and can be more critical than insertion loss

Analog Applications

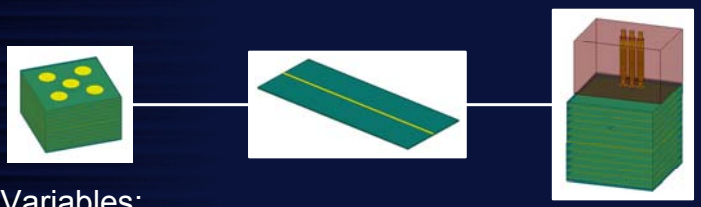
- -3dB rule of thumb is insufficient
- Some applications can handle up to -10dB
- Concern is narrowband (one specific frequency range) instead of broadband
- Tuning is often required for analog signals to optimize performance



Realistic Loss Expectations

- Simulation Example

  Tester Via → PCB Trace → PCB/Contactor



- Variables:

Tester Via	PCB Trace	PCB/Contactor
Backdrill (Y/N)	uStrip/Stripline	Backdrill (Y/N)
	Trace Width	Signal Layer
	PCB Material	$Z_{CONTACTOR}$

Realistic Loss Expectations

- Simulation Example Results
  Tester Via → PCB Trace → PCB/Contactor

	(-3dB)
• System w/ 2” Trace	3-20 GHz
• System w/ 4” Trace	2.5-10 GHz
• System w/ 8” Trace	1.5-6 GHz
• System w/ 12” Trace	1-4 GHz
• System w/ 16” Trace	0.7-3 GHz

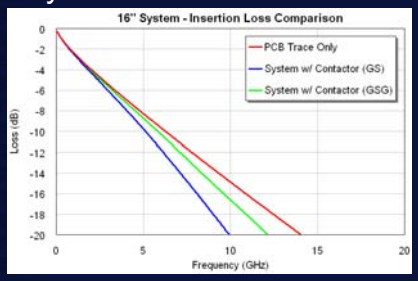
Realistic Loss Expectations

- Simulation Example Results
- Variables that impact bandwidth

	Lower S_{21}	Higher S_{21}
• Backdrill	No	Yes
• Topology	Stripline	Microstrip
• Trace Width	Narrow	Wide
• PCB Material	FR4-type	Exotic
• Signal Layer	Close to Surface	Close to Center
• $Z_{CONTACTOR}$	GS	GSG, GSSG

Source of Loss

- Example: 16” System**



	1GHz	5GHz
• Loss		
• PCB Trace	2.3dB (95%)	8.3dB (85-95%)
• Vias/Contactor	0.1-0.2dB (5%)	0.5-1.5dB (5-15%)
• Total	2.4-2.5dB	8.8-9.8dB

**See Appendix 4 for comparisons with other trace lengths

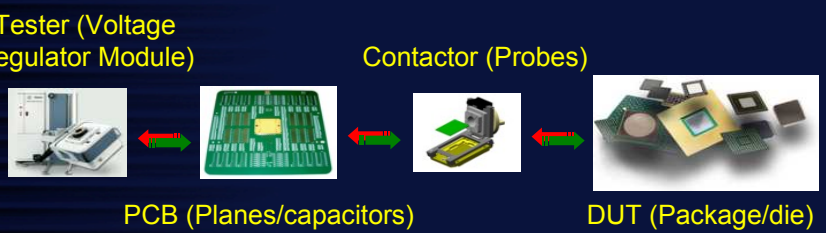
Power Integrity in the Test Interface

PDN Agenda

- Introduction to Power Delivery Network
- Key PDN Concepts
- PDN Example

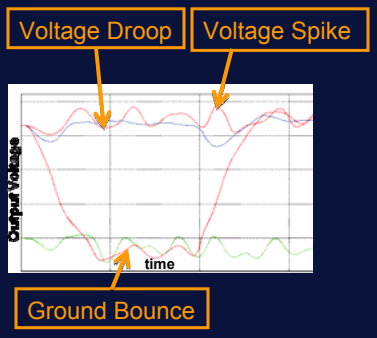
Introduction to the PDN

- Goal of Power Delivery Network (PDN)
  - Provide constant voltage to DUT in high di/dt environment
- Requirement of PDN
  - Maintain low impedance path from tester to DUT across all operating frequencies of device



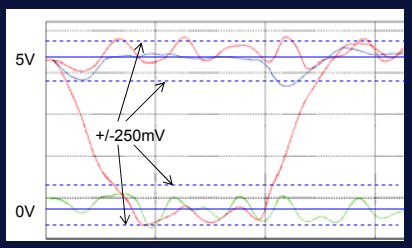
Introduction to the PDN

- Good PDN design minimizes noise on the power and ground rails
- Problems caused by poor PDN:
  - Voltage droop
  - Rail collapse
  - Voltage spikes
  - Ground bounce
  - Simultaneous Switching Noise
  - Power-supply-induced jitter



Introduction to the PDN

- IC Power Supply Voltage
  - Yesterday 5V
  - Today 1V (5x reduction)
- Typical Supply Ripple allowed
  - Yesterday 5-10%
  - Today 0.5% (up to 20x reduction)
- Current requirements
  - Yesterday 10A
  - Today 150A (15x increase)
- Z_{TARGET} requirements
  - Yesterday 100mΩ
  - Today 1mΩ (100x reduction)

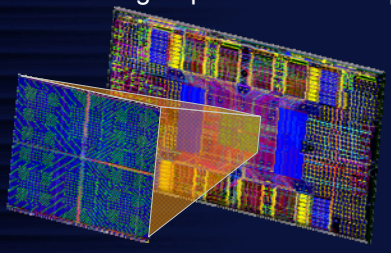


Year	Power (W)	Vdd (V)	Idd (A)
2010	146	0.97	151
2011	161	0.93	173
2012	158	0.90	176
2013	149	0.87	171
2014	152	0.84	181
2015	143	0.81	177
2016	130	0.78	167

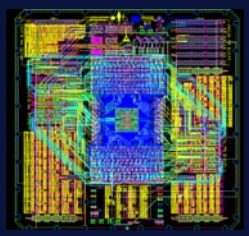
Data courtesy of ITRS 2010

Considerations for ATE Environment

- High-layer-count PCB requires long vias
  - Increases distance to capacitors
- Large PCB
  - Increases distance to power supply and capacitors
- High-density PCB
  - Routing requirements limit space for capacitors



1 mm pitch 7396 pin BGA
46 electrical layers

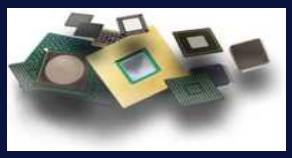


1 mm pitch 1924 pin BGA
1900 components, 592 relays

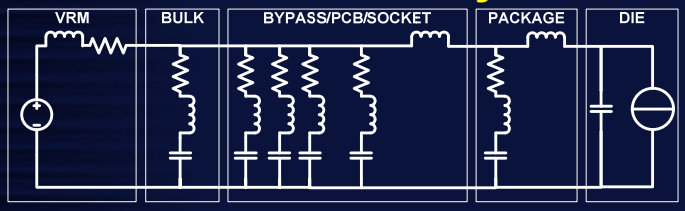
Considerations for ATE Environment

- Contactor
  - Increases distance to capacitors

- Limited specifications
  - Detailed device power consumption unavailable
  - Requires approximations to be made for PDN design
  - Wide range of devices
  - Requires generic rules and conservative design



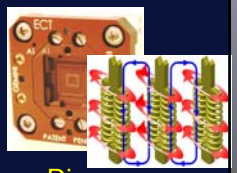
Path of Power Delivery Network



Voltage Regulator Module (VRM)

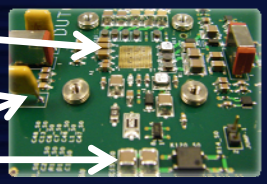
Power/Ground Planes

Contactor

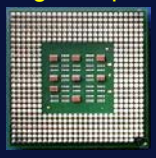


Bypass Capacitors

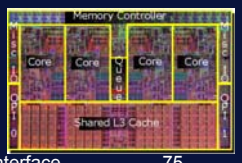
Bulk Capacitors



Package /Capacitors



Die

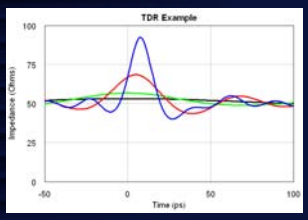


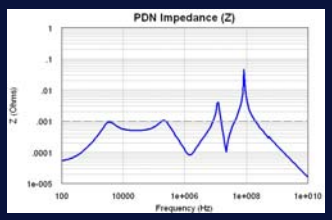
Impedance in Power Delivery Network

SI Impedance	**PDN Impedance**
Ideal Z = 50Ω	Ideal Z ≈ 0 Ω
Ideal Z → high bandwidth	Ideal Z → constant voltage
Instantaneous impedance	Aggregate impedance response
Time domain	Frequency domain

$$Z = \sqrt{\frac{L}{C}}$$

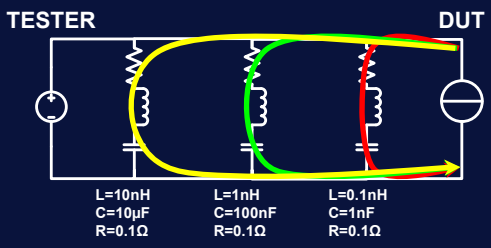
$$Z = R + 2\pi fL + \frac{1}{2\pi fC}$$





Understanding the PDN Impedance

- Lowest path to ground will vary based on frequency

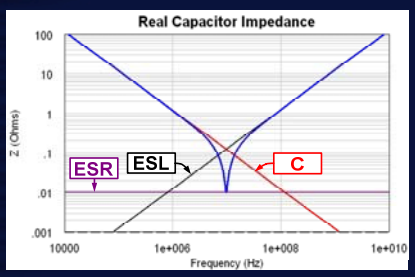


Signal Frequency	Impedance		
• 250 MHz	15Ω	2Ω	***0.5Ω***
• 80 MHz	5Ω	***0.5Ω***	2Ω
• 30 kHz	***0.5Ω***	53Ω	5300Ω

Capacitance in PDN

- Ideal capacitors (C) have linear frequency response
- Real capacitors include parasitic inductance and resistance
  - Equivalent Series Inductance (ESL)
    - Inductance of path from the DUT to the capacitor
    - Limits the useful frequency range of capacitor
  - Equivalent Series Resistance (ESR)
    - Dampens the impedance peaks
    - Minimum impedance of capacitor

$$Z = R + 2\pi fL + \frac{1}{2\pi fC}$$



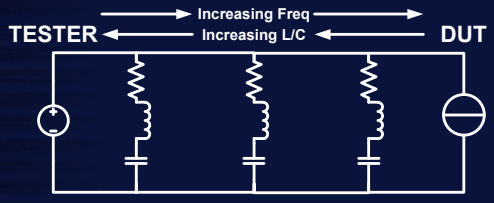
Capacitance in PDN

- Capacitors used to provide low impedance (AC) from power to ground
- Multiple capacitors placed throughout PCB to cover all frequencies

Large caps (Bulk)
High C and High L
Low Z at low frequency

Small Caps (Bypass)
Low C and Low L
Low Z at high frequency

$$Z = R + 2\pi fL + \frac{1}{2\pi fC}$$

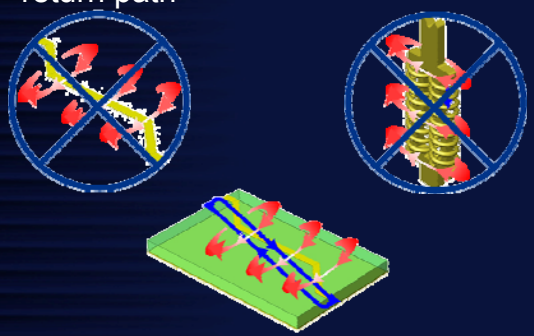


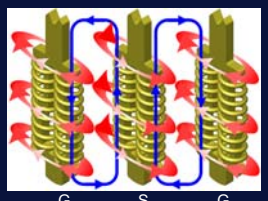
Inductance in PDN

- Inductance of single probe/via/trace is not practical
- Equation for loop inductance:

$$L_{LOOP} = L_{SELF\text{-}SIG} + L_{SELF\text{-}RTN} - 2 \times L_{MUTUAL}$$

- L_{MUTUAL}: Mutual Inductance between signal path and return path



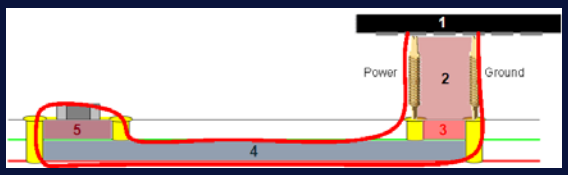


See also "Determining Inductance in Contactors", Ryan Satrom, BiTS 2007

Inductance in PDN

ESL includes the path from the DUT to the capacitor

1) Die/Package
2) Contactor
3) DUT Vias
4) Planes
5) Vias/Capacitor



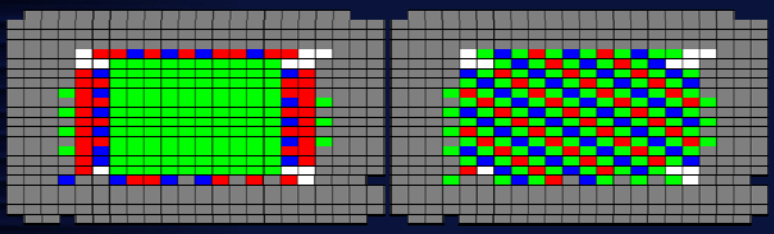
- PCB Inductance is based on:
  - Cap to DUT distance
  - Power/Ground core thickness
  - Power plane geometry
  - Via length
- Contactor Inductance is based on:
  - Probe length
  - Probe diameter
  - Proximity of power pins to ground pins
  - Number of power ground pairs

Inductance in PDN

- In BGAs, inductance minimized by alternating powers and grounds in layout.
- Typical power/ground to signal ratio 1:1
- Grouping all grounds together yields higher inductance
- Grounds in center have no impact on improving inductance

RED = VDD1 BLUE = VDD2 GREEN = GND WHITE = N/C

POOR LAYOUT GOOD LAYOUT



Minimizing the Inductance

- Use short, low inductance contactor
  - e.g. Gemini™, Mercury™ contactors
- Minimize area of current loops
  - Use low ESL capacitors
  - e.g. X2Y®, Capacitor Arrays
  - Place power/ground vias as close to each other as possible
  - Place bypass capacitors as close to DUT as possible
  - Capacitor interposers (e.g. 3M™, AVX ™)
- Maximize width of conductors
  - Wide traces, wide planes
- Minimize spacing between ground and power planes
  - Thin-core dielectrics (e.g. Faradflex™, ZBC®, Integra™)
- Use multiple parallel paths, pairs of vias, pairs of planes
- Alternate polarity of capacitor vias

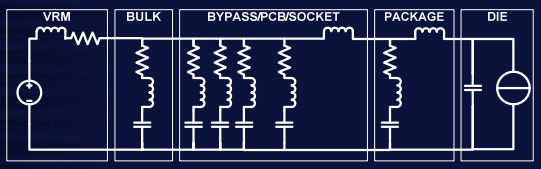
Defining the Target Impedance

- Required impedance is application-specific
  - Every device has its own unique current profile
  - Difficult to apply a standard to PDN design
- Device specification dependent
  - Impedance calculated from datasheet specifications
- Z_{TARGET} approximated using one of the following:
  - Transient currents
  - Power consumption
  - Simulated IC models
  - Equation for target impedance using transient current:

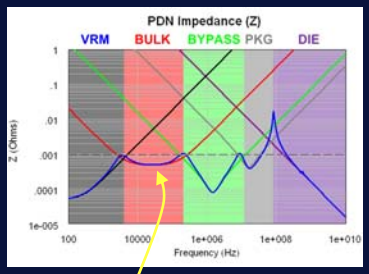
$Z_{TARGET} = V_{CC} \times V_{RIPPLE}(\%) / I_{TRANSIENT}$ [where $I_{TRANSIENT} = ½ I_{CCMAX}$]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{CC}	Power supply voltage	7.6	8.0	8.4	V
I_{CC}	Power supply current		190	250	mA

Impedance Profile of PDN

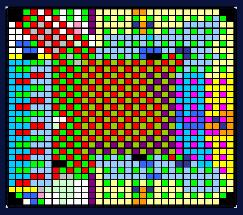


1. VRM (sub-10kHz)
2. Bulk capacitors (1kHz - 5MHz)
3. Bypass capacitors (1MHz - 100MHz)
4. Package (10MHz - 300MHz)
5. On-die decoupling (100MHz+)

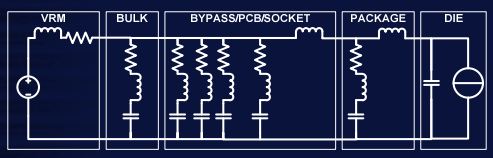


Aggregate Response

PDN Example



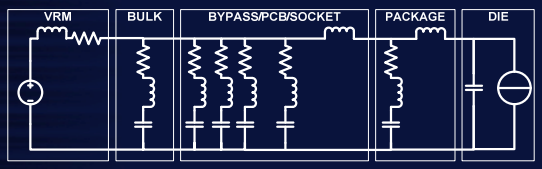
- Example: 1000-pin BGA 1mm pitch
  - V_{CC} = 1V (5% ripple), I_{MAX} = 100A
- Pin Assignment Approximations:
  - 25% Power, 25% Ground, 25% Status I/O, 25% HS I/O
- Use one voltage supply – 250 PWR, 250 GND pins*
- Solving for the required impedance
  - $Z_{TARGET} = V_{CC} \times V_{RIPPLE}(\%) / I_{TRANSIENT}$
  - Z_{TARGET} = 1V x 0.05 / 50A = 1mΩ



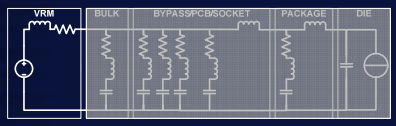
***Most large BGAs have multiple power supplies. One supply is used to simplify example.**

PDN Example

- Design Strategy:
  - Define Z_{PDN} independently across each PDN region
  - Determine the aggregate response including each successive region
  - Optimize Z_{PDN} to meet Z_{TARGET} of 1mΩ across all frequencies



PDN Region #1: VRM



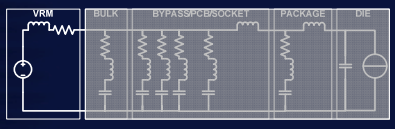
- VRM
  - Provides the power to the DUT
  - Senses voltage at DUT and changes current to maintain constant DC voltage
  - Effective for very low frequencies
  - Typical value for L = 25-50nH
- Performance limited by the inductance:

$$Z_L = 2\pi f_{MAX} L$$

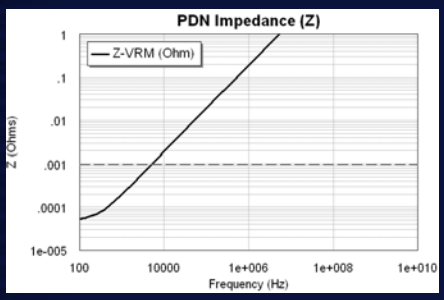
- Assuming L = 30nH, Z_{TARGET} reached at:

$$f_{MAX} = \frac{Z_{TARGET}}{2\pi * L_{VRM}} = \frac{1m\Omega}{2\pi * 30nH} = 5kHz$$

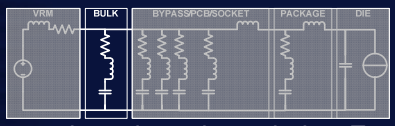
PDN Region #1: VRM



- Plot shows impedance below Z_{TARGET} up to 5kHz



PDN Region #2: Bulk Capacitors



- Bulk capacitance must keep impedance below Z_{TARGET} beyond 5kHz
- Bulk capacitor ESR typically 2-100mΩ
- Equation for impedance of a capacitor:

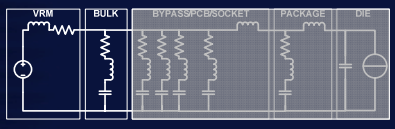
$$Z_C = \frac{1}{2\pi f_{MAX} C}$$

- Using f=5kHz and Z_{TARGET} = 1mΩ

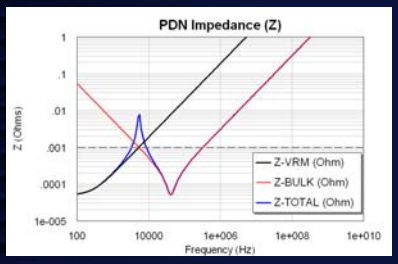
$$C_{BULK} > \frac{1}{Z_{TARGET} * 2\pi * 5kHz} = 30{,}000\,\mu F$$

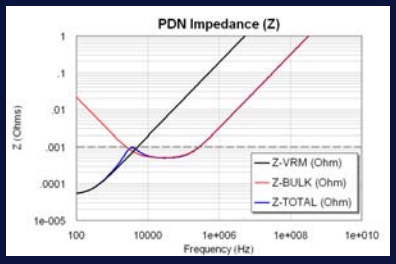
- Total C_{BULK} will be split up between multiple capacitors with value of C_{BULK}/n, where n= # of capacitors

PDN Region #2: Bulk Capacitors

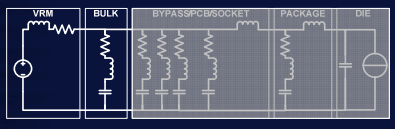


- Results for C_{BULK}=30,000µF creates peak at 5kHz
- Peak reduced by increasing capacitance to 75,000µF and ESR from 2mΩ to 5mΩ
- f_{MAX} is determined by inductance from DUT to bulk capacitors

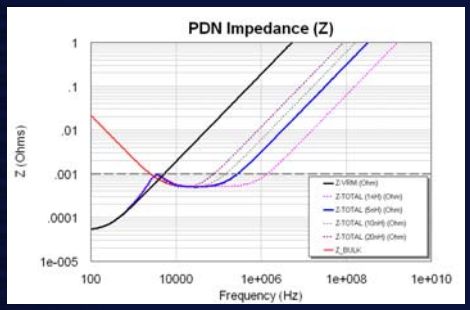




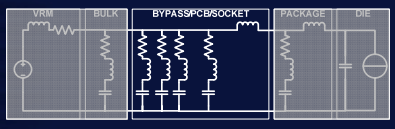
PDN Region #2: Bulk Capacitors



- Typical values of L_{BULK} are 1nH-20nH
- Results in f_{MAX} from 80kHz-1.4MHz
- 5nH (blue) will be used for L_{BULK} (f_{MAX} = 300kHz)



PDN Region #3: Bypass/PCB/Contactor



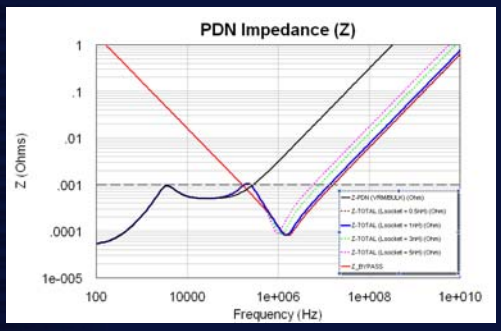
- Bypass capacitance must provide low impedance path beyond 300kHz
- Using f=300kHz and Z_{TARGET} = 1mΩ, solving for C:

$$C_{BYPASS} > \frac{1}{Z_{TARGET} * 2\pi * 300kHz} = 500\mu F$$

- Total C_{BYPASS} will be split up between hundreds of capacitors with value of C_{BYPASS}/n, where n= # of capacitors

PDN Region #3: Bypass/PCB/Contactor

- One capacitor per pin (250 capacitors total)
- C_{BYPASS} set to 1000µF to minimize impedance peak (250 x 4µF)
- L_{BYPASS} varies from 2.5nH-7.5nH (3nH is used)
- Plot shows impact from varying contactor inductance
- Results in f_{MAX} from 6MHz-16MHz

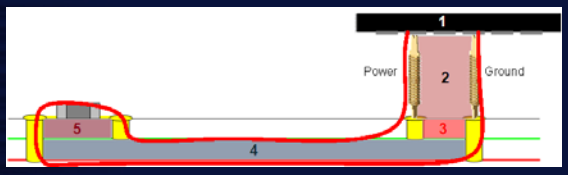


PDN Region #3: Bypass/PCB/Contactor

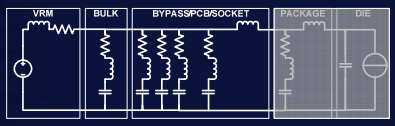
- f_{MAX} of bypass path is maximum frequency that the ATE interface can keep impedance below Z_{TARGET}
- f_{MAX} is determined by inductance of path from DUT to bypass capacitors (L_{BYPASS})

$$Z_{BYPASS} = 2\pi f_{MAX} L_{BYPASS}$$

- Typical f_{MAX} ranges from 1-100MHz
- Contactor inductance only impacts PDN up to ~ f_{MAX}

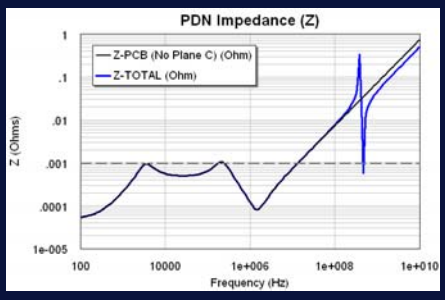


PDN Region #3: Bypass/PCB/Contactor

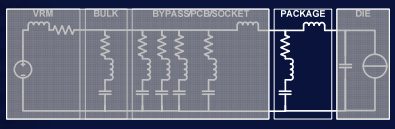


- PCB Planes
  - The capacitance of the PCB planes will interact with the parallel loop inductance of the bypass network to create a resonance

$$f_{RES} = \frac{1}{2\pi * \sqrt{L_{BYPASS} * C_{PLANES}}}$$

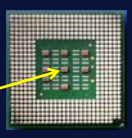


PDN Region #4: Package



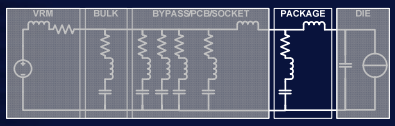
- The package inductance limits f_{MAX} of the ATE interface
- Some packages can add capacitors to help increase f_{MAX}

Package Caps

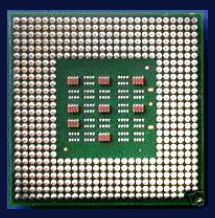


- Typical inductance values (per power/ground pair)
  - Leaded packages ~3-7nH
  - Chip-scale packages ~1-3nH
  - BGA packages (wire-bond) ~ 1-5nH
  - BGA packages (flip-chip) ~0.1-0.5nH

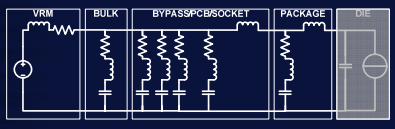
PDN Region #4: Package



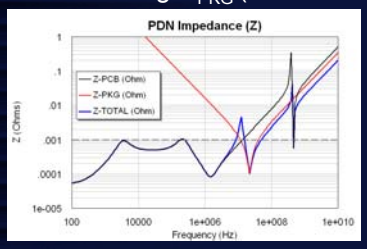
- Package Inductance
  - Flip-Chip technology, L = 0.1nH
  - L_{PKG} = 0.1nH/250 power pins = 0.4pH
- Package Capacitors
  - 10 capacitors
  - C_{PKG} = 1000nF x 10 capacitors = 10µF
  - $L_{PKG-CAP}$ = 50pH / 10 capacitors = 5pH
- 1st order approximation for f_{MAX} of Package:
  - $Z_{PDN} < 2\pi \times (L_{PKG} + L_{PKG-CAP}) \times f_{MAX}$
  - $f_{MAX} \approx Z_{PDN} / (2\pi (L_{PKG} + L_{PKG-CAP})) \approx 0.001 / (2\pi \times 5.4pH)$
  - $f_{MAX} \approx 30MHz$

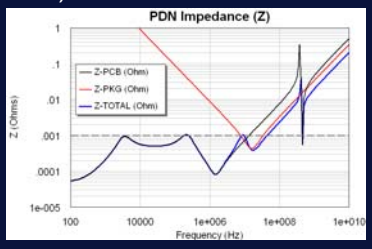


PDN Region #4: Package

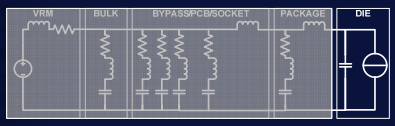


- Results create peak above Z_{TARGET}
- Peak can be reduced by:
  - Decreasing L_{BYPASS} (set at 3nH)
  - Increasing C_{PKG} (from 10 x 1µF to 25 x 1uF)
  - Increasing R_{PKG} (from 1mΩ to 5mΩ)



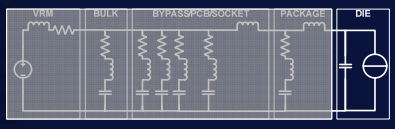


PDN Region #5: Die



- Remaining decoupling must be accomplished by the capacitance on the die
- On-die capacitance comes from three areas:
  - Power ground grid
  - Gate capacitance due to millions of transistors
  - Thin oxide capacitance in silicon

PDN Region #5: Die



- On-die capacitance can be approximated based on technology*:

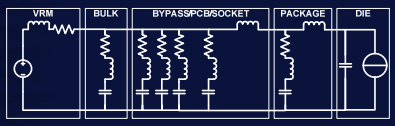
Channel Length	Capacitance
130nm	130nF/cm^2
65nm	260nF/cm^2
50nm	340nF/cm^2
32nm	520nF/cm^2
22nm	770nF/cm^2

- Assume DIE_{SIZE} = 2cm^2**
- Technology → 32nm**

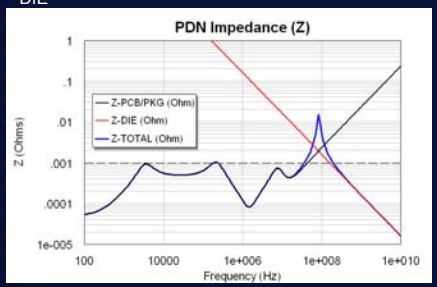
$$C_{DIE} = \frac{520nF}{cm^2} * 2cm^2 = 1.04\mu F$$

***See "Signal and Power Integrity – Simplified", Eric Bogatin, p677**
****Reflects current BGA technology**

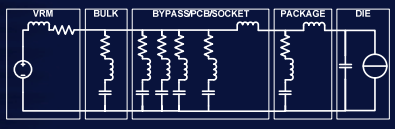
PDN Region #5: Die



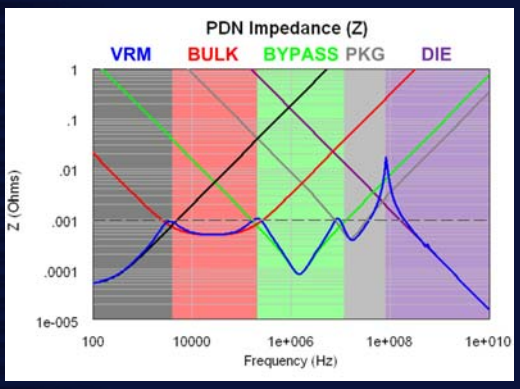
- Results create additional peak above Z_{TARGET}
- Peak can be reduced by:
  - Decreasing L_{PKG}
  - Increasing C_{DIE}



PDN System Summary



- Plot overlay shows the frequencies where each region has impact



PDN Example Limitations

- This PDN design results in impedance higher than Z_{TARGET} for frequencies in the 100MHz range
  - The only way to meet the target impedance is to decrease inductance (L_{BYPASS}, L_{PKG}) or increase capacitance (C_{PKG}, C_{DIE})
  - Design may cause problems if device has a large number of signals in the 100MHz range
  - Impedance target can be very difficult to meet across all frequencies

PDN Conclusions

- Power Delivery Network design is complicated
- Devices have unique impedance profile requirements
- The task of accurately modeling the PDN is challenging
- PCB, contactor, package and die all play a role in the PDN
- Understanding how each component impacts the overall performance of the PDN is required to design a quality system
- The focus on power integrity will increase in the coming years

Recommended Resources

- "Power Integrity Modeling and Design for Semiconductors and Systems", Ege Engin and Madhavan Swaminathan, 2007.
- "Signal and Power Integrity – Simplified", Eric Bogatin, 2nd edition, 2009.

Appendix 1 – Modifying PCB Impedance

- There are several factors that impact impedance
- In PCB Traces: **Z**
  - ↑ Trace Width ↓
  - ↑ Dielectric Thickness ↑
  - ↑ Trace Thickness ↓**
  - ↑ Dielectric constant of material ↓
  - ↑ Trace Length ↔

**Minor impact

Appendix 2 - Contactor Return Loss (-10dB)

SINGLE-ENDED (Z_0=50Ω)

- G-S-G (GND SIG GND)** 5-25 GHz
- G-S (GND SIG) 2-8 GHz
- G-S (DIAG) (FLOAT SIG / GND FLOAT) 1.5-5 GHz
- G-X-S (GND FLOAT SIG) 1-3.5 GHz
- G-X-X-S (GND FLOAT FLOAT SIG) 0.5-2.5 GHz

DIFFERENTIAL (Z_0=100Ω)

- S-S (SIG SIG) 12-30 GHz
- G-S-S (GND SIG SIG) 12-30 GHz
- G-S-S-G (GND SIG SIG GND) 12-30 GHz

**GSG is standard datasheet specification

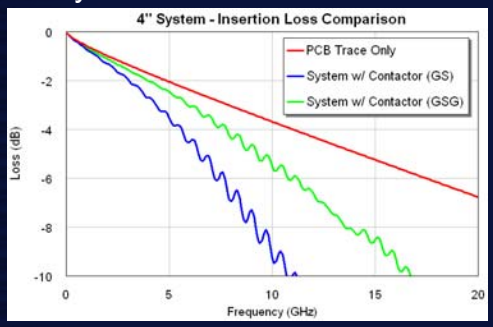
Appendix 3 - Modifying Contactor Impedance

- There are several factors that impact impedance
- In contactors:

	Z
↑ Number of adjacent GND pins	↓
↑ Pitch	↑
↑ Probe Diameter	↓
↑ Dielectric constant of material	↓
↑ Probe Length	↔

Appendix 4 - Source of Loss (4")

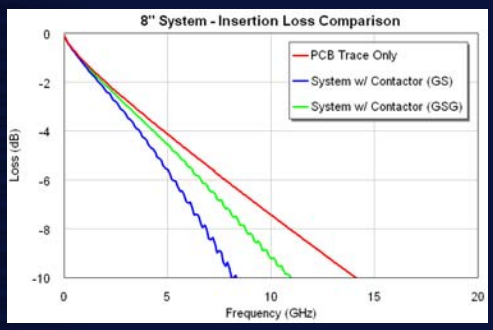
- Examples: 4" System



	1GHz	5GHz
• Loss		
• PCB Trace	0.6dB (75-85%)	2dB (60-80%)
• Vias/Contactor	0.1-0.2dB (15-25%)	0.5-1.5dB (20-40%)
• Total	0.7-0.8dB	2.5-3.5dB

Appendix 4 - Source of Loss (8")

- Examples: 8" System



	1GHz	5GHz
• Loss		
• PCB Trace	1.2dB (85-95%)	4dB (75-90%)
• Vias/Contactor	0.1-0.2dB (5-15%)	0.5-1.5dB (10-25%)
• Total	1.3-1.4dB	4.5-5.5dB