BiTS Burn-in & Test Socket Workshop 2011

Session 5

ARCHIVE 2011

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Probing Inside the Socket
Marc Moessinger—Verigy

Pin Grid Array Current Sense Interposer Application Featuring Vertical Embedded Resistors
Shaul Lupo, Omer Vikinski—Intel Corporation

PCB Pad Wear Analysis at 0.4mm Pitch - the story continues...
Valts Treibergs, Christopher Cuda—Multitest

Thermal Testing - some tidbits from the lab
James Forster—Wells-CTI
John Moore—Texas Instruments

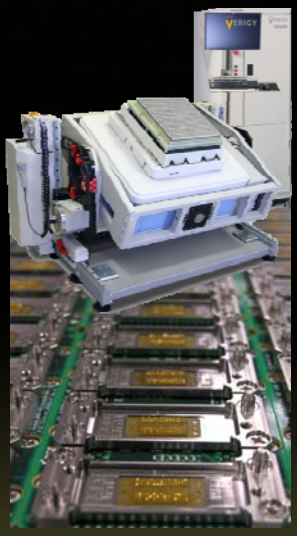
Probing Inside the Socket

Marc Moessinger
Verigy

2011 BiTS Workshop
March 6 - 9, 2011

The challenge

- For Semiconductor Test Systems, the performance is usually specified at the interface between tester and DUT (**D**evice **U**nder **T**est) Board
- But the user would like to know the performance at the device, preferably directly at the device pins inside of the socket



A short excursion into German Language

He measures = Er misst

The crap = Der Mist

First law of measurement engineering:

- Wer misst misst Mist
- The one who measures measures crap

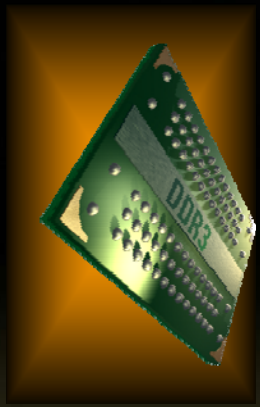
How to measure inside of the socket and to avoid measuring crap?

Objective of this presentation

- Explain the impact of the socket and the DUT on the signals
- Present solutions to measure the electrical signal performance inside of the socket
  - Very practical approach, no theory
  - Removable probes, non-destructive
  - Including a solution to reflect the impact of the DUT
- Use a typical DDR3 engineering and high-volume manufacturing test environment as example
  - Can be leveraged to other applications

Problem of probing - Accessibility

- BGA type of devices doesn't allow access of socket pins or device balls
- Small device size doesn't allow easy probing
- Small ball pitch makes probing difficult



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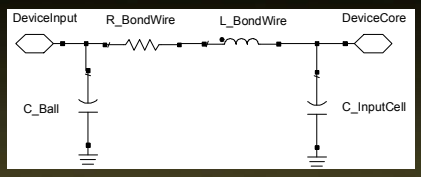
Problem of probing - DUT influence

- The device itself has significant impact on the signal shape
  - Input capacitance caused by balls, package traces and pads
  - Bond wire inductance
  - Signal path resistance



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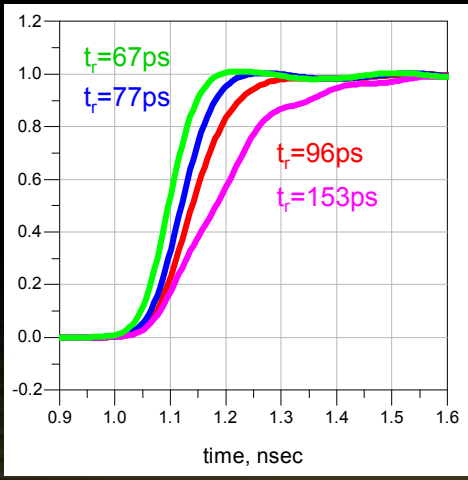
Influence of the DUT - a simple Simulation



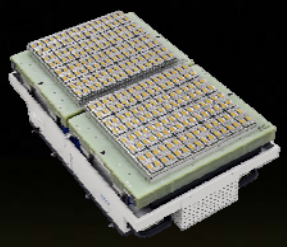
- Source only (with or without termination)
- 50Ω Terminated, 1pF Load
- Unterminated, 1pF Load
- Complex DUT

(ADS Simulation, Normalized)

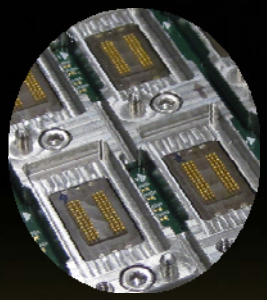
Depending on the DUT loading, the rise time can easily increase by a factor of two

The real setup: Characterization of a DDR3 Production Environment

HSM3G DDR3 Memory Tester

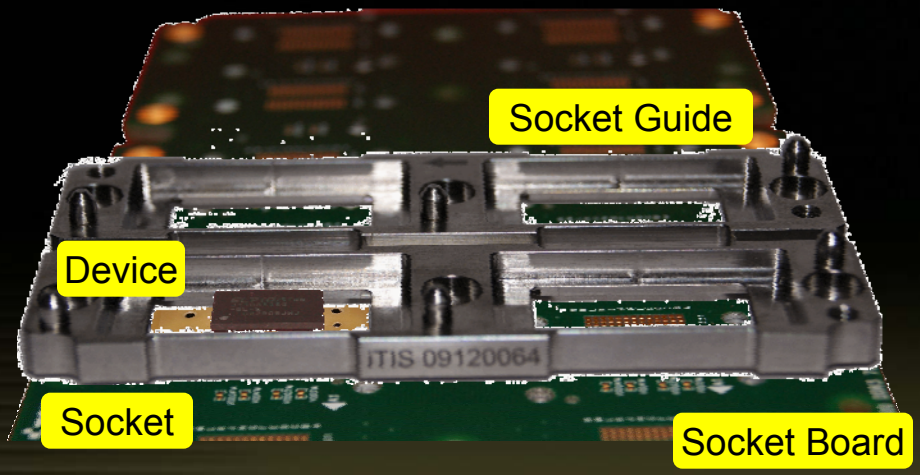


256 site DDR3 Test Interface



2.1mm Sockets

The Socket Mechanics



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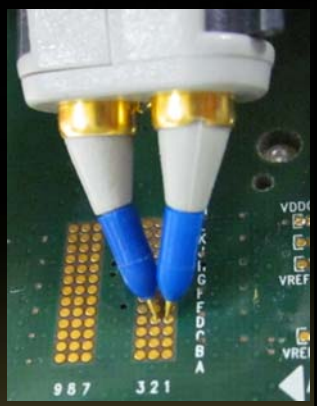
The most common Approach: Probing on the PCB

Advantages

- Easy way of probing
- No special tooling required
- Probes readily available from several vendors
- All device pins accessible



Disadvantages

- The influence of the socket and DUT is missing
- Manual probing makes it non-repeatable
- The socket board pads may be damaged

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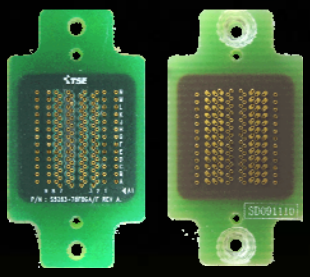
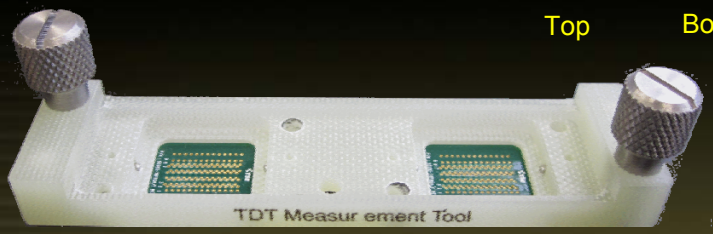
Measurement Tool

- Simple PCB with vias for Signals
  - Pads on bottom side on same location as the device
- Probe pads for signal and GND
- Mechanical structure to insert the PCB into the socket
  - Replaces the device



Top Bottom



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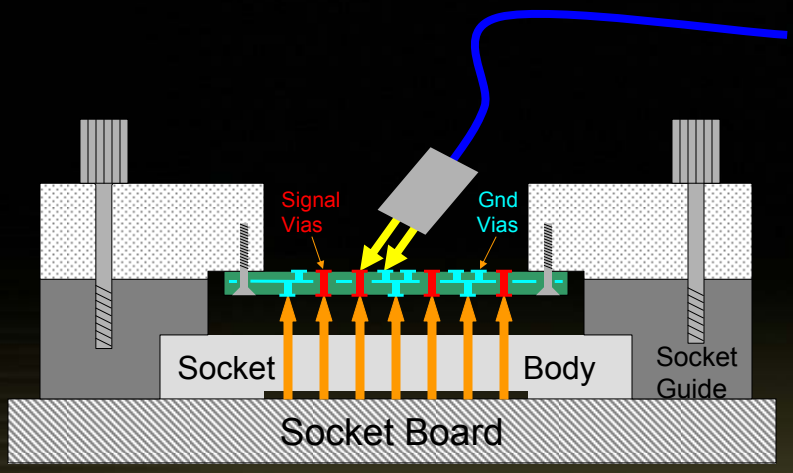
Measurement Tool



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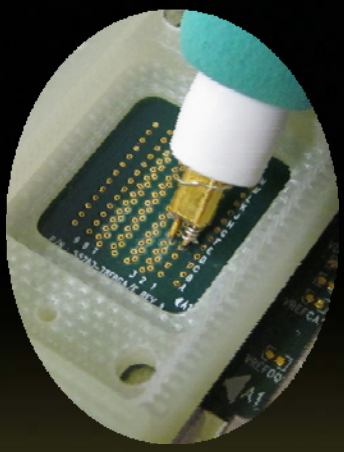
Measurement Tool

Advantages
- Easy and repeatable way of probing
- Measurement includes socket influence
- GND pads available at a fixed pitch
- All device pins accessible
- No damage to socket board pads or the socket

Disadvantages
- Adds a via to the signal path
- Influence of the DUT is missing



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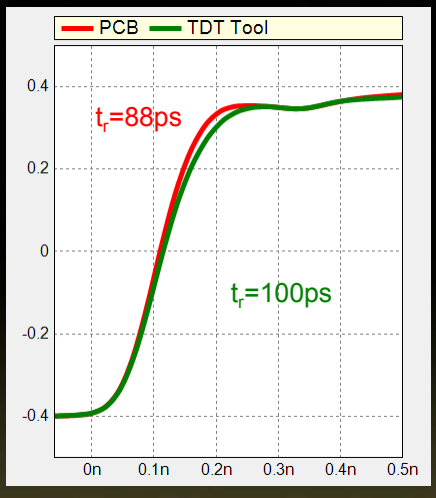
Measurement result

- **Measurements into 50Ω**
  - **Directly on the PCB**
  - **with socket & Measurement Tool**
- **Very similar waveforms**
- **Influence of the socket and Measurement Tool is almost negligible**



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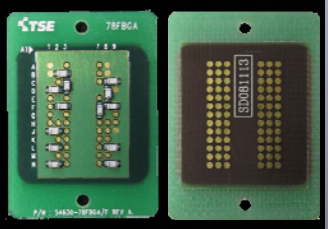
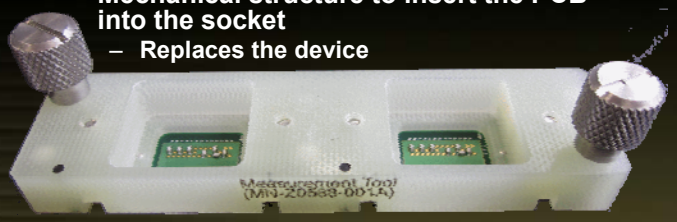
DUT Simulation Tool

- Simple PCB with vias for signals
  - Pads on bottom side on same location as the device
- Discrete components on top side for device simulation
  - Capacitors for input capacitance
  - Resistors for On-Die Termination (ODT)
- Probes can be soldered directly to the component pads
- Mechanical structure to insert the PCB into the socket
  - Replaces the device



Top Bottom



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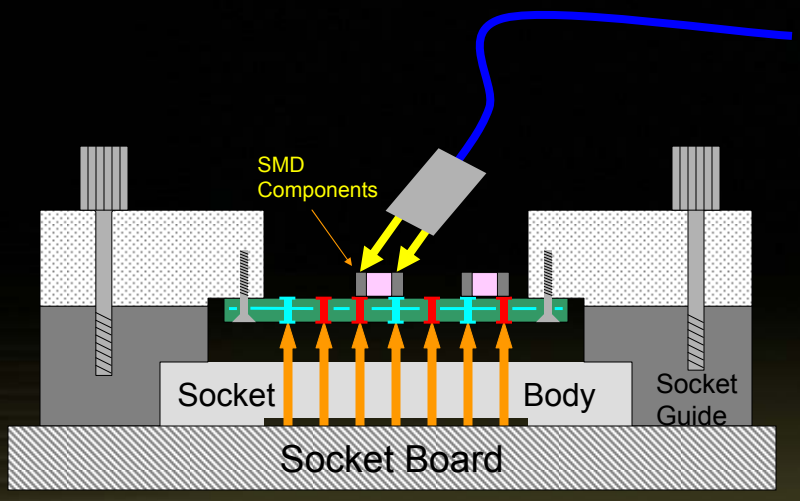
DUT Simulation Tool



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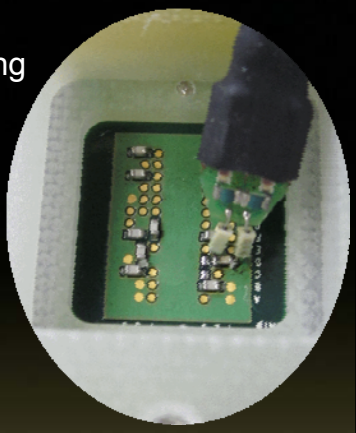
DUT Simulation Tool

Advantages

- Easy and repeatable way of probing
- Measurement includes socket and DUT influence
- No damage to socket board pads or the socket

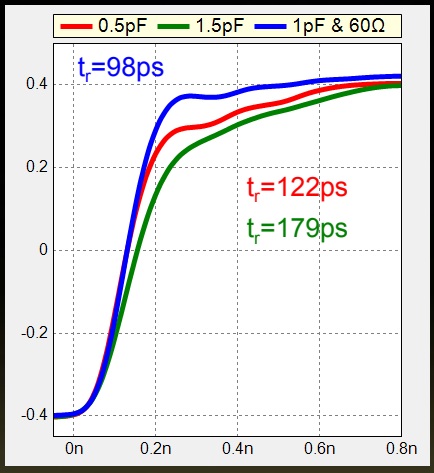


Disadvantages

- Due to space constraints, usually only a few pins can be probed
- Adds a via to the signal path

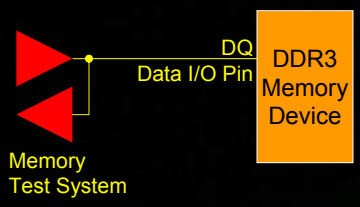
Measurement result

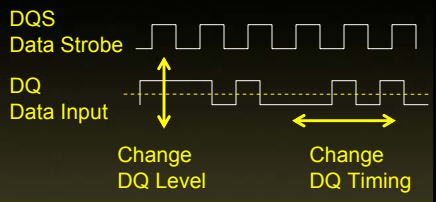
- **Measurements with DUT Simulation Tool and different loading:**
  - **0.5pF**
  - **1.5pF**
  - **1pF and 60Ω**
- **Impact of loading is significant**



Comparison to ATE: Measurement with Memory Test System

- Tester writes data into memory
- Tester reads data from memory and compares to expected data → generates pass/fail information
- By changing input timing and levels during write operation, an Input Eye Diagram can be generated
- Eye Diagram is measured 'through' the device and affected by the memory device input characteristics





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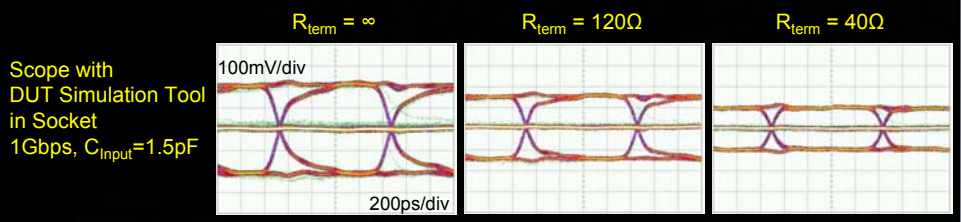
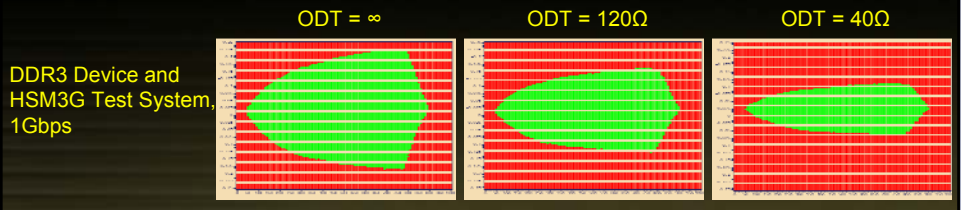
Comparison between Scope and Test System



Note: Scope also captures transition to mid-level during device read operation (straight line in horizontal eye center)



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Conclusion from Measurements

- The DUT input capacitance has a significant impact onto the signal shape and transition time
- A small, well-designed PCB with vias can be used to reliably probe signals inside the socket
  - the signal degradation caused by the PCB is low
  - Discrete SMD components can be added to represent the DUT input behavior
- The Scope measurement using these PCBs correlate well to ATE results

… so where is this approach useful?

- Characterizing sockets, e.g. for effects like cross-talk
- Performing measurements where the influence of the DUT cannot be neglected (e.g. if the bus is part of a tapped bus and the reflections of the DUT have significant impact)
- And, last but not least, make a customer happy when he requests to see the 'real signal at the DUT'

Acknowledgements

- Claus Pfander and Jose Moreira from Verigy HSM R&D, Germany
- Michael Daub from Verigy COE, Germany
- TSE Co., Ltd., Korea

Pin Grid Array Current Sense Interposer Application Featuring Vertical Embedded Resistors

Shaul Lupo, Omer Vikinski
Intel Corporation

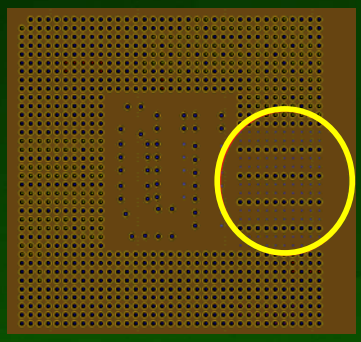
2011 BiTS Workshop
March 6 - 9, 2011

Current Sense Interposer - Development

- Background
- Impact on Testing Operation
- Concept
- Testing mode
- Project advantages

Background

- Microprocessor unit have few power supply rails
- Every rail is fed through multiple socket pins shunted together in package and board level

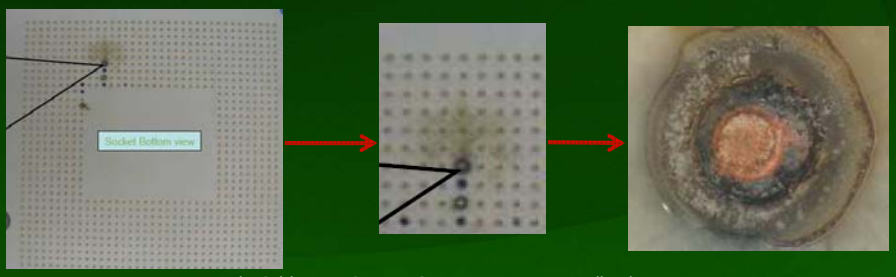


Background

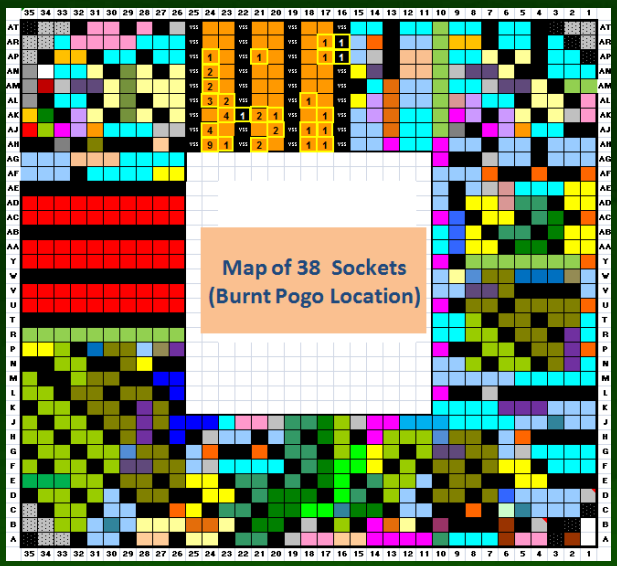
- Current consumption through each package pin is not necessarily equal due to parasitic resistance and inductance paths on board and package along with die relative position

Background

- As we started testing our new Microprocessor product on ATE boards, we faced tens of burnt sockets
- Issue happened mainly in specific areas of one of the power supply rails



Background



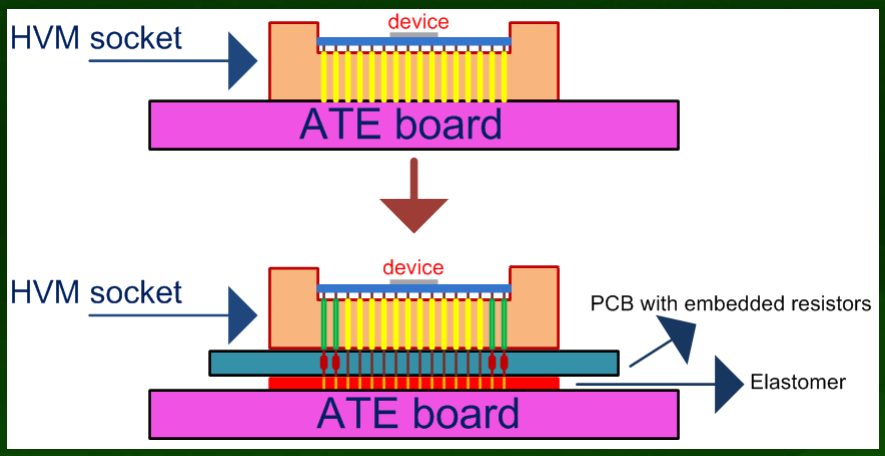
Impact on Testing Operation

- Sockets damage
- ATE boards burnt pads
- Units damage due to bent pins (when pogo pin is stuck in the socket)
- Frequent job interruptions

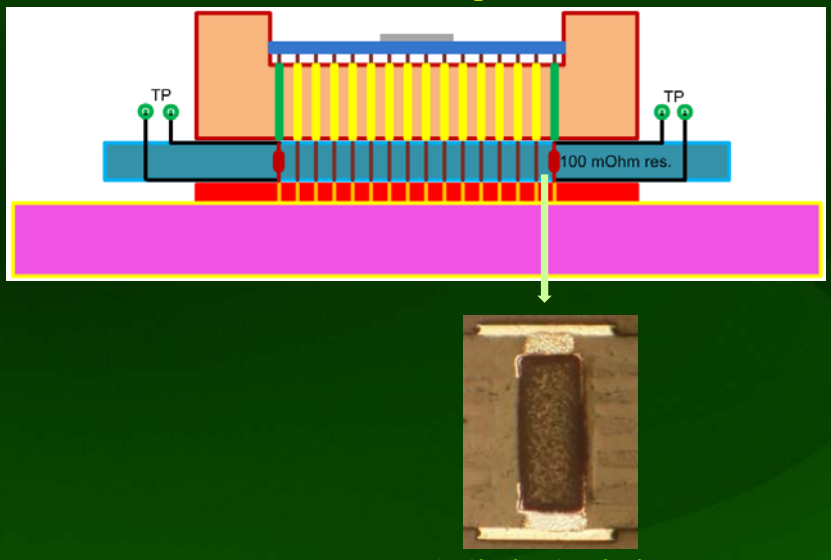
Concept

- The issue mentioned in the previous foils, drove the idea to build a project that will enable to measure current consumption through each pin in the power supply rail, during regular device testing
- A PCB with vertical embedded discrete resistors founded to implement this application
- Contact from PCB to the board implemented by Elastomer design

Concept



Concept



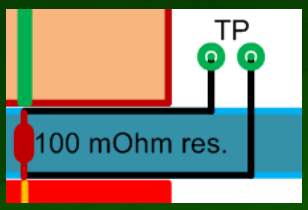
R&D Circuits EC Technology™

Concept

Concept

Testing Mode

- The terminals of every resistor are connected to a common sense probe
- Dynamic voltage drop on the resistor can be measured using multi inputs oscilloscope (during device test)
- Current through the corresponding pin can easily be calculated



Project Advantages

- Better quantification of current distribution across pin field
- Board and package design improvements
- Test programs control to avoid tests which are over stress on socket pogo pins
- HVM socket pogo pins design to the needed CCC (current carrying capacity)
- Reduce or eliminate job interruptions caused by burnt sockets

PCB Pad Wear Analysis at 0.4mm Pitch

- the story continues...

Valts Treibergs & Chris Cuda
Multitest

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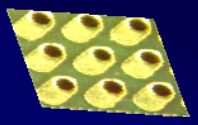
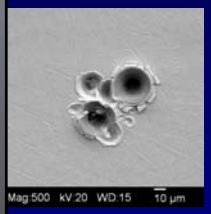
Presentation Agenda

- Recap of 2010 - .8mm pad wear highlights
- .4mm pad construction
- Experimental setup and method
- Objectives of investigation
- Results: Probe tip impact on .4mm pads
- Results: 1.27µm vs 0.75µm gold
- Results: Via-fill material impact on pad wear
- Results: Alternative platings
- Summary

Recap of Results at .8mm Pitch

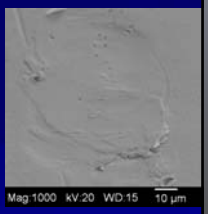
- PCB pad wear-out is a costly issue
- PCB pad wear can be minimized by:
  - Specifying spherical or radius-flat probe tip geometries for socket pins





Tip	SPEAR		CONICAL		SPHERICAL		CROWN		R-FLAT	
	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu
SEVERITY	2	2	3	3	1	1	2	1	0	0
SCORE	4		6		2		3		0	

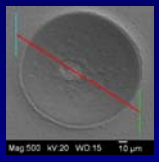
Winners!

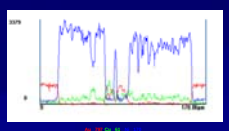


Recap of Results at 0.8mm Pitch

- Gold thickness (.75µm vs 1.27 µm) on PCB pads does not have a significant impact on board longevity
- PCB pad wear can be minimized by:
  - Specifying spherical or radius-flat probe tip geometries for socket pins
  - Insure that socket pin preload is maintained to minimize probe chatter

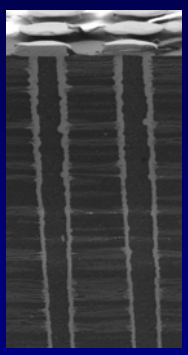
PCB	SCORE
.75 µm Au	17
1.27 µm Au	15

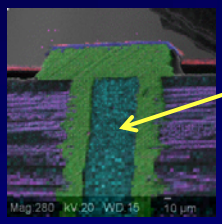




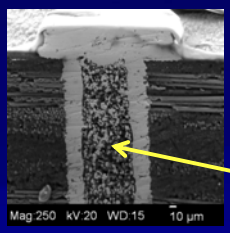
Pad Construction for 0.4mm

- .4mm geometries require socket pads be placed directly over via – Via-in-pad
- Vias are filled with epoxy (conductive or non-conductive), and over plated



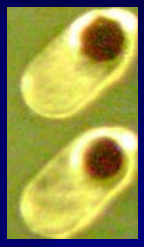


San-ei nonconductive via fill



Tasuda conductive via fill material

Via-in-pad

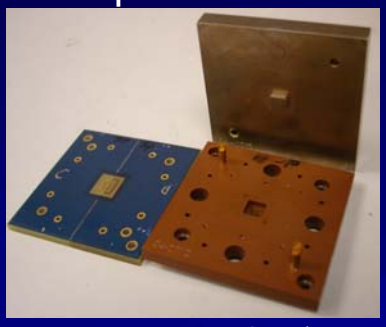


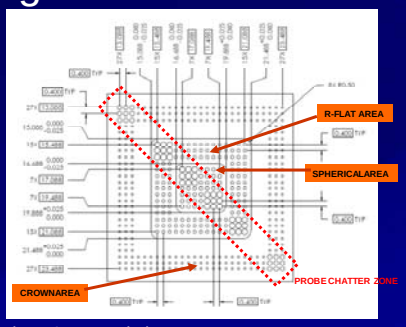
Offset Via

03/2011 PCB Pad Wear Analysis at 0.4mm Pitch 5

Experimental Setup 0.4mm

- Test socket accommodates 3 probe styles:
  - crown tip, radius flat, and spherical
- Socket designed with preload and chatter zone
- Hardened tool steel cycle plate
- PCBs split to run 2 configurations at once





03/2011 PCB Pad Wear Analysis at 0.4mm Pitch 6

Test Methodology

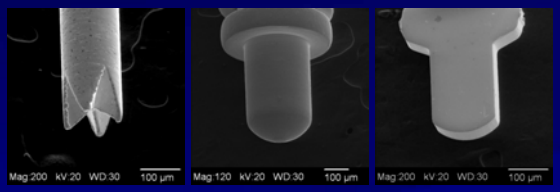
1. New probes loaded in test fixture – tip condition photographed
2. PCB pads optically photographed – new
3. Fixture mounted and cycled to 1 million actuations at ~1Hz
4. Probes replaced at 1 million
5. Cycle to 2 million actuations at ~1Hz
6. PCB pads optically photographed @ 2M
7. SEM analysis: SE images of pads and marks, EDS analysis through marks 2M
8. Scoring and ranking for comparison

Objectives of This Investigation

- Investigate probe tip geometry impact on 0.4mm pad-on-via
- Determine if 1.27µm or 0.75µm gold is required on 'standard' Ni/Au plating process
- Compare via fill types (conductive vs. non-conductive epoxy) and effect on pad wear
- Test non-traditional plating alternatives

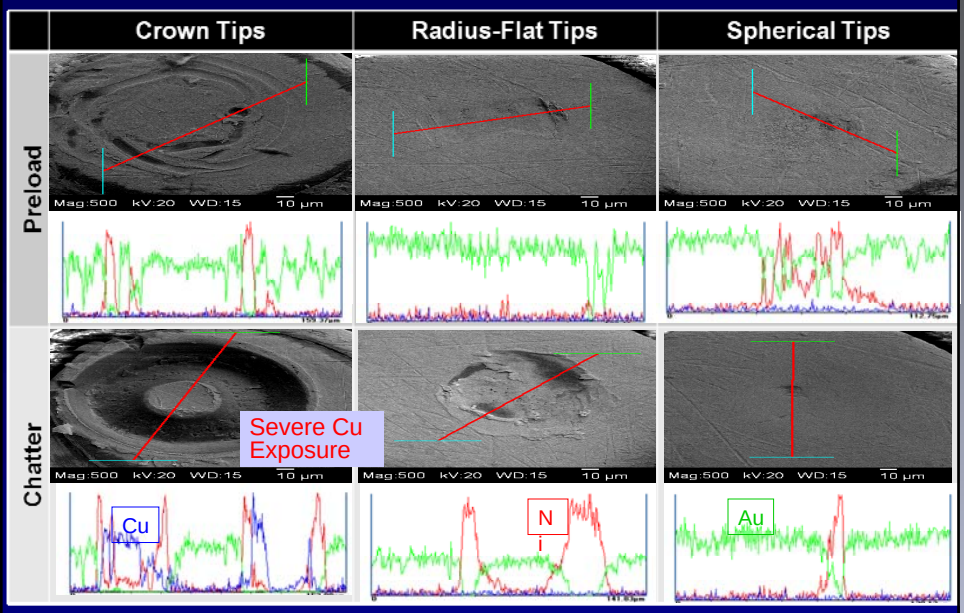
Probe Tips On 0.4mm Pads

- Standard Au/Ni plated PCB pads (1.27 or 0.75 µm Au over 5 µm Ni)
- 3 probe tips: spherical, crown, radius-flat
- 3 probe styles:
  - ECT CSP4 (24g) – double-ended conventional probe
  - ECT BTM040(37g) – machined 2-piece probe – external spring
  - MT MER040(30g) – flat technology probe
- Probes fully preloaded to the PCB and chattering on PCB



CROWN SPHERICAL RADIUS-FLAT

Probe Tip Marks – 7.5µm Ni, 0.5µm Au



Results – Probe Tip Severity Score

- Standard Ni/Au platings – all via-fill types

		Probe Type								
		Crown			Rad-Flat			Spherical		
PCB Plating	Material	Ni	Cu	Visual	Ni	Cu	Visual	Ni	Cu	Visual
Avg Probe Severity	Preload	1.365	0.000	1.946	0.771	0.041	0.858	0.354	0.000	0.286
	Chatter	2.813	0.375	2.583	1.563	0.000	1.624	0.313	0.000	0.583
	Combined	1.871	0.219	2.138	1.016	0.025	1.054	0.331	0.000	0.375
Probe Severity - Total Material Exposure	Preload	0.683			0.406			0.177		
	Chatter	1.594			0.781			0.156		
	Combined	1.045			0.521			0.166		
Total Severity Score Probe (all platings)		1.479			0.772			0.249		

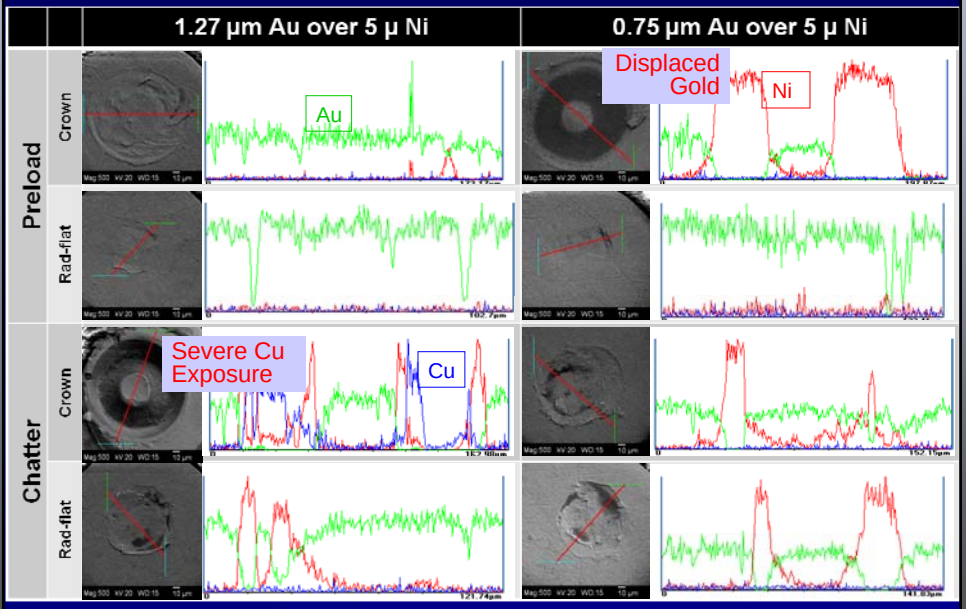
Best

Table Legend (Severity Score):
None (0): No material detected
Slight (1): Traces of exposed material on 10% of pad contact area or less
Moderate (2): Exposed material up to 50% of pad contact area
Severe (3): Exposed material – damaged pads > 50% of contact area

1.27µm vs. 0.75µ Gold Plating

- Standard Au/Ni plated PCB pads (1.27 or 0.75 µm Au over 5 µm Ni)
- 3 probe tips: spherical, crown, radius-flat
- 3 probe styles:
  - ECT CSP4 (24g) – double-ended conventional probe
  - ECT BTM040(37g) – machined 2-piece probe – external spring
  - MT MER040(30g) – flat technology probe
- Fully preloaded to the PCB and chattering on PCB

1.27µm / 0.75µm Au – 5µm Ni



03/2011 PCB Pad Wear Analysis at 0.4mm Pitch 13

Results – 1.27µm/0.75 µm Score

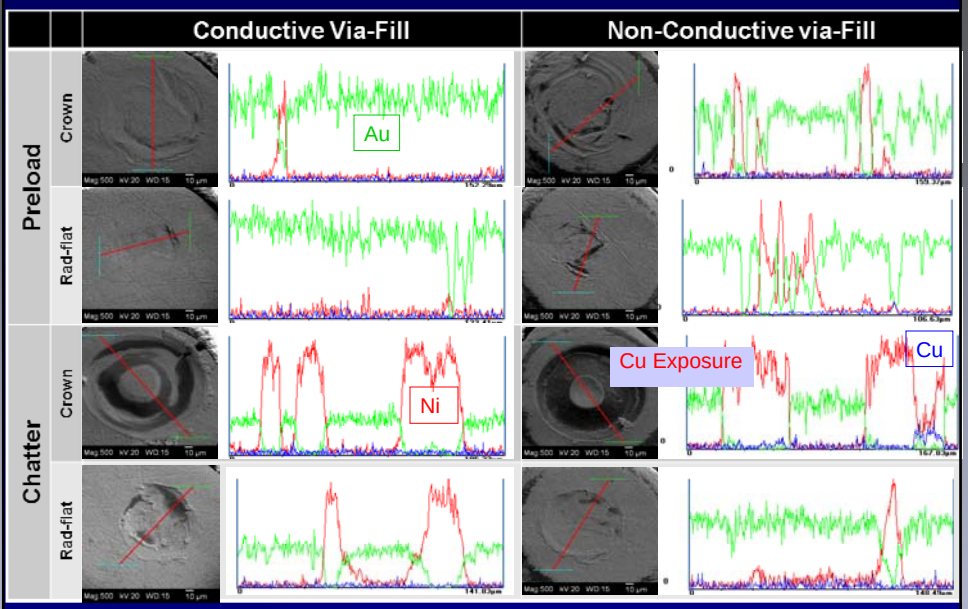
Preloaded in Socket		No Preload - Chatter	
Gold Thickness	Severity Avg Au Thickness	Gold Thickness	Severity Avg Au Thickness
30µin Au (.75 µm)	0.721	30µin Au (.75 µm)	1.143
50µin Au (1.27 µm)	0.528 Marginally better	50µin Au (1.27 µm)	1.046 No better

03/2011 PCB Pad Wear Analysis at 0.4mm Pitch 14

Conductive vs. Non-conductive Via Fill

- Standard Au/Ni plated PCB pads (1.27 or 0.75 µm Au over 5 µm Ni)
- 3 probe tips: spherical, crown, radiused-flat
- 3 probe styles:
  - ECT CSP4 (24g) – double-ended conventional probe
  - ECT BTM040(37g) – machined 2-piece probe – external spring
  - MT MER040(30g) – flat technology probe
- Probes fully preloaded to the PCB and chattering on PCB

Preloaded – .75µm Au CVF vs. NCVF



Results – CVF/NCVF Severity Score

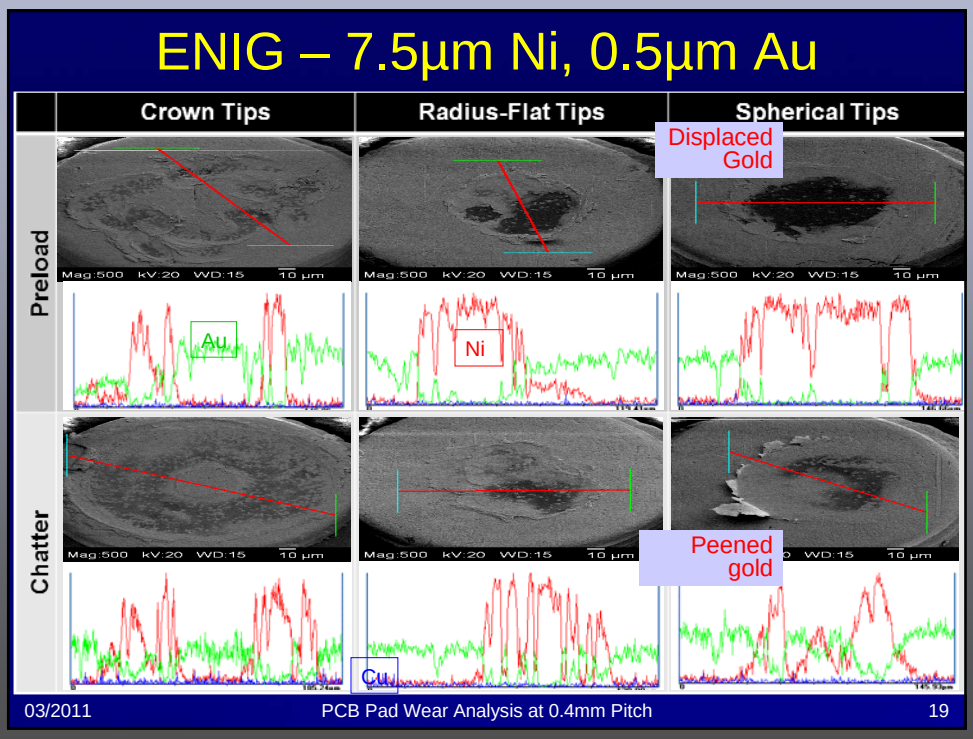
Preloaded in Socket		No Preload - Chatter	
Via Fill Type	Severity Avg VIA FILL	Via Fill Type	Severity Avg VIA FILL
Nonconductive Via Fill	0.695	Nonconductive Via Fill	1.129
Conductive Via Fill	0.554	Conductive Via Fill	1.060

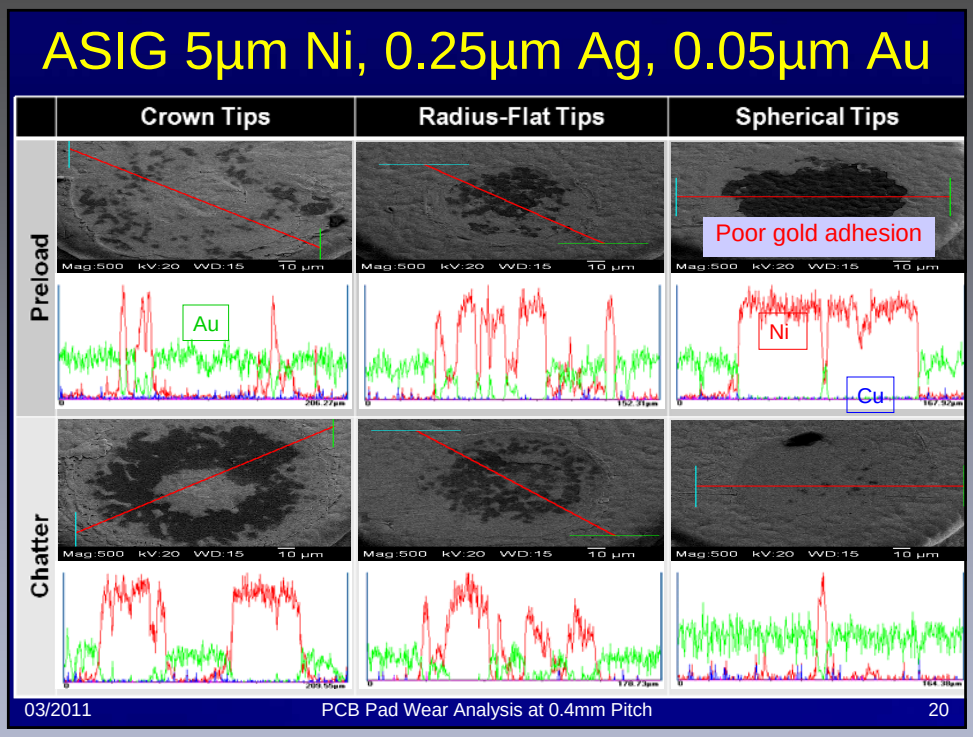
No Difference

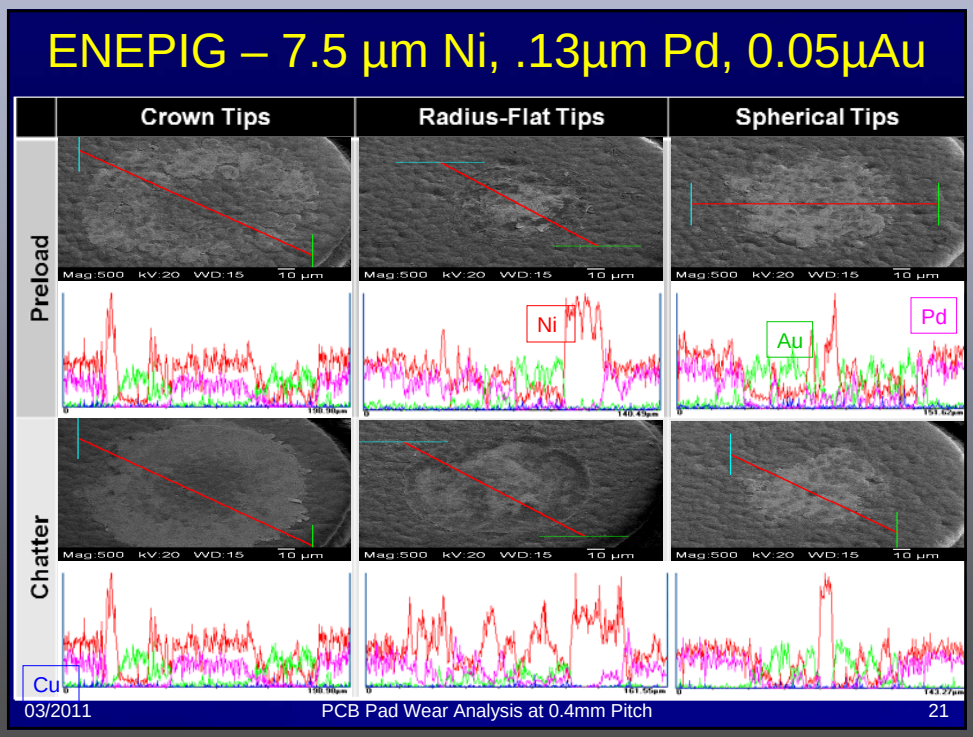
No Difference

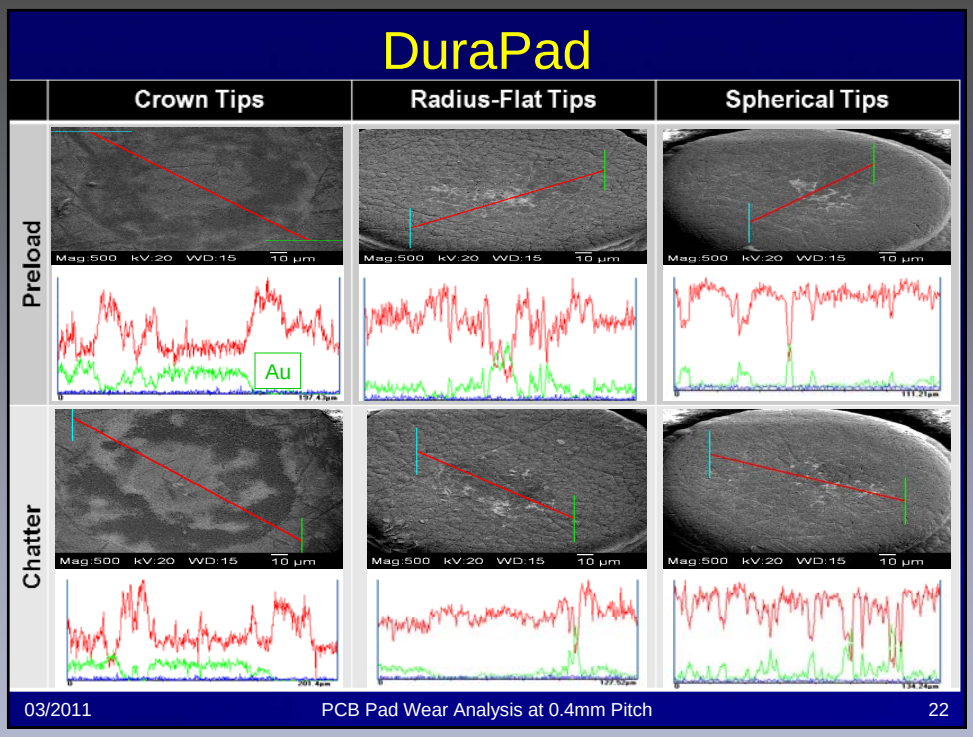
Alternative Plating Formulations

- Pad platings investigated:
  - ENIG – Electroless Nickel, Immersion Gold
  - ASIG – Autocatalytic Silver, Immersion Gold
  - ENEPIG – Elctroless Nickel, Electroless Palladium, Immersion Gold
  - DuraPad – new proprietary formulation
- 3 probe tips: spherical, crown, radiused-flat
- 3 probe styles:
  - ECT CSP4 (24g) – double-ended conventional probe
  - ECT BTM040(37g) – machined 2-piece probe – external spring
  - MT MER040(30g) – flat technology probe
- Probes fully preloaded to the PCB and chattering on PCB


ENIG – 7.5µm Ni, 0.5µm Au
Crown Tips
Radius-Flat Tips
Spherical Tips
Preload
Chatter
Displaced Gold
Peened gold
Au
Ni
Cu
03/2011
PCB Pad Wear Analysis at 0.4mm Pitch
19


ASIG 5µm Ni, 0.25µm Ag, 0.05µm Au
Crown Tips
Radius-Flat Tips
Spherical Tips
Preload
Chatter
Poor gold adhesion
Au
Ni
Cu
03/2011
PCB Pad Wear Analysis at 0.4mm Pitch
20

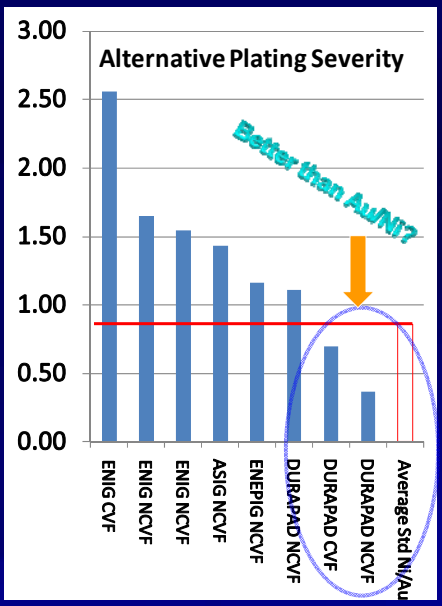

ENEPIG – 7.5 µm Ni, .13µm Pd, 0.05µAu
Crown Tips
Radius-Flat Tips
Spherical Tips
Preload
Chatter
Ni
Au
Pd
Cu
03/2011
PCB Pad Wear Analysis at 0.4mm Pitch
21


DuraPad
Crown Tips
Radius-Flat Tips
Spherical Tips
Preload
Chatter
Au
03/2011
PCB Pad Wear Analysis at 0.4mm Pitch
22

Paper #3
11

Alternative Plating Severity

PCB Plating	COMBINED SEVERITY CHATTER	COMBINED SEVERITY PRELOAD	ALL SEVERITY
DURAPAD CVF	0.703	0.698	0.701
DURAPAD NCVF	0.370	0.370	0.370
ENIG 7.5µNi/0.5µAu CVF	2.649	2.469	2.559
ENIG 7.5µNi/0.5µAu NCVF	1.500	1.594	1.547
DURAPAD NCVF	1.167	1.054	1.111
ASIG 5µNi,.25µAg,.05µAu NCVF	1.370	1.497	1.433
ENEPIG 7.5µNi,.13µPd,.05µAu NCVF	1.278	1.052	1.165
ENIG 7.5µNi/0.5µAu NCVF	1.741	1.556	1.648



Summing It All Up

16 PCBs were cycled to 2M insertions each – 200 EDS analyses and 1000+ SEM/optical images were taken over the course of 1 year

- PCB pad wear can be minimized by:
  - Specifying spherical or radius-flat probe tip geometries for socket pins
  - Insure that socket pin preload is maintained to minimize probe chatter
- There is no significant difference in PCB pad wear whether vias filled with conductive or non-conductive filler
- 1.27µm Au offers no significant advantage for pad life compared to 0.75µm
- Alternate plating formulations used in other electronic applications do not perform better than standard Ni/Au, however, DuraPad shows interesting results and merits further study

Thermal Testing – some tidbits from the lab

James Forster[+] and John Moore*
[+] WELLS-CTI *Texas Instruments

2011 BiTS Workshop
March 6 - 9, 2011

Agenda

- Introduction and background
- Review of past BiTS
- The language of thermal testing
- So what and who cares?
- Experimental issues and difficulties
- Closing comments

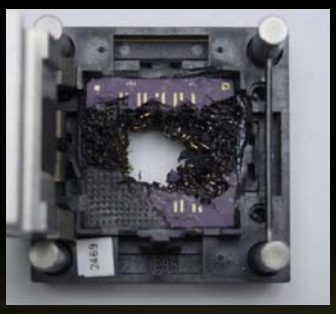
Introduction

- Why are we interested in thermal?
  - Every year engineers develop smaller, more powerful electronics.
  - The drum beat of Moore's Law pushes them to faster, smaller.
  - More power → More heat
  - What does this mean to the burn-in or test engineer?
  - How do we handle it when we are trying to accelerate failures by increasing temperature?

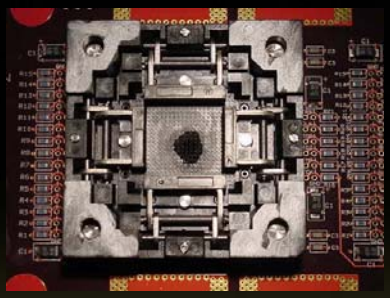
3/2011 Thermal Testing – some tidbits from the lab 3

Introduction

- Sometimes not very well?



From presentation by Mark Miller titled: "Burn-in & Test System for Athlon Microprocessors : Hybrid Burn-in". BiTS 2001



From presentation by James Forster titled "Thermal Testing of Burn-In Sockets" BiTS 2003

3/2011 Thermal Testing – some tidbits from the lab 4

Introduction

- Consumers can buy a variety of 3rd party cooling products to help cool laptops etc

Thermaltake ISGC 200

Notebook Cooler from Antec

Thermaltake Massive23 ST

Sub Zero X1

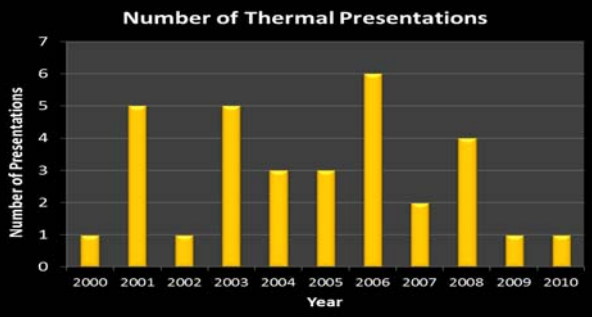
Thermaltake SpinQ VT

- Yet the test professional must heat a device to 125°C+ and control the temperature

Review of Past BiTS

- Thermal management has been a topic at every BiTS workshop.
- The first presentation given at BiTS was titled:-
  "Thermal Management & The Parameters That Affect Heat Dissipation During Burn-in" by Erik Orwoll.
- This is still a good overview of the issues
- Since that time - 29 presentations and 8 sessions dedicated to thermal management.
- Other presentations worthy of mention are include:
  "Burn-in & Test System for Athlon Microprocessors : Hybrid Burn-in", by Mark Miller , BiTS 2001
  "Socket and Heat Sink Considerations in High Power Burn-In" by John McElreath, BiTS 2007.

Thermal Presentations



- Thermal management is of interest.
- There is a challenge!
- ITRS projection for 14nm node is:-
  - Power density of 100W/cm2
  - Junction to ambient thermal resistance <0.2 degC/watt

3/2011 Thermal Testing – some tidbits from the lab 7

The Language of Thermal Testing

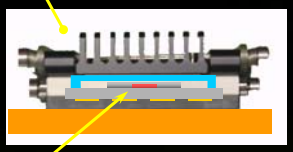
- The basic physics of heat transfer :
  - Conduction
  - Convection, forced and natural
- Flow rates of air in LFM or m/s
- Junction temperature
- Theta j-a – Thermal resistance.
- Temperature diode
- Passive thermal control
- ATC – Active thermal control
- TCU – Thermal Control Unit
- TIM – Thermal Interface Material

3/2011 Thermal Testing – some tidbits from the lab 8

The Language of Thermal Testing

- **Thermal resistance which is a simple ratio.**

$T_{(Ambient)}$ Temp of air



$T_{(Junction)}$ Temp of Die

- **It is defined as:**

$$\theta ja = \frac{T1 - T2}{Power}$$

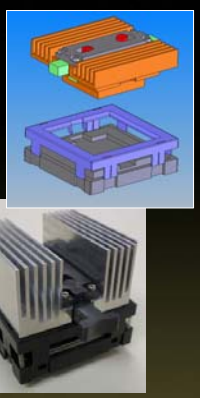
- **There are a number of thermal resistances**
  - **Theta j-a (θ_{ja}) junction to ambient**
  - **Theta j-c (θ_{jc}) junction to case**
  - **Theta c-a (θ_{ca}) case to ambient**
  - **Theta j-b (θ_{jb}) junction to board.**

3/2011 Thermal Testing – some tidbits from the lab 9

The Language - Passive Thermal Control

- **Add a heat sink to a socket**
- **Reduces Theta ja - therefore the junction temperature**

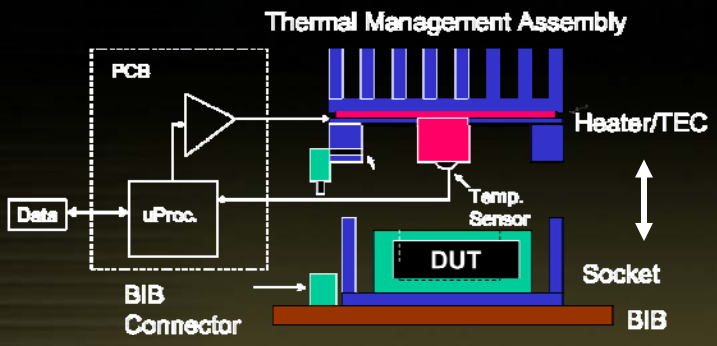
Some early solutions



3/2011 Thermal Testing – some tidbits from the lab 10

The Language - Active Thermal Control

- Introduced in 1999 Active Thermal Control is the process where the temperature of each DUT is monitored and controlled.
- ATC establishes "micro-environments" with local heating to control the temperature of each DUT



3/2011 Thermal Testing – some tidbits from the lab 11

Active Thermal Control

- Available as a rack or as a single site, with or without integrated cooling.
- A variety of different ATC sockets and racks

3/2011 Thermal Testing – some tidbits from the lab 12

The Use of Thermal Resistance (θja)

- All devices have a range of powers.
- John McElreath at BiTS in 2007 stated:-
  - Device power +/- 40%
  - Oven airflow +/- 30%
- How does that impact test or burn-in?
- Does it matter?
- Example:- A 3 watt device is +/- 1 watt
  - Thermal resistance is 21.0°C/Watt
  - What is the oven ambient for a junction temperature of 140°C?

$$\theta ja\ (21) = \frac{Tj\ (140) - Ta\ (Oven)}{Power\ (3)} \quad So \quad Ta\ (oven) = 77°C$$

BUT .....

- Some devices are 2 watts and some are 4. With an oven temperature of 78°C the junction temperatures of these devices will be different.
- Using the formula for θja we calculate that the junction temperature s will be:-

Oven temp 77 °C θja = 21 °C/watt	Power (Watts)		
	2	3	4
T Junction (°C)	119	140	161
Delta to nominal	-21	0	21

What If? Passive Thermal Control…….

- If we add a heat sink θja for the package will be reduced to 5 °C/watt
- For a 3 watt device and a junction temperature of 140°C we can calculate the air temperature should be: 125°C
- For the other devices at 2 and 4 watts the junction temperature will be:-

Oven temp 125 °C θja = 5	Power (Watts)		
	2	3	4
T Junction (°C)	135	140	145
Delta to nominal	-5	0	5

Impact of Passive Thermal Control

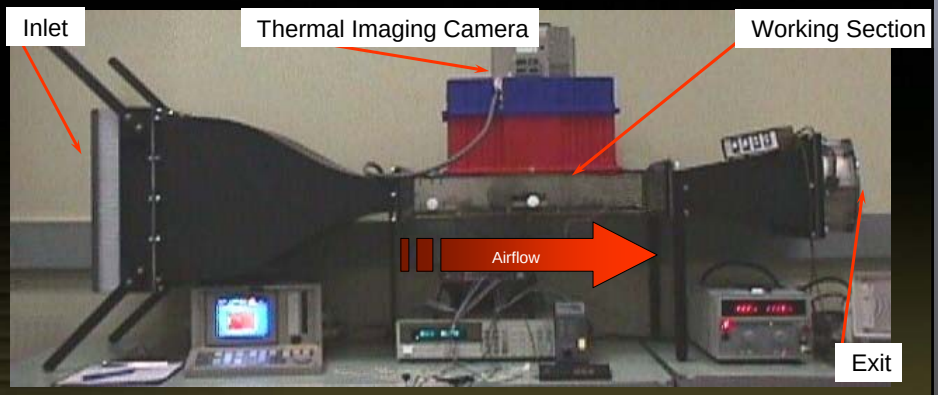
- The heat sink reduces the thermal resistance and the range of junction temperatures variation is significantly reduced.

Power (Watts)	T Junction (°C)	
	No heat sink θja = 21	With Heat sink θja = 5
2	119	135
3	140	140
4	161	145
Delta to Nom.	+/- 21	+/-5

- Controlling the junction temperature allows controlled burn-in and can help reduce the chance of thermal runaway.

Introduction - Experimental Work

A wind tunnel helps standardize the test conditions and examine the effect and impact of different airflows.

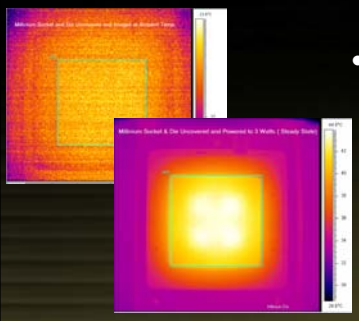


3/2011 Thermal Testing – some tidbits from the lab 17

Introduction – Experimental Work

Socket

- **A thermal imaging camera allowed non-contact temperature measurements. thermal test package.**
- **More importantly the thermal images revealed subtle changes which would not have been apparent**

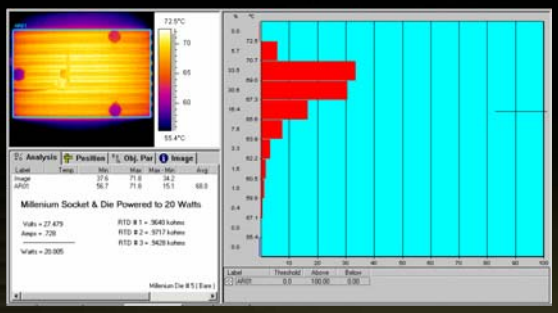


Thermal image

3/2011 Thermal Testing – some tidbits from the lab 18

Introduction – Experimental Work

- Thermal imaging indicates the temperature distribution and provides an idea of uniformity.



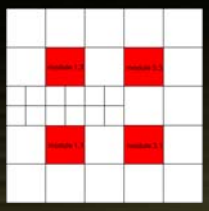
Temperature of heat sink uniform.

Histogram reveals 85% of heat sink between 60 and 62.6°C

Introduction - Experimental Work

Lidded

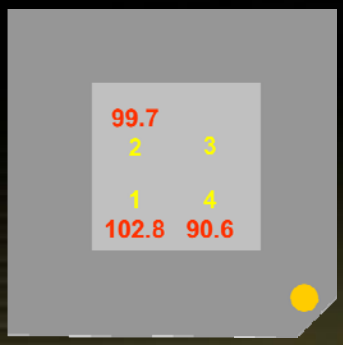
Bare die



- Experimental work involved detailed testing of a ceramic LGA thermal test packages.
- The thermal test die had multiple zones with heaters and diodes allowing the measurement of junction temperature at different locations.

Using Thermal Test Die

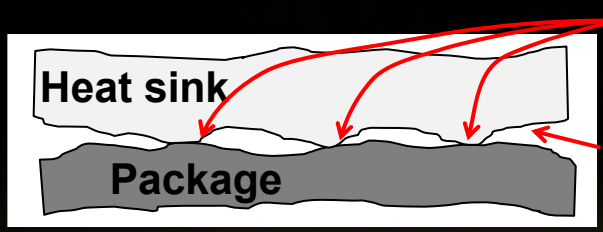
- The ability to monitor temperature in the die using a thermal diode provides data and insights not immediately obvious.



- Results of die temperatures for a test at 40 watts and 650 LFM
- Tests at other powers mimicked the temperature distribution.
- Positions 1 and 2 were always hotter….. Why?

Interface Resistance

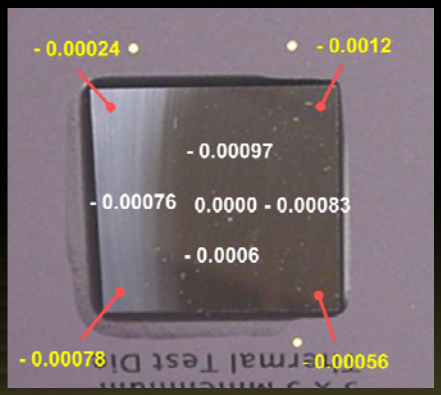
- The mating surface between a heat sink and a package is an important interface for heat transfer.



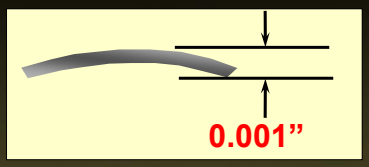
- Thermal Interface Materials or TIM's do not work well in burn-in applications due to high temperatures and, repeated cycling .

Regardless - Things Are Not Flat

- Extensive efforts are spent to improve surface finish but …… The die is not flat



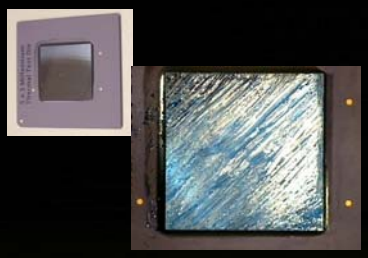
- The flatness of a die was measured at 9 points
- "0" is the datum.
- Height above the plane is +'ve



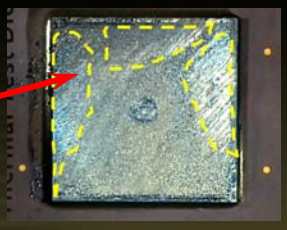
3/2011 Thermal Testing – some tidbits from the lab 23

The Real Contact Surface.

- Ink smear test on bare die



- Ink smeared on the top of the die and documented



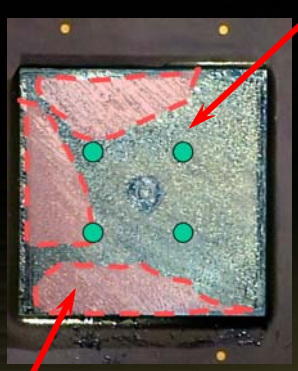
- Socket actuated.
- Heat sink contacts die.
- Smear pattern reveals contact areas.

3/2011 Thermal Testing – some tidbits from the lab 24

The Impact.

- Poor contact results in local heating of the die

Approximate position of temp sensor



Non Contact Area

Temperature distribution on die

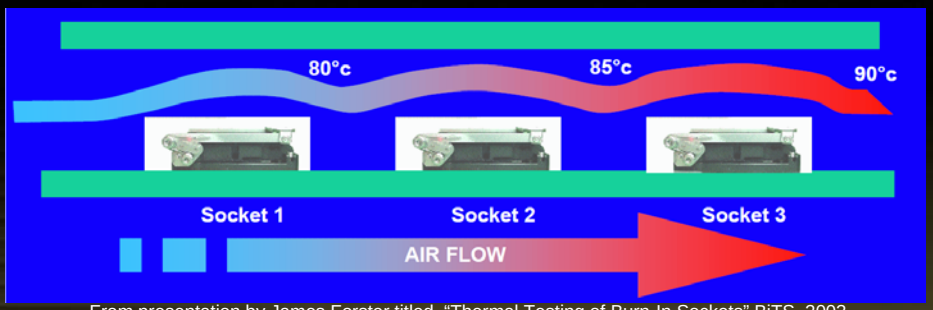
Impact of Interface Resistance

- Several tests were run with a dry interface between the package and the heat sink.
- Some experiments were also run with thermal grease to attempt to measure the resistance of the interface .
- The results indicate the thermal resistance of a dry interface is 0.2°C/watt

Airflow (Wind Tunnel)	250 LFM					
Power (Watts)	10	20	30	40		
Interface	Dry	Dry	Dry	Dry		
θja	2.1	2.1	2.1	2.1		
Airflow (Wind Tunnel)	650 LFM					
Power (Watts)	10	20	30	40	40	50
Interface	Dry	Dry	Dry	Dry	TG	TG
θja	2.0	2.0	2.0	2.0	1.8	1.8

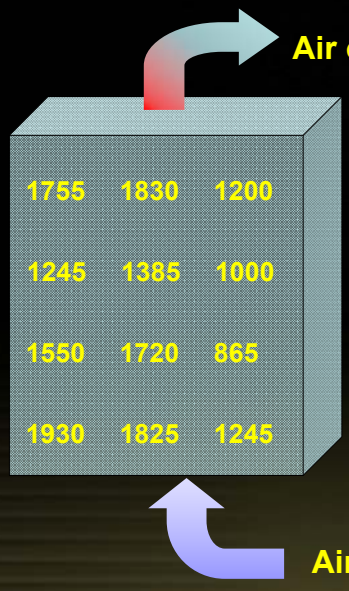
Temperature Uniformity

- The temperature of the airflow can also vary due to indirect heating.
- This graphic from 2003 shows a 10°C variation in the ambient air.
- Each device experiences a different burn-in environment.



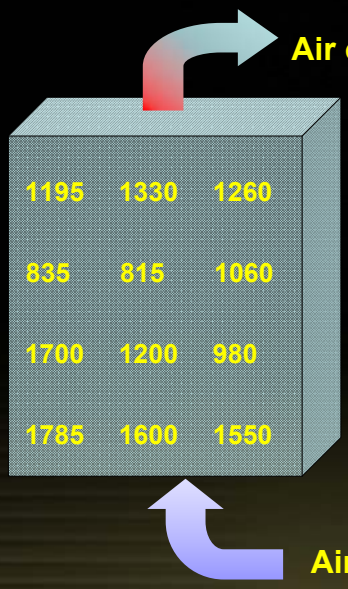
From presentation by James Forster titled "Thermal Testing of Burn-In Sockets" BiTS 2003

Airflow



- The airflow variation in an oven can be significant.
- This data, from a commercial operation, shows the variation
- Max. 1930 LFM
- Min. 865 LFM
- Variation +/- 50% of average.

Airflow

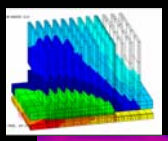
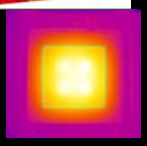


- The airflow is also very dependent on the oven loading
- The oven, shown in the previous slide, was partially loaded.
- Max. 1785 LFM
- Min. 815 LFM
- Variation again +/- 50% of average. But the distribution is very different.

Conclusions & Closing Comments

- Use the thermal test die whenever possible.
- Even though silicon is a good conductor temperature distributions on the die should be anticipated.
- Use thermal cameras and thermal images to describe temperature profiles and validate thermal models.
- Be aware that die and packages are not flat.
- Examine the impact of airflow – the oven/chamber is not uniform.

Conclusions & Closing Comments

- Thermal management is complex.
- There are many variables but it is a science.
- There is a language which must be learned to allow efficient communication
- Increasing DUT power will require innovative solutions in test.
- Engineers will have to consider how to handle Moore power.

Final Thought

So what temperature are you actually testing at?