BiTS™ Burn-in & Test Socket Workshop 2011

Session 3

ARCHIVE 2011

GET ON BOARD!

Optimizing the Motherboard for High Speed Signal Propagation
Mustapha Abdulai, Erkan Acar, Anbinh Nguyen—Intel Corporation

HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
Harsha Reddy—Gorilla Circuits

Embedded Thin-Film NiP Resistors in Burn-In Trays
Bruce Mahler—Ohmega Technologies, Inc.

Benefits & Risks of High Aspect Ratio Vias in ATE Boards
Christopher Cuda—Multitest

Optimizing the Motherboard for High Speed Signal Propagation

Mustapha Abdulai, Erkan Acar and Anbinh Nguyen
Intel Corporation

2011 BiTS Workshop
March 6 - 9, 2011

Agenda

- Motivation
- Sources of signal degradation on system boards
- Mitigation Options
- Simulation Results
- Measured Results
- Conclusion
- Acknowledgement

Motivation

Higher signal speeds on current and next generation system buses are exposing the limits of existing test systems

Addition of test features makes the test platforms have significantly worse margins when compared with the end-use systems

Can recoup most of the system margin @ 5GT/s
- with minimal re-design effort
- small cost increases

Motivation

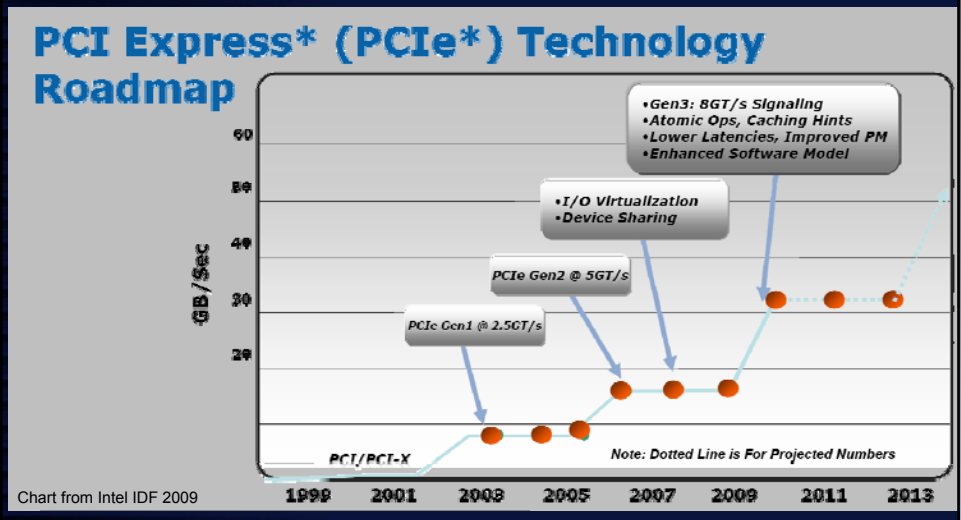
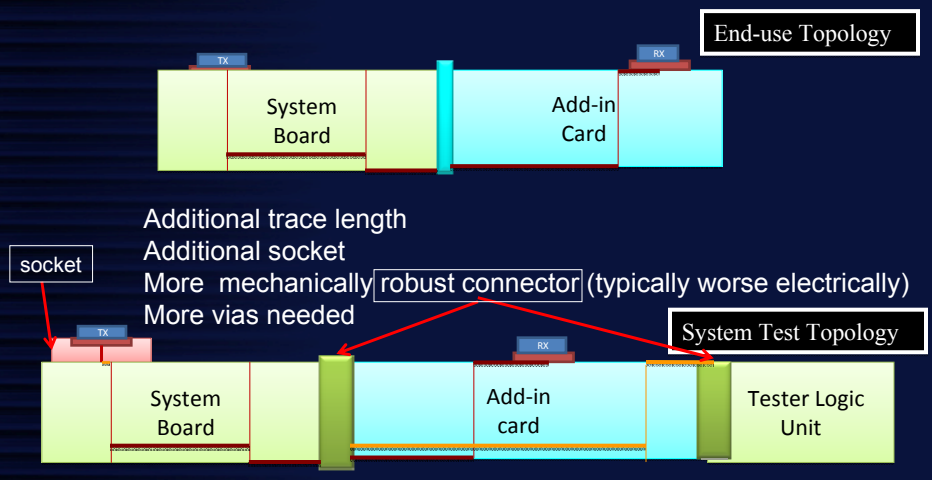


Chart from Intel IDF 2009

*based on X16 Channel

Topology of a typical System Board



3/2011 Optimizing the Motherboard for High Speed Signal Propagation 5

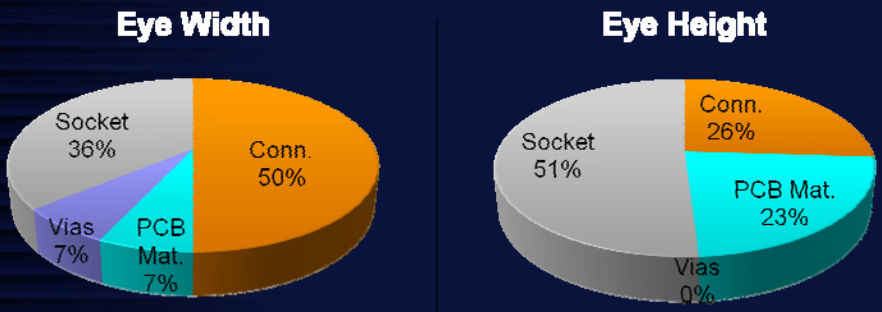
Major Causes of Signal Degradation on System Boards

- Impedance discontinuities due to
  - PCB manufacturing tolerances
  - Vias and Pins
  - Component tolerances
- Cross talk
- Copper loss due to
  - Finite electrical conductivity of Copper
  - Surface roughness of Copper
- Dielectric loss due to
  - Non-unity and frequency-dependant dielectric permittivity of FR4 or other PCB material

3/2011 Optimizing the Motherboard for High Speed Signal Propagation 6

PCIe2 margin degradation on test vs. end-use platform

Contribution of the major test fixtures on the additional signal degradation seen on test platforms as compared to end-use platforms



3/2011 Optimizing the Motherboard for High Speed Signal Propagation 7

Different PCB Dielectric

FR4 can be replaced with either Nelco-13SI or Rogers 4350 material.

Nelco-13SI does not require PCB vendors to make drastic process changes

Board assembly houses can reuse their existing equipment with the same reflow and soldering profiles

Property	FR4	Rogers 4350	Nelco-13SI
Relative Permittivity (Er)	4.4	3.6	3.4
Loss Tangent (TanD)	0.02	0.004	0.01

3/2011 Optimizing the Motherboard for High Speed Signal Propagation 8

FR4 to Nelco Design issues

Converting an existing CAD design from FR4 to Nelco involves

- –changing differential pair trace spacing to maintain impedance
- –moving ground planes closer to signal planes
- –making core thicker to maintain same board thickness

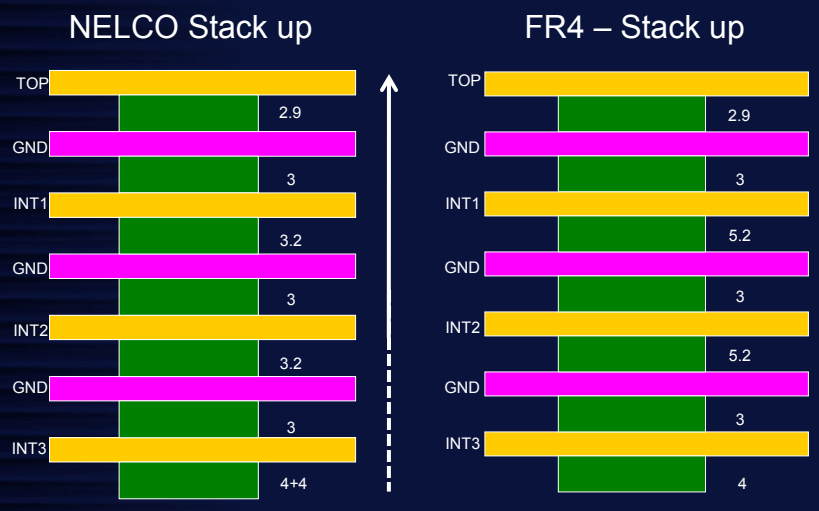
*80 ohm diff	trace width (mils)	trace spacing (mil)
FR4	4.00	5
Nelco	3.75	7

*45 ohm SE	trace width (mils)
FR4	4.0
Nelco	3.4

*stripline

3/2011 Optimizing the Motherboard for High Speed Signal Propagation 9

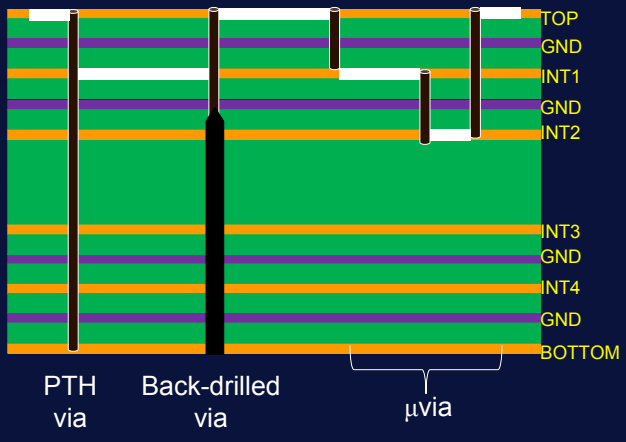
FR4 to Nelco Stack up changes



3/2011 Optimizing the Motherboard for High Speed Signal Propagation 10

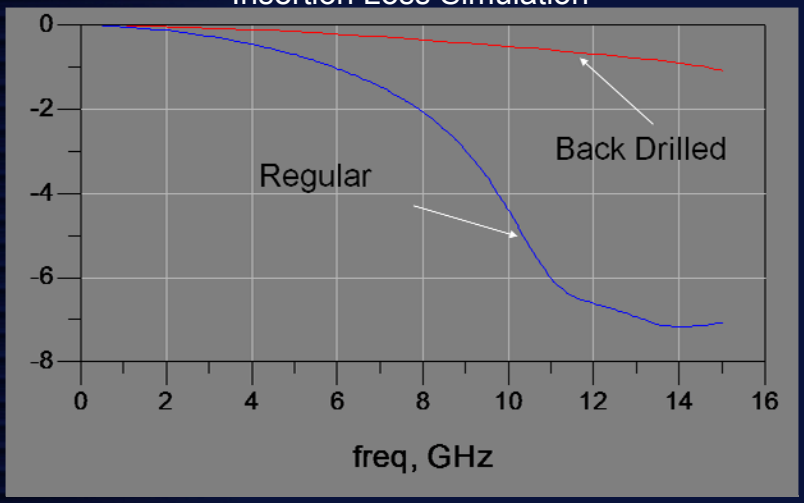
Via Options

- **PTH**
  - Top layer to bottom layer
- **Back drilling**
  - top layer to bottom layer, then stub mechanically drilled
- **µVia (blind and buried)**
  - Via going only between connecting layer



Via Options

Insertion Loss Simulation

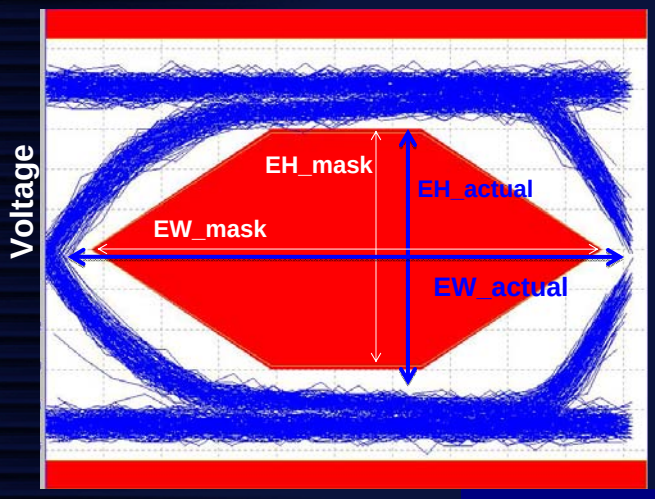


Via Design issues

Converting an existing CAD design from PTH to back-drilled via involves
- –Putting a "FAB note" in the CAD file
- –Making sure the PCB vendor has this capability
- –Re-running the DRC check to account for the Keep-Out-Zone of the drill

Converting an existing CAD design from PTH to µVia involves
- –Replacing all the PTH vias with µVia
- –Making sure the PCB vendor has this capability

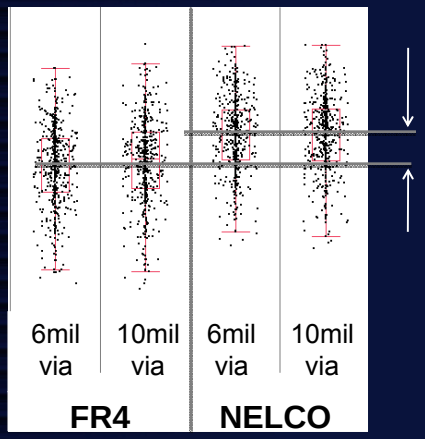
Definition of analysis metric



All measured or simulated bits are overlaid, then compared with the eye mask which is generated from the spec

EH_actual – EH_mask = V_margin
EW_actual – EW_mask = T_margin

Simulation Results Single Ended Bus

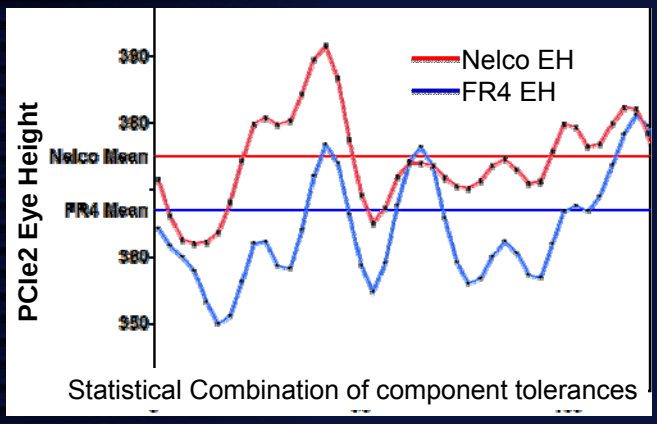


18% average improvement

Worst Case improvement

	Low 95% EH margin
FR4, back-drilling	37mV
Nelco, back-drilling	78mV

Simulated Results showing impact of PCB material on PCIe2 routing

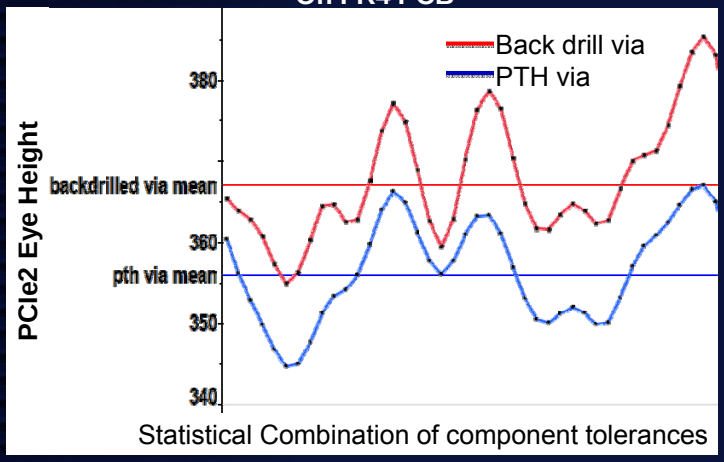


Each case (x-axis) represent a unique combination of trace impedances, trace lengths, and component parameters within the manufacturing tolerance

In almost all cases the Nelco Board has a higher response that the FR4 board

Simulated Results showing impact of PTH vs. back drilled vias

On FR4 PCB

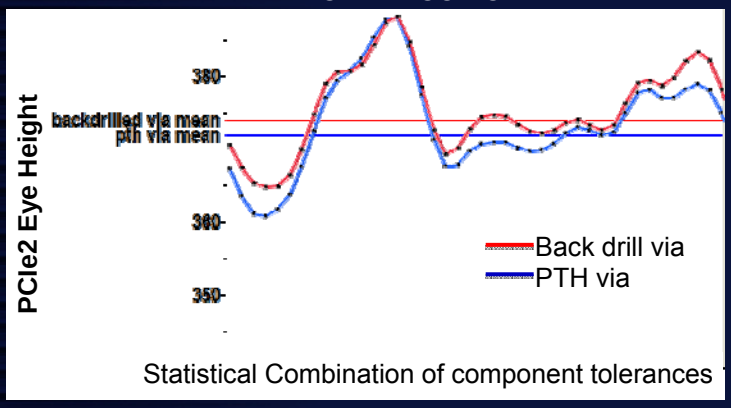


Back drilling improves the margins significantly on the FR4 boards

3/2011 Optimizing the Motherboard for High Speed Signal Propagation 17

Simulated Results showing impact of PTH vs. back drilled vias

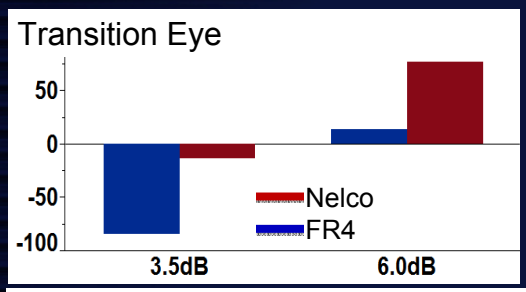
On NELCO PCB

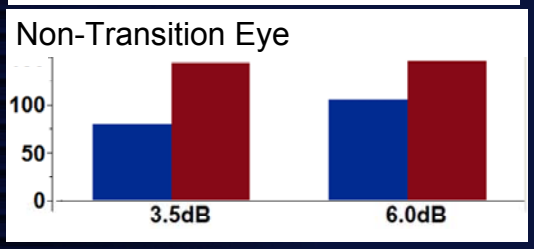


No significant improvement is seen with back drilling on the Nelco board

3/2011 Optimizing the Motherboard for High Speed Signal Propagation 18

Measured Results
PCISIG PCIe2 Compliance setup

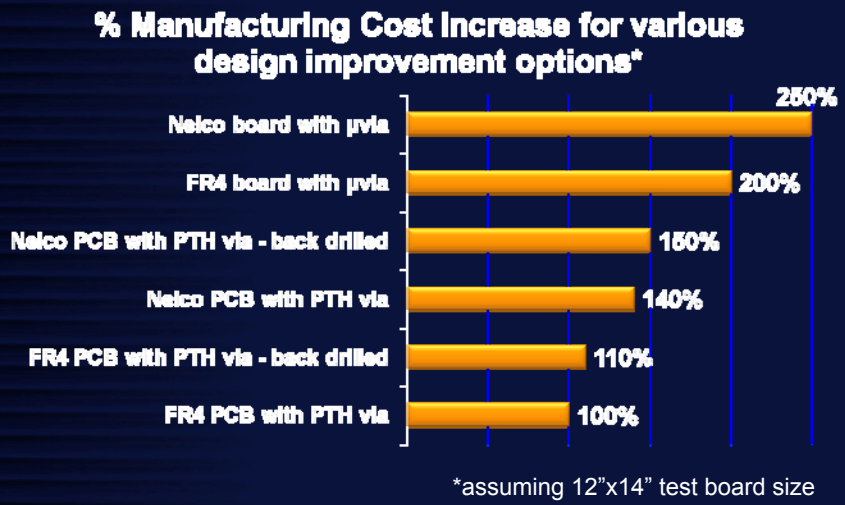




Measurement on a system board taped out in both FR4 and Nelco (both with PTH vias) show that the PCIe2 margin can be improved by

- average of 70mV for -3.5dB equalized channels (normally used for short channels under 10") and
- average of 50mV for -6.0dB equalized channels (normally used for longer channels).

Cost implications



*assuming 12"x14" test board size

Conclusion

We can recoup significant margin by making only PCB changes @ 5GT/s, higher speeds will require more changes

Cost of changes should decrease with continued adoption of HDI manufacturing techniques

Component manufactures should continue to improve the SI performance of test fixtures (sockets, connectors, etc)

Design tools need to be developed to easily convert existing designs

Acknowledgements

Beng Siong Ho

Rudy Setyawan

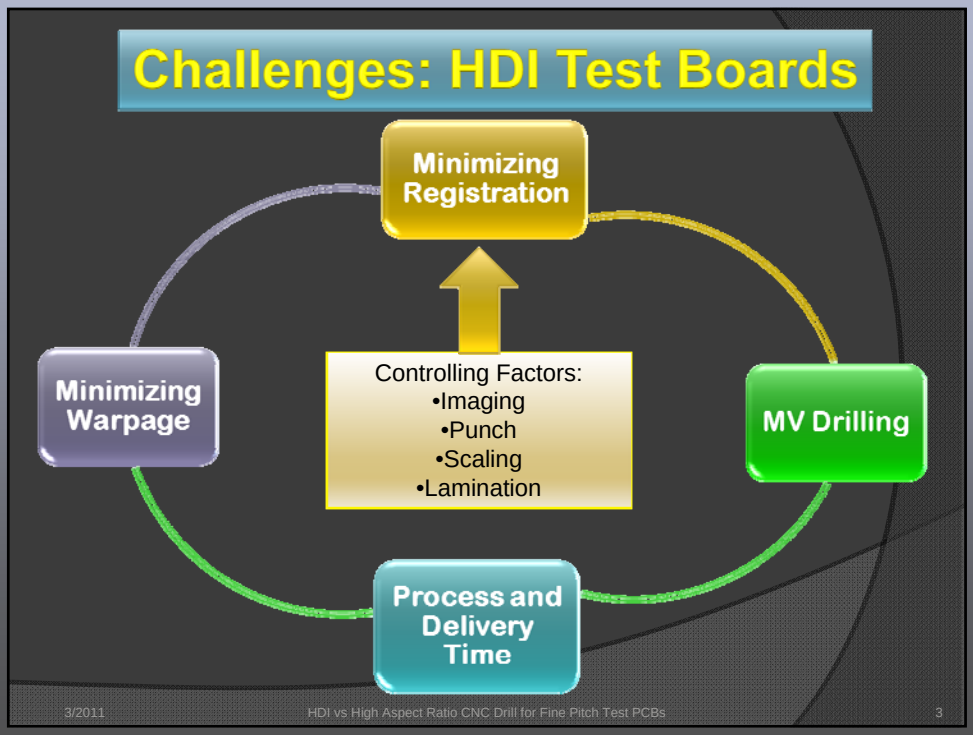
HDI VS HIGH ASPECT RATIO CNC DRILL FOR FINE PITCH TEST PCBS

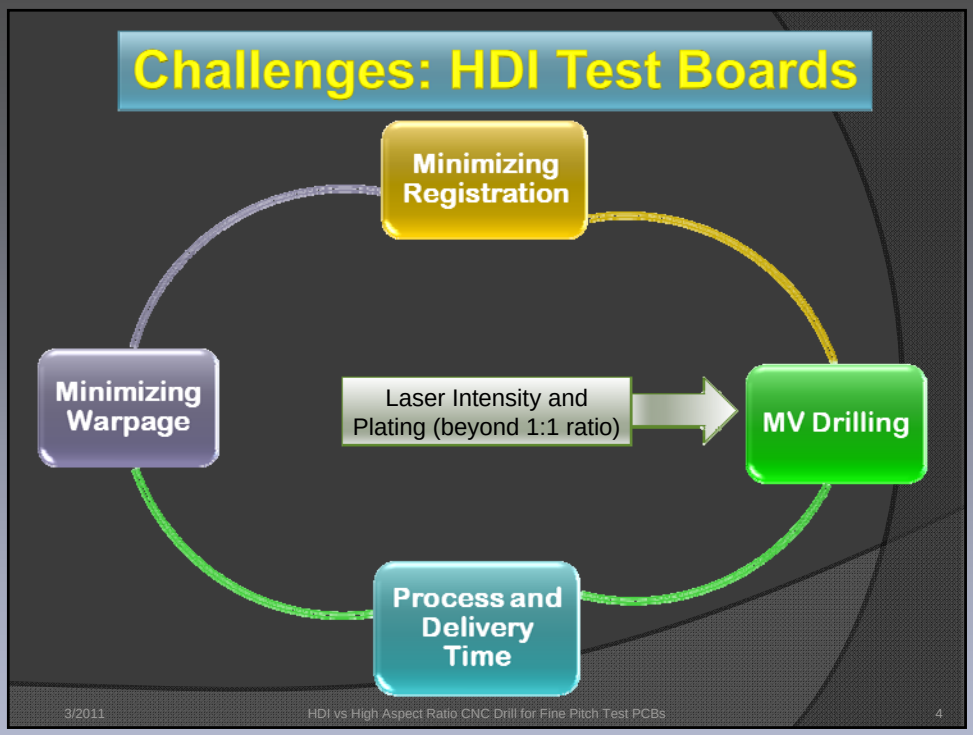
Harsha Reddy
Gorilla Circuits Inc.

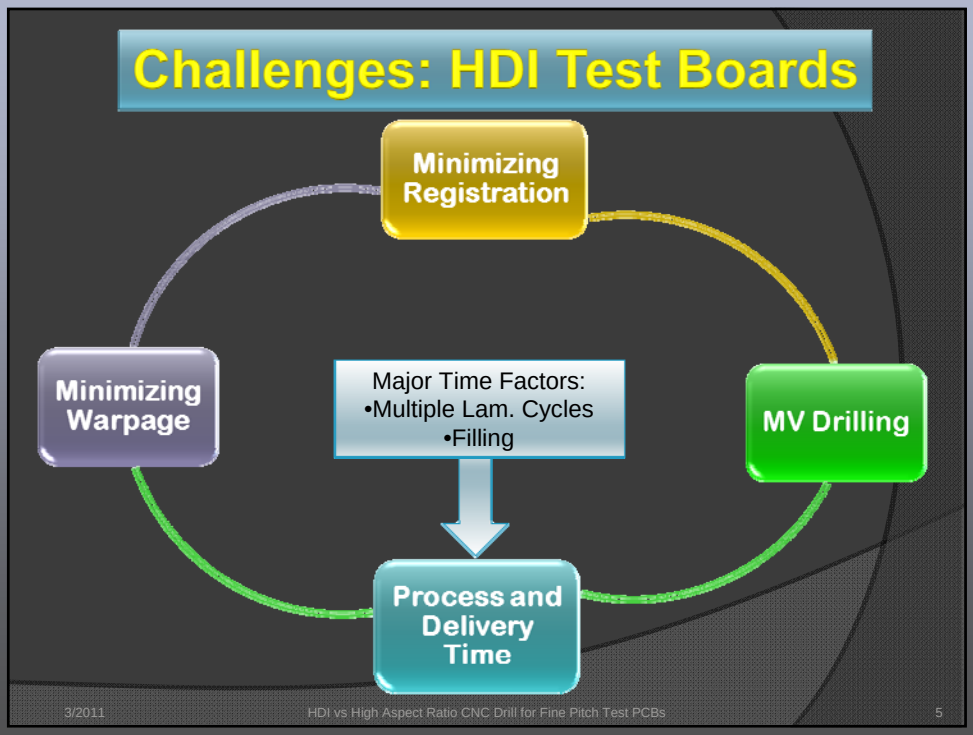
2011 BiTS Workshop
March 6 - 9, 2011

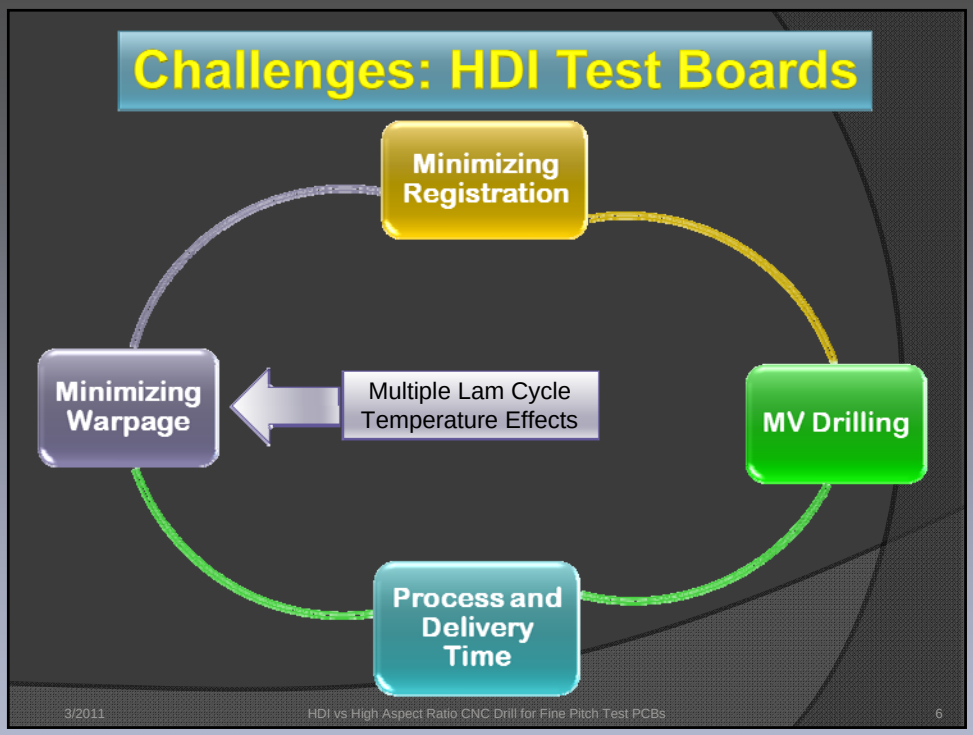
AGENDA

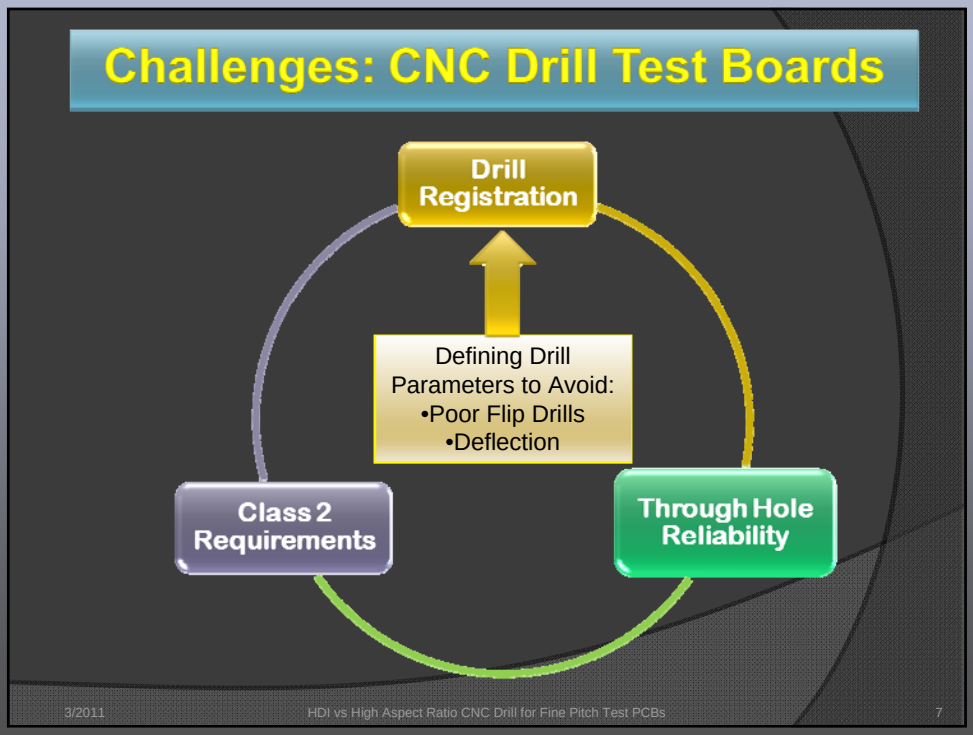
- Challenges with HDI Test boards
- Challenges with High Aspect Ratio CNC drill Test boards
- Cost and lead-time comparisons
- First Pass Yield comparisons
- High Aspect Ratio CNC drill Test Board experience and examples with definitions and measurements
- HDI ATE Test board experience and examples with definitions and measurements
- Technical Road Map
- Pitch Designs
- 2010 Equipment
- Summary of Pros and Cons in manufacturing
- Overall Summary

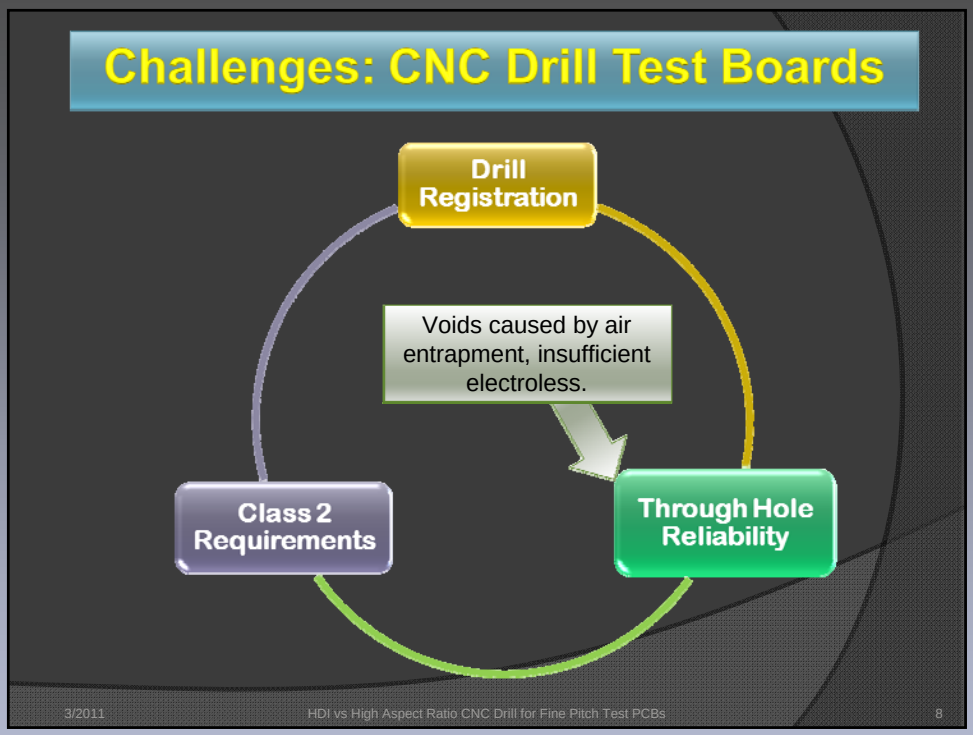

Challenges: HDI Test Boards
Minimizing Registration
Minimizing Warpage
Controlling Factors:
•Imaging
•Punch
•Scaling
•Lamination
MV Drilling
Process and Delivery Time
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
3


Challenges: HDI Test Boards
Minimizing Registration
Minimizing Warpage
Laser Intensity and Plating (beyond 1:1 ratio)
MV Drilling
Process and Delivery Time
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
4

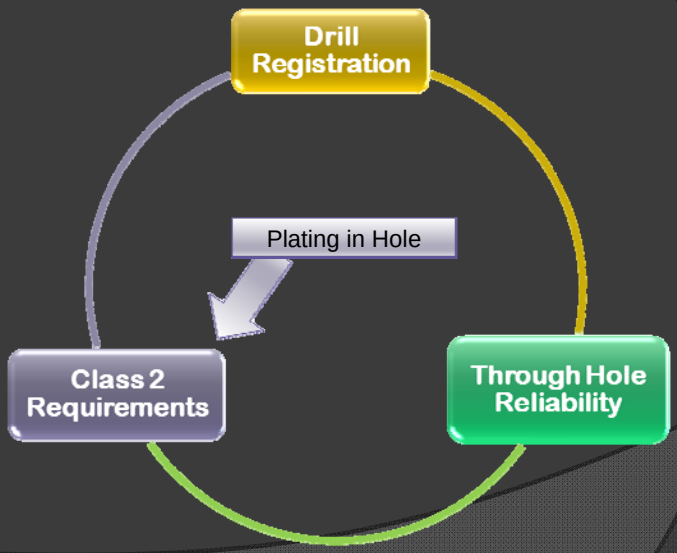

Challenges: HDI Test Boards
Minimizing Registration
Minimizing Warpage
Major Time Factors:
•Multiple Lam. Cycles
•Filling
MV Drilling
Process and Delivery Time
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
5


Challenges: HDI Test Boards
Minimizing Registration
Minimizing Warpage
Multiple Lam Cycle Temperature Effects
MV Drilling
Process and Delivery Time
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
6


Challenges: CNC Drill Test Boards
Drill Registration
Defining Drill Parameters to Avoid:
•Poor Flip Drills
•Deflection
Class 2 Requirements
Through Hole Reliability
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
7


Challenges: CNC Drill Test Boards
Drill Registration
Voids caused by air entrapment, insufficient electroless.
Class 2 Requirements
Through Hole Reliability
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
8

Challenges: CNC Drill Test Boards



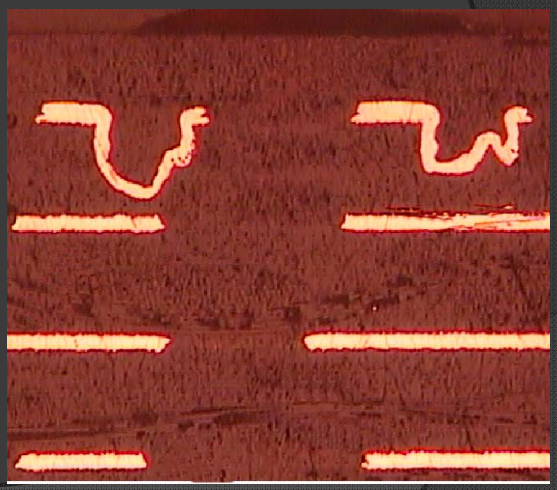
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 9

Challenges: HDI Test Boards

Shallow Micro Vias

Caused By:

Insufficient Laser Intensity



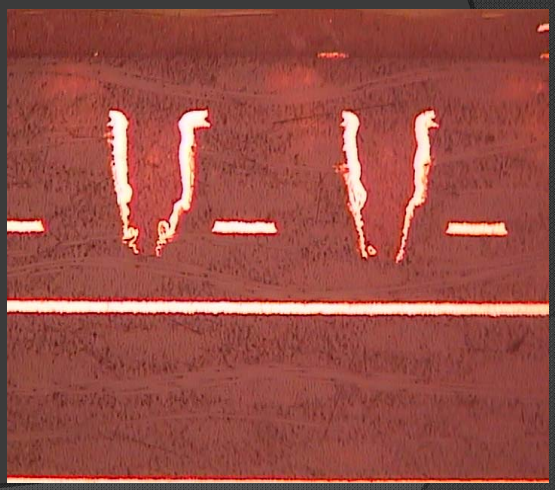
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 10

Challenges: HDI Test Boards

Poor Registration

Caused By:

- Shift in inner layers
- Wrong scale factors
- Drill Misfire



3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 11

Challenges: HDI Test Boards

VOID

Caused By:

- No electroless Copper Coverage due to exceeding 1:1 aspect ratio

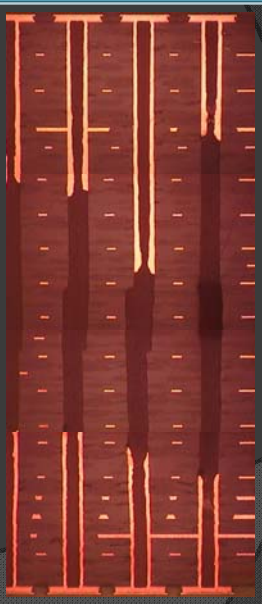
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 12

Challenges: CNC Drill Test Boards

VOIDs

Caused By:

- Air entrapment during electroless copper process
- Insufficient nickel coverage prior to the etch process
- Poor flip drill registration and overall drill quality



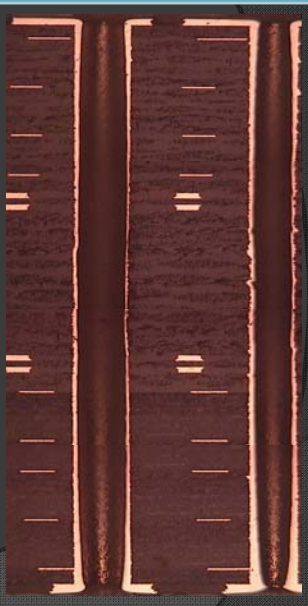
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 13

Challenges: CNC Drill Test Boards

SHORTS (Poor Registration)

Caused By:

- Inner layer image shift
- Shifts in the post etch punch
- Lamination
- Wrong scale factors
- Drill mis-registration



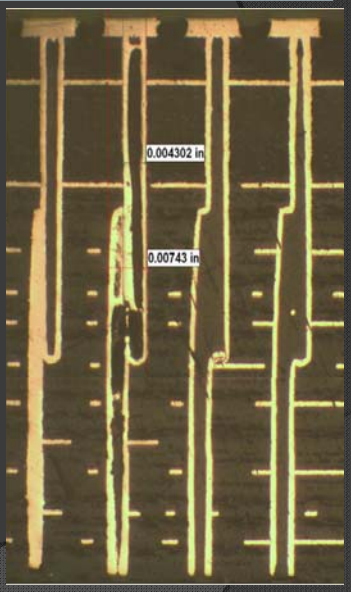
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 14

Challenges: CNC Drill Test Boards

SHORTS (Poor Registration)

Caused By:

- Inner layer image shift
- Shifts in the post etch punch
- Lamination
- Wrong scale factors
- Drill mis-registration



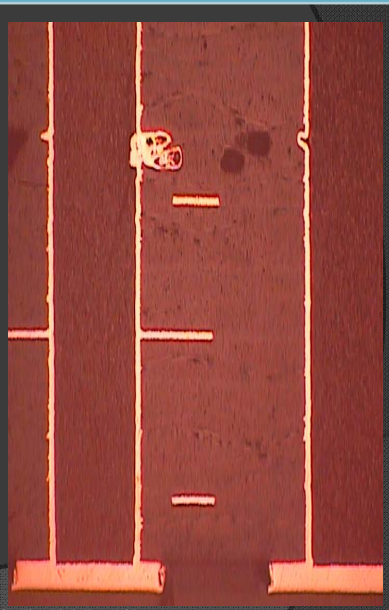
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 15

Challenges: CNC Drill Test Boards

SHORTS (Other)

Caused By:

- Delamination
  - Copper plating in delaminated areas



3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 16

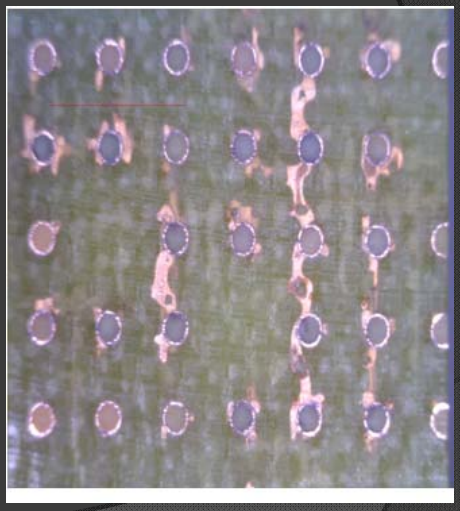
Challenges: CNC Drill Test Boards

SHORTS (Other)

Caused By:

- Delamination
  - Copper plating in delaminated areas

Surface View

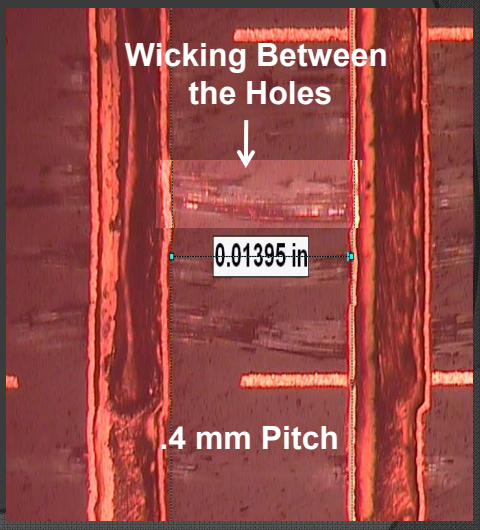


Challenges: CNC Drill Test Boards

SHORTS (Other)

Caused By:

- Delamination
  - Copper plating in delaminated areas
- Wicking
  - Drilling fractures material allowing copper to connect two holes



Challenges: CNC Drill Test Boards

SHORTS (Other)

Caused By:

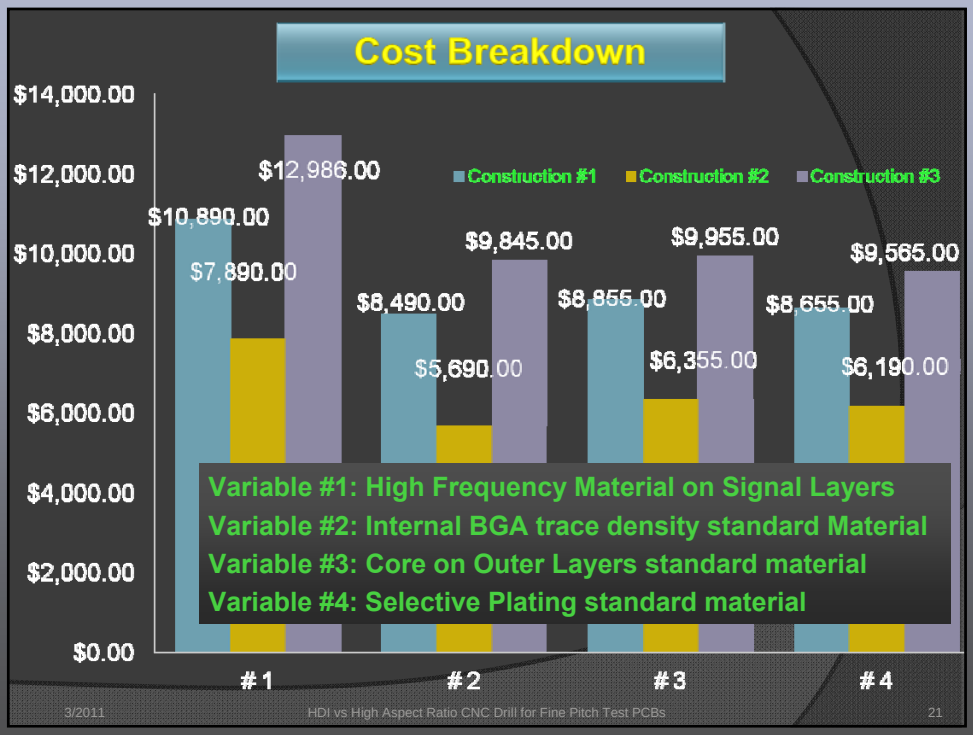
- Delamination
  - Copper plating in delaminated areas
- Wicking
  - Drilling fractures material allowing copper to connect two holes

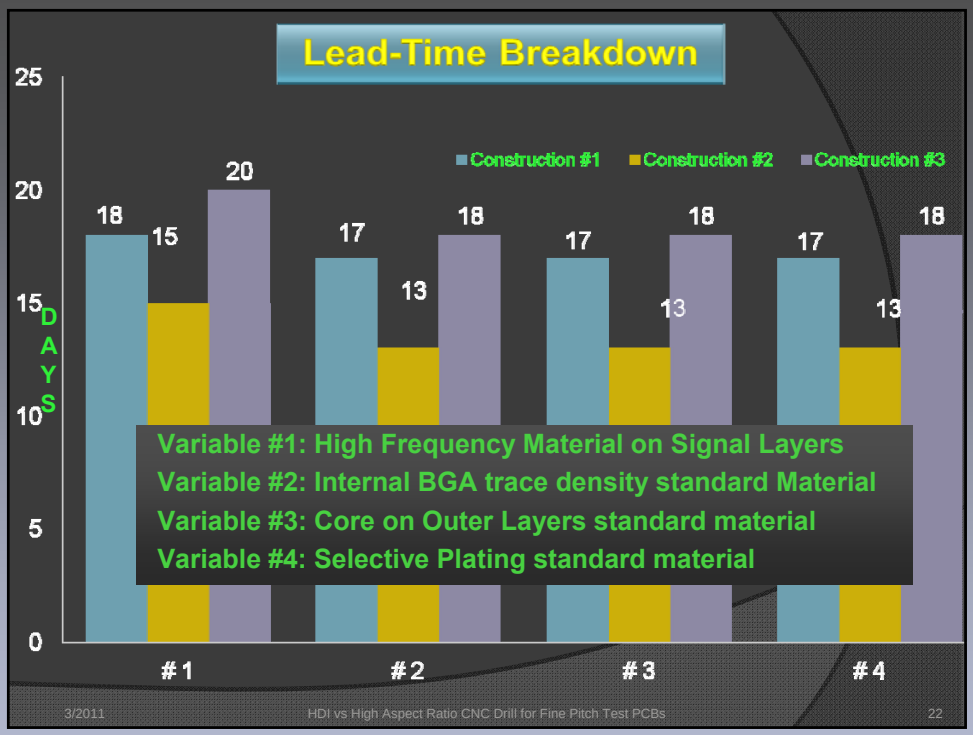
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 19

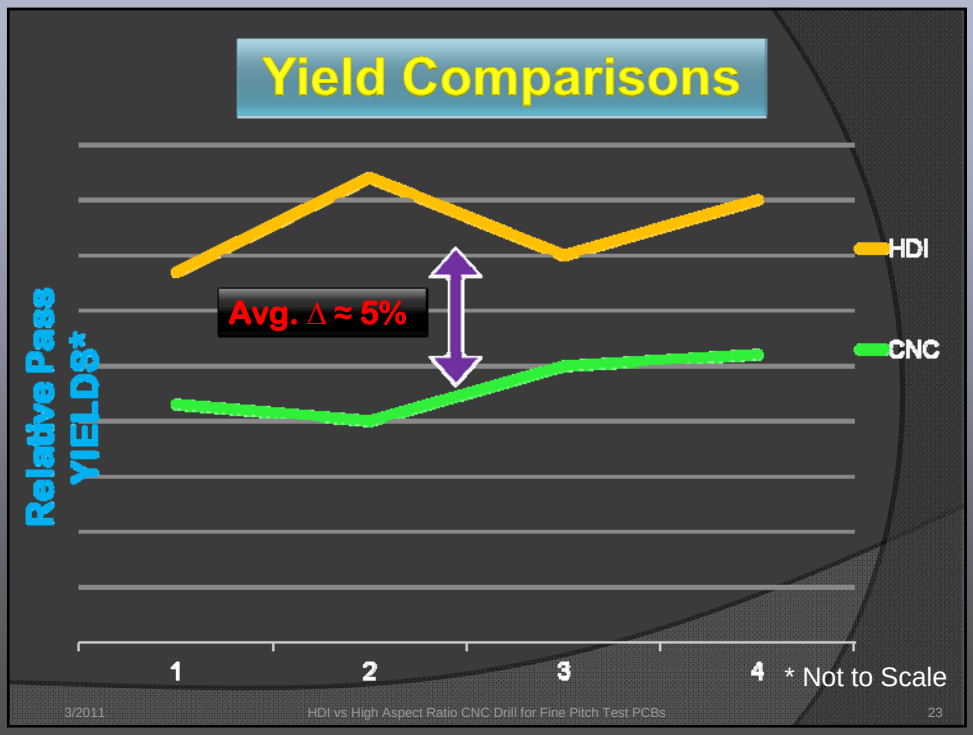
Cost and Lead-Time Breakdown for HDI vs. High Aspect Ratio Constructions

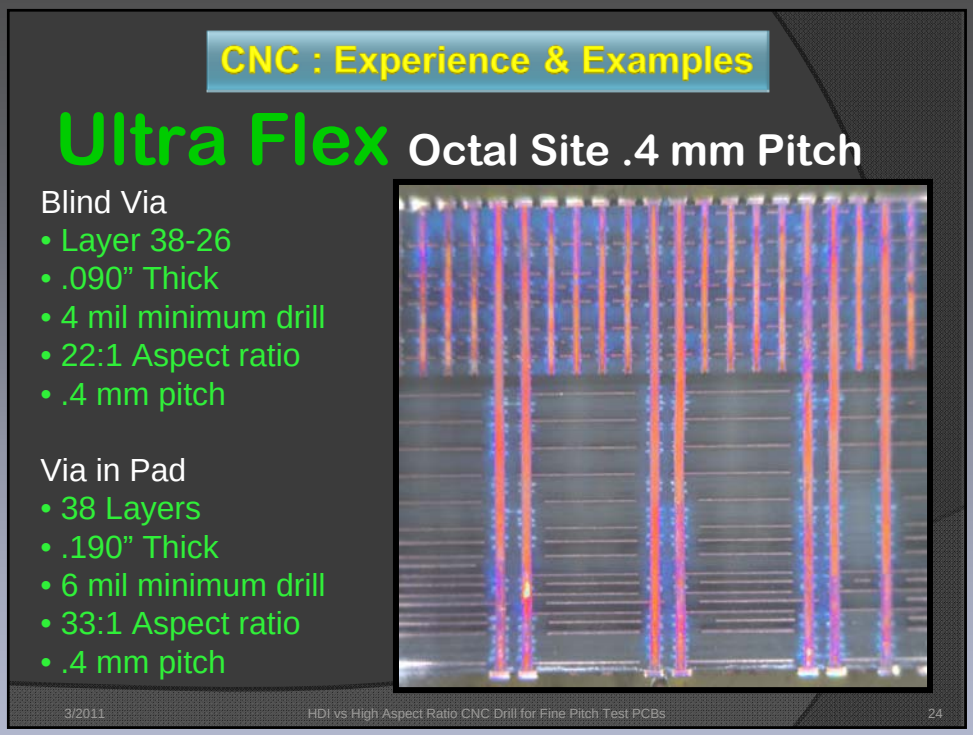
- Based on an order for 2 pcs of a 28 layer Full Size Verigy 93k DUT board with 20x20 .4mm BGA package Quad-Site, .187" thick
- Comparisons:
  - Construction #1: L1-L2, L2-L3, L3-L4, L4-L10, L10-L28, stacked-filled configuration
  - Construction #2: .004" CNC drill (L1-L16+L16-L28), .080" thick, 20:1 aspect ratio
  - Construction #3: L1-28 using .005" drill (37.4:1 aspect ratio)

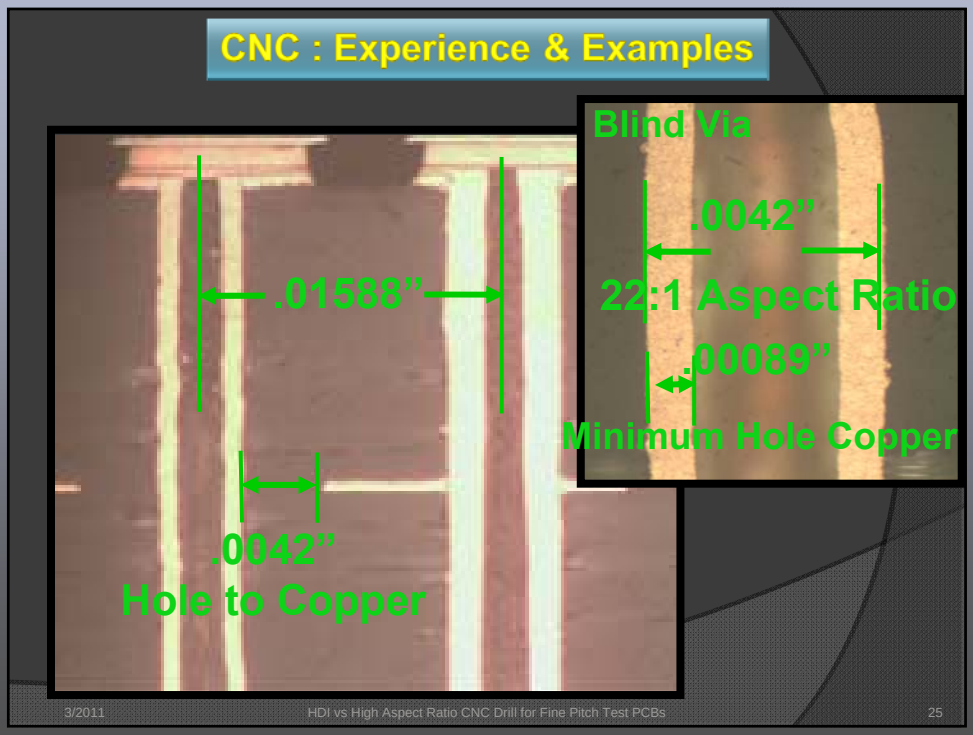
3/2011 HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs 20

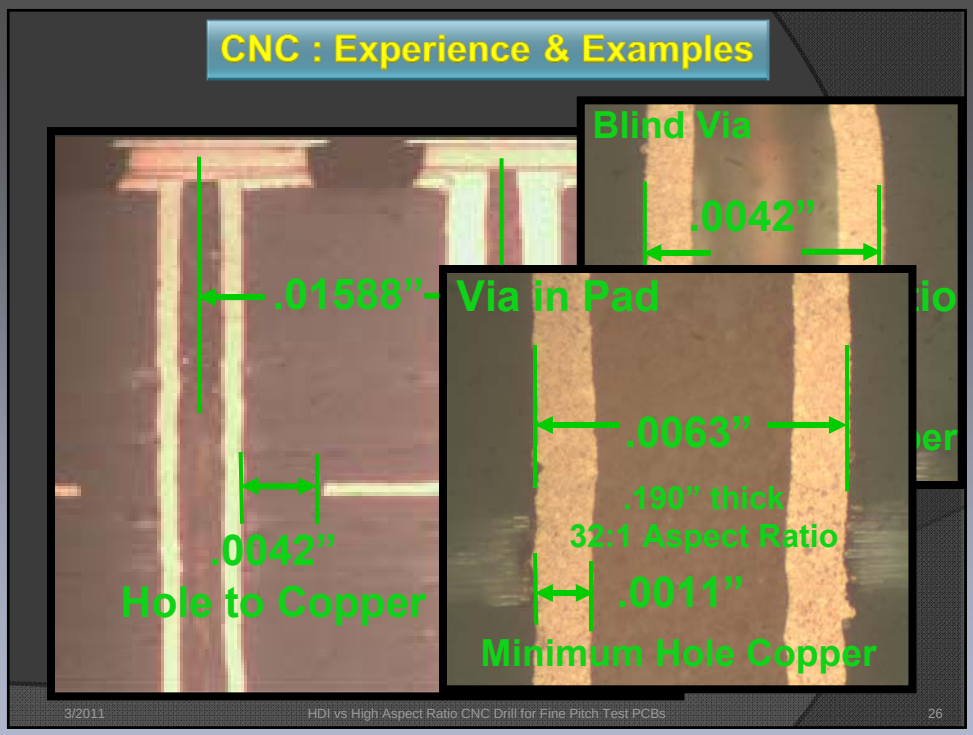

Cost Breakdown
$14,000.00
$12,000.00
$10,000.00
$8,000.00
$6,000.00
$4,000.00
$2,000.00
$0.00
Construction #1
Construction #2
Construction #3
$10,890.00
$7,890.00
$12,986.00
$8,490.00
$5,690.00
$9,845.00
$8,855.00
$6,355.00
$9,955.00
$8,655.00
$6,190.00
$9,565.00
Variable #1: High Frequency Material on Signal Layers
Variable #2: Internal BGA trace density standard Material
Variable #3: Core on Outer Layers standard material
Variable #4: Selective Plating standard material
#1
#2
#3
#4
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
21

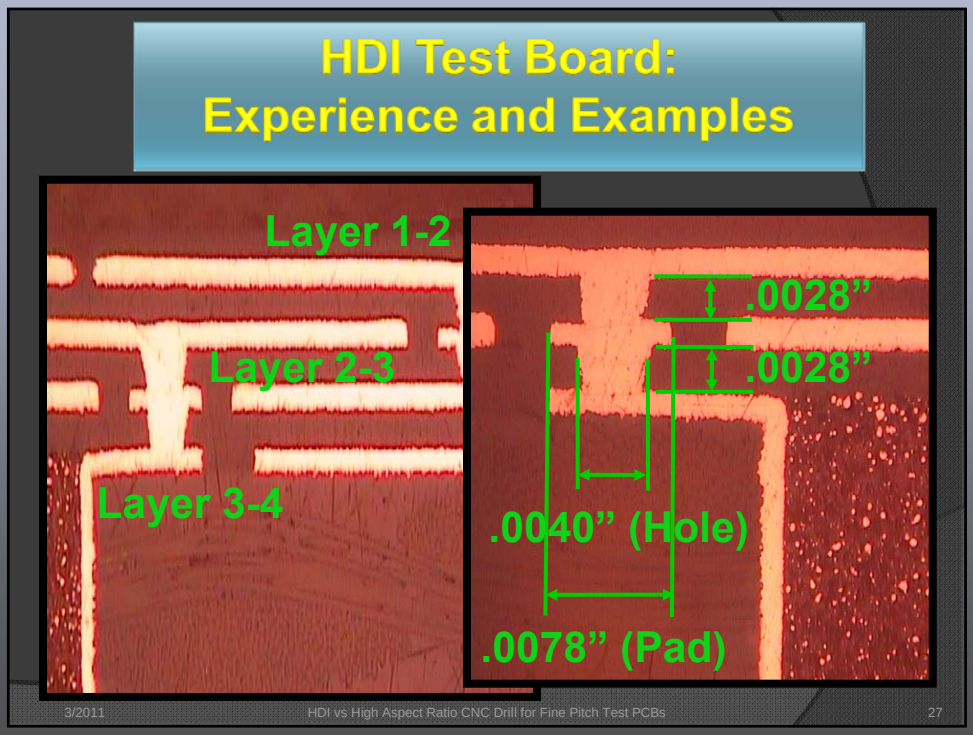

Lead-Time Breakdown
25
20
15
10
5
0
DAYS
Construction #1
Construction #2
Construction #3
18
15
20
17
13
18
17
13
18
17
13
18
Variable #1: High Frequency Material on Signal Layers
Variable #2: Internal BGA trace density standard Material
Variable #3: Core on Outer Layers standard material
Variable #4: Selective Plating standard material
#1
#2
#3
#4
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
22

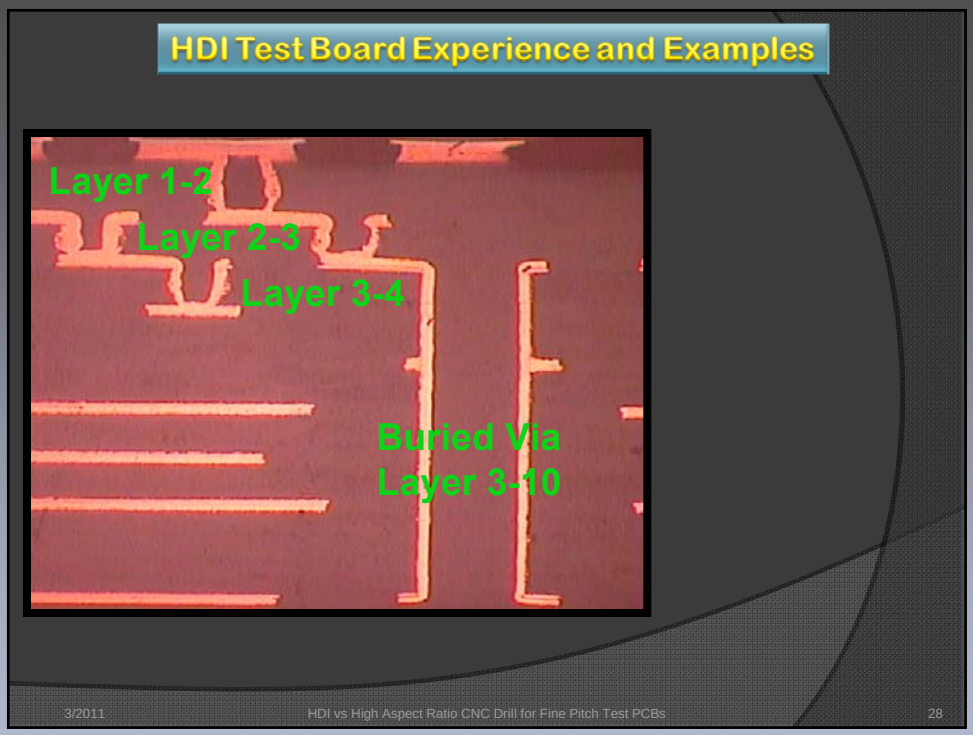

Yield Comparisons
Relative Pass YIELDS*
Avg. Δ ≈ 5%
HDI
CNC
1
2
3
4
* Not to Scale
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
23

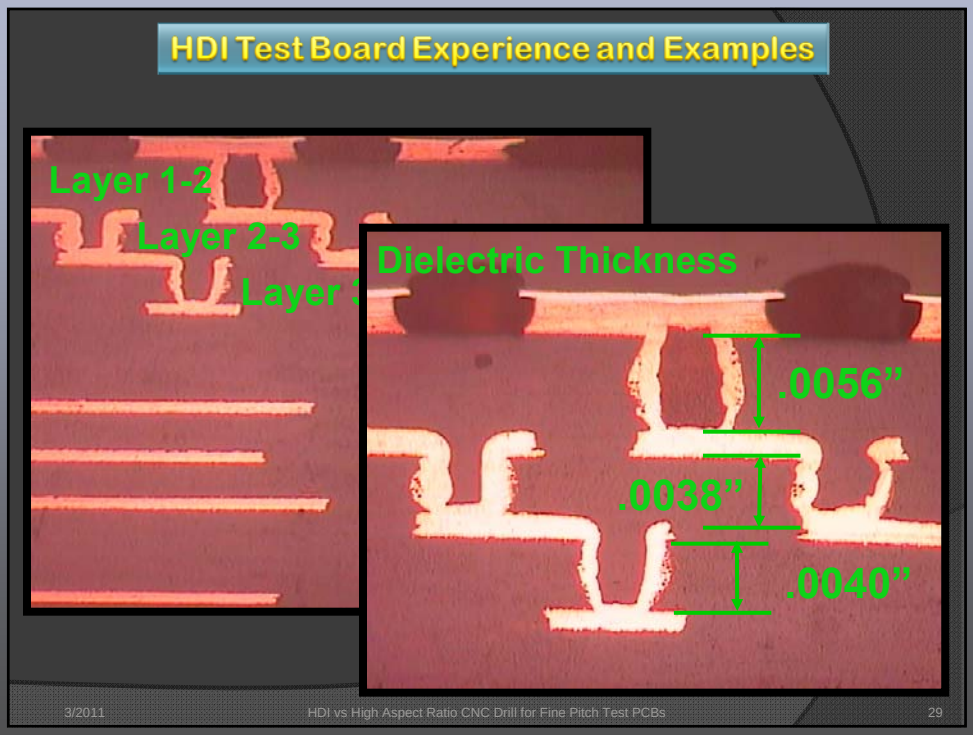

CNC : Experience & Examples
Ultra Flex Octal Site .4 mm Pitch
Blind Via
• Layer 38-26
• .090" Thick
• 4 mil minimum drill
• 22:1 Aspect ratio
• .4 mm pitch
Via in Pad
• 38 Layers
• .190" Thick
• 6 mil minimum drill
• 33:1 Aspect ratio
• .4 mm pitch
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
24

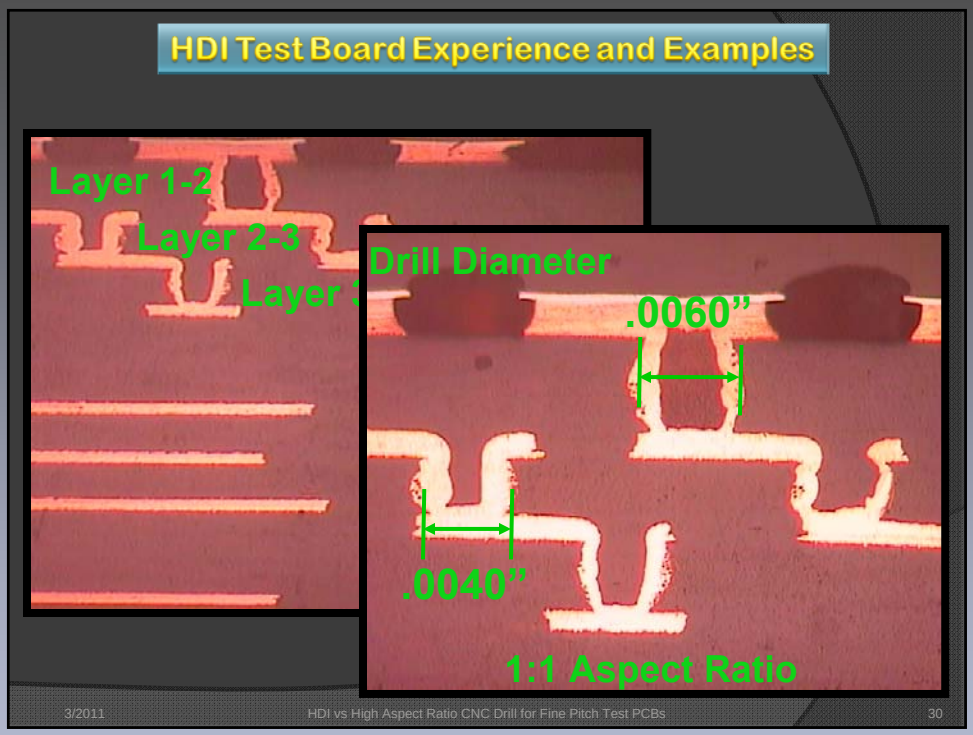

CNC : Experience & Examples
Blind Via
.0042”
22:1 Aspect Ratio
.00089”
Minimum Hole Copper
.01588”
.0042”
Hole to Copper
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
25

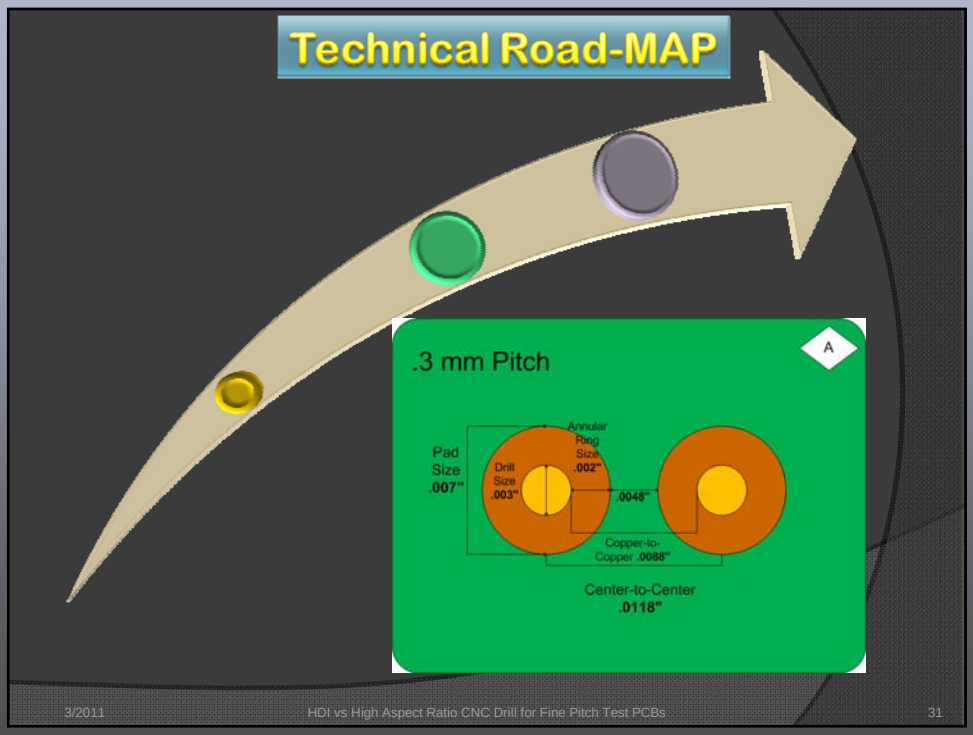

CNC : Experience & Examples
Blind Via
.0042”
.01588”
Via in Pad
.0063”
.190” thick
32:1 Aspect Ratio
.0011”
Minimum Hole Copper
.0042”
Hole to Copper
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
26

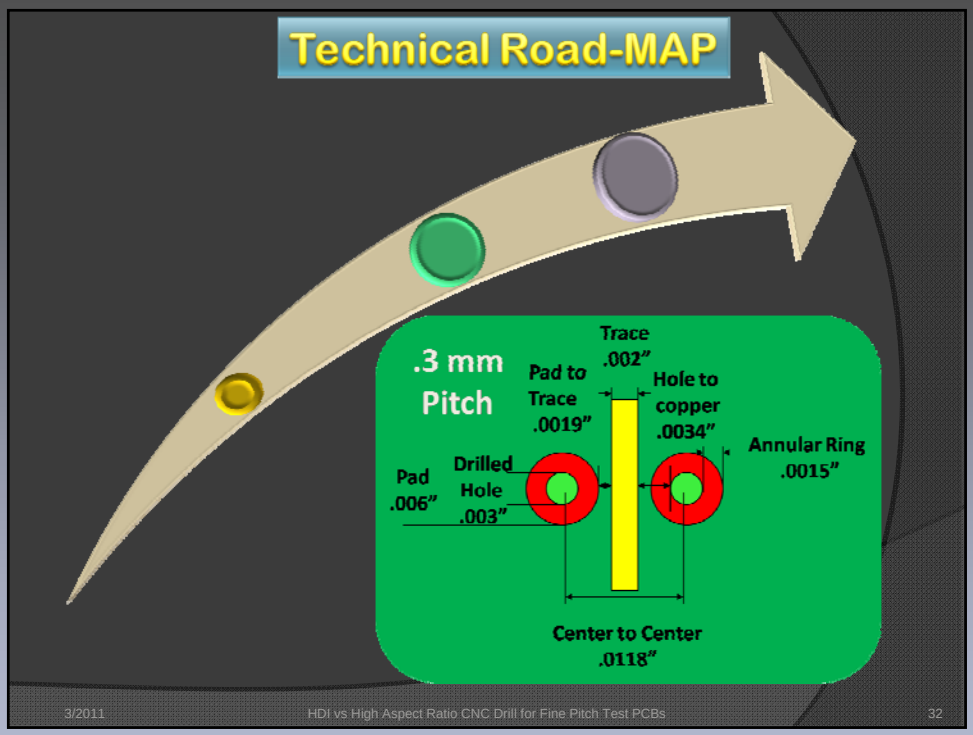

HDI Test Board:
Experience and Examples
Layer 1-2
Layer 2-3
Layer 3-4
.0028”
.0028”
.0040” (Hole)
.0078” (Pad)
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
27

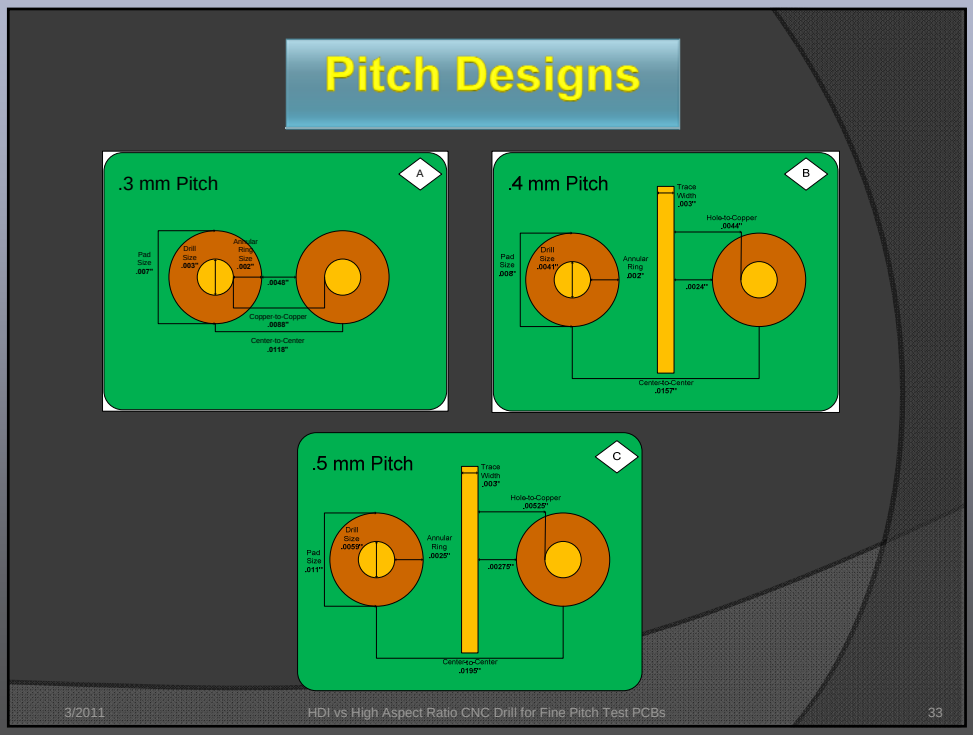

HDI Test Board Experience and Examples
Layer 1-2
Layer 2-3
Layer 3-4
Buried Via
Layer 3-10
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
28

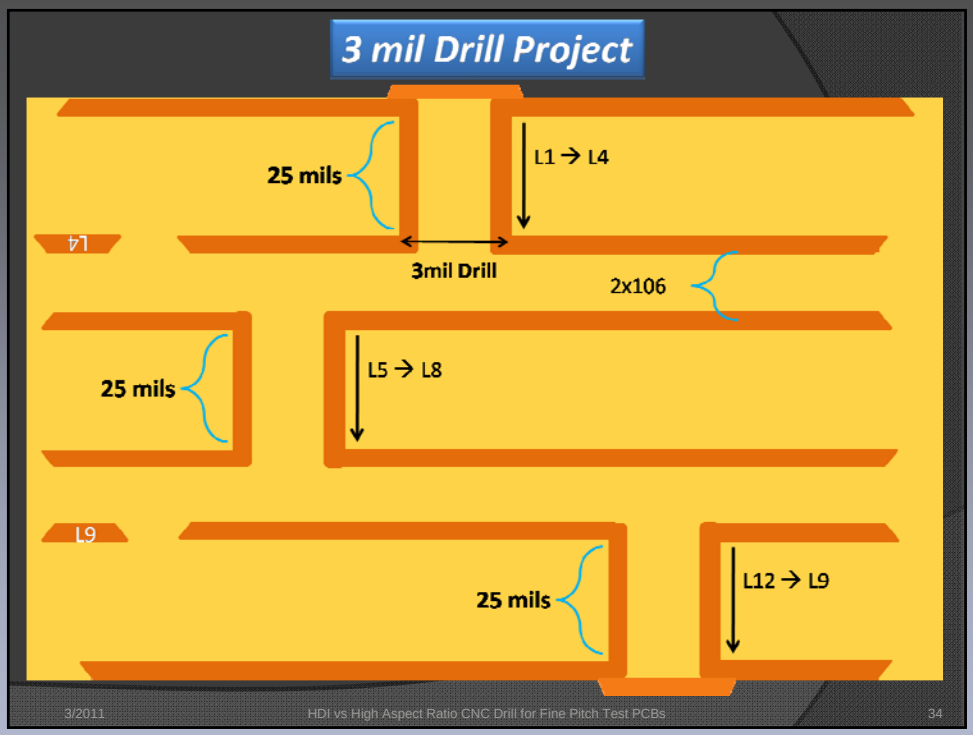

HDI Test Board Experience and Examples
Layer 1-2
Layer 2-3
Dielectric Thickness
.0056”
.0038”
.0040”
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
29

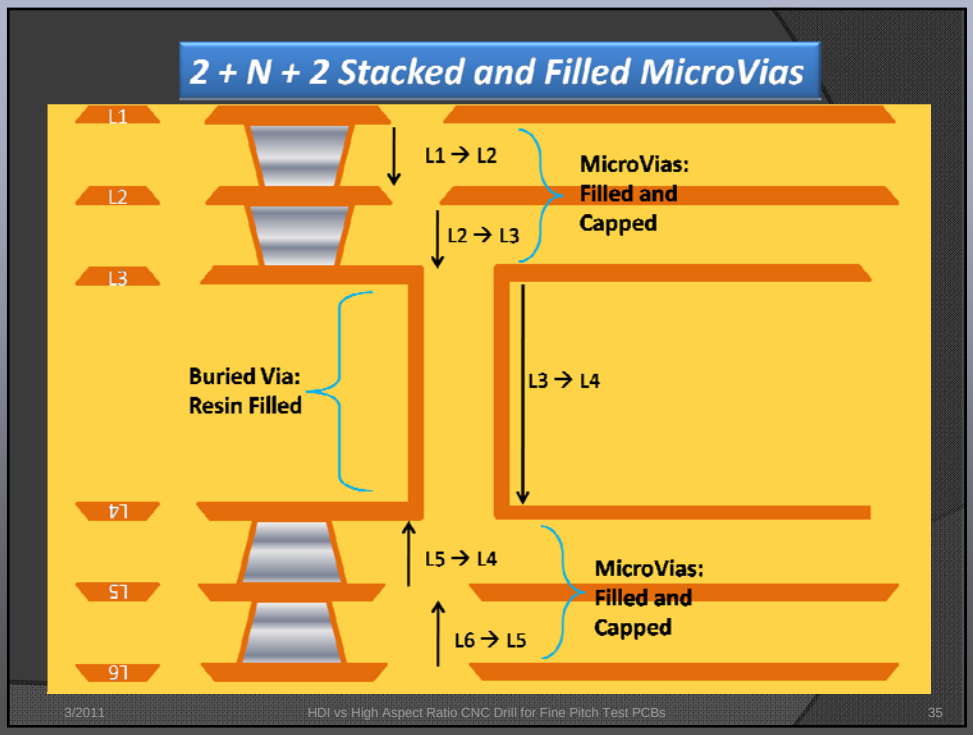

HDI Test Board Experience and Examples
Layer 1-2
Layer 2-3
Drill Diameter
.0060”
.0040”
1:1 Aspect Ratio
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
30

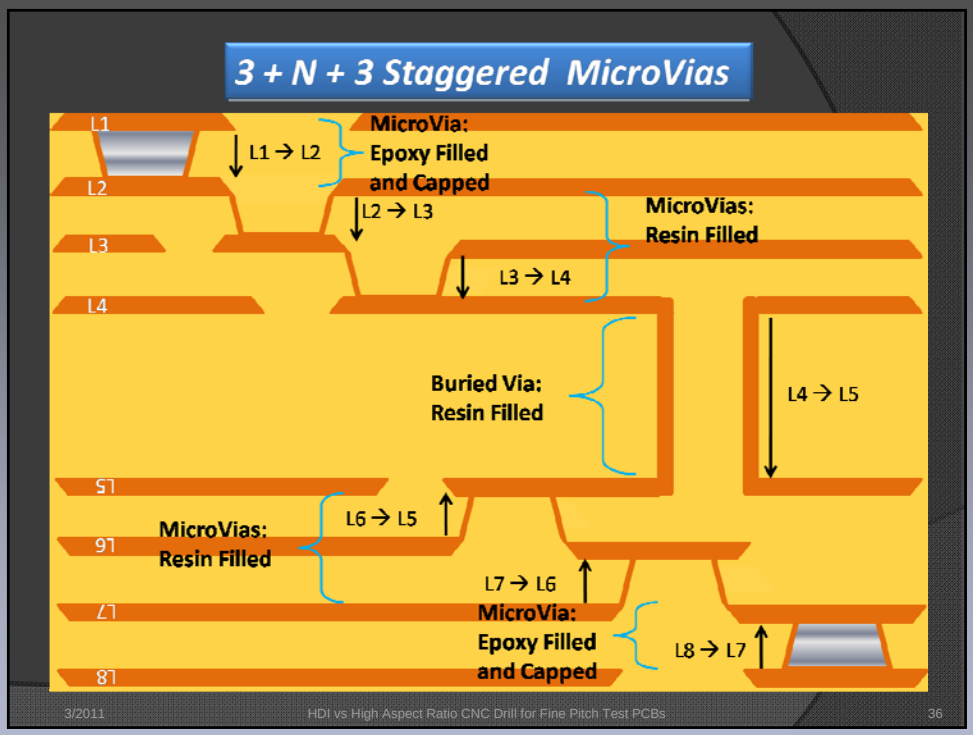

Technical Road-MAP
.3 mm Pitch
A
Pad Size .007"
Drill Size .003"
Annular Ring Size .002"
.0048"
Copper-to-Copper .0088"
Center-to-Center .0118"
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
31

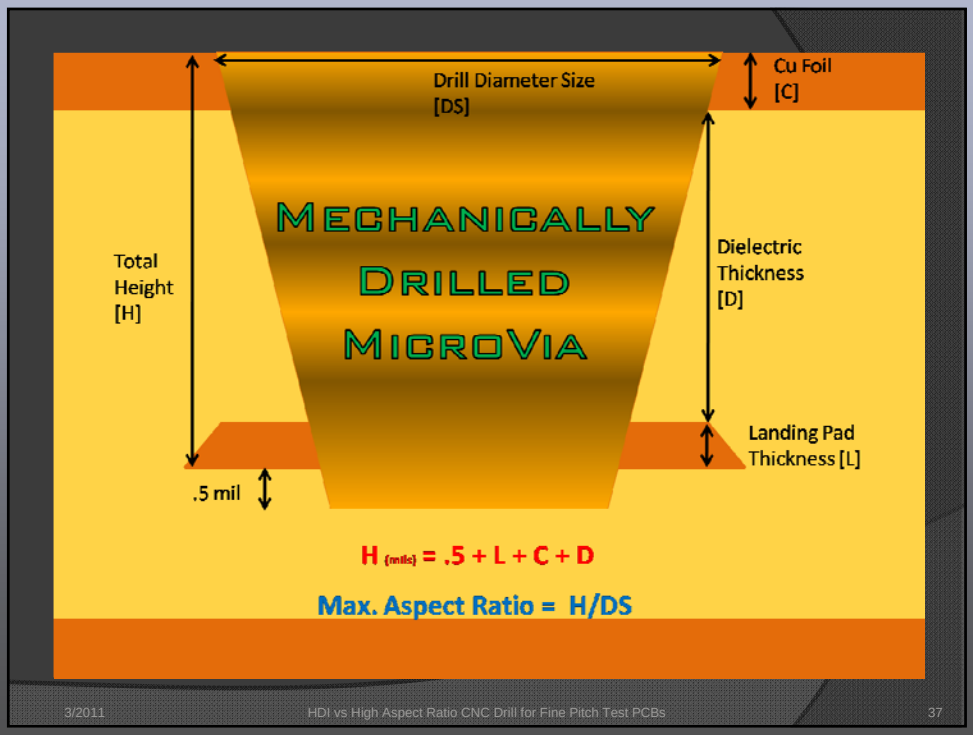

Technical Road-MAP
.3 mm Pitch
Trace .002"
Pad to Trace .0019"
Hole to copper .0034"
Annular Ring .0015"
Pad .006"
Drilled Hole .003"
Center to Center .0118"
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
32

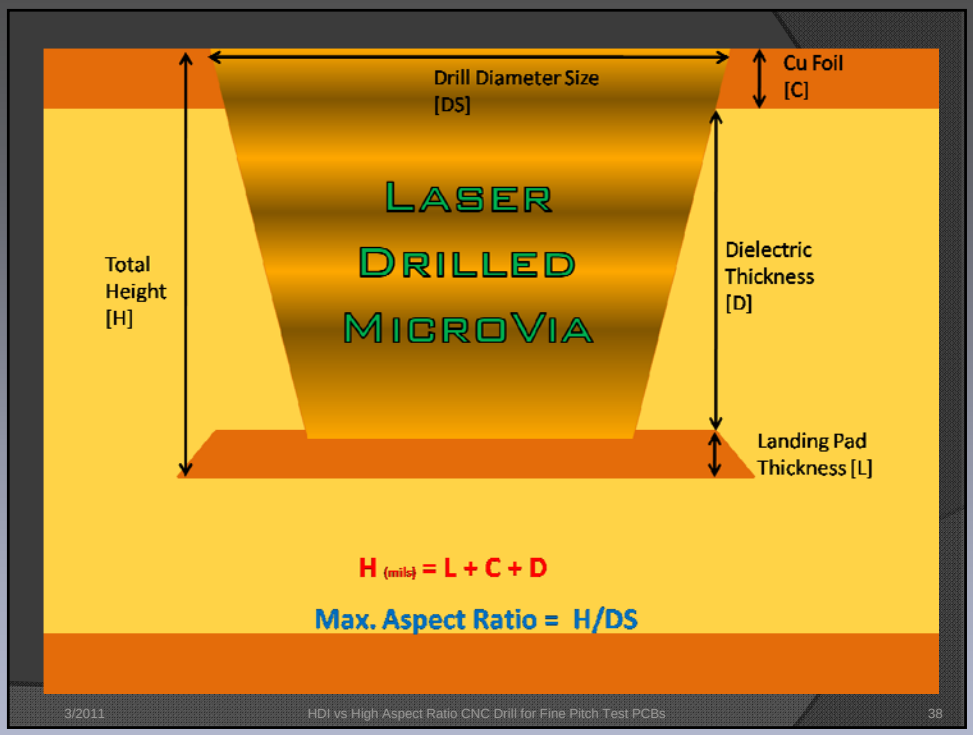

Pitch Designs
.3 mm Pitch
A
.4 mm Pitch
B
.5 mm Pitch
C
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
33

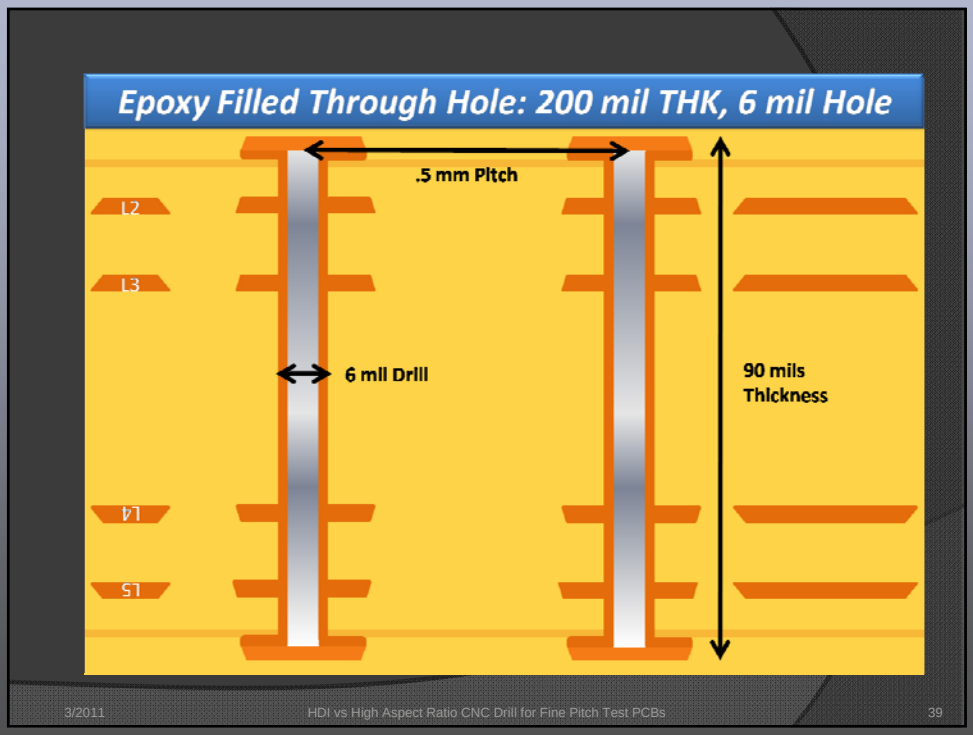

3 mil Drill Project
25 mils
L1 → L4
L4
3mil Drill
2x106
25 mils
L5 → L8
L9
25 mils
L12 → L9
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
34

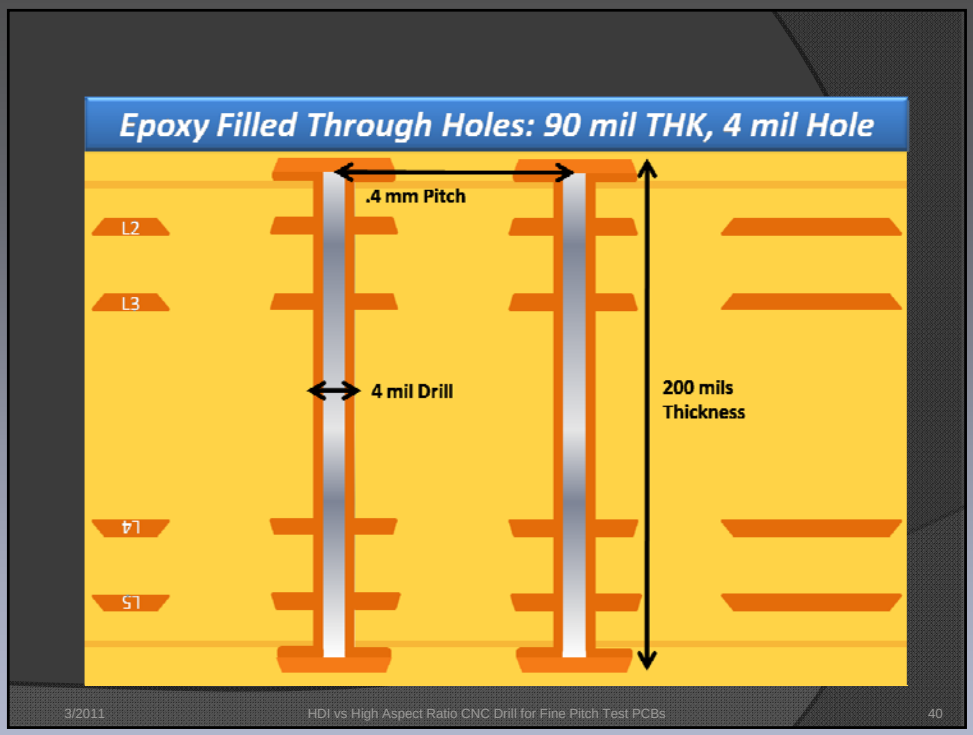

2 + N + 2 Stacked and Filled MicroVias
L1
L2
L3
L4
L5
L6
L1 → L2
L2 → L3
MicroVias:
Filled and
Capped
Buried Via:
Resin Filled
L3 → L4
L5 → L4
L6 → L5
MicroVias:
Filled and
Capped
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
35


3 + N + 3 Staggered MicroVias
L1
L2
L3
L4
L5
L6
L7
L8
L1 → L2
MicroVia:
Epoxy Filled
and Capped
L2 → L3
MicroVias:
Resin Filled
L3 → L4
Buried Via:
Resin Filled
L4 → L5
L6 → L5
MicroVias:
Resin Filled
L7 → L6
MicroVia:
Epoxy Filled
and Capped
L8 → L7
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
36


Drill Diameter Size
[DS]
Cu Foil
[C]
MECHANICALLY
DRILLED
MICROVIA
Total
Height
[H]
Dielectric
Thickness
[D]
Landing Pad
Thickness [L]
.5 mil
H (mils) = .5 + L + C + D
Max. Aspect Ratio = H/DS
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
37


Drill Diameter Size
[DS]
Cu Foil
[C]
LASER
DRILLED
MICROVIA
Total
Height
[H]
Dielectric
Thickness
[D]
Landing Pad
Thickness [L]
H (mils) = L + C + D
Max. Aspect Ratio = H/DS
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
38


Epoxy Filled Through Hole: 200 mil THK, 6 mil Hole
.5 mm Pitch
L2
L3
6 mil Drill
90 mils
Thickness
L4
L5
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
39


Epoxy Filled Through Holes: 90 mil THK, 4 mil Hole
.4 mm Pitch
L2
L3
4 mil Drill
200 mils
Thickness
L4
L5
3/2011
HDI vs High Aspect Ratio CNC Drill for Fine Pitch Test PCBs
40

2010 Equipment

Pros & Cons in Manufacturing: HDI

- **PROs:**
  - Staggered will reduce processing time, Stacked MV's need to be plated shut or filled, which is time consuming.
  - Ease to de-smear, reduce the risk for reliability issues.
  - Fit higher layer count in a tight pitch design.
- **CONs:**
  - Multiple Lamination cycles needed.
  - Longer production delivery times.
  - Higher Risk for Miss-registration:
    - Assumption: Access to LDI Imaging, X-ray drill capability, In-house Laser Drill capability, Multiple Drill Processes.

Pros & Cons in Manufacturing: CNC Drill

- **PROs:**
  - Shorter processing times.
  - Lower risk for layer to layer and core to core miss-registration.
  - Quicker delivery times.
  - Lower risk for Warpage, single lam cycle and balanced construction.
- **CONs:**
  - Increase risk for though via capability (yields).
  - Increase risk for drill miss-registration if not well defined drilling processing parameters.
  - Increase risk for reliability issues. Chemical de-smear and/or Plasma. Plasma equipment capability limitations.
  - Challenge to meet class 2. Plating in the holes.

SUMMARY

- The broad spectrum of device specifications and Test requirements has proven that both HDI and High Aspect Ratio will continue in Fine-Pitch Final Test PCB demand.
- Our goal in this comparative study is to share the challenges and concerns in each respective method of PCB manufacturing.
- Market trends indicate that pitch of devices will continue to decrease, and pin-counts will increase.

Embedded Thin-Film NiP Resistors in Burn-In Trays

Bruce Mahler
Vice President
Ohmega Technologies, Inc.

2011 BiTS Workshop
March 6 - 9, 2011

Discrete resistors used on burn-in boards for isolation, termination and pull-up/down have several drawbacks:

- They take up valuable real estate
- They require costly assembly
- They increase burn-in board design complexity
- They decrease board reliability, especially with potential solder joint failures

Advantages of Embedded Thin Film NiP Resistors:

- Shorter signal paths and reduced series inductance
- Reduced cross talk, noise and EMI
- Increased socket density
- Reduced board size
- Improved board layout due to elimination of vias and discrete resistors, pads and traces

Advantages of Embedded Thin Film NiP Resistors (continued):

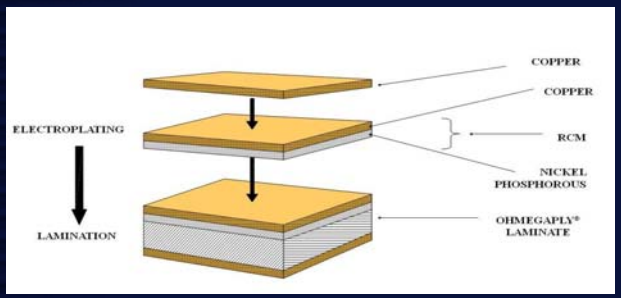
- Improved reliability with the elimination of solder joints
- Embedded resistors are stable at elevated temperatures
- Cost savings by elimination of discrete resistor purchase and assembly
- The greater the number of resistors the lower the cost per unit resistor

Embedded NiP Resistor Technology

- Electrodeposited thin film resistive material
- Standard subtractive PWB processing
- Global PWB sourcing
- Surface or embedded resistors
- Mature technology (36+ years)
- Field proven, excellent long term reliability

NiP Resistive Material Manufacturing Overview

- Electrodeposited Nickel Phosphorous(NiP) metal alloy onto the matte side of copper foil
- The NiP thin film alloy/copper foil is laminated to a dielectric
- Standard subtractive PCB processing produces copper circuitry and planar resistors



NiP Sheet Resistivity Offerings

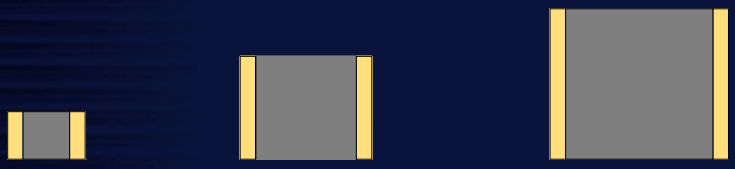
Sheet Resistivity	Material Tolerance
10 Ω/□	3%
25 Ω/□	5%
50 Ω/□	5%
100 Ω/□	5%
250 Ω/□	10%

Ohms Per Square

Sheet resistivity (stated in Ohms per square) is dimensionless

- A square area of resistive material = sheet resistivity of resistive material

E.g., a 25 Ω/(Ohms/Square) sheet resistance



L1 = W1
R1 = 25 Ohms

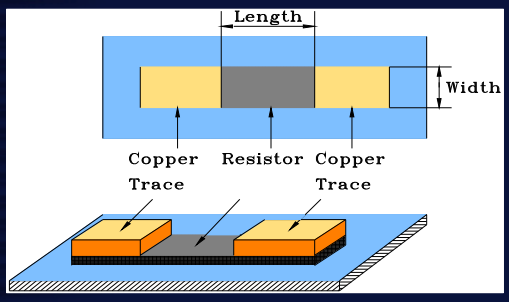
L2 = W2
R2 = 25 Ohms

L3 =W3
R3 = 25 Ohms

Ohms Per Square

- Resistor value = sheet resistivity x ratio length to width (R =Rs x L/W)

E.g., a 25 Ω/ sheet resistivity
Length = 0.030" (30 mils), Width = 0.015 " (15mils)
Resistor value = 25 Ω/ x (30mils/15mils)
= 25 Ω/ x 2 squares = 50 ohms



Burn–in Board Application A

BOARD PARAMETERS

- Polyimide multilayer PCB construction
- Tray designed for 150°C continuous operation
- 2 KΩ embedded isolation resistor using 100 Ω/□ NiP resistive material
- Resistor rated for 1/8 watt.

DESIGN RESULTS

- Tray with surface isolation resistors: 138 sixteen-pin parts
- Tray with embedded NiP isolation resistors: 240 sixteen-pin parts

Burn–in Board Application A

RELIABILITY TEST RESULTS

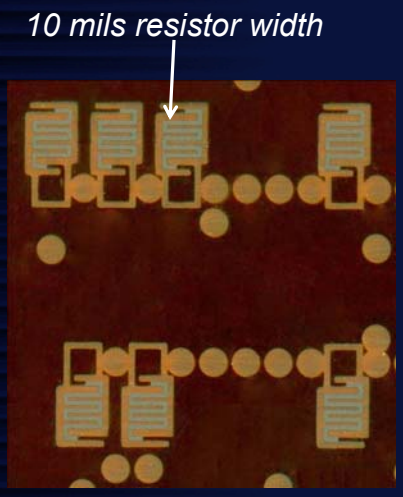
- **Thermal shock** (50 cycles, -65°C to +150°C; 15 minutes dwell, at temperature; 2 minute transfer cycle)

  No evidence of measling, blistering or delamination

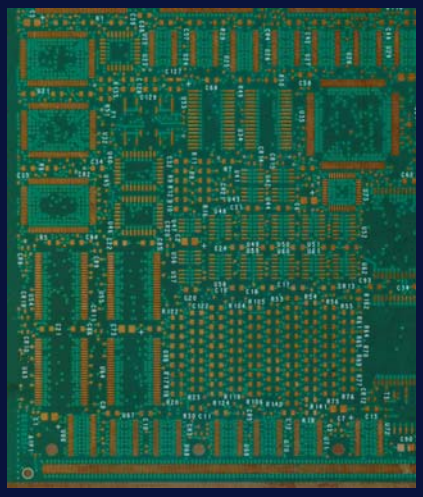
- **Thermal Soak** (160°C ambient)

HOURS	Δ Resistance 1 WATT/SQ. IN.	Δ Resistance 10 WATT/SQ. IN.
1400	+2.0%	+5%
2500	+2.5%	+5%
3500	+2.5%	+6%

Thermal Soak Test for Burn-in Application B

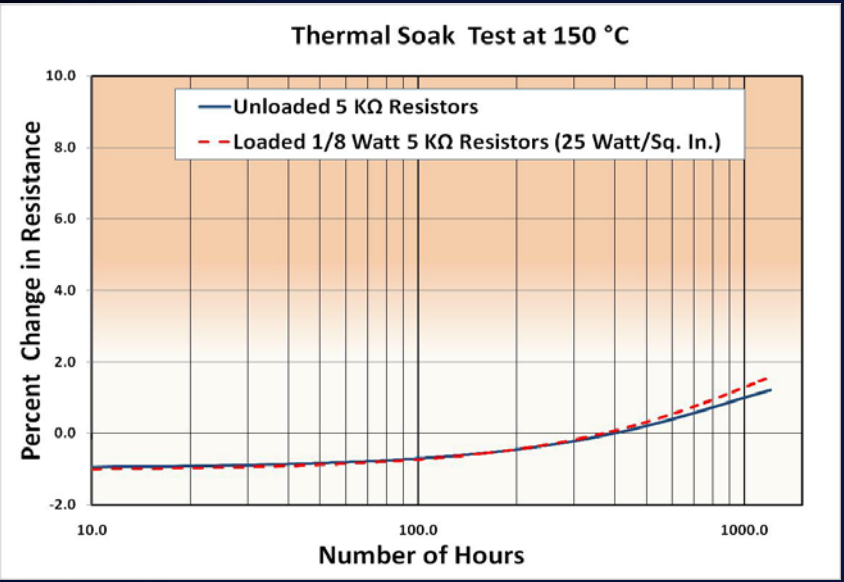


△ *Enlargement of inner layer with 5 KΩ NiP Resistors (100 Ω/□)*



△ *Multilayer PCB (polyimide substrate)*

Thermal Soak Test for Burn-in Application B



Burn-In Board Design C

Size: 30.7″x 11.4″ = 350 sq″

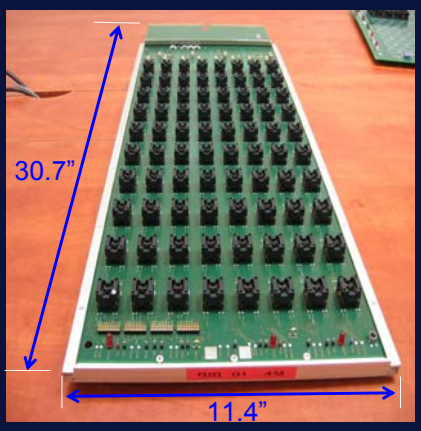
100 pins gold edge Connector

Material: FR4, Hi-TG

Industrial components

Termination and P/U Resistors 2,300

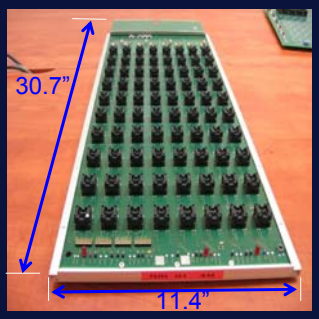
Controlled Impedance signals 50/100ohm



Courtesy of Adcom, Inc.

Problem: Board size is 30.7”x 11.4”

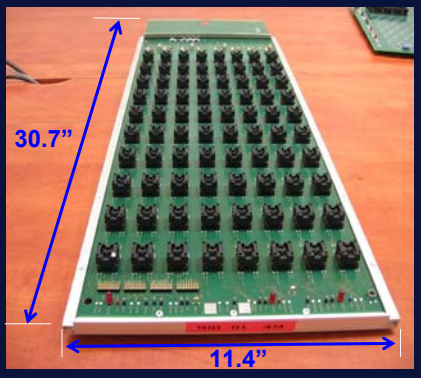
- A limited number of PCB shops could handle this **size board**. For those that could, the purchase **cost** would be high.
- Even fewer assembly houses would be able to place a board of this **size** within the stencil, on the pick & place machines, and then through the re-flow oven.



The following criteria led to the selection of the NiP Embedded Resistor Technology:

Availability of:

- ✓ Design tools
- ✓ PCB layout tools
- ✓ PCB manufacturers
- ✓ Reliability data
- ✓ Assembly houses



Case study: the board, designed with NiP Embedded resistor technology

Size: 12.9″ x 14.4″ =185 sq″

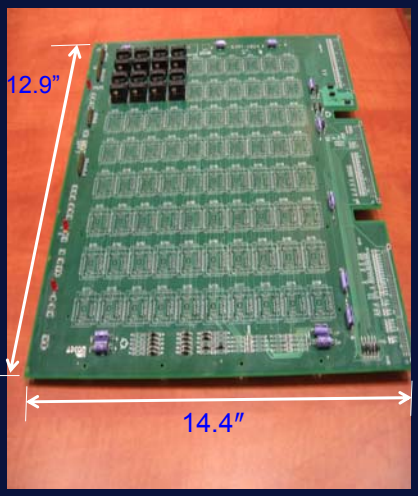
PCB Thickness 1.6mm

Material FR4 Hi-TG

Industrial components

Embedded Resistors 2,300

Controlled Impedance signals 50/100ohm



Comparison of boards

Board designed with embedded resistors is 53% the size of original design

What was gained?

- ✓ Smaller PCB size in production
- ✓ Cheaper Assembly
- ✓ Faster Assembly
- ✓ Higher Reliability
- ✓ Shorter Signal Traces
- ✓ Gained Component storage area
- ✓ Reduced purchase costs

Summary and Conclusions

- Thin Film NiP Resistive Material
- Standard Subtractive PWB Processing
- PWB Global Sourcing
- Mature Technology (36+ years)
- Field Proven, Excellent Long Term Reliability
- Performance Enhancing, Cost Effective Resistor Technology for Burn-In and DUT Boards

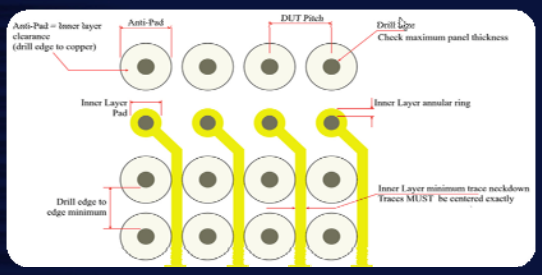
Benefits & Risks of High Aspect Ratio Vias in ATE Boards

Christopher Cuda
Multitest

2011 BiTS Workshop
March 6 - 9, 2011

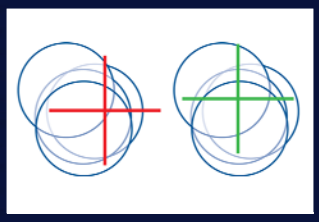
Problems

- As pin counts and test parallelism increase so does the PCB layer count.
- Micro/blind via construction requires multi-lamination processing:
  - More lamination means more exposure to micro factures, and the consequent current leakage.
- Pad to pad spacing is determined by the DUT, but space allocation is determined by the PCB manufacturers preferences or Design For Manufacturing (DFM) guidelines.



High Aspect Ratio Via (HAV) Solutions

- Advancements in drilling and inner layer registration have enabled smaller, mechanically drilled, plated-through holes at higher aspect ratios with tighter anti-pads



- When Combined with reduced trace widths HAV can:
  - Allow for higher routing density at standard pitch
  - Allow for monolithic stack ups for fine pitch arrays

Agenda

- Case study of HAVs for layer count reduction
- Case study of HAVs for monolithic stack up
- Review signal integrity, reliability & current conductivity with HAV geometries
- PCB manufacturing flow & cost factors
- HAV reliability
- Risks

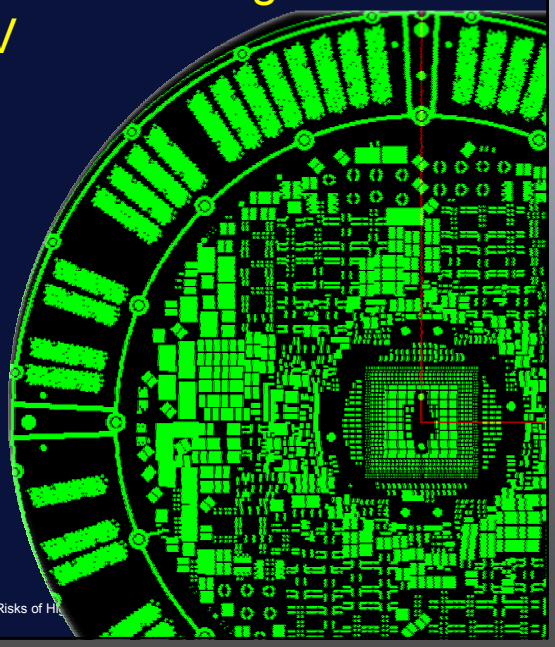
Example of Improved Routing Density with HAV

Project Parameters:

- 3044 pin array @ 0.8mm pitch
- >900 unique passive component positions
- >250 relays and active components

HAV Approach:

Shrink the geometries at the DUT to double routing density



3/2011 Benefits & Risks of Hi

Stack Up Comparison

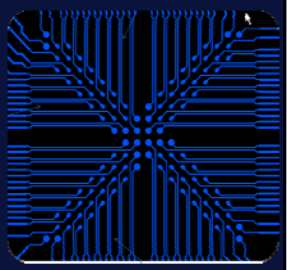
	Standard Build	HAV Geometries
Total Layer count	58	40
Signal Layers	19	10
Ground Layers (GSG)	28	20
Power Layers	8	8
Thickness	0.250”	0.187”

Via Diameter reduced 17%

Trace width reduced 20%

Anti-pad to via ratio reduced from 2.9:1 to 2.6:1

Price reduced 43%



3/2011 Benefits & Risks of High Aspect Ratio Vias in ATE Boards 6

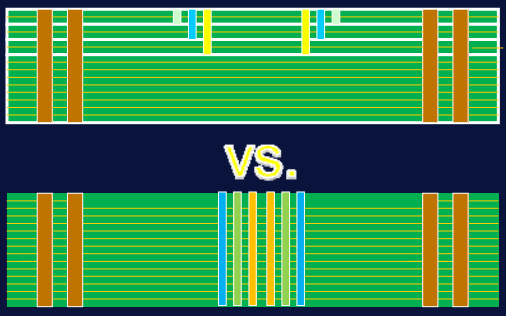
Example of Fine Pitch Using HAV

Project Parameters:

- 25 pin WLCSP @ 0.5mm pitch
- Four DUT sites
- Low component & routing density
- Leakage sensitive test

HAV Approach:

Using HAVs in the DUT pattern to allow a monolithic stack up



Build Comparisons

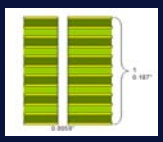
Micro / Blind vias for DUT Escape

- Four via spans used with blind vias:

  - L1 – L3
  - L1 – L5
  - L1 – L7
  - L1 – L10
- Four lamination-plating-drill cycles

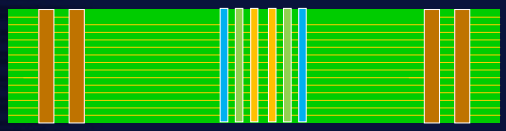
High-Aspect-Ratio Geometries

- One via span used:



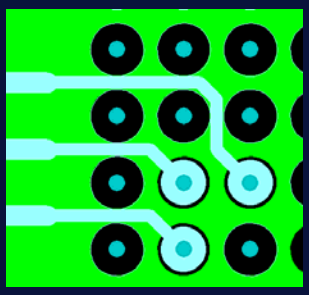
- Single lamination-plating-drill cycle
  - Through-hole vias with reduced trace width and anti-pad geometries
  - 20% reduction in cycle time

HAV Fine-Pitch Routing



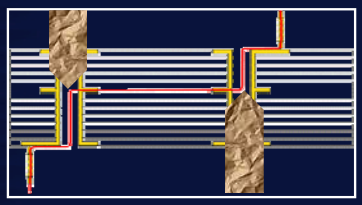
Routes from Top

Inner Layer View



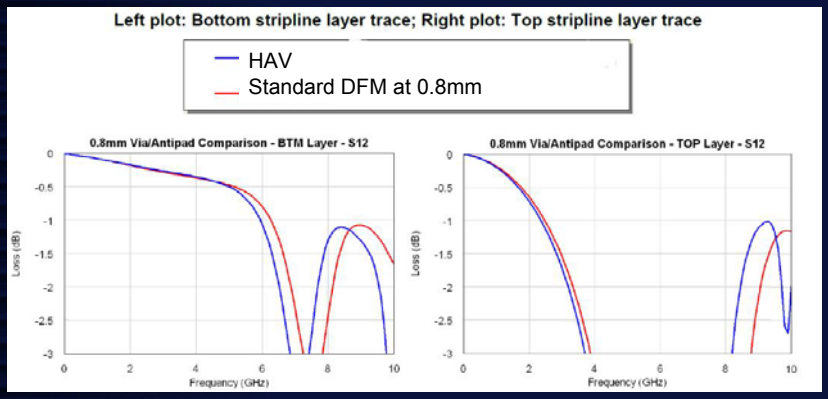
Signal Integrity: Stubs

- Micro / Blind vias are effective at eliminating unused via length, minimizing signal reflection at high speeds
- Mechanical stub removal is an alternative method of eliminating unwanted via length and is often more cost effective



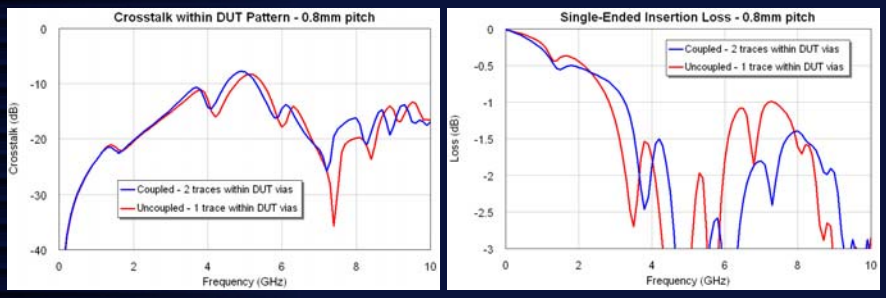
Signal Integrity: Via Size & Anti-Pads

- Smaller via diameters and reduced anti-pad ratios have an insignificant impact on signal performance:



Signal Integrity: Traces

- Double density routing
  - Reduced trace-to-trace spacing → can increase crosstalk
  - Reduced trace width → can increase impedance mismatch
- Simulation results
  - Socket/via launch dominate crosstalk/impedance in DUT area
  - Impact due to double density routing is negligible



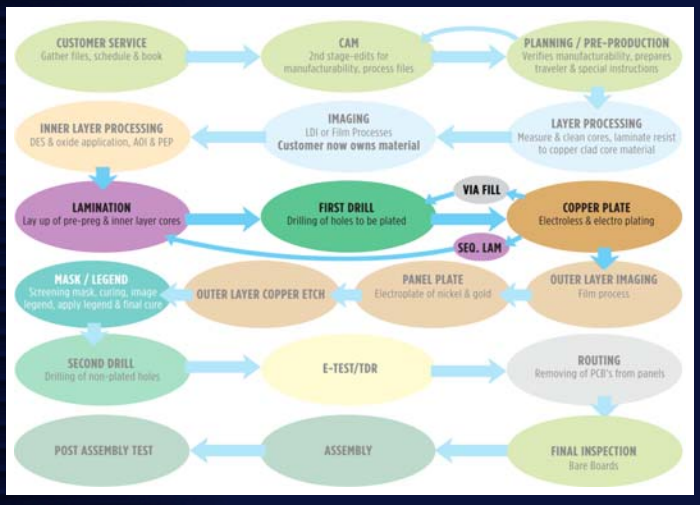
Electrical Performance: Conductivity

- HAV & fine trace widths can carry more current than most pogo pins
  - When used with the proper laminates
  - 0.006" vias demonstrated the ability to carry >50 Amps of continuous current at 80°C temperature rise
  - Traces are the limiting factor:

1/2-oz Traces			
TW (mil)	20° T-rise	40° T-rise	60° T-rise
2.5	1.6	2.0	
3	1.7	2.1	2.2
3.5	1.8	2.2	2.6
4	1.8	2.3	2.6
5	2.1	2.6	3.0
6	2.4	3.0	3.4
7	2.3	3.0	3.4
9.7	2.8	3.7	4.3
14.4	3.3	4.5	5.5

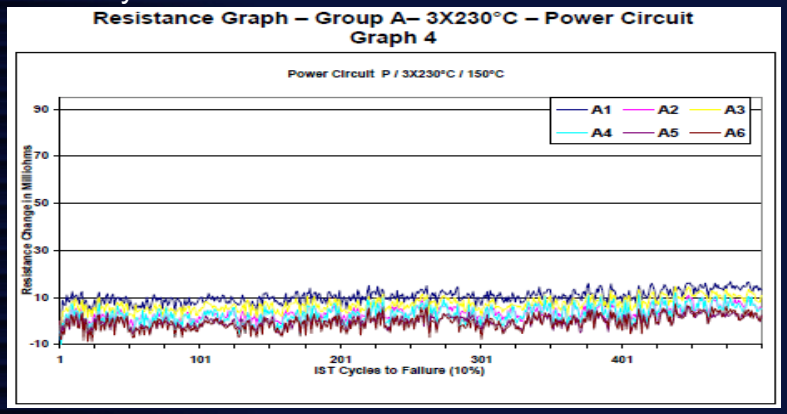
@ 0.5mm pitch, loss of 0.4 Amps

Cost & Cycle Time Savings



Are HAVs Reliable?

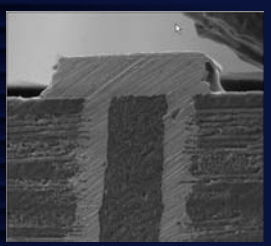
- *Yes!*
- Industry recognized Interconnect Stress Tests (ISTs) prove that if built to IPC standards, HAVs are very reliable



Risks

HAVs

- Via plating
  - Potentially thin Cu plating can create a high resistance path
  - May not be exposed until after thermal shock of assembly process



Blind /Microvias

- PCB manufacturers must compensate for inner layer x/y registration

- Laminates are not designed to be exposed to repeated lamination cycles

Summary

- HAVs are a valuable tool to reduce PCB costs by reducing layer counts
- HAVs can allow for monolithic stack ups at fine pitch
- HAVs are reliable
- Every application is different, HAVs (and also blind / microvias) are not a fit for every project

Thank You!

- Interconnect stress testing provided by PWB Solutions Inc.
- Via current testing provided by Trace Laboratories Inc.
- Signal integrity data courtesy of Jason Mroczkowski & Ryan Satrom at Multitest.