BiTS™ Burn-in & Test Socket Workshop 2011

Session 1

ARCHIVE 2011

CRANKING UP THE FREQUENCY

Evaluation of Contactor Impedance Mismatch on RF Performance

James Migliaccio, John Capwell—RF Micro Devices

Contact Optimization for Signal and Power Integrity

Gert Hohenwarter—GateWave Northern, Inc.

A Complete High Frequency Interconnect Scheme for Testing >20Gb/s Interfaces

Thomas P. Warwick, Thomas Smith, Dan Turpuseema—R&D Circuits

Frequency-Domain and Time-Domain Impact of Spring-Probe Socket Geometry on High-Speed IO Testing

Se-Jung Moon, Selim S. Akbay, Mustapha Abdulai—Intel Corporation

Evaluation of Contactor Impedance Mismatch on RF Performance

James Migliaccio / John Capwell
RF Micro Devices

2011 BiTS Workshop
March 6 - 9, 2011

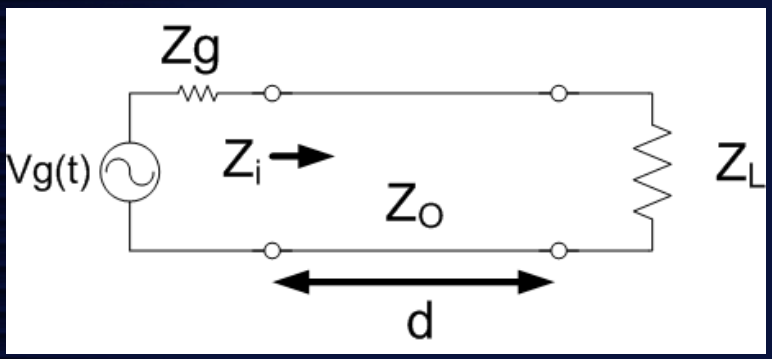
Problem Description

- Most RF measurement systems are 50Ω
- Typically this characteristic impedance (50Ω), can be maintained from the tester to the contactor
- The impedance through the contactor to the DUT may not be 50Ω
- This presentation will investigate what effect this mismatch has on measurement performance

Simplifying Assumptions

- Contactor will be replaced by a length of transmission line
- DUT is 50Ω and the source side of the contact is 50Ω
- Only the contactor itself is non-50Ω (discontinuity)
- The transmission line is lossless

Schematically



Simplifying Assumptions

- A source is connected to a load by a transmission line (contactor) of characteristic impedance of Z_o and length d
- The source Vg and series impedance of Z_g can be thought of an input impedance of Z_i
- The load impedance is Z_L

Transmission Lines

- In circuit theory max power transfer occurs when the load impedance is the complex conjugate of the source impedance.
- In transmission line terms, a line is matched when the load impedance is equal to the characteristic impedance of the line.
- At a mismatch in the impedance, a portion of the power to the load will reflect towards the source. This causes standing waves on the transmission lines.

VSWR

The standing waves on the line yields a couple equations

The voltage reflection coefficient of the load impedance is defined as

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o}$$

The standing wave ratio Vmax/Vmin or VSWR is

$$S = \frac{1 + |\Gamma|}{1 - |\Gamma|}$$

Input Impedance (what the source sees)

At the source end of the transmission line, the generator sees an input impedance of

where

$$Z_i = Z_o \frac{Z_L + jZ_o \tan\beta d}{Z_o + jZ_L \tan\beta d}$$

$$\beta d = 2\pi d/\lambda$$

When the load is a short or open, it can be seen that Z_i will be capacitive or inductive depending on βd

continued

- As frequency increases, the wavelength (λ) decreases, this in turn affects Z_i
- When d = λ/2, $Z_i = Z_o$, the output impedance is transferred to the input
- The ratio of power transferred to power available expressed in dB is Insertion Loss (S_{21})

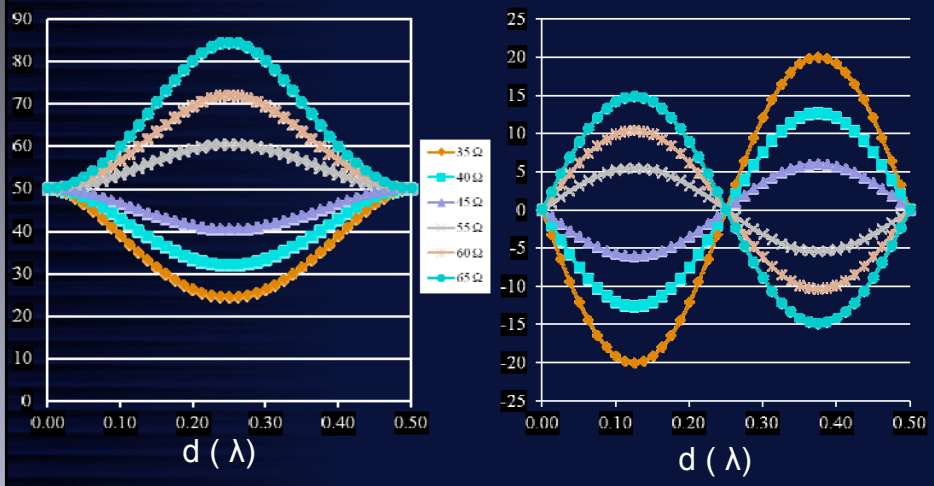
$$IL = -10log_{10}(1 - |\Gamma|^2)$$

- The ratio of power reflected back towards the source expressed in dB is Return Loss (S_{11})

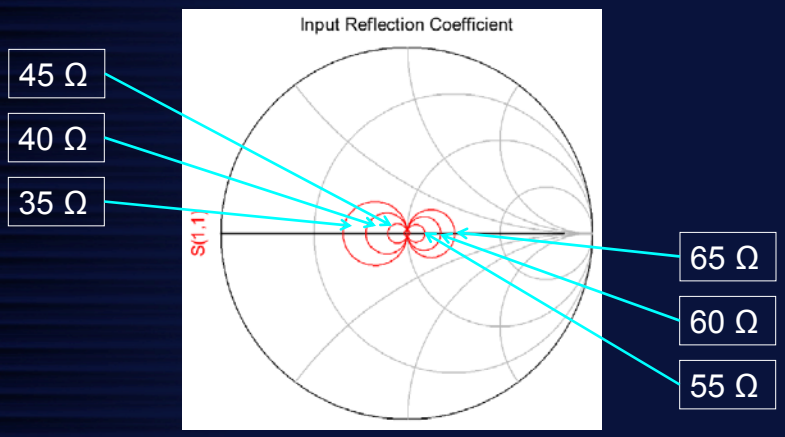
$$RL = -20log_{10}|\Gamma|$$

Effect of d and Z_o on Input Impedance (Z_i)

Real (Z_i) Imaginary (Z_i)



Effect of d and Z_o on Z_i on the Smith Chart



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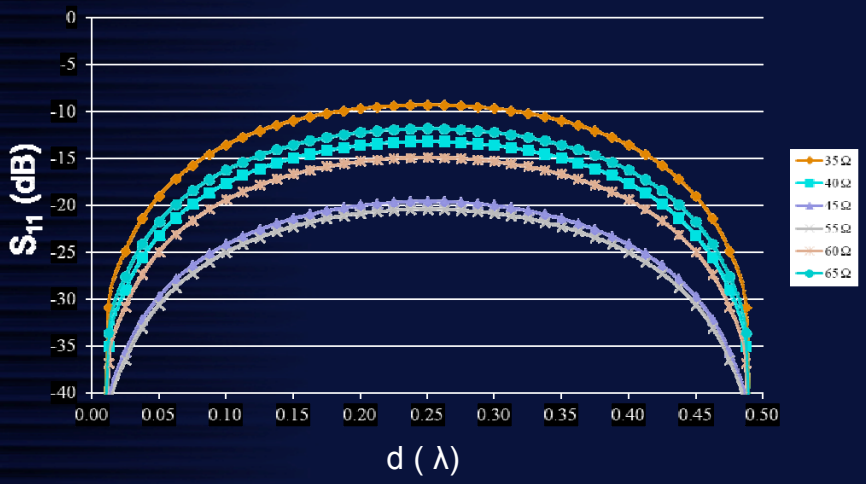
Effect d and Z_o has on Return Loss



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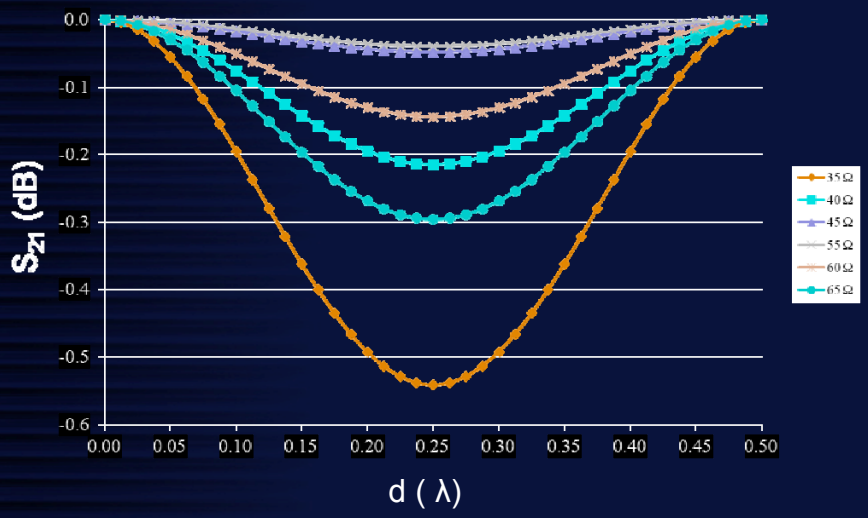
Insertion Loss as a Function of Wavelength



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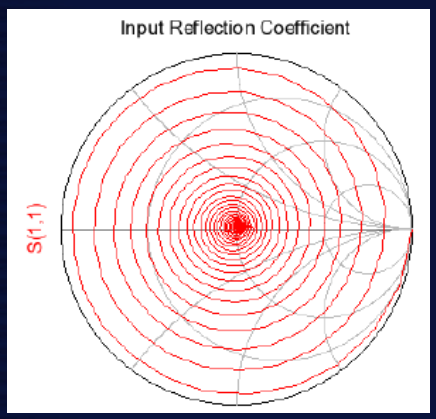
Long Lossy Open Circuit Transmission Line



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Conclusion

- The frequency (wavelength) and characteristic impedance of the contactor changes what impedance the DUT sees
- The impedance can be inductive or capacitive depending on the electrical length
- The frequency of operation makes a difference when dealing with losses and lossy transmission lines
- The higher the frequency, the greater the effect discontinuities will have on the DUT

Contact Optimization for Signal and Power Integrity

Gert Hohenwarter
GateWave Northern, Inc.

2011 BiTS Workshop
March 6 - 9, 2011

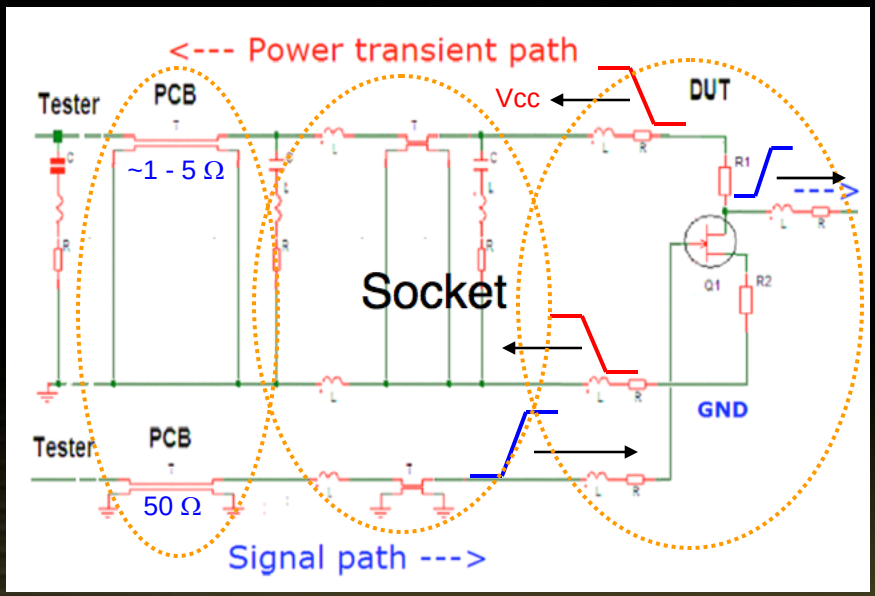
Objective

- Outline basic contact selection criteria for signal and power integrity
- Highlight how parameters interact
- Identify critical parameters
- Show design approach

'Intro'

- Signal integrity:
  - -Provide 'smooth' path for high frequency information transmission events
  - - Allow rapid change of 'states'
- Power integrity:
  - - Prevent propagation of high frequency power transmission events
  - - Prevent 'state' changes

Signal and power path example



Some relevant parameters….

- Impedance Z_o
- Delay t_d
- Capacitance C
- Inductance L
- Mutual elements C_m, L_m

RF

Cross-section
Length
Dielectric mat'ls
Conductor mat'ls
Coatings

Physical

Signal/ground patterns
Power/ground loop size
Plane thermals

Environmental

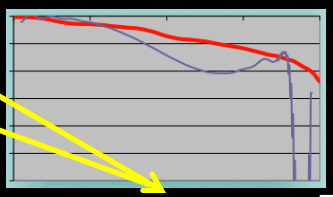
- Resistance Cres
- Thermal performance

DC

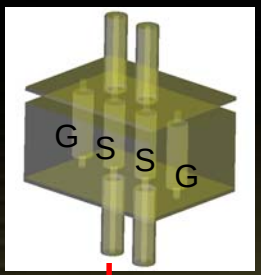
Signal Integrity:

… performance parameters vs. electrical characteristics …

- Insertion loss (S21)
- Return loss (S11)
- Crosstalk (S31, S41)



Port 1 ↓ ↑ Port 3

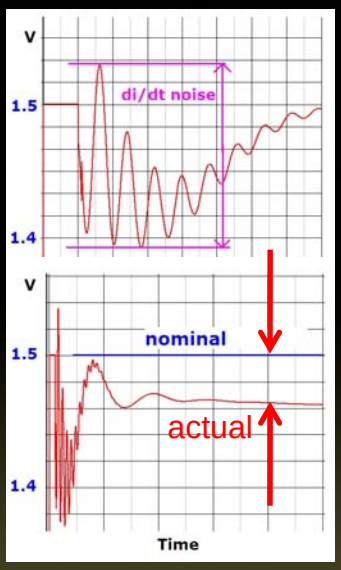


Port 2 ↓ ↓ Port 4

- Impedance Z_o $= \sqrt{L / C}$
- Delay t_d
- Capacitance C
- Inductance L
- Mutual elements C_m, L_m

Power Integrity:
… performance parameters …

- di/dt noise
- voltage drop
- maximum current capability



Power Integrity:
… performance parameters vs. electrical characteristics …

- di/dt voltage -> v = L * di/dt
- voltage drop -> v= R* i
- maximum current capability -> low Rth, Cres

- Inductance L
- Resistance R (Cres) *
- Thermal properties

* It is important to note that the resistance R contains both bulk (body) resistance and resistance at the interfaces as contributors

Trend tables: Electrical vs. mechanical characteristics

	Mechanical parameters			Properties	
Electrical characteristics	diameter	length	pitch	conductivity	dielectric constant
L	vvv	^^	^^	--	--
C	^^^	^^	vv	--	^^
Lm	vv	^^	vv	--	--
Cm	vv	^^	vv	--	^^
Cres	vv	^^	--	vv	--
Zo	vvv	--	^^	--	vv
td	--	^^	--	--	^

Legend:

An increase of the table parameter results in the following change ---->

^^^	strong increase
^^	increase
--	neutral
vv	decrease
vvv	strong decrease
v^	either way

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Trend tables: Electrical characteristics vs. performance

	Electrical parameters						
Performance parameters	L	C	Lm	Cm	Cres	Zo	td
S11	v^	v^	v^	v^	--	v^	--
S21	v^	v^	v^	v^	--	v^	--
S41	v^	v^	v^	v^	--	--	^
didt	^	--	--	--	^	--	--
Zpds	^	--	--	--	--	--	--
Rdc	--	--	--	--	^	--	--
Qdot	--	--	--	--	^	--	--

These tables are based on basic mathematical relations and frequently observed responses- they are only meant to serve as a guide.

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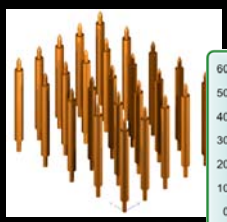
Trend tables: Physical characteristics vs. performance

	Mechanical parameters			Properties	
Performance parameters	diameter	length	pitch	conductivity	dielectric constant
S11	v^	^	v^	--	v^
S21	v^	^	v^	--	v^
S41	v^	^	v^	--	v^
didt	v	^	^	--	--
Zpds	v	^	^	--	--
Rdc	v	^	--	v	--
Qdot	v	^	v	v	--

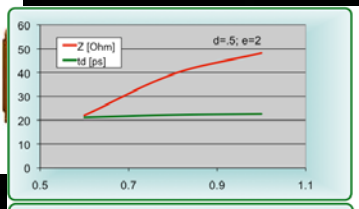
These tables are based on basic mathematical relations and frequently observed responses- they are only meant to serve as a guide.

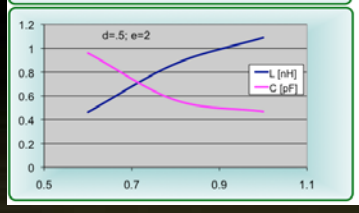
Impact of dimensions

Pitch and diameter

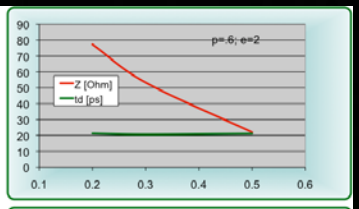


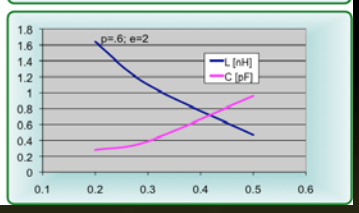
Pitch





Diameter





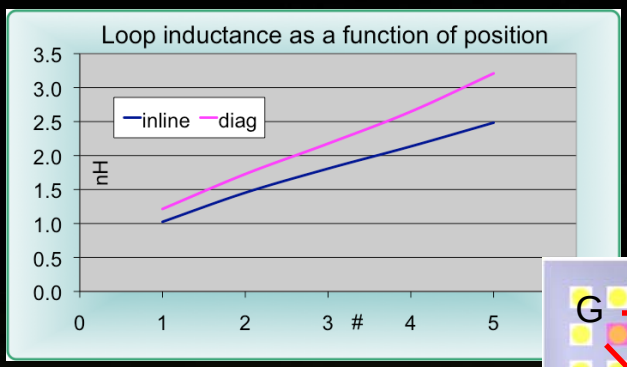
Mutuals will change significantly, too

Impact of dimensions

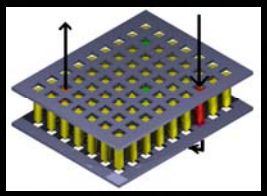
Length (simulated result)

Except for an offset at 0 length due to 'current spreading' inductance is essentially proportional to length.

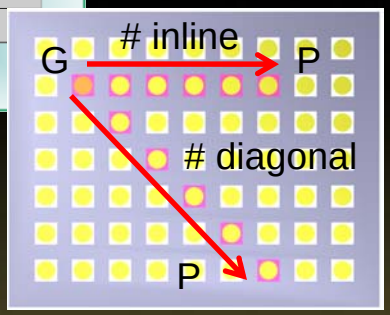
Impact of configuration on inductance



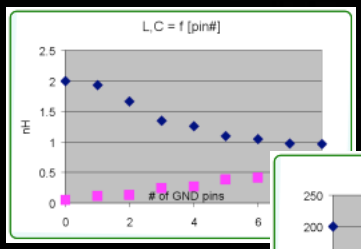
Loop inductance between ground pin and power pin as a function of distance between pins



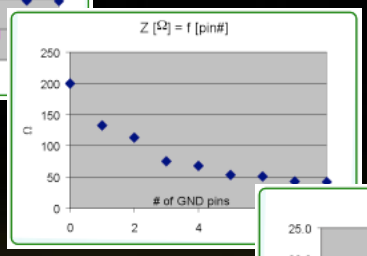
Current flow

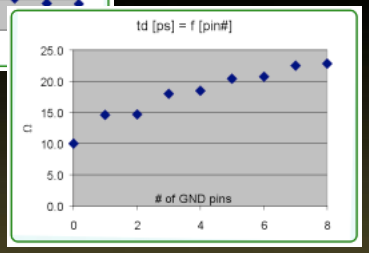


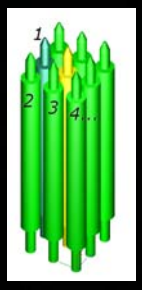
Impact of number of ground pins



L decreases, C increases



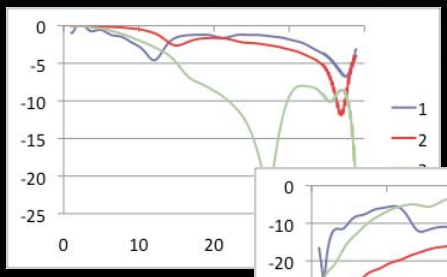




Z shows dramatic initial decrease but flattens when more than 2 ground pins are present

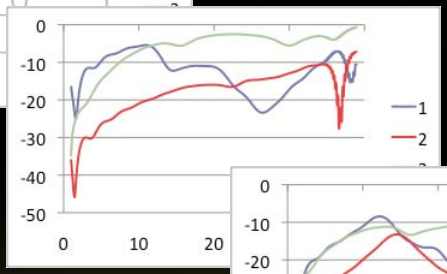
Impact of pin dimensions on SI

S21



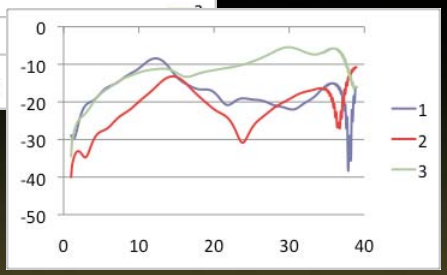
Insertion loss

S11



Return loss

S41



Forward crosstalk

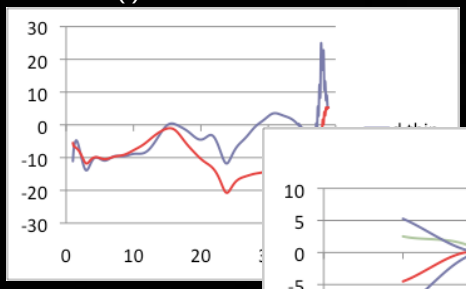
1 – slender

2 – nominal

3 – voluminous

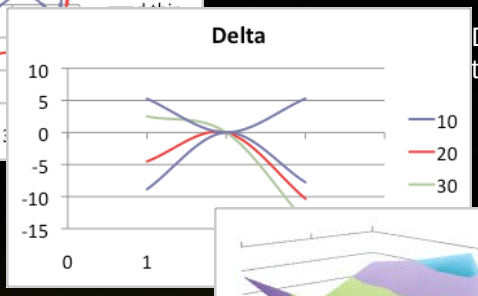
SI sensitivity assessment options

Delta= f(f)



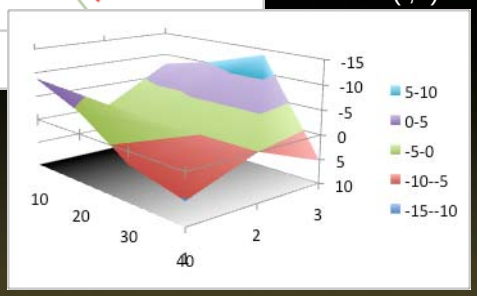
Insertion loss

f(#)



Difference to 'nominal'

f(f,#)



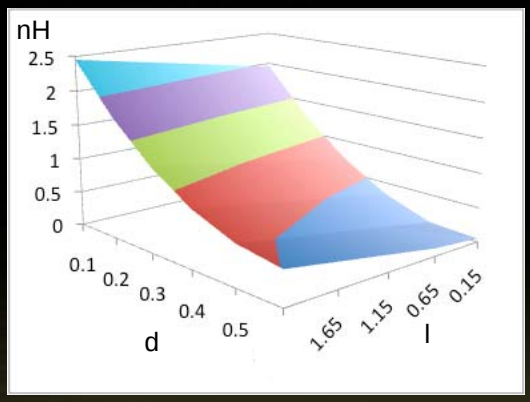
Alternate visualizations allow for design optimization via sensitivity and 'sweet spots'

3D representation

Impact of pin dimensions on PI

L= f (dia, pitch) [nH]

V_{noise} ~ length, di/dt



The boundaries in the 3D representation define design limits

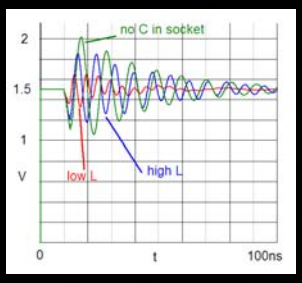
Contact selection
… how to…

- Define design envelope, parameters
  - Example: Determine di/dt limits for L (see slide 18)
- Find socket sensitivities [simulated, measured]
  - Use Z models (see slide 12) to get approach 50 Ohms
- Set up path models in SPICE
  - Find best S21, S11 and 41 socket performance (slide 16)
- Verify SI, PI overall system performance

Contact selection
… comments derived from 'daily' practice…

- DUT parameters and limits must be known
- PI may supersede SI if signal integrity performance is close to target
- Contact length, lateral dimensions are most important parameters for power integrity
- Contact 'bulk' and dielectric constant are likely the most important parameters for SI

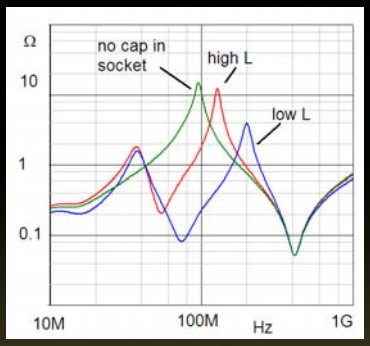
Is a short contact really the best PI solution?

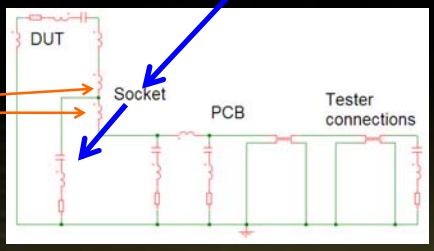


di/dt
Voltage noise

In-socket bypass capacitor

Z(f) Impedance

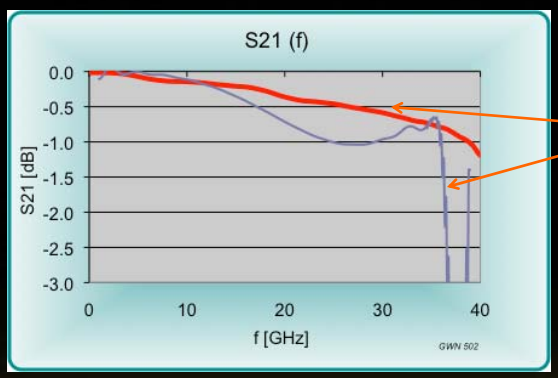




Top
Bottom

PI depends on what criteria are applied and can not be globally assessed

SI caveat: S21 insertion loss simulation vs. measured performance



Measured
Simulated

Surprisingly, measured performance is better than simulated.

Cause: At high frequencies the dielectric properties deviate from the values published for low frequencies

Conclusion

- Socket design, analysis and measurement for SI is straightforward
- Socket design, analysis and measurement for PI requires good understanding of operating environment
- Socket optimization for a given application will likely be case specific
- Careful overall system analysis is a must

A Complete High Frequency Interconnect Scheme for Testing >20GB/s Interfaces

Thomas P. Warwick, Director of Signal Integrity
Thomas Smith, Lead Process Engineer
Dan Turpuseema, Director of Engineering

R&D Circuits

2011 BiTS Workshop
March 6 - 9, 2011

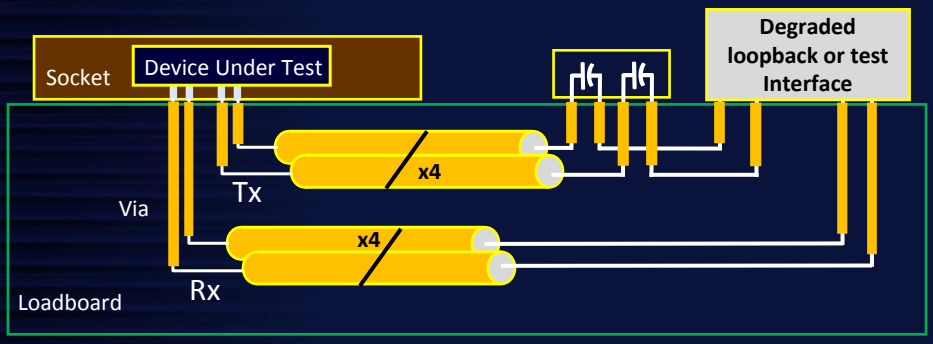
1) Purpose and Outline

Purpose –
To outline the forthcoming challenges for very high data rate devices and to discuss emerging technologies that help address these issues.

Outline –

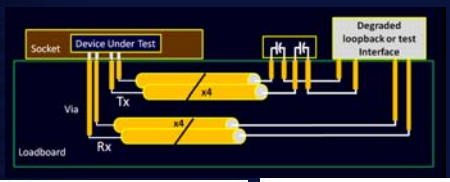
- Understanding the unique challenges of >20GB/s data rate applications
- The Test Philosophy and its interconnect Implications
- Common Industry Limitations
- Emerging Solutions with Test and Simulation Data
- Concluding Comments

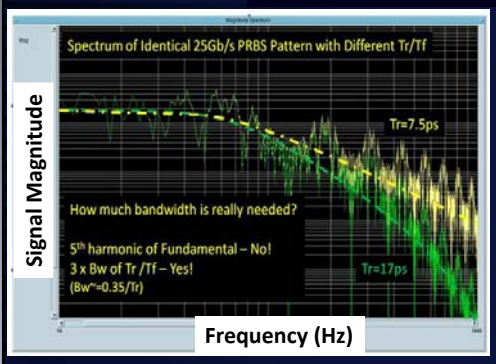
2) Understanding the 25Gb/s Problem: Jitter and Bandwidth Considerations

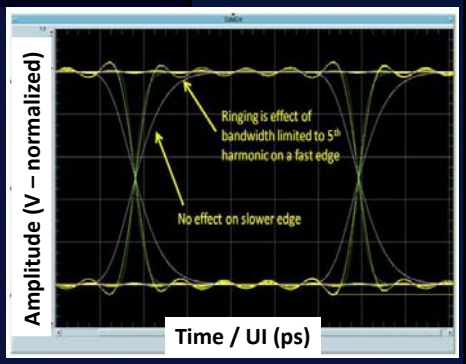


Assumed Test Setup [1]

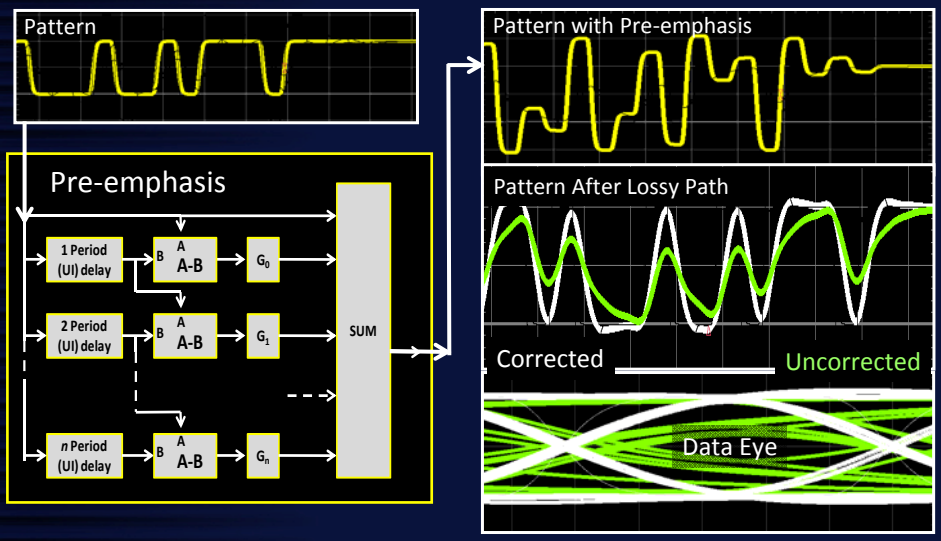
2) Understanding the 25Gb/s Problem: Jitter and Bandwidth Considerations







2) Understanding the 25Gb/s Problem: Equalization / Pre (de) emphasis [1]



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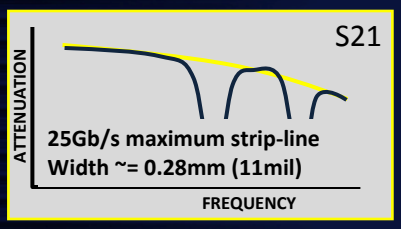
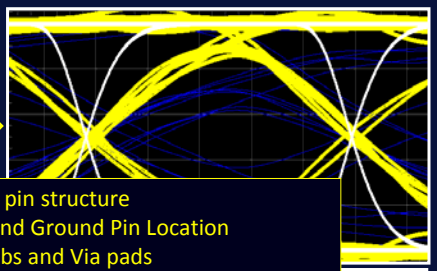
2) Understanding the 25Gb/s Problem: Problems for Equalization Data Correction

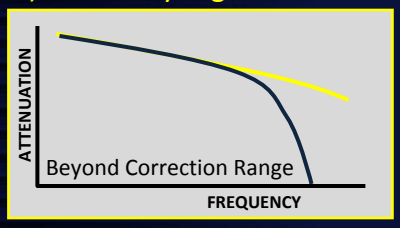
1) Resonant Structures

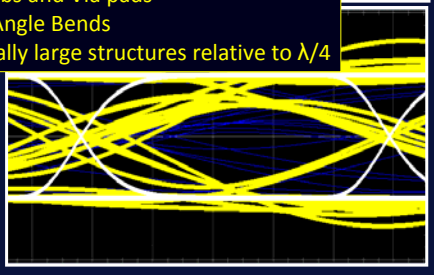




→Socket pin structure
→Pitch and Ground Pin Location
→Via stubs and Via pads
→Right Angle Bends
→Physically large structures relative to λ/4

2) Extremely High Loss





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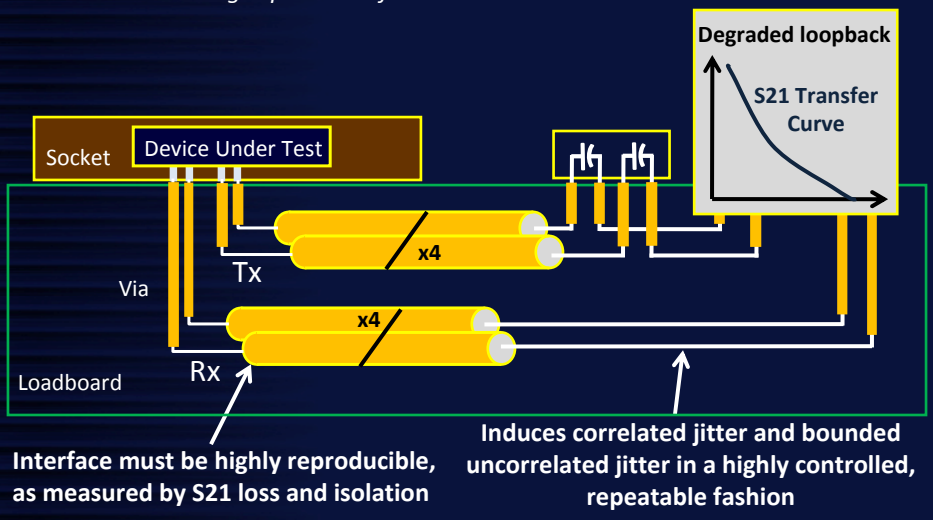
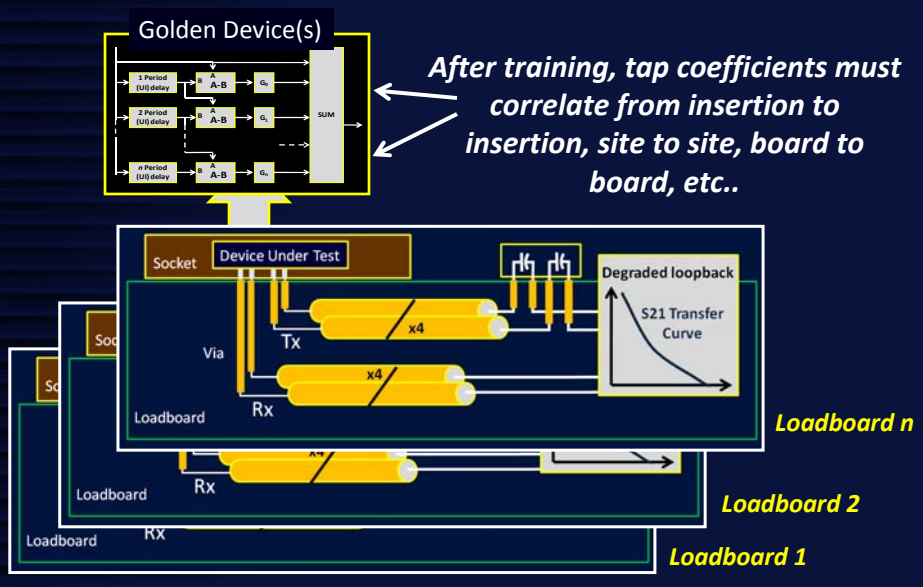
3) The Test Philosophy: An Overview

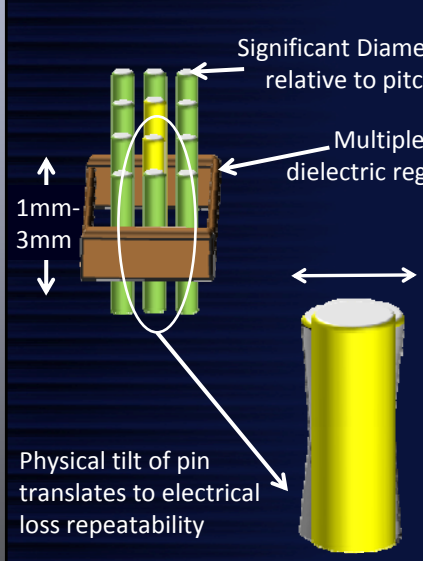
This philosophy has been presented for discussion purposes. Any external test of a high speed interface will encounter these issues.

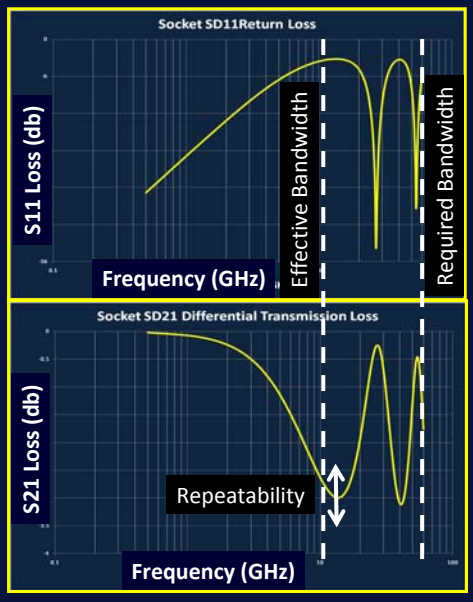


3) The Test Philosophy: Hardware Concerns [2]



4) Problems in the Industry: Sockets



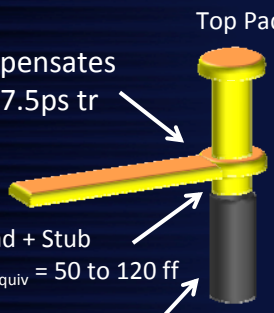


S21: 0.3db to 1 db typical @ 20GHz

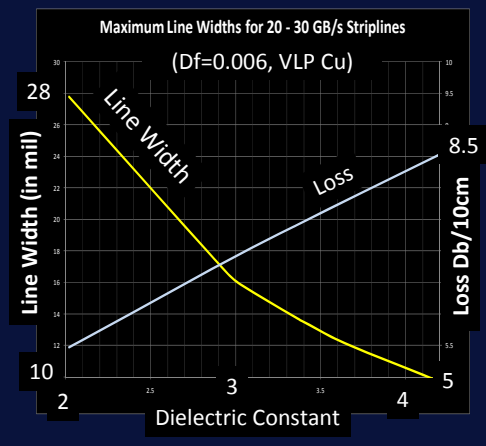
4) Problems in the Industry: PC Board Losses

Via Structure and Right Angle Joint

(Growing Concern)

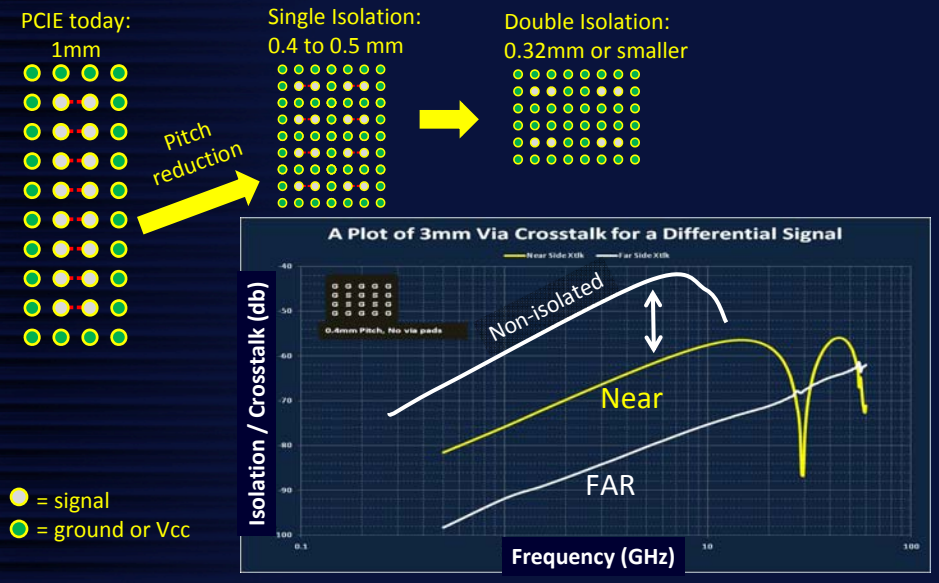


Line Loss



Higher frequency limits line width!

4) Problems in the Industry: Pitch and Pin-out



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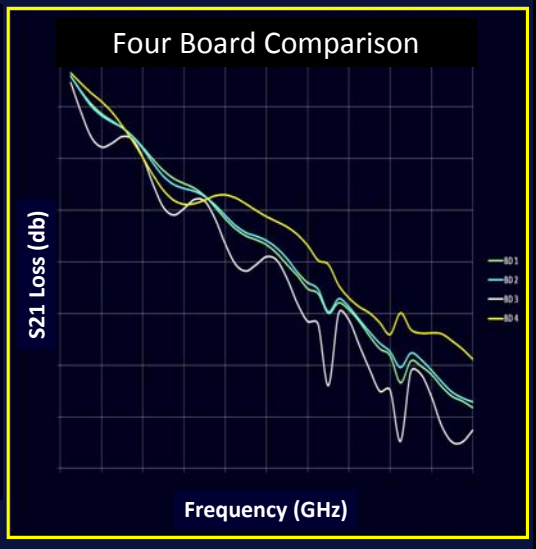
4) Problems in the Industry: Repeatability

PC board Process Variations [2]

1. *Thinner Lines* for Higher Speeds
2. Etch Tolerance
3. Material Thickness Tolerance
4. Within Sheet Thickness Variation
5. Material Weave and Dielectric Variation
6. Metal Plate Variation
7. Regional Variation within a Board
8. Copper Roughness



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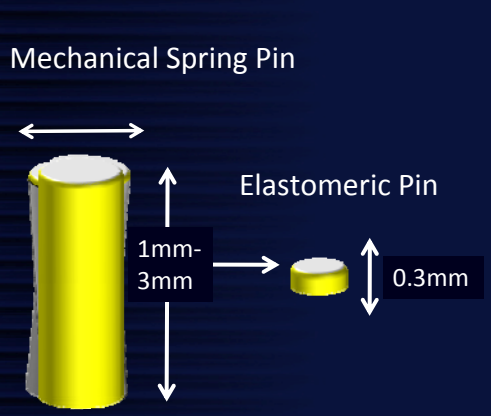
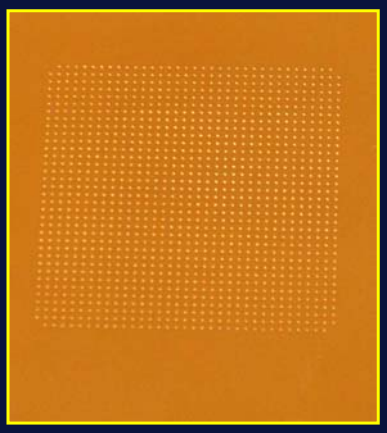
5) Emerging Solutions: Elastomeric Sockets

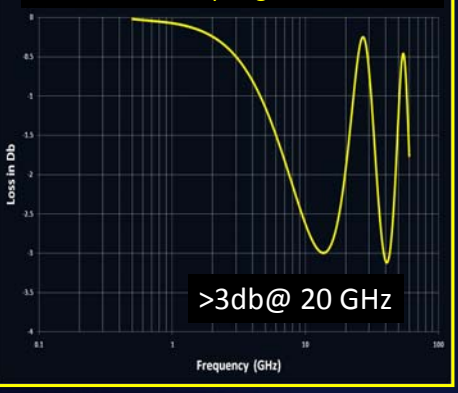




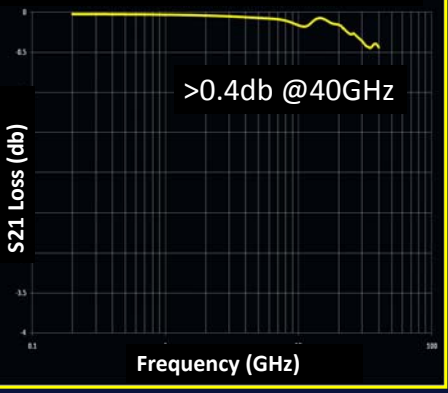
Elastomeric Socket Interface
0.4mm pitch, >40GHz Bandwidth

5) Emerging Solutions: Elastomeric Sockets

Conventional Spring Probe Socket



Next Generation Elastomeric Socket

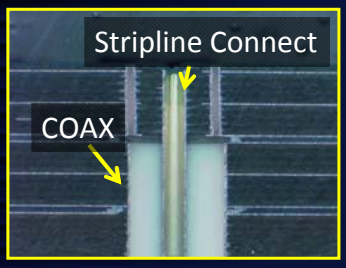


Pogo Pin Style Socket
0.4mm pitch, ~15 GHz Bandwidth

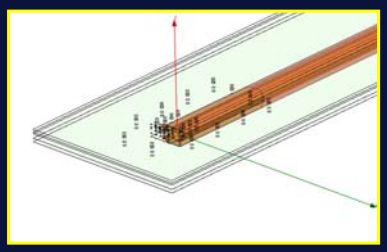
Elastomeric Socket
0.4mm pitch, >40 GHz Bandwidth

5) Emerging Sol'n: Embedded Coax Structures

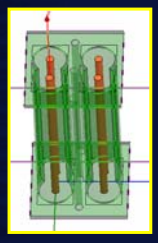
Coaxial Via SEM



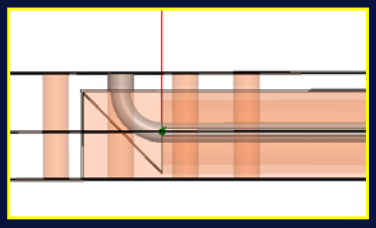
Horizontal Coaxial Structure



0.4mm Twin Axial Via



High Performance Right Angle Bend



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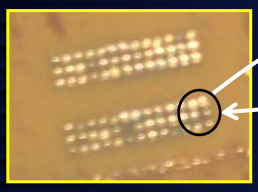
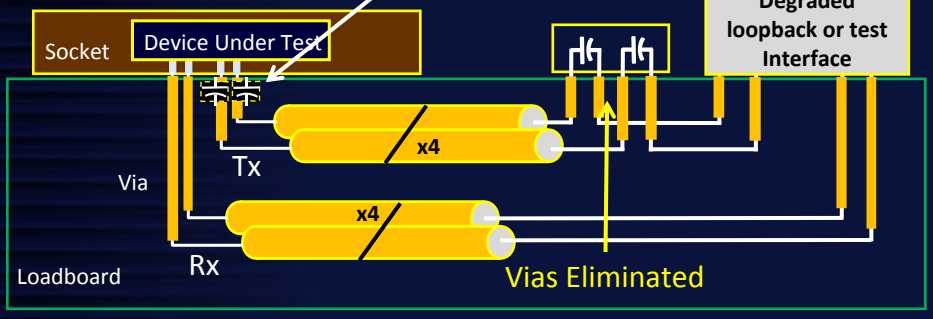
5) Emerging Sol'n: Embedded Coupling Caps



Vertically Embedded Component

Coupling caps physically reside within the pc board



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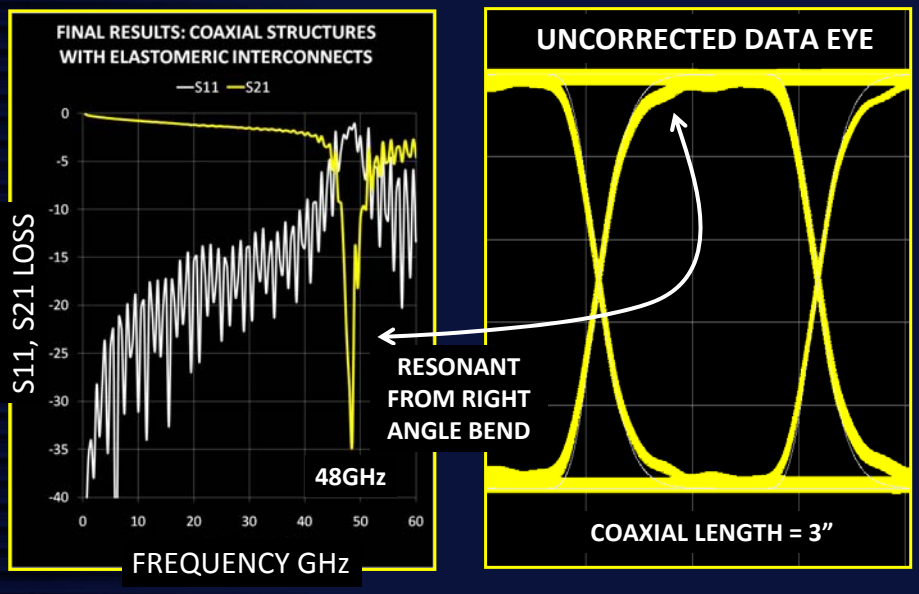
5) Emerging Solutions: Results



6) Concluding Comments

- >20GB/s data transmission will require greater consideration of common high speed concerns, such as socket interfaces, vias, trace loss, and crosstalk.
- Some significant growing and new concerns include trace tolerance, required use of thinner lines (and thus higher losses), resonant structures, and much greater bandwidths.
- The test environment must now be evaluated on repeatability and duplication, not just absolute error.
- Emerging technologies do provide a repeatable path to >20GB/s. These include ultra low profile sockets (elastomers), embedded coupling capacitors, coaxial / twin axial vias, and embedded coaxial structures.

Acknowledgements

The authors wish to acknowledge or reference:

Dane Thompson, PhD, Ansys Corporation, for his patient assistance in helping with 3D EM modeling (Ansoft HFSS).

Hongjun Yao, PhD, Qualcomm Corporation, for his tutorials on pitch and pin-out patterns.

David Waite, PhD, Qualcomm Corporation, for his assistance with PC board process variation issues.

(1) Moreira, J., and Workmann PhD, H., Automated Testing of High Speed Interfaces, Artech House, Norwood, MA,© 2010, ISBN 13 978-1-060783-983-5

(2) Warwick, T., Turpuseema, D., "The Quest for the Perfect Loadboard: Understanding the Issues and Technology Advances in Device-to-Tester Interface Assemblies" Proceedings of the 2010 Silicon Valley Test Conference, San Jose, CA, Nov. 8, 2010

Frequency-Domain and Time-Domain Impact of Spring-Probe Socket Geometry on High-Speed IO Testing

Se-Jung Moon
Selim S. Akbay, Mustapha Abdulai
Intel Corporation

2011 BiTS Workshop
March 6 - 9, 2011

Outline

- Motivation
- Procedure
- Spring Probe Socket Model
- Socket Model and Measurement Correlation
- DOE for Socket Parameter Impact Analysis
- Result
- Conclusion and Future Work

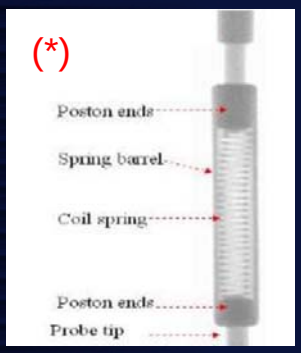
Motivation

- Need to understand spring-probe socket to establish secured SI environment on a testing board from the design level.
- Need to find key parameters that affect socket performance and the high-speed IO channel performance to optimize the socket design.

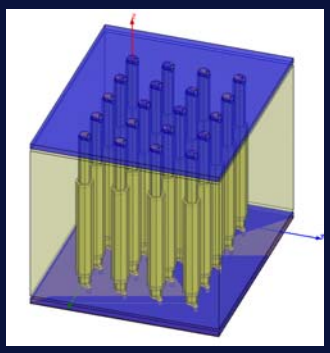
Procedure

- A spring probe socket model was built in 3D EM solver and its accuracy is verified by measurement data.
- We adapted Response Surface Modeling method as a DoE (Design of Experiment) to measure the impact of socket parameters on socket/high-speed bus performance.

Spring-Probe Socket Model



X-ray picture of spring-probe pins

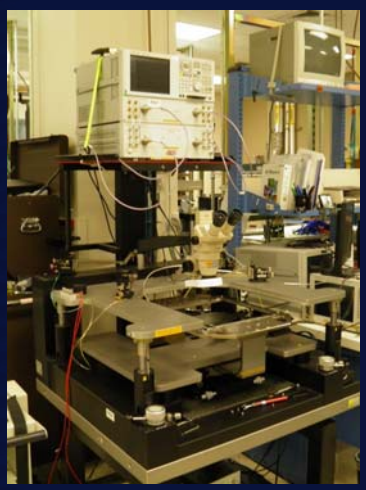


3D EM socket model

- In this numerical model, no cavity and no spring is inside the pins.

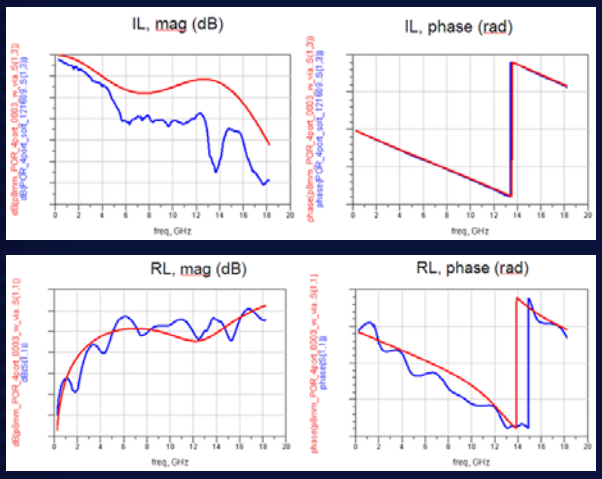
(*) is captured from http://www.ems007.com/pages/zone.cgi?a=60561&artpg=78&topic=0

VNA Measurement

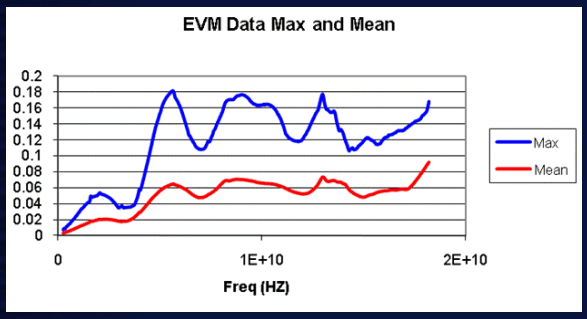


Socket Model Validation

Blue: meas. data
Red : model data

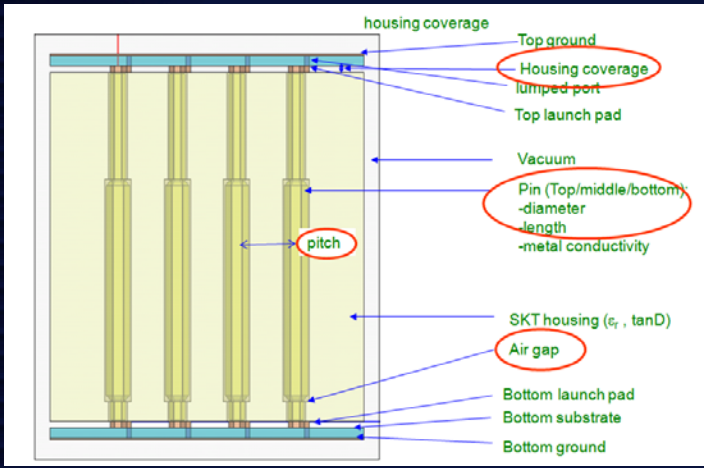


EVM (Error Vector Magnitude)



EVM values are less than 0.2 overall frequency region up to 18.25GHz, which supports model accuracy.

List of Socket Parameters



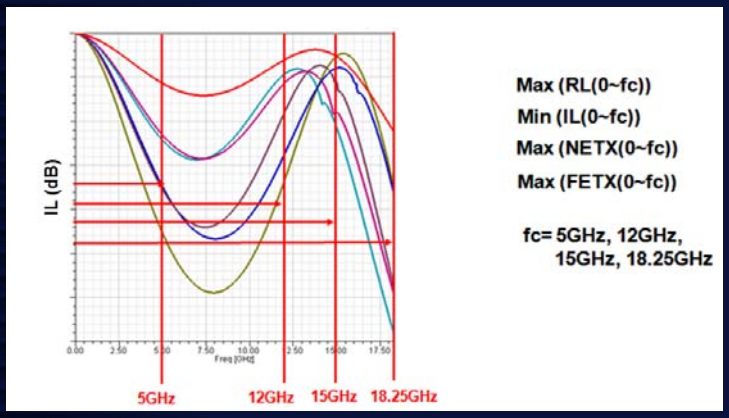
9 Parameters under Consideration

- 9 parameters in the previous slide are used for DOE screening
- 4 parameters are selected for impact analysis:
  1. Pin Middle length
  2. Pin Middle Diameter
  3. Airgap
  4. Pitch

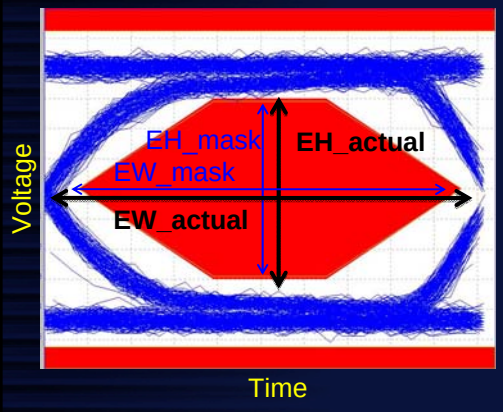
DOE Parameters and Settings

- Take the typical values of 4 parameters and tweak the parameters with 10% of the typical values.
- 10% is small enough for RSM (Response Surface Methodology) and larger than manufacturing tolerance to see design to design variation.

Frequency Domain Metric

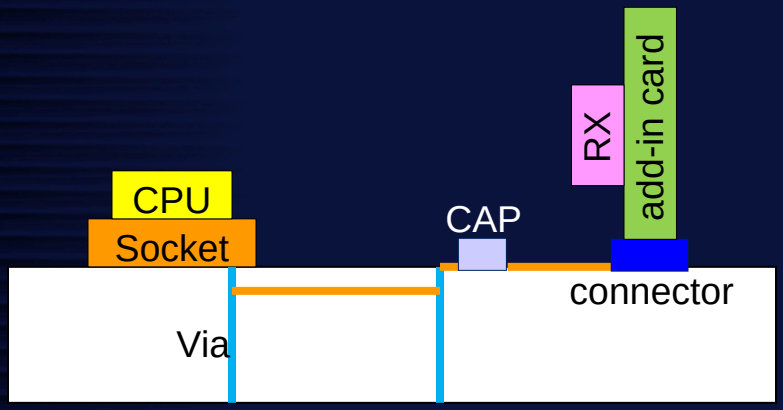


Time-Domain Metric



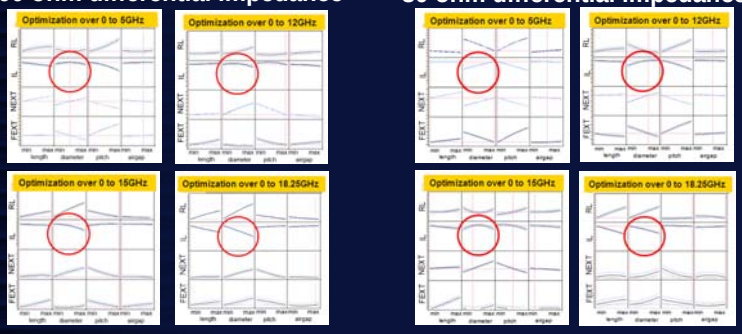
EH_actual – EH_mask = Vmargin
EW_actual – EW_mask = Tmargin

PCIe Gen3 Topology



Optimization in Frequency-Domain Metric

100 ohm differential impedance **80 ohm differential impedance**



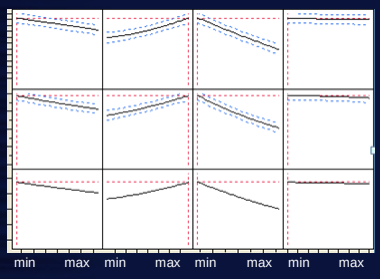
Depending on the impedance and the frequency region, the optimized design structure changes.

Optimization in Time-Domain Metrics

Vmargin

Tmargin

Desirability



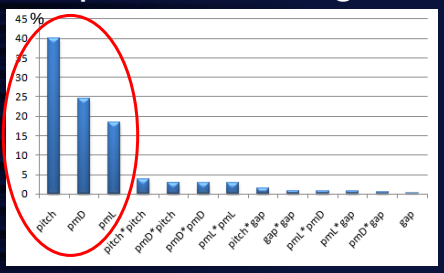
ΔVmargin = 20mV

ΔTmargin = 0.02UI

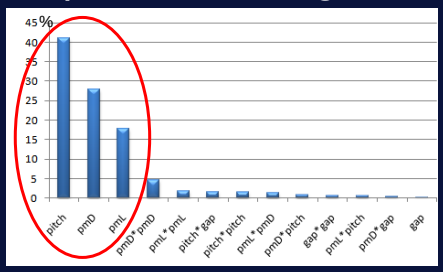
This optimized design matches with the optimized design form in FD metrics with 80 ohm termination over 0-5GHz.

Impact of Parameters on Eye Opening (Pareto Plot)

Impact on Vmargin



Impact on Tmargin



Pitch, pin diameter and pin length have highest impact in order.

Conclusion

- Pitch has highest impact on Vmargin and Tmargin.
- At one pitch, pin diameter and pin length have highest impact on the PCIe Gen3 performance on our actual testing board. As pin length (pin radius) decreases (increases), Vmargin and Tmargin increases.
- To optimize the socket performance based on the frequency-domain metric, the differential characteristic impedance for the socket S parameter should match with PCIe gen 3 impedance. Also, socket design optimization over 0 to 5 GHz range of the fundamental frequency matches with the one in time-domain metric.

Future Work

- Expand this study for single-ended interconnect.
  ex. DDR3/4, GDDR, etc.
- Extend ranges of DOE design corners.
- Seek a new type of metric to evaluate the socket performance properly without the full channel simulation.
  ex. TDR, etc.

Acknowledgement

- **Brett Grossman**
- **Evan Fledell**
- **Erkan Acar**
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- **Tomas Ruttan**