BiTS™ Burn-in & Test Socket Workshop 2011 Market Update

ARCHIVE 2011

IC PACKAGE MINIATURIZATION AND SYSTEM IN PACKAGE (SiP) TRENDS

by

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ABSTRACT

This brief packaging market overview presentation will provide a perspective of overall IC package trends. A short discussion on fine pitch leadframe packages, Wafer Level CSP trends, and System-In-Package (SiP) evolutions such as stacked die, Package on Package (PoP), and 3D TSV will provide a global perspective of market sizes and adoption rates.

IC PACKAGE MINIATURIZATION AND SIP TRENDS

Brandon Prior
Prismark Partners

2011 BiTS Workshop
March 6 - 9, 2011

PACKAGE SIZE REDUCTION AND SYSTEM IN PACKAGE (SiP)

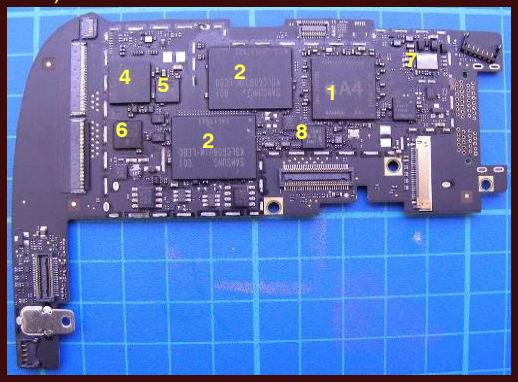
- System Level Size Reduction
  - Mobile Consumer Electronics (Notebooks, Media Tablets, Smartphones, etc.) are representing an ever increasing portion of electronics value, and have been driving package roadmaps for the last fifteen years
  - Although system size is no longer decreasing dramatically, the area and volume allocated to PCB assembly is getting squeezed out in favor of larger battery, display, and overall thinner systems
- Package Size Reduction
  - Array Packages and Pitch reduction (0.5 → 0.4 → 0.3mm)
  - Wafer Level CSP – the Package-less Package
- SiP Approaches
  - Adoption of stacked die and package stacking was first phase of 3D
  - 3D TSV and Silicon Interposers will be the "package" challenge over the coming decade

APPLE iPad MAIN BOARD ASSEMBLY

510.10/360bp

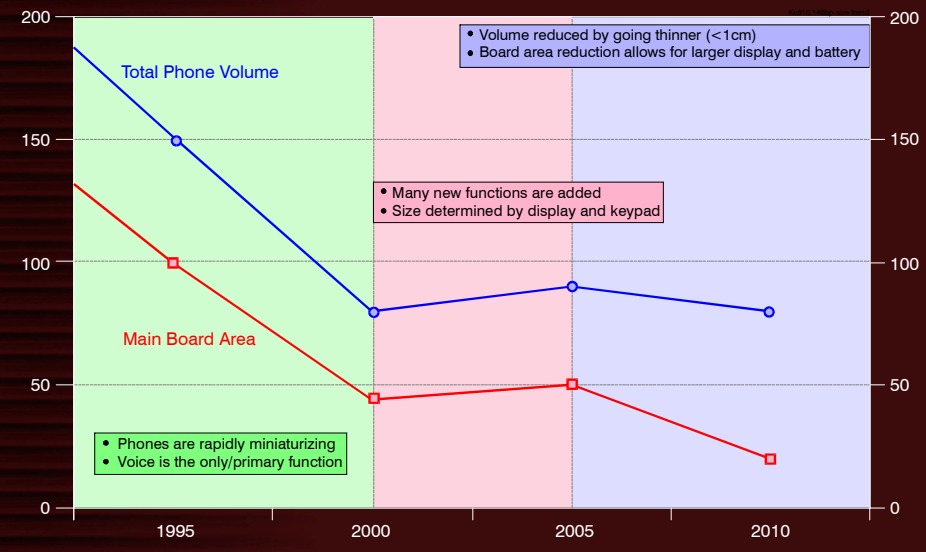
- 1-8-1 Microvia Main Board Assembly
  - 12 x 5cm, plus 4 x 1cm extension
  - 790μm PCB thickness, 630μm core
  - PCB is 15% of iPad area and 4% of volume

1. Apple/Samsung A4/SDRAM PoP: 14 x 14 x 1.2mm
2. Samsung 8GB NAND Flash: 14 x 18 x 0.6mm
3. Dialog Power Manager (backside)
4. Broadcom Touch Controller: 10 x 10 x 1.25mm
5. Broadcom Touch Driver
6. TI Touch Driver
7. Cirrus Audio Processor
8. NXP Display MUX/DEMUX



03/2011 IC Package Miniaturization and SiP Trends 3

MOBILE PHONE SIZE TRENDS



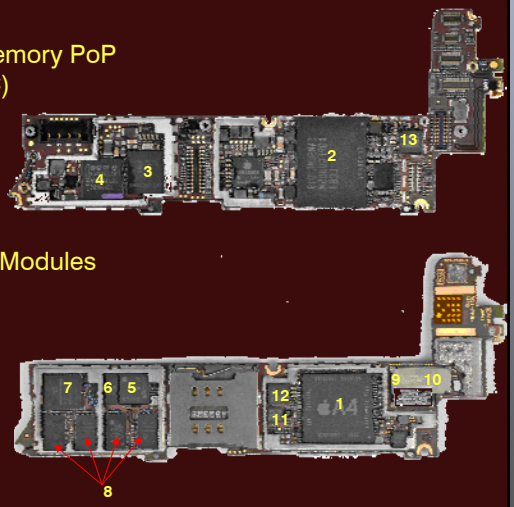
03/2011 IC Package Miniaturization and SiP Trends 4

iPhone 4 MAIN BOARD ASSEMBLY

610.4/062jpp

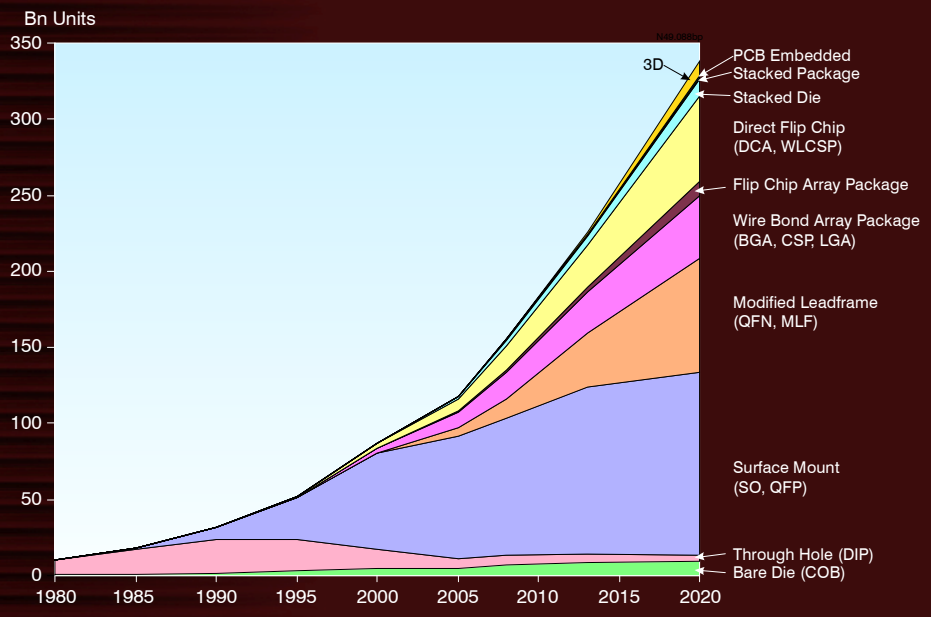
- 10cm x 2cm L-Shaped Main Board
  - Double-Sided assembly
  - 4-2-4 microvia

1. Apple A4 Processor/Samsung Memory PoP
2. Samsung 16-32GB NAND (eMMC)
3. Infineon Baseband
4. Numonyx Memory
5. Infineon RF Transceiver
6. Murata LNA Module
7. Skyworks GSM Transmit Module
8. Skyworks/TriQuint WCDMA PAiD Modules
9. Broadcom WLAN/BT/FM
10. Broadcom GPS
11. STMicro Gyroscope
12. STMicro Accelerometer
13. TI Touch Controller



03/2011 IC Package Miniaturization and SiP Trends 5

IC SHIPMENTS BY PACKAGE CATEGORY



03/2011 IC Package Miniaturization and SiP Trends 6

0111.1/086bp

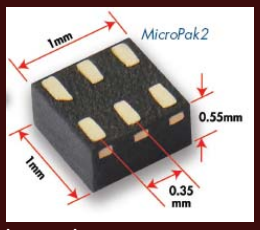
TRANSITION TO 0.4mm PITCH PACKAGES

- Leadframe packages (TSOP, QFP) have used 0.4mm pitch for a long time
  - QFN, FBGA, and WLCSP packages in high volume production at 0.4mm and 0.35mm
  - Sub-0.4mm packages used in limited applications thus far
- All subcons and leading QFN users offering 0.4mm pitch designs
  - 0.35mm pitch availability from Carsem, Fairchild, NXP, and others
- Reliability/feasibility testing ongoing at OEMs and package assemblers
  - Wafer CSP at 0.3mm or below
  - FBGA at 0.3 and 0.35mm for high leadcount devices
- Demand for sub-0.4mm pitch packages
  - Prismark forecast calls for >20% of FBGA/WLCSP to be 0.4mm or less pitch by 2015
  - Challenges remain PCB routing and assembly yield/process/ materials at 0.3mm pitch and below

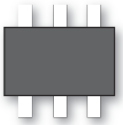
FAIRCHILD MicroPak2™

0111.1/115bp

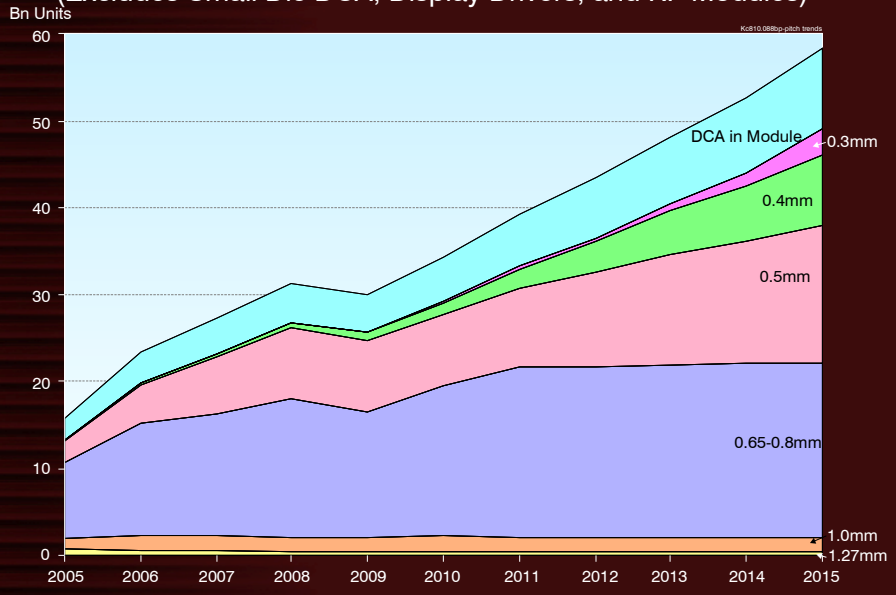
- MicroPak2 is a small QFN style package offering
  - 1.0 x 1.0mm six-lead package
  - 0.35mm pitch
  - 0.55mm mounted height
- Offered since 2005/2006
  - Limited acceptance prior to 2008
  - Today have over fifty devices considered for this package



Fairchild Offers a Variety of Industry Leading Packages

Package Migration Comparison and Options			
Measurements (mm)	**SC70-6**	**MicroPak-6**	**MicroPak2-6**
Mounted Width	2.10	1.00	1.0
Body Width	1.25	1.00	1.0
Length	2.00	1.45	1.0
Height	0.90	0.55	0.55
Pin Pitch	0.65	0.50	0.35

ARRAY PACKAGE PITCH TRENDS (BGA, CSP, PGA, LGA, WLCSP)
(Excludes Small Die DCA, Display Drivers, and RF Modules)



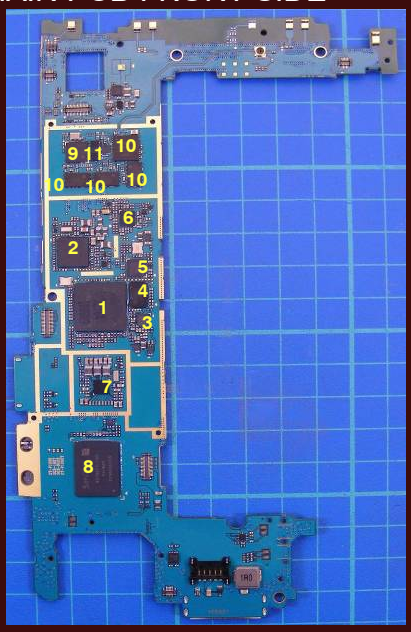
Note: Sub 0.5mm was 2% of overall volume in 2008. By 2015 this will increase to 19% or 11Bn units

03/2011 IC Package Miniaturization and SiP Trends 9

SAMSUNG GALAXY TAB – MAIN PCB FRONT SIDE

1110.10/360bp

1. Samsung APP/Memory PoP:
2. 14 x 14 x 1.5mm U/F
3. Infineon Baseband Processor:
4. 9 x 9 x 0.8mm FCCSP, U/F
5. Silicon Image HD Link
6. TI LVDS
7. Samsung Display Driver
8. Wolfson Audio Codec:
9. 4.5 x 4.0mm WLCSP, no U/F
10. Maxim Power Management:
11. 4.2 x 4.2mm WLCSP, no U/F
12. SanDisk 16GB NAND (eMMC)
13. Infineon HEDGE Transceiver
14. TriQuint Transmit Modules, U/F
15. Infineon LNA

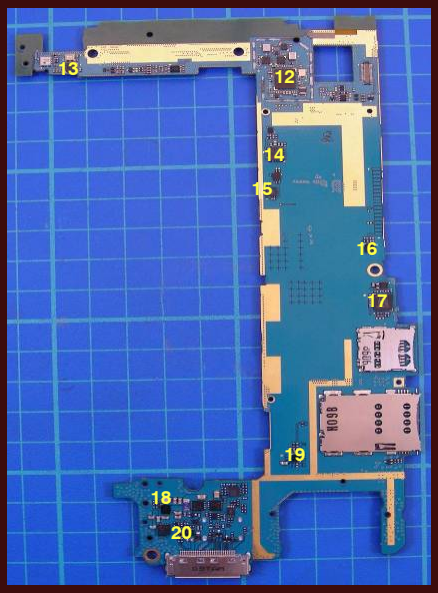


03/2011 IC Package Miniaturization and SiP Trends 10

1110.10/360bp

SAMSUNG GALAXY TAB – MAIN PCB BACK SIDE

12. Broadcom BT/FM/WLAN: 6.5 x 5.5 mm WLCSP, No U/F
13. Broadcom GPS: 2.9 x 2.8 mm WLCSP, no U/F
14. ST Gyro
15. Bosch Accelerometer
16. AKM Compass
17. Atmel Touchscreen Controller: 4.9 x 4.9mm WLCSP, no U/F
18. Summit Battery Charger: 2.8 x 2.4mm WLCSP, no U/F
19. Unknown: 2.1 x 2.0mm WLCSP, no U/F
20. Unknown: 1.2 x 1.5mm WLCSP, no U/F



89.1/105bp

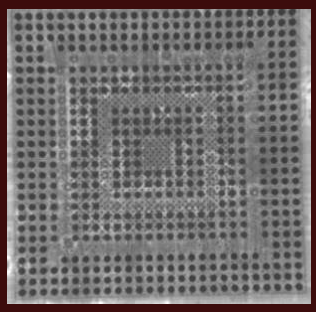
SiP/MCP FORECAST

Product/Package Type Volume (Bn Units)	2010	2015 Forecast	Leading Suppliers/Players
Stacked Die In Package	5.7	8.5	ASE, SPIL, Amkor, STATS ChipPAC, Samsung, Micron, Hynix, Toshiba, SanDisk
Stacked Package on Package (PoP/PiP)	0.49	1.0	Amkor, STATS ChipPAC, ASE, SPIL, TI, Samsung, Renesas, Sony, Panasonic
PA Centric RF Module	2.1	3.8	RFMD, Skyworks, Anadigics, Renesas, TriQuint
Connectivity Module (Bluetooth/WLAN)	0.4	0.7	Murata, SEMCO, Panasonic, Taiyo Yuden
Graphics/CPU or ASIC MCP	0.11	0.2	Intel, IBM, Fujitsu
Leadframe Module (Power/Other)	1.8	2.9	NXP, STMicro, TI, Freescale, Toshiba, NEC, Infineon, Renesas, IR, ON Semi
TOTAL	10.6	17.1	

SAMSUNG HUMMINGBIRD

1110.6/193bp

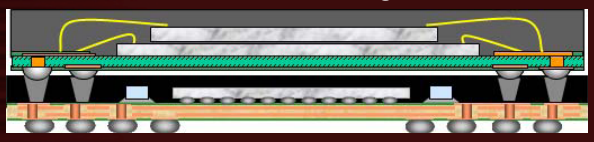
- Samsung Hummingbird (S5PC110A01) Application Processor
  - ARM Cortex A8 core operating at 1GHz
  - 14 x 14 x 1.5mm; Underfilled
- Bottom Package: Application Processor
  - 600 balls at 0.5mm pitch
  - ~600 SnPb bumps, 200μm pitch, 65μm standoff height
  - 8 x 8 die, 100μm thick
  - 1-2-1 substrate, 320μm thick, 25μm L/S
- Top Package – 4 Memory Die
  - 8Gb OneNAND, 4Gb Mobile DDR, 2Gb OneDRAM
  - Up to 288 balls at 0.5mm pitch
  - 50, 60, and 90μm thick



Photos source: Prismark/Binghamton University

AMKOR PoP WITH THROUGH MOLD VIAS (TMV)

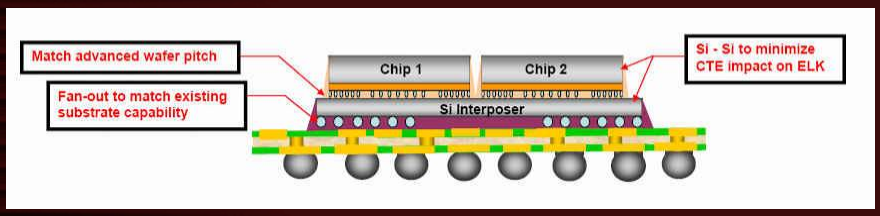
- Uses standard FBGA package with wire bond, flip chip, or stacked die
  - After molding, blind via created through mold compound to expose bond pads on package substrate
  - Vias filled with conductive material to help attach top solder balls
- Two key advantages
  - Eliminates warpage problems as entire package is molded
  - Enables reduced pitch on top package
- Test vehicle uses 14 x 14mm size
  - 620 balls at 0.4mm pitch bottom package
  - 200 balls in two rows at 0.5mm pitch top package
- Production started Q3 2010 on two design wins



710.5/294bp

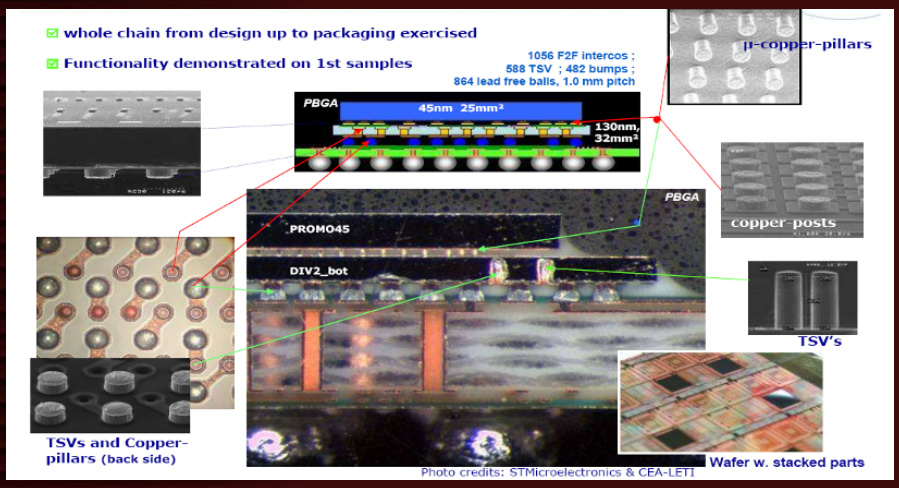
Si INTERPOSER VIEWPOINT – ASE

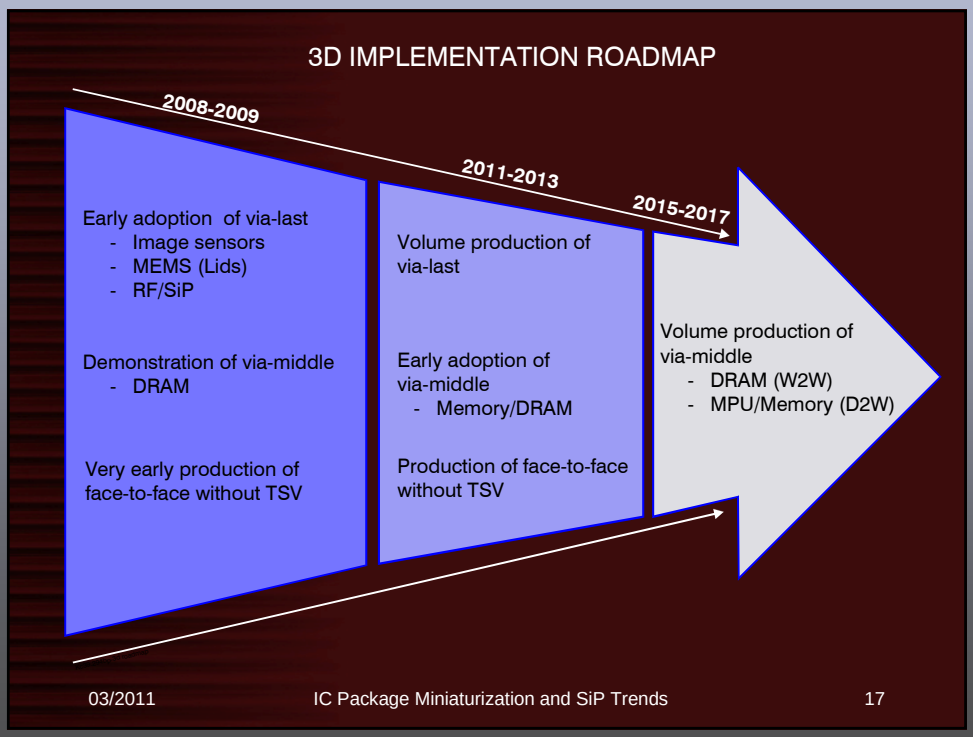
- Alleviate ELK/ULK stress in large die
- Bridge organic substrate gap for dense, complex substrate
- Package advanced wafer node with tighter bump pitch
- Integrate multichip SiP platform
- Design IPD into interposer (inductor, capacitor) using Ansoft library
- Status: ASE has developed capability for TSV and Si interposer assembly capabilities working with key partners
- Completed initial package and board level reliability tests



109.294mvc

STMICRO DEMONSTRATOR OF TSV 3D STACK

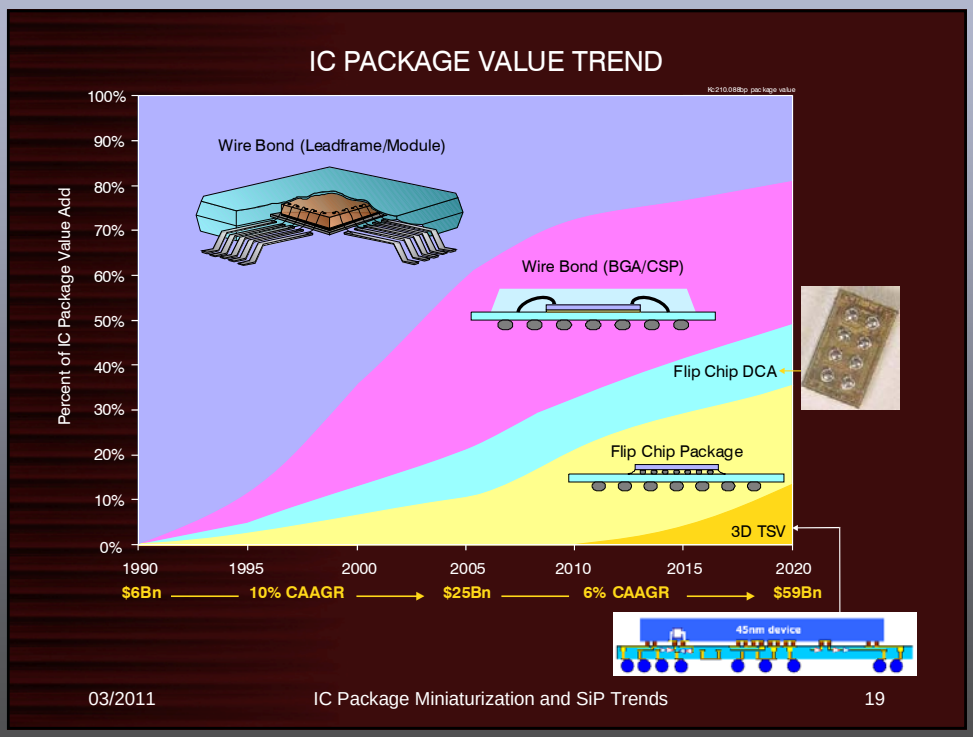




CONCLUSIONS

- **Package size reduction is ongoing, but pitch limitations draw a logical path towards 3D**
- **A few clear trends are enabling miniaturization:**
  - **Fine Pitch Array Packages (0.5 → 0.4 → 0.3mm)**
  - **Stacked Die (Mainly Memory) and Package Stacks (Logic/Memory)**
  - **Wafer Level CSP**
- **3D TSV and Silicon Interposer approaches are still in development, with high volumes products expected in next six to eight months**
  - **Challenges emerge for die level test at pitches <80μm**
  - **Test before die to die or die to wafer assembly often required**

03/2011 IC Package Miniaturization and SiP Trends 18


IC PACKAGE VALUE TREND
Percent of IC Package Value Add
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
1990
1995
2000
2005
2010
2015
2020
Wire Bond (Leadframe/Module)
Wire Bond (BGA/CSP)
Flip Chip DCA
Flip Chip Package
3D TSV
$6Bn
10% CAAGR
$25Bn
6% CAAGR
$59Bn
45nm device
03/2011
IC Package Miniaturization and SiP Trends
19