ARCHIVE 2011

3D TEST: YOU TELL ME AND WE'LL BOTH KNOW

by

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ABSTRACT

The Industry wants to move to die stacking as the way to continue keeping Moore's Law valid. Form factor has been driving the trend for hand-held and small-sized products by doing Package-on-Package and other externally assembled 3D architectures.

The next logical step being worked on is to connect bare-die to bare-die using Through-Silicon-Vias (TSVs). There are two different drivers for TSV-based design: high-performance computing that can reduce the size of complex microprocessor and graphic processors to increase yield and to include different die functions made in different processes that can support different voltages, but all done by one vertically integrated design house; and the "competitive socket" where the space above a base-die can be filled by multiple providers delivering die that implement the same function.

The high-performance computing sector can custom design how they intend to test the die and the stack and the final packaged device; but the competitive socket sector has to have a successful test strategy that will "magically appear" when disparate die are stacked and where each die regardless of provider will be interoperable in a test sense with the other die in the stack.

In addition, the test strategy must allow for wafer-testing and wafer-level burn-in, bare-die or known-good-die testing, partial-stack testing, completed-stack testing, package testing and must carry forward to allow debug-diagnosis, yield-analysis, in-system, and field-return testing. The requirement is not to test to the level to "throw away packages", but to identify the die within a stack or the core within a die — test is not effective without allowing feedback to fix a yield problem.

This talk will investigate the goals of 3D testing and the issues for making a "per die" test strategy that can meet these conditions; and will introduce the new IEEE Standard effort for 3D Test, P1838.

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3D Test: You Tell Me and We'll Both Know

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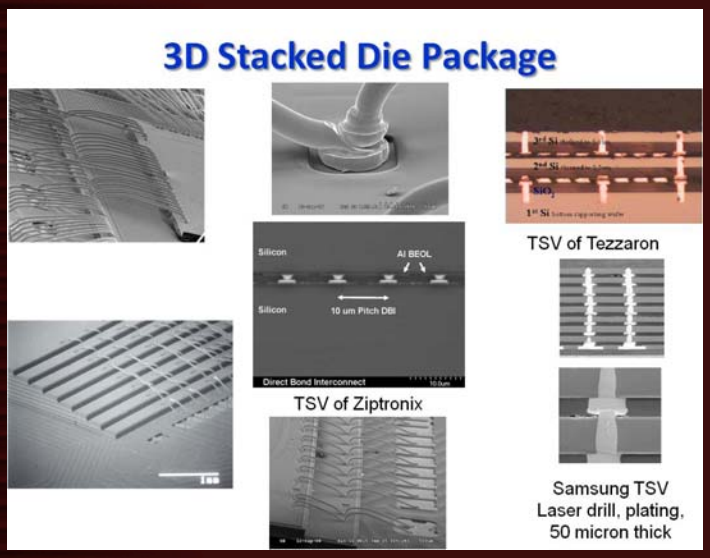
Obligatory Ooh-Ahh slide…



Bill Bottoms, SIP White Paper

What does this have to do with Burn-In?

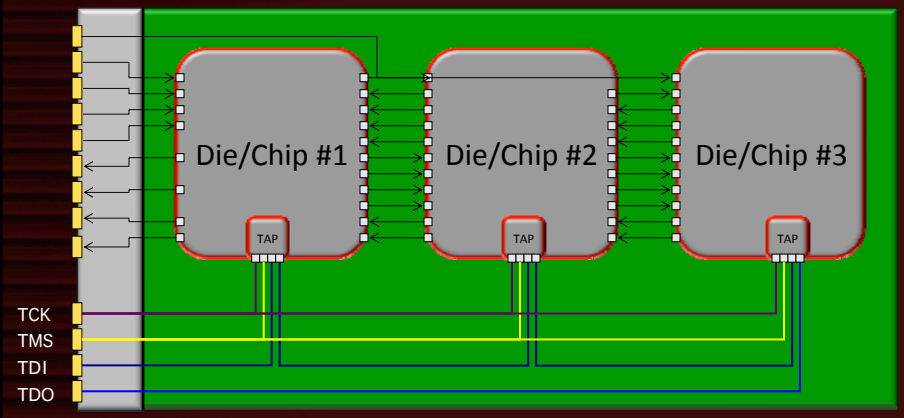
- 3D will require much more "embedded content" to allow test, debug, characterization
- Access to these "instruments" can enable more sophisticated burn-in
- Wafer-level burn-in may be required to produce KGD (known good die)

So, What are the Problems?

- Test and Debug of 3D Stacked Die are not as simple as they are with "planar IC's" or with "Chips on a Board"
- Even MCM's have accessible I/O…
- 3D Stacks (especially with TSV's) have only one die with board connections, the rest are buried between Si-Layers
- Given Moore's Law (Yup, still going strong)…there are whole systems of logic on each of those stackable die and each of those die have tons of Test & Debug requirements and maybe even embedded features…

What does Board-Test expect from 1149.1

Standardized TAP on every chip/board
Small Instruction Registers
Standard Instructions
Low Cost Test Access (not the Multi-$$$Million ATE Chip Testers)



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What are we Testing? Chip vs Board

- There are Chip (IC) Tests
  - Fault Coverage (e.g. Stuck-At, Path Delay, Transition Delay, n-Detect)
  - Defect Coverage (shorts, opens, bridges, GOS)
  - Parametrics (Max FRQ, Leakage – iDDQ, IOH,IIL, VOH, VIL)
  - Functional (Read, Write, Bus Transactions, etc.)
  - Embedded BIST (Logic, Memory, HSIO)
- There are Board Tests
  - PCOLA
  - SOQ
  - FAM

3D Test is a combination of Both

ScanWorks® Platform for Embedded Instruments

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What are the Problems/Issues - in Words?

- Bare "first-floor" die must be chip tested and to become KGD
  - Must be manufactured, tested and delivered before stacking
    - Has Probe Pads for Chip-to-Package Connections
  - Must be stacked (W-on-W, D-on-D, D-on-W)
  - Must be chip tested after stacking – partial, total, final
  - May need test-debug after packaging (IC failure-analysis, board test, system test, field returns)
- Bare "upper-story" die must be chip tested to become KGD
  - Must be manufactured, tested and delivered before stacking
    - Must support "Some" Probe Pads
  - Must be stacked (W-on-W, D-on-D, D-on-W)
  - Must be chip tested after stacking – partial, total, final
  - May need test-debug after packaging (IC failure-analysis, board test, system test, field returns)

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What are the Problems/Issues - in Words?

- Whole Stack may have requirements different than single IC or planar-MCM
  - There are Board Test concepts such as PCOLA/SOQ – Placement, Correctness, Orientation, Live, Alignment, Shorts, Opens, Quality of Connections
  - There are new defect/fault models such as thermal hot spots or die-to-die noise interference
  - There may be a need to test individual die or to access items on individual die without involving other die or other items (test/debug in isolation)
  - There are die-to-die tests such as interconnect or unit-to-unit operations or the impact of one die's thermal image onto another die
    - SerDes-to-SerDes BERT

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P1838 – thanks to Erik Jan Marinissen

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37. Lee	Whetsel	Texas Instruments	Distinguished Member Technical Staff	Dallas, Texas, USA

And many more over the past few weeks!

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The P1838 3D Test Working Group Goal

- To investigate whether an IEEE Standard is needed to cover 3D chips – the consensus was YES! This includes Physical, Architecture, and Descriptions

5.2 Scope of Proposed Standard: The proposed standard is a 'die-centric' standard; it applies to a die that is pre-destined to be part of a multi-die stack and such a die can be compliant (or not compliant) to the standard. The proposed standard defines die-level features, that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks, in both pre-packaging and post-packaging situations. The primary focus of inter-die interconnect technologies addressed by this standard is Through-Silicon Vias (TSVs); however, this does not preclude its use with other interconnect technologies such as wire-bonding.

The standard will consist of two related items.

1. **3D Test Wrapper On-die hardware features that enable transportation of test (control and data) signals in the following configurations.**
- Pre-stacking: From on-die I/Os to die-internal DfT features, and vice versa.
- Post-stacking
  - 'Turn' mode: From on-die I/Os to die-internal DfT features, and vice versa. These on-die I/Os might be external I/Os and/or inter-die interconnections coming from (or going to) an adjacent die.
  - 'Elevator' mode: From on-die I/Os, through THIS DIE, to the inter-die interconnections to an adjacent die, and vice versa. These on-die I/Os might be external I/Os and/or inter-die interconnections coming from (or going to) another adjacent die.

2. **Description A description of the Test Wrapper features in a standardized human- and computer-readable language. This description should allow the usage of the die within a multi-die stack for test and test access purposes.**

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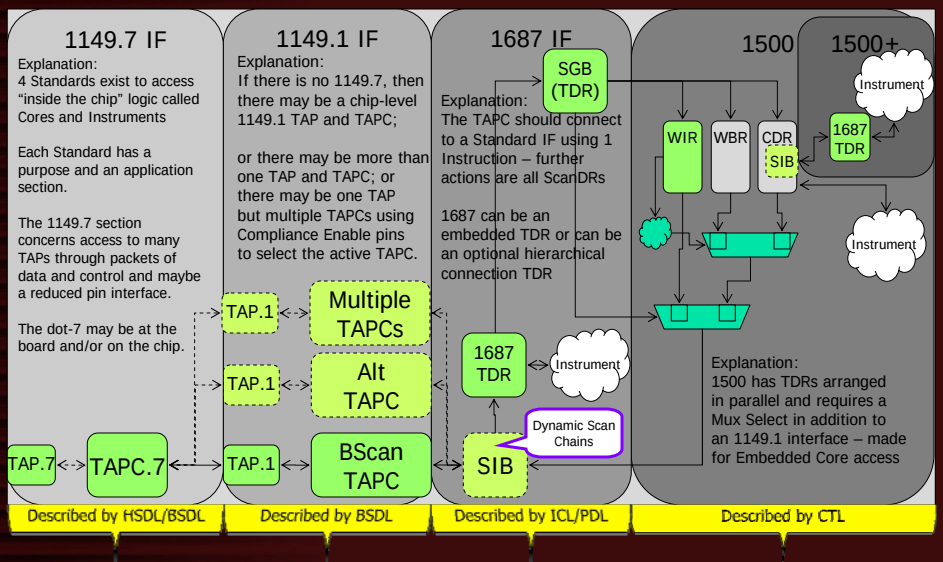
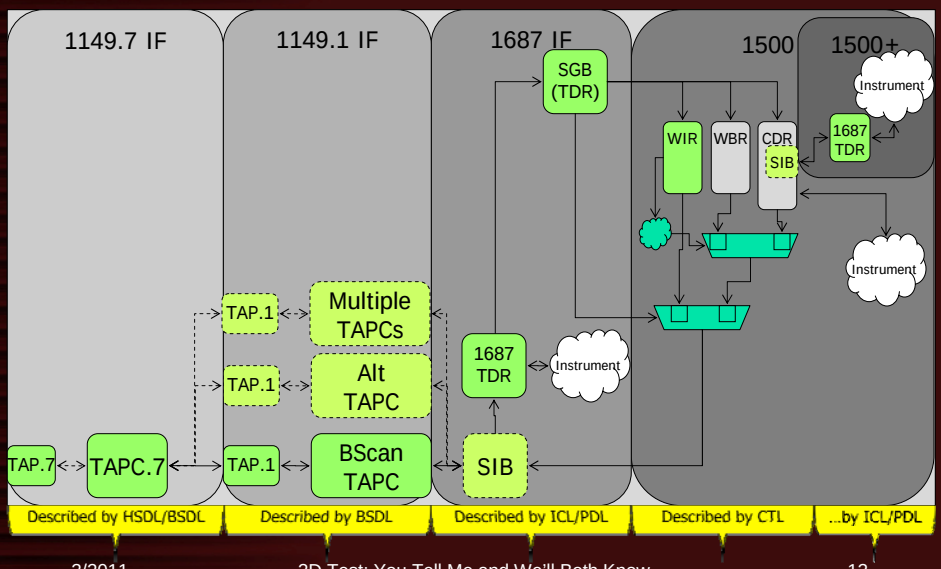
What does this mean?

- Human POV: We want to treat individual die like "Lego Blocks"
  - The Board-to-Chip is the Big Green thing
  - The Chip-to-Chip are the bumps and holes
- The PAR is to create the Working Group to investigate:
  - the JTAG-like connection to the Big Green thing…
    - Is it 1149.1, is it 1149.7, is it other? Do we stipulate this, or assume it
  - …and to define the per-die connection for test/debug on each die
    - Physical Vias/Locations, Pin/Signal Protocol, Number of, etc.
  - …and the support and interaction for existing and proposed IEEE Standards such as 1149.1, 1149.6, 1500, P1687
    - Incorporate the existing, create and add the new

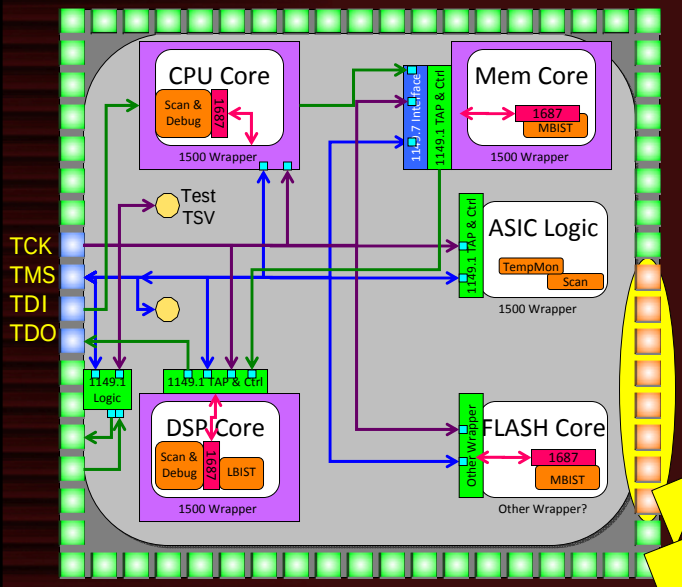
Distribution of IEEE Standard Solution Spaces



Distribution of IEEE Standard Solution Spaces



What's the Problem – in Pictures?



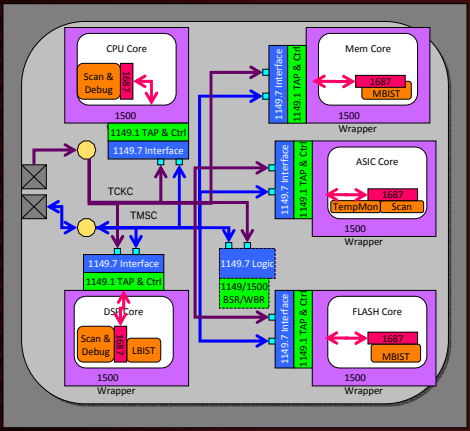
Bottom or Base Die can be Tested to become a (KGD) Known-Good-Die
- Want high coverage
- No Test Escapes

Must have Probe Pads
Must have a TAP
- TAP-1 or TAP-7
- 1149.1 B-Scan for I/O
- must have access to:
  - Core Test
  - Embedded Test
  - Embedded Debug
- must have TSVs to:
  - access upper die

High Speed IO

Boundary Scan

What's the Problem – in Pictures?



Each "Upper" Die must have:
- Known-Good-Die Test
- Stack Test

Must have a few Probe Pads for bare-die test or partial stack test

May use 1500 WBR or 1149.1 BSR for Interconnect Test

Prefer P1687 SIB for management of Scan Path lengths and Instrument Scheduling

Dot-7 I/O on each Die has 2 TSVs to feed Stacked-Die
- TMSC
- TCKC

Some Various Access Proposals

- The "1149.7 Multiple-TAP Access" Proposal
- The "1149.1 TAP on Base-Die Only" Proposal
- The "1149.1 Prime TAP on each Die" Proposal
- The "1149.7 to Prime TAP on each Die" Proposal

The 1149.7 Multiple TAP Proposal

- There is an 1149.7 TAP on the Base Die which becomes a two-wire distribution network to all the TAPs one each die
- There are two-TSVs on each die to deliver these signals (three-signals and three-TSVs if a Mux is used instead of a bidirectional TDI-TDO function)
- There are 1149.1 TAPs associated with groups of logic or cores – and there is an 1149.7 Controller in front of each 1149.1 TAP
- This method places more logic on each die (multiple dot-1 and dot-7 TAPs, multiple core-wrappers), but makes each addressable item a self-contained and locally controlled unit with 1149.7 only being a data/control delivery conduit – not a controller source for configuration or instructions.

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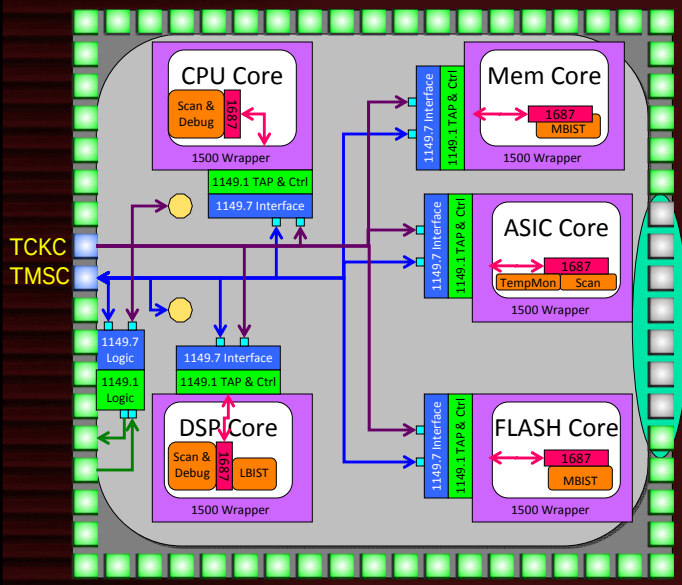
An Access Solution: "1149.7 Multiple-TAP Access"



Bottom Die
Known-Good-Die

Must have Probe Pads
Must have a TAP
- TAP-1 or TAP-7
- Speed to Instrument 1149.1 Boundary Scan for I/O

Dot-7 has two TSVs to feed Stacked-Die
- TMSC
- TCKC

My Preference
- More on-chip Logic
- but Self-Contained and Scalable

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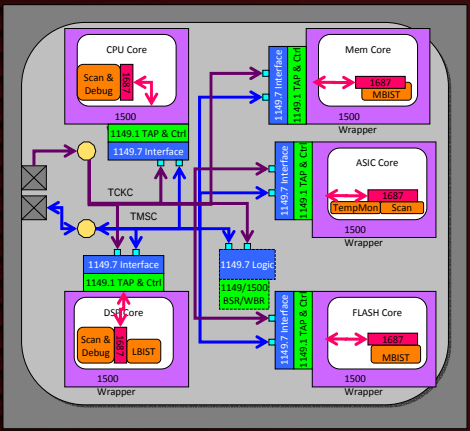
An Access Solution: "1149.7 Multiple-TAP Access"



Die 2-up-to-Die N
- Known-Good-Die Test
- Stack Test

Must have a few Probe Pads (Mux or SIB) for KGD

May use 1500 WBR or 1149.1 BSR for Interconnect Test

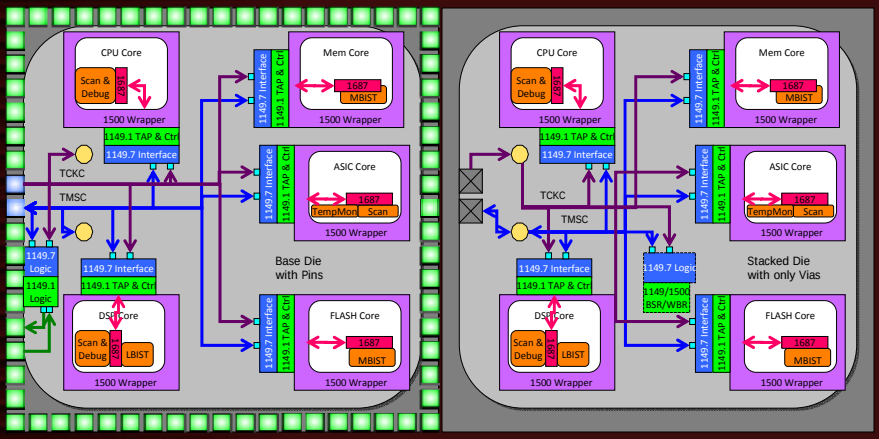
Prefer P1687 SIB for management of Scan Path lengths and Instrument Scheduling

Dot-7 I/O on each Die has 2 TSVs to feed Stacked-Die
- TMSC
- TCKC

Issue: each grouping adds a TAP and a Wrapper (Logic)

Note: many die already have multiple TAPs and could extend easily

An Access Solution: "1149.7 Multiple-TAP Access"

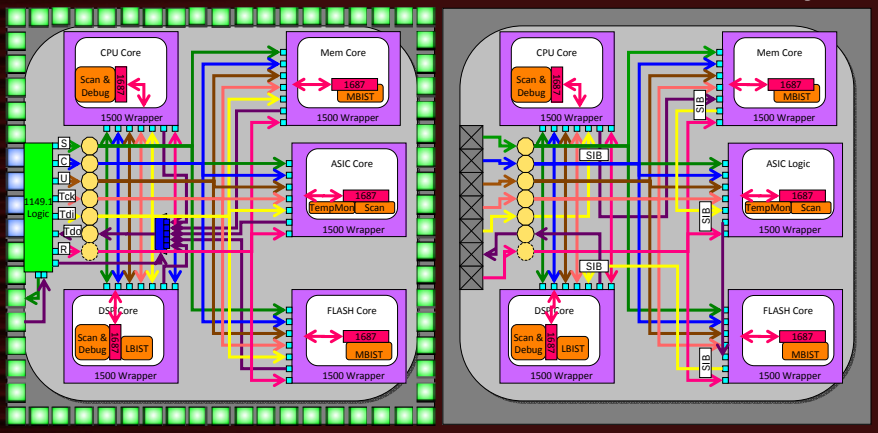


There are 2 physical Vias
The connection is broadcast-Star
There is more logic to define address and extract packet data
There are probe pads on upper die
There is a 1500 or 1149.1 type boundary scan for TSVs between die

The 1149.1 TAP on Base-Die Only Proposal

- There is one 1149.1 TAP on the Base Die which becomes a controller for all die in the stack – it provides the control signals for all JTAG-compliant object in the entire die stack
- There are up to seven-TSVs on each die to deliver these signals control and data signals
  - ShiftEn
  - CaptureEn
  - UpdateEn
  - TCK
  - TDI
  - TDO (single TDO requires a Multiplexor and a Select on each die)
  - ResetN (opt)
- There are 1500 Wrappers/1687 Registers associated with groups of logic or cores – and they use these 1149.1 signals to coordinate all operations
- This method places the entire brunt of signal loading and instruction delivery on the single TAP Controller on the Base-Die – even if the die and number of die to eventually be placed above the base-die are unknown at the time of design; there is also a TDO management issue if only one TDO-TSV is used

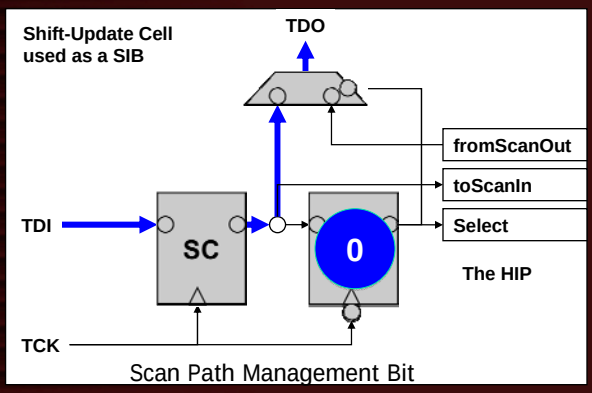
An Access Solution: "1149.1 TAP on Base-Die Only"



There are 7 physical Vias – issue, unknown loading on base die instruction-register
The connection is serial-daisy-chain with SIB for turn-around
There is more routing to create access and control
The 1687 SIB or a 1500 Mux structure can be used for bypass and turn-around
There are probe pads on upper die
There is a 1500 or 1149.1 type boundary scan for TSVs between die

The Segment-Insertion-Bit (SIB)

The Key Element for Adding, Organizing, Managing Embedded Content

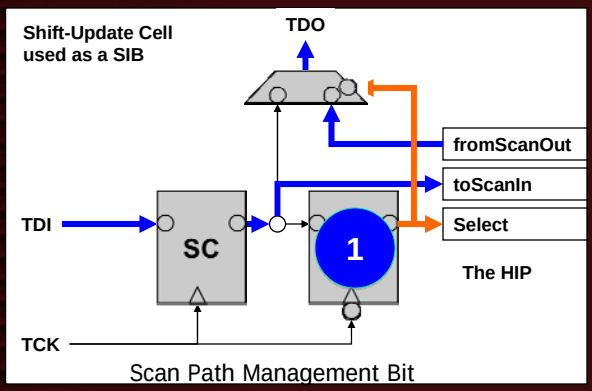


Normal TDI-TDO Scan Path

Default Configuration from Reset

The Segment-Insertion-Bit (SIB)

The Key Element for Adding, Organizing, Managing Embedded Content

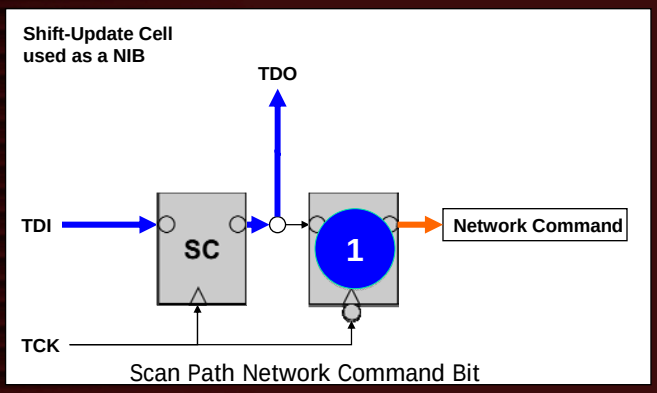


Added Network Scan Path

Can access other SIBs or Instrument Interface TDR

The Network-Instruction-Bit (NIB)

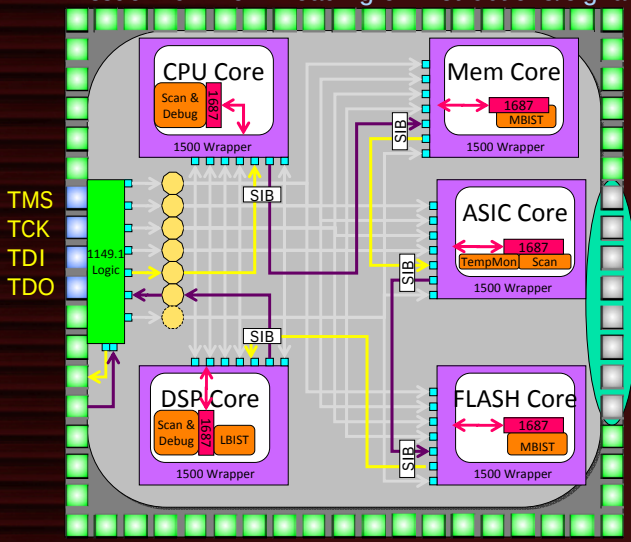
The Key Element for Local Configuration of Scan Path Networks



Can access other SIBs or Instrument Interface TDRs

An Access Solution: "1149.1 TAP on Base-Die Only"

Issue – unknown loading on instructions/signals



Bottom Die
Known-Good-Die

Must have Probe Pads
Must have a TAP
- TAP-1 or TAP-7
- Speed to Instrument

1149.1 Boundary Scan for I/O

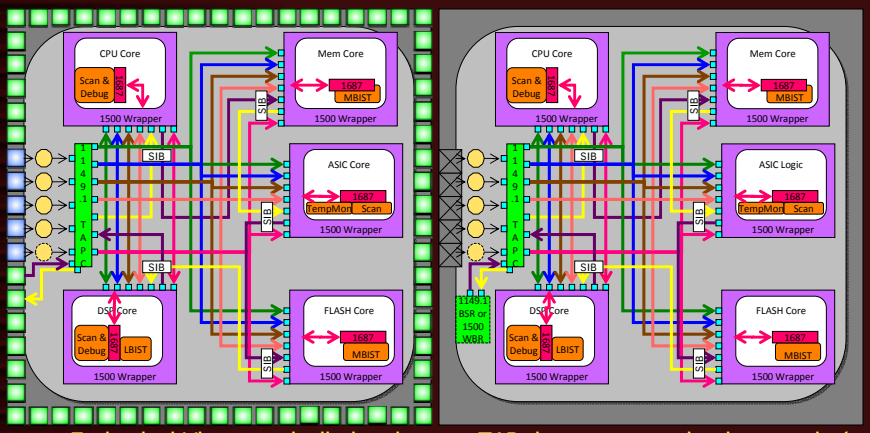
Dot-1 on 1st floor-only has seven TSVs to feed Stacked-Die
- ShiftEn
- CaptureEn
- UpdateEn
- TCK
- TDI
- TDO
- ResetN (opt)

Note: 3 potential TDO architectures – Mux, Daisy-Chain, **SIB**

The 1149.1 Prime TAP on Each Die Proposal

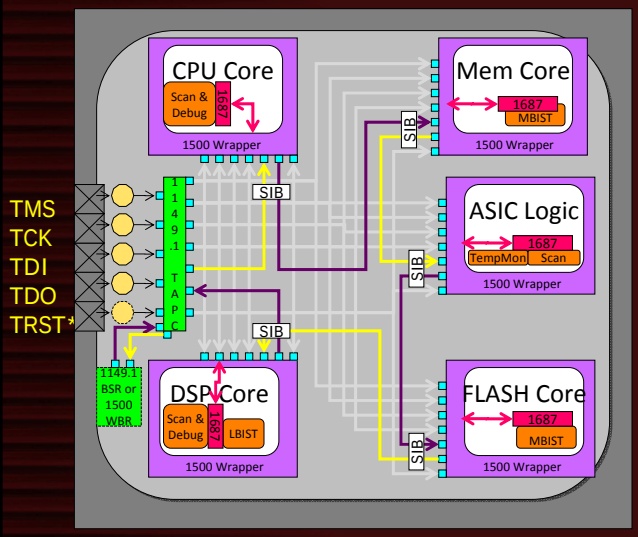
- There is one 1149.1 TAP on Each Die which becomes a controller for all JTAG-Compatible functions on each die – it locally provides the control signals for all JTAG-compliant objects in each die
- There are up to five-TSVs on each die to deliver the 1149.1 TAP signals
  - TMS
  - TCK
  - TDI
  - TDO (TDO managed to one pin on each die)
  - TRST* (optional)
- Each die is a complete system similar to testing an MCM or chips on a board
- This method creates an Instruction Compatibility Issue in that parallel operation of each TAP implies parallel (Identical) operation of each TAP Controller (identical data and instruction flows into each dies TDI) – unless each die's TDI-TDO is daisy chained

An Access Solution: "1149.1 Prime TAP on each Die"



There are 7 physical Vias – each die has its own TAP that operates simultaneously (star)
The internal die connection is serial-daisy-chain with SIB for turn-around
There is more routing to create access and control
The 1687 SIB or a 1500 Mux structure can be used for bypass and turn-around
There are probe pads on upper die
There is a 1500 or 1149.1 type boundary scan for TSVs between die

An Access Solution: "1149.1 Prime TAP on each Die"



Issues: 1149.1 TAPC Instruction Overlap TAPs operate in parallel
- Must have CE TSV per Die

Die 2-to-N
- Known-Good-Die
- Stack Test

Must have a few Probe Pads (Mux or SIB) for KGD

May use 1500 WBR or 1149.1 BSR for Interconnect Test

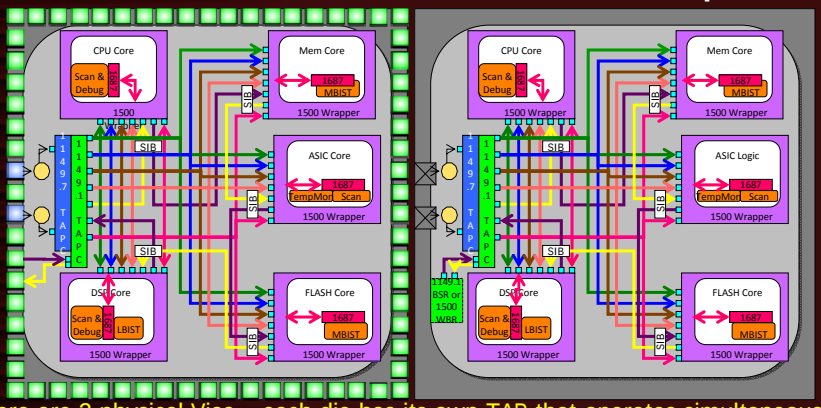
Prefer P1687 SIB for management of Scan Path lengths and Instrument Scheduling

Dot-1 I/O on each Die has 4/5 TSVs to feed Stacked-Die
- TMS, TCK, TDI, TDO
- TRST*

The 1149.7 to Prime TAP on Each Die Proposal

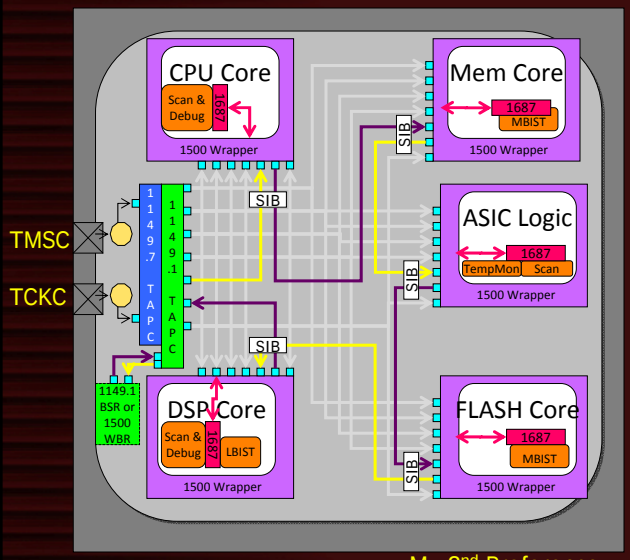
- There is one 1149.1 TAP on Each Die which becomes a controller for all JTAG-Compatible functions on each die – it locally provides the control signals for all JTAG-compliant objects in each die
- There are two-TSVs on each die to deliver the 1149.7 TAP signals
  - TMSC
  - TCKC
- The two-TSVs feed the one Prime TAP on each Die
- Each die is a complete system similar to testing an MCM or chips on a board
- This method solves the Instruction Compatibility Issue the previous method in that each TAP only processes the packets targeted to its 1149.7 address

An Access Solution: "1149.7 to Prime TAP per Die"



There are 2 physical Vias – each die has its own TAP that operates simultaneously and those TAPs are addressed by 1149.7 2-wire interface
The internal die connection is serial-daisy-chain with SIB for turn-around
There is more routing to create access and control
The 1687 SIB or a 1500 Mux structure can be used for bypass and turn-around
There are probe pads on upper die
There is a 1500 or 1149.1 type boundary scan for TSVs between die

An Access Solution: "1149.7 to Prime TAP per Die"



Die 2-to-N
- Known-Good-Die
- Stack Test

Must have a few Probe Pads (Mux or SIB) for KGD

May use 1500 WBR or 1149.1 BSR for Interconnect Test

Prefer P1687 SIB for management of Scan Path lengths and Instrument Scheduling

Dot-1 I/O on each Die has 4/5 TSVs to feed Stacked-Die
- TMS, TCK, TDI, TDO
- TRST*

My 2nd Preference

Summary-Conclusions

- An IEEE effort has been started with P1838
- The Working Group has started and has had meetings
- There are a number of potential architectures that have been investigated to help define the elements of the work to be done
- The effort will include definition of an architecture, a description language, and maybe a vector relationship
- Architecture tradeoffs will include number of TSVs, location of TSVs, impact of logic/routing/power, and maybe required structures, and access efficiencies