BiTS™ Burn-in & Test Socket Workshop 2011 **Poster Session**

ARCHIVE 2011

HVM Socket Development for System Validation Boards, Featuring an Increasing MTBF

Shaul Lupo—Intel Israel

Solution for a 26 GHz, Tri-Temperature Test

Ryan Satrom, Paul Hurst—Multitest

BGA Interconnect Cres and Lifetime Characterization Methodology and its Challenges

Weida Qian, Jun Ding, Boon Tatt Gan—Intel Corporation

High Force Hand Socket Lid

Chia Seong Lim—Test Tooling Solutions Group

Does a Conductive Elastomeric Socket Have the Same Electrical Performance as the Soldered Unit Attachment?

Oren Ganon—Intel Corporation

BGA Spring Probe for WLCSP (P0.4mm) - Multipoint Contact to BGA

Eichi Osato—Micronics Japan Co., Ltd.
Fred Megna—MJC Electronics Corporation

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HVM Socket Development for System Validation Boards, Featuring an Increasing MTBF

Shaul Lupo - Intel Israel

Problem Statement:

Regular HVM socket CRES results on system boards are worse by definition comparing to ATE board and option for continuity issues, due to the next reasons:

1.Thin board 1.6mm - Board bending

2.Solder mask – Flatness issues

3.Pads are soft gold or tin plated – Issues of softness, oxidize, flatness

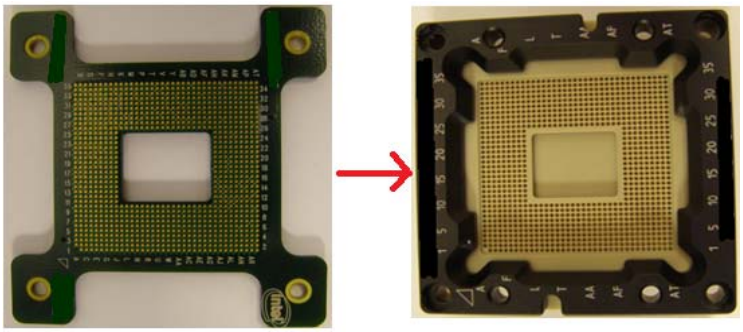
4.Tens thousand of cycles – Holes on the pads & board damage

Previous Solution:

Design interposer with balls which converts to hard gold pads (the same surface as ATE boards)

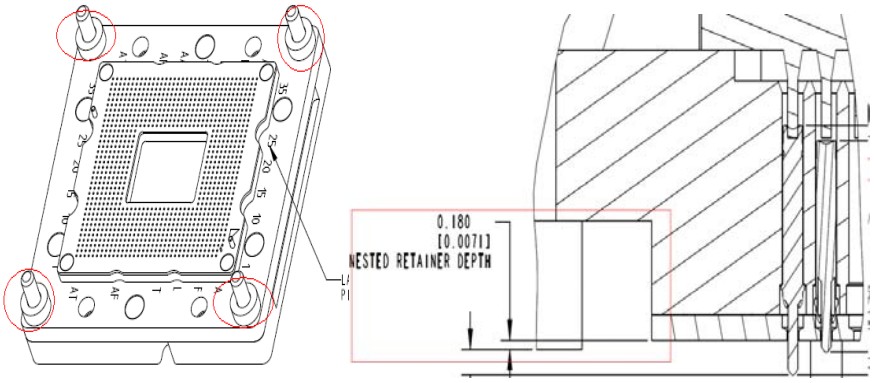
New Solution (HVM socket DEV.):

Design new socket to overcome the above issues



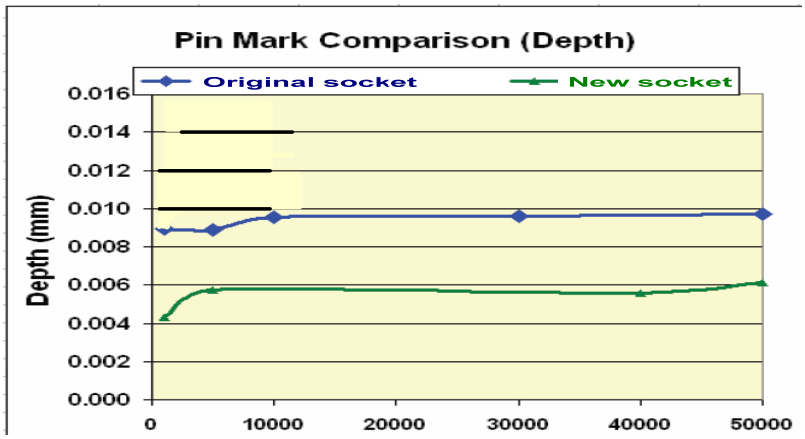
New socket advantages

1. Switch to MDS100 material which is more rigid than common socket materials – Less deflections, higher tensile strength
2. Use pogo pins with hammering effect lower by 50% comparing original socket (6gr VS. 10gr). This reduced holes depth on system board pads. Hammering (load force – preload force)
3. 4 socket's posts are higher by 0.18mm than socket retainer, this cancel the impact of board flatness issue exist on system board

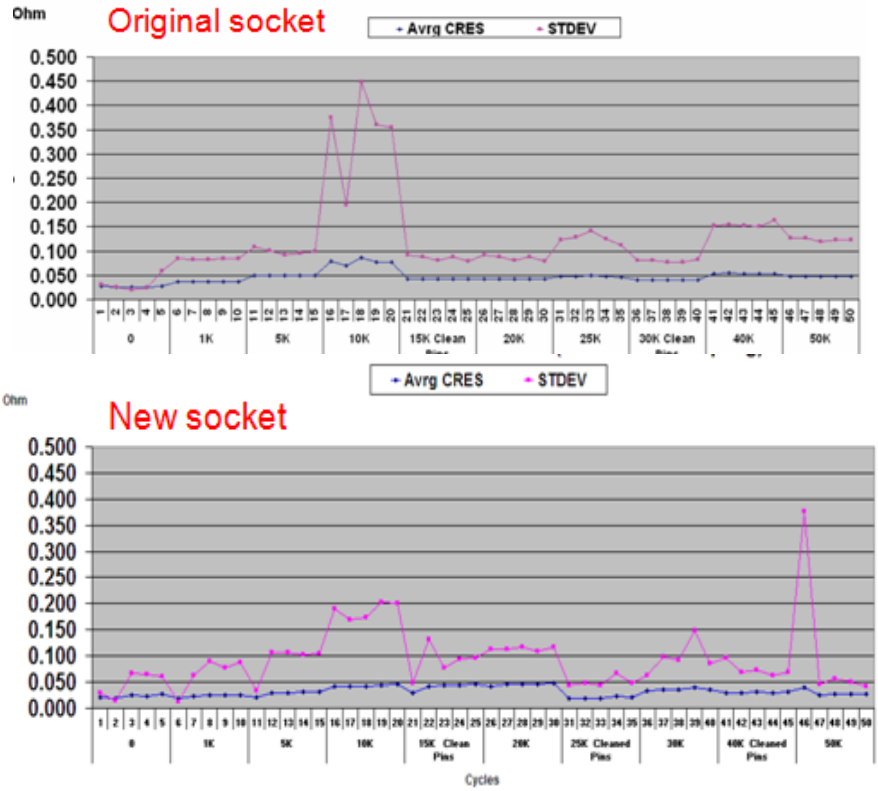


4. Change pogo bottom tip to be less sharp and decrease the stamping on the pad

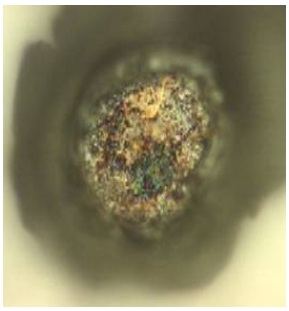
Results



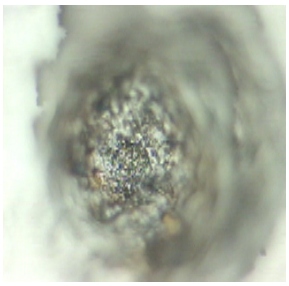
Results (Cont.)



Original socket:
Plating exposed
after 10K cycles



New socket:
No plating
exposure
after 50K cycles



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Solution for a 26 GHz, Tri-Temperature Test

Ryan Satrom, Paul Hurst
Multitest

Project Description

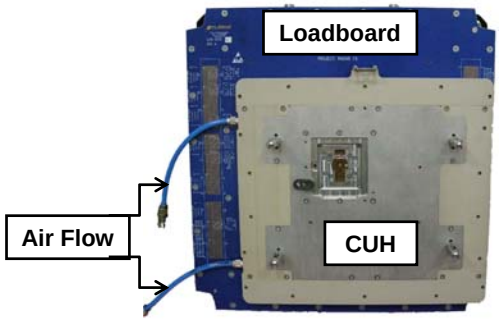
• Test cell infrastructure for an automotive/radar application (vehicle anti-collision system)

Special Requirements

• Tri-Temperature Test
• High Frequency

Involved Products

• Hardware Design and Fabrication
  • Test Handler
  • Conversion Kit
  • Contactor
  • Loadboard
• Simulation/Measurement



Challenges

• Design/fabricate a loadboard/contactor assembly that includes a balun with 23GHz to 26.5GHz passband and the following specs:
  • Less than 8dB loss (23-26.5GHz)
  • Less than 2dB of ripple in passband (23-26.5GHz)
• Achieve temperature accuracy of ±2°C at cold test (die temperature) while maintaining RF requirements
  • RF electrical requirements force plunge-to-board
  • Insulation cannot be placed on handler-side of PCB
• Avoid condensation at cold test

CONTACTOR
LOADBOARD
INSULATOR BLOCK

Ideal RF Configuration
- Short RF probe
- No insulator block

Ideal Thermal Configuration
- Insulator block on handler-side of PCB

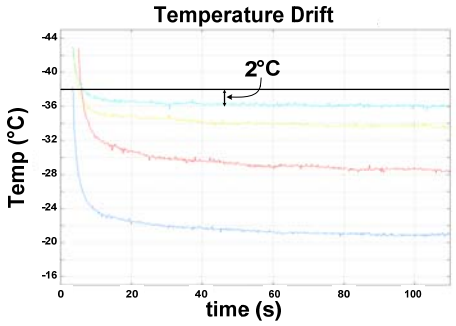
Required Configuration

???
Solution must meet both RF and thermal requirements

Meeting the Temperature Requirements

1) Experiments optimized thermal stability

- Insulation and/or air purging compared to optimized design
- Experimental results showed best configuration used no hot air purge with insulation across entire loadboard



50°C hot air purge

30°C hot air purge

50°C hot air purge/ Reduced air flow

No hot air purge/ Custom insulation

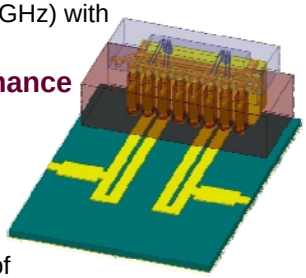
2) Contactor optimized for thermal stab

- Air flow integrated with handler kit provides required temperature to DUT
- Ground slug improves thermal stability at DUT

Meeting the RF Requirements

1) High frequency contactor met requirements

- Minimal length probe required to meet 26.5GHz max bandwidth
- Solution: Gemini socket (1.54mm length, S_{12} – 40+ GHz) with ground slug provides ideal performance

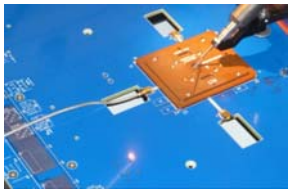


2) Simulation tuned for narrow-band performance

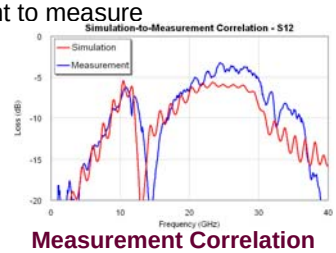
- Simulation included loadboard, contactor, package
- Simulation required to dictate balun design
- Design optimized through several iterations

3) Measurements verified simulations

- Stringent specification requires precise correlation of simulation-to-measurement
- Application requirements (Single Ended-to-Differential, 26.5GHz) create very difficult environment to measure



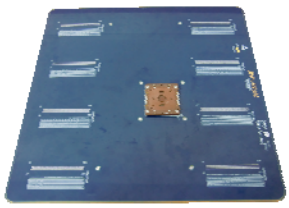
Measurement Setup



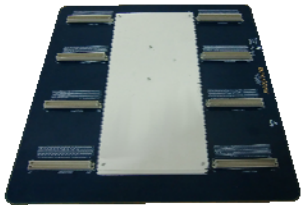
Measurement Correlation

Final Concept

- Insulator block placed on tester-side of loadboard to provide sufficient isolation, while maintaining adequate RF performance



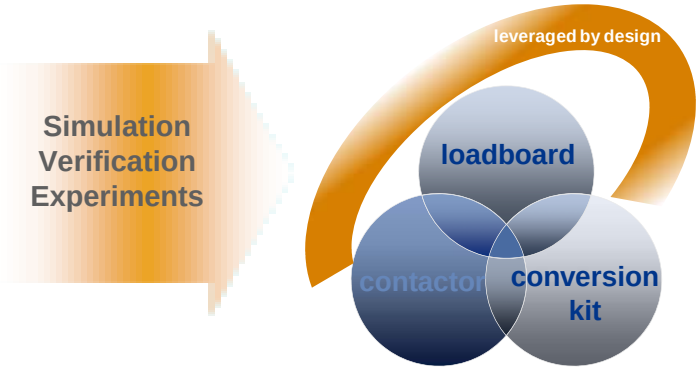
Handler-Side Contactor



Tester-Side Insulator

Integrating All Components

- Contactor, load board, and test handler conversion kit designed and manufactured in-house
- Pre-manufacturing experiments and simulations predicted the thermal and RF performance prior to fabrication
- Measurements verified performance prior to shipping to customer
- One-stop solution provided accountability and project management



Requirements for Success

• Simulation of loadboard, contactor, and package as one system

• Experiments with loadboard and handler contacting unit to verify thermal performance

• Fluid integration of RF simulation, thermal expertise, PCB and contactor design, and electrical verification into one successful product

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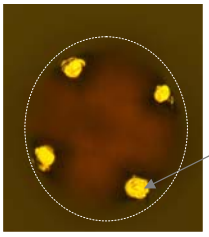
BGA Interconnect Cres and Lifetime Characterization Methodology and its Challenges

Weida Qian, Jun Ding and Boon Tatt Gan
Intel Corporation

Traditional LGA device simulators no longer suitable for BGA pin characterizations

- Differences in material hardness
- Differences in contact geometry
- Contact surface/material interactions

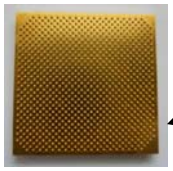


Tip flattering after 40k cycles on a BeCu flat device simulator coated with Au

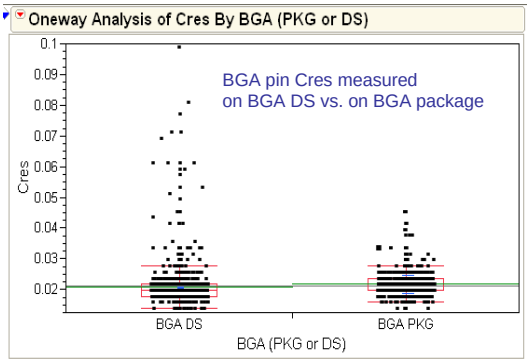
Material Hardness	
Related Materials	**Vickers Hardness (in MPa)**
Package LGA pads	~ 2030 - 5684
Package BGA balls	~ 314
304 Stainless Steel	2067
BeCu	4027-4459
440C Stainless steel	6500
Sputter deposited gold film	2350
Hard Au coating	1137-1842
Bulk gold	640

BGA device simulator may be used for estimating pin initial Cres and spring lifetime, but…

- Not for BGA pin lifetime
- Not for surface interactions
- Not for material contamination



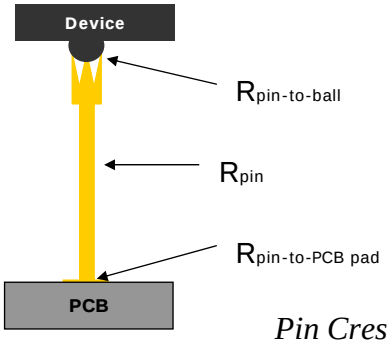
A BGA device simulator

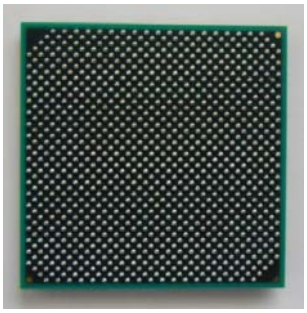


Poster #3
1

BGA interconnects need to be characterized using BGA package units for both Cres and pin lifetime

- Use four-wire (Kelvin) method for Cres measurement
- Measure at the recommended operating stroke for both Cres and lifetime testing
- Measure on minimum of 122 pins evenly distributed around center, and 4 corner areas of the pin array
- Prefer using shorted BGA packages or BGA balls connected to a single power or ground plane (To avoid internal trace resistances)
- Performing visual/mechanical inspection and Cres check at proper intervals during pin lifetime test, e.g. 0k, 5k, 10k, 20k, 40k, 70k, 100k
- Measure Cres on a fresh BGA package unit when possible





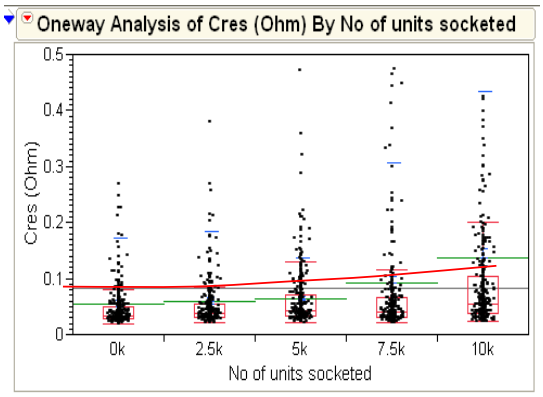
$$Pin\ Cres = R_{Pin-to-Ball} + R_{Pin} + R_{Pin-to-PCB\ pad}$$

Examples of pin characterization using BGA package units

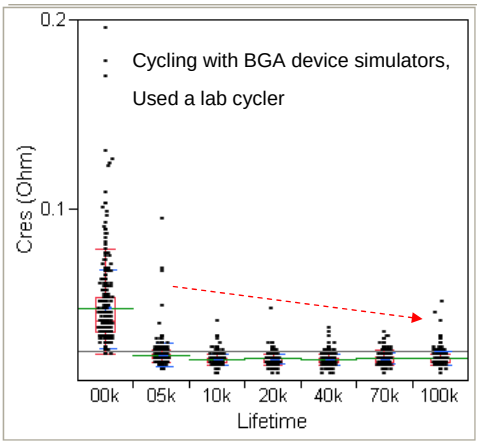
a). Impact on Cres with # of BGA units cycled

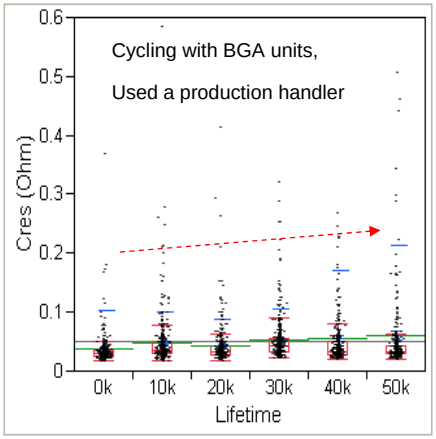
- **Without tip cleaning**
- **BGA package units for cycling**
- **Cycled in a production handler**
- **BGA pkg for measuring Cres**

➔ **Cres increases with increasing number of units cycled, due to solder contamination.**

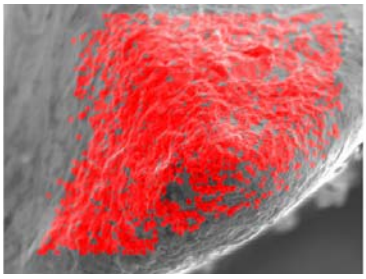


b). Pin lifetime is often over estimated with device simulator cycling

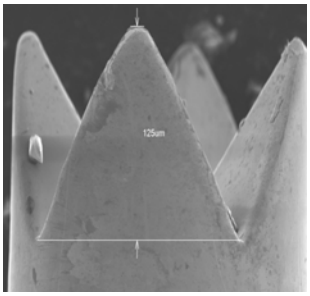




c). Pin tip condition study with BGA package units cycling



Tin mapping at 40k



No significant pin tip worn out after ~ 40k

Summary:

Not suitable	**Metal device simulators (LGA or BGA)**
Acceptable	**BGA units having more than 122 balls with ball size/composition matching with actual product. Use no more than 1000 cycles on each ball. Fresh balls for Cres.**
Ideal	**Simulate the actual production test condition in lab environment: BGA units, production handler, at temperature, fresh units, regular pin cleaning, etc.**

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"High Force Hand Socket Lid"

Lim Chia Seong
Test Tooling Solutions Group

Design Goal:

• Ergonomic Hand Socket Lid design for high force (> 100kg) / high pin count (> 2000 pins) package testing without the pain.

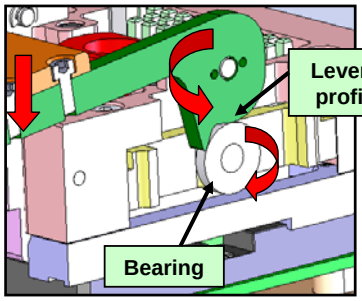
Design Concept:

•Bearing is used and integrated in the design:

- •To reduce friction between 2 contacts surfaces
- •To allow smoother rotation movement

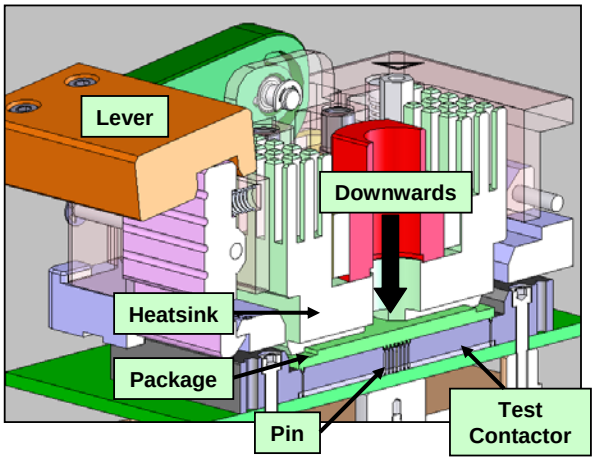
Patent Pending

1) Lever is actuated



2) Lever's profile contacts and rotates the Bearing.

3) Heatsink moves downwards to push the package and compress the pin to working stroke.



4) The Bearing reduces friction and promotes a smooth movement. Thus, the user does not have to exert much force compared to actuating socket lids without the Bearing.

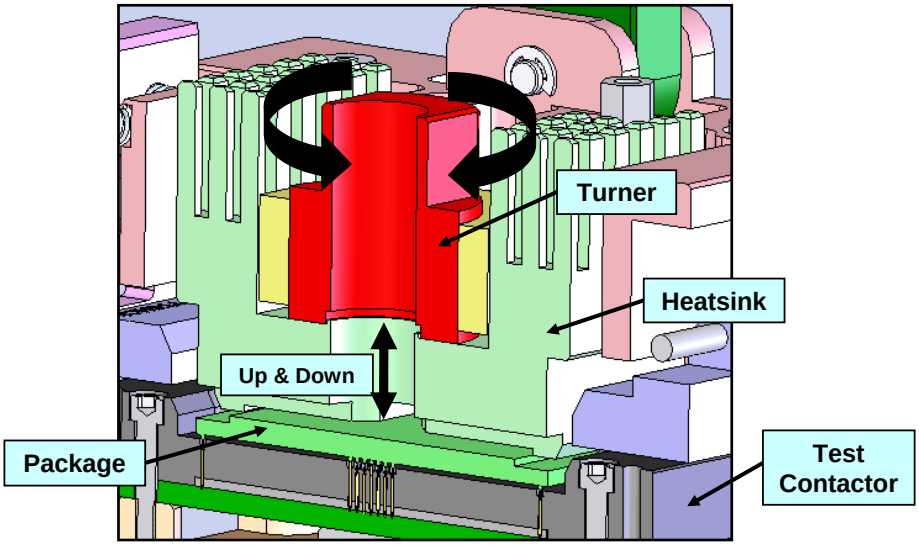
5) As a result, no hand pain is experienced by the user.

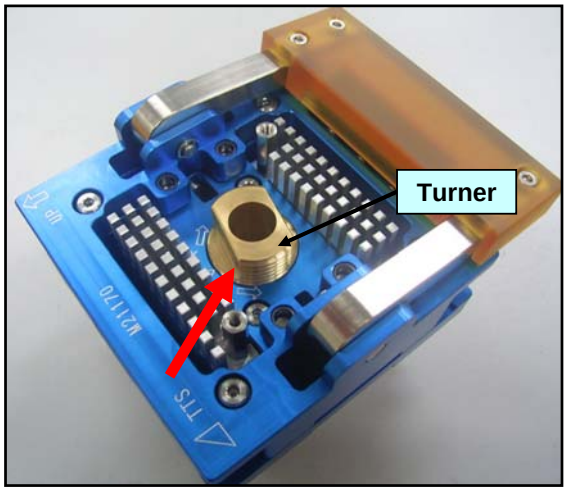
Additional Design advantages:

1) Adjustable Pedestal / Heatsink height
2) Locking Latch

1) Adjustable Pedestal / Heatsink Height

•Provided with adjustable Pedestal / Heatsink by pushing down the package cater for the different thickness with same pin map configuration design of Package.

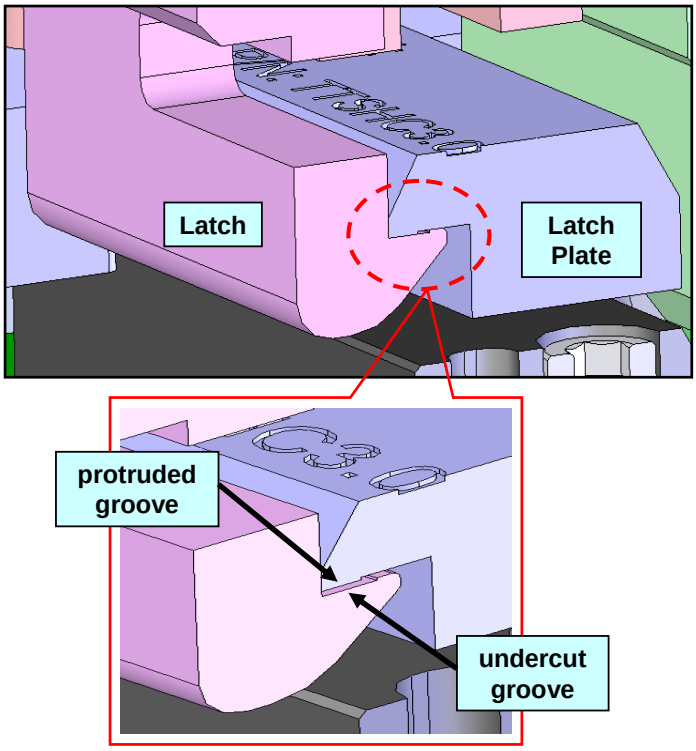




• Height can be adjusted by using the Turner which does not require any additional tools.

2) Locking Latch

•Poka-yoke design concept to prevent accidental opening of the latch during the test mode (compression mode) which can affect the testing process.



•When engaged, both latches complement each other and will not be easily opened.

Summary:

1) The design ergonomics of the Hand Socket Lid to allows a pain-free high force compression task for the user.

2) Adjustable Pedestal / Heatsink provides compliance flexibility for different package thickness testing especially during engineering development stage.

3) Latching mechanism ensures customer testing can be progressed securely.

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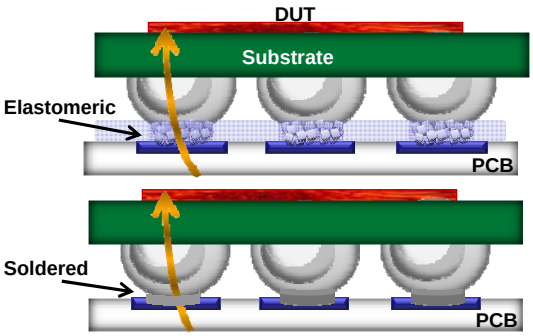
Does a Conductive Elastomeric Socket Have the Same Electrical Performance as the Soldered Unit Attachment?

Ganon Oren oren.ganon@intel.com
Contributors: Dahan Elico eliakim.dahan@intel.com,
Manukovsky Alex alex.manukovsky@intel.com
LAN Access Division, Intel



This poster presents an evaluation of high-speed conductive rubber socket technology for electrical validation applications.

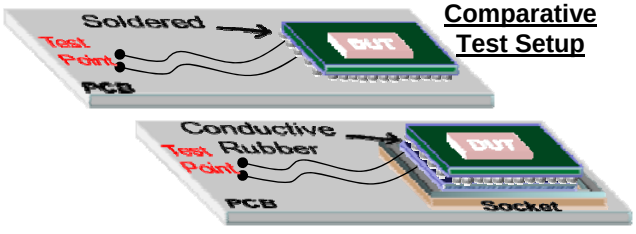
It offers a comparative high data rate analysis for tests performed on conductive rubber socket vs. soldered unit attachment.

In the field of silicon electrical validation it is important that accurate measurements are available, especially on high frequency tests. For example, 10GBase-KR Backplane Ethernet technology (IEEE 802.3ap standard) requires very accurate transmitter characterization measurements of jitter and waveform characteristics such as 40mv steps of 10GB/s PRBS signal. During this investigation we design a conductive rubber socket for our 10GB/s electrical validation product. The socket is based on conductive rubber pogo pins and pinned in a 25x25mm array with 625 pins on a 1 mm pitch.

The comparative test setup is composed of a test-board with both options available: a conductive rubber socket and a soldered unit. An integrated circuit is used as a signal transmitter and various test instruments are used to take measurements at the test-point.

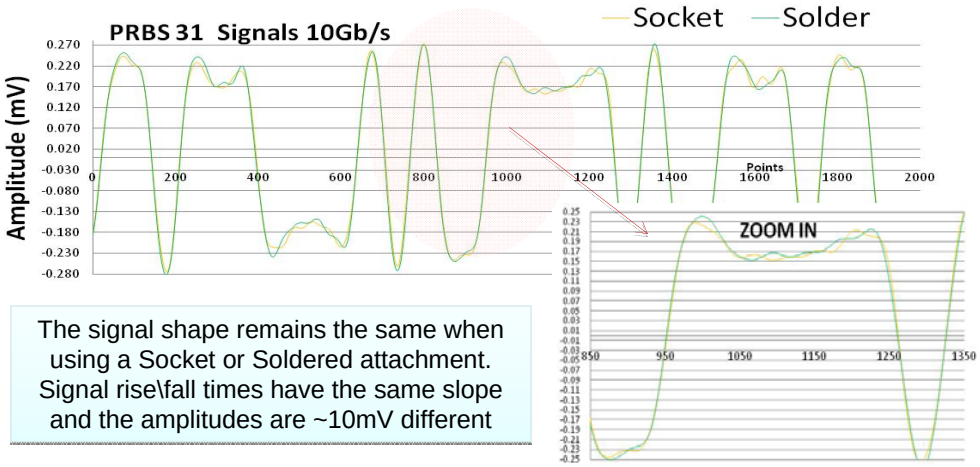
High bandwidth Oscilloscopes and a Vector Network Analyzer (VNA) have been used to extract the measurements at Test Point edge

Comparative Test Setup



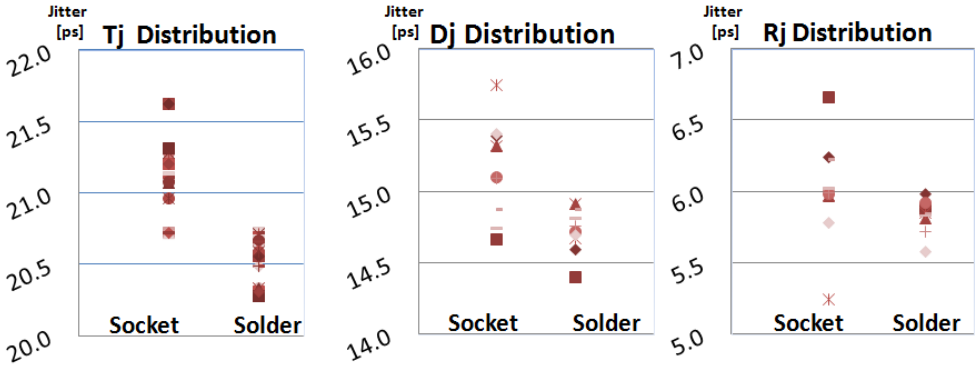
Poster #5

Intersymbol interference (ISI) is a form of signal distortion when one symbol interferes with subsequent symbols. One of the ISI causes known as multipath propagation occurs when the signal from a transmitter reaches the receiver via multiple paths simultaneously in either a Socket or Soldered attachment. In this experiment we transmit a long random pattern (PRBS31) at 10G/b and capture the waveform at the test point using a DSA91304A real time scope.



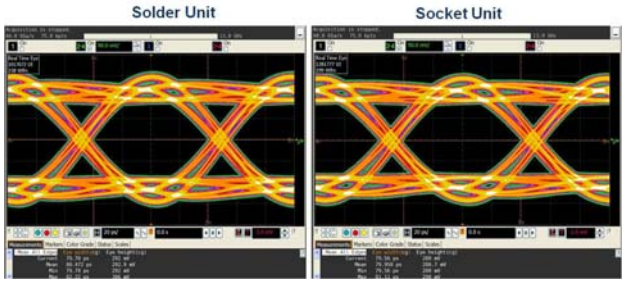
The signal shape remains the same when using a Socket or Soldered attachment. Signal rise\fall times have the same slope and the amplitudes are ~10mV different

Jitter is the deviation of the signal's transitions from its ideal position in time. Jitter can be categorized by its causes. It can be the result from random thermal sources (RJ) or deterministic sources (DJ) . Total Jitter is a composition of Rj and Dj. Signal transitions are affected by the channel and the way the DUT is attached to the board, i.e. Socket or Soldered. In this experiment we transmit a long random pattern (PRBS31) at 10G/b and took jitter signal measurements at $1e^{12}$ BER with an Agilent DSA91304A real time scope. The tests are done 10 times for different temperatures.



The soldered unit introduces lower jitter results - 0.5ps-1ps lower than the Socket. The Solder gives a smaller standard deviation. Soldering moderates standard deviation. When using the socket, equal pressure must be applied on the unit during the test (difficult to achieve over time).

The **Eye diagram** is a voltage diagram that displays a number of superimposed data patterns that resemble an eye. It can be a common indicator of performance in digital transmission systems. Signal jitter, voltage swing and transition time can be extracted from the diagrams. In this experiment we transmit a long random pattern (PRBS31) at 10G/b and capture ~1 million symbols (UI) .
The eye-diagram was composed using an Agilent DSA91304A real time scope.



The Eye diagrams have the same shape in both cases: Socket and Solder attachment. Eye height and eye width remain similar with a slight difference of 0.5ps and 10mV accordingly

Return loss (RL) is the difference, in dB, between forward and reflected power measured at a test point. The return loss value describes the reduction in the amplitude of the reflected energy compared to the forward energy. RL is a way to characterize the severity of an impedance mismatch, i.e Socket or Soldered attachment. In this experiment the DUT was measured with an Agilent N5230C VNA

The ratio of reflected/forward energy from our DUT remains similar in both cases (for Socket and Soldered attachment) over the entire frequency span

Conclusion

The Electrical validation test done with a conductive rubber socket gives adequate results compared to the electrical validation test done with a soldered unit. Conductive rubber has many advantages like: no damage to the board and solder ball, can handle BGA & LGA units & is easy to maintain. During the work it was noticed that the units substrate must be flat and compression is needed to achieve a certain amount of force per pin.

Acknowledgments: The author would like to thank Dahan Elico and Manukovsky Alex for extracting the waveforms and differential 4-port models for the various test sockets. We are thankful to the Intel electrical validation team for their continuous discussions and feedback on our analysis techniques and results.

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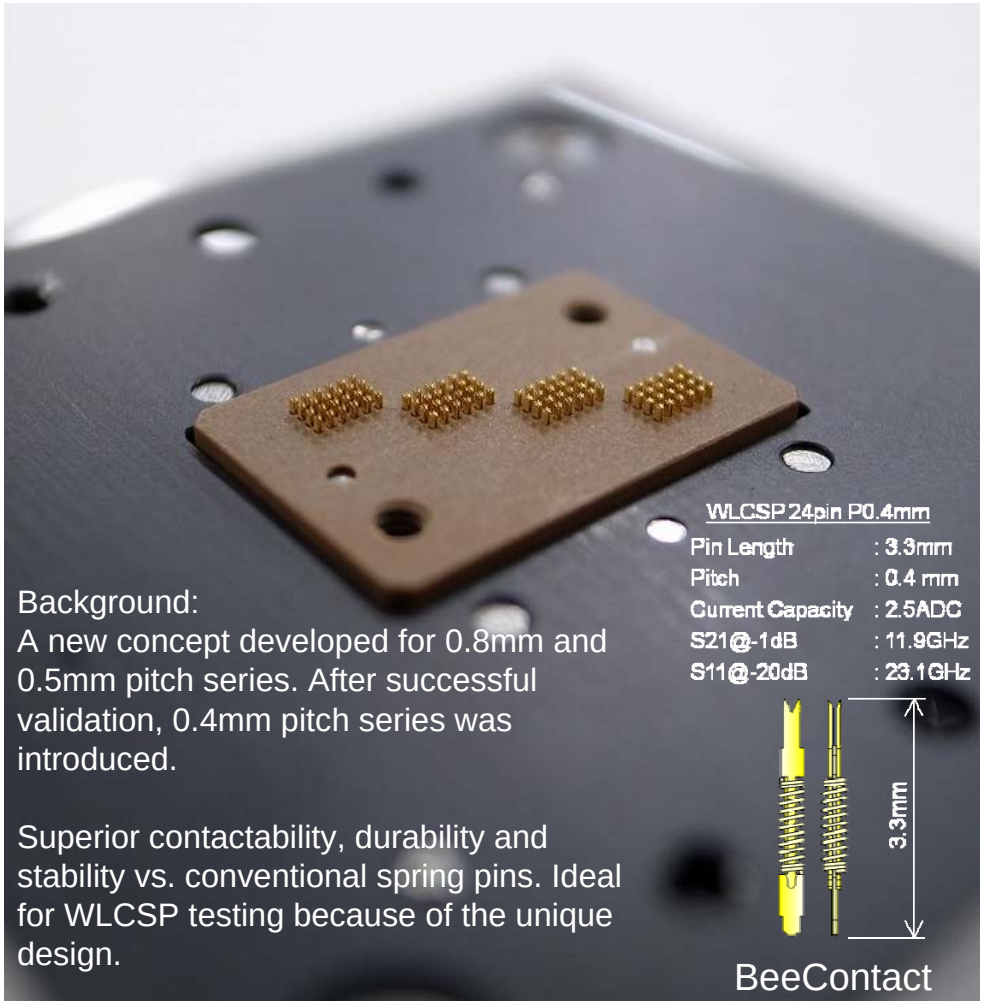
BGA Spring Probe for WLCSP (P0.4mm)

Multipoint Contact to BGA

Eichi Osato, Micronics Japan Co., Ltd.
Fred Megna, MJC Electronics Corp.

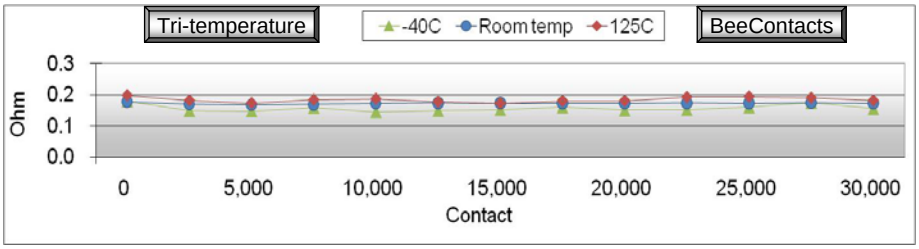


Background:
A new concept developed for 0.8mm and 0.5mm pitch series. After successful validation, 0.4mm pitch series was introduced.

Superior contactability, durability and stability vs. conventional spring pins. Ideal for WLCSP testing because of the unique design.

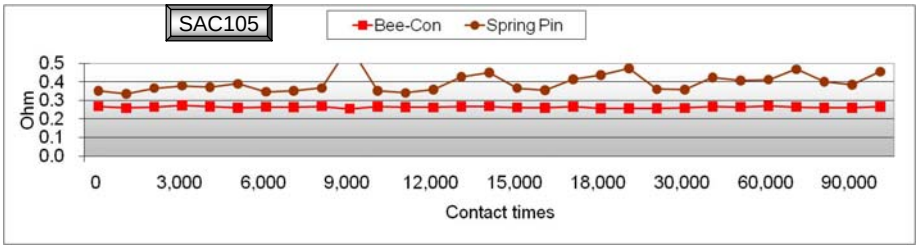
1. Internal Evaluation (Contact Test, tri-temp)

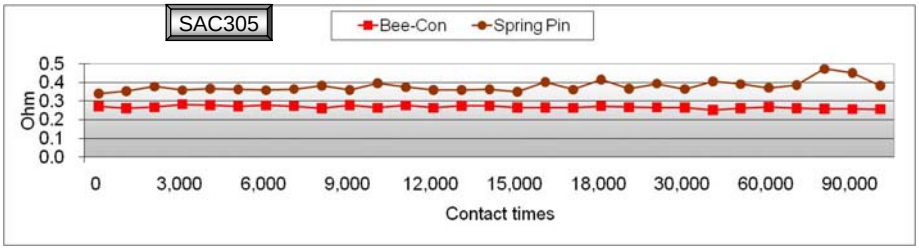
-Gold plate (8 inch)
-Temperature: Tri-Temp (-40C, Room temp, +125C)
-Contact times: 0~30,000

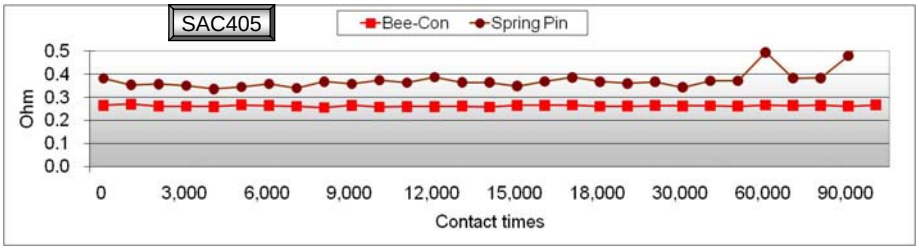


2. Internal Evaluation (Contact Test, tri-solder)

-Solder plate: SAC105, SAC305, SAC405
-Temperature: Room temp
-Contact times: 0~100,000

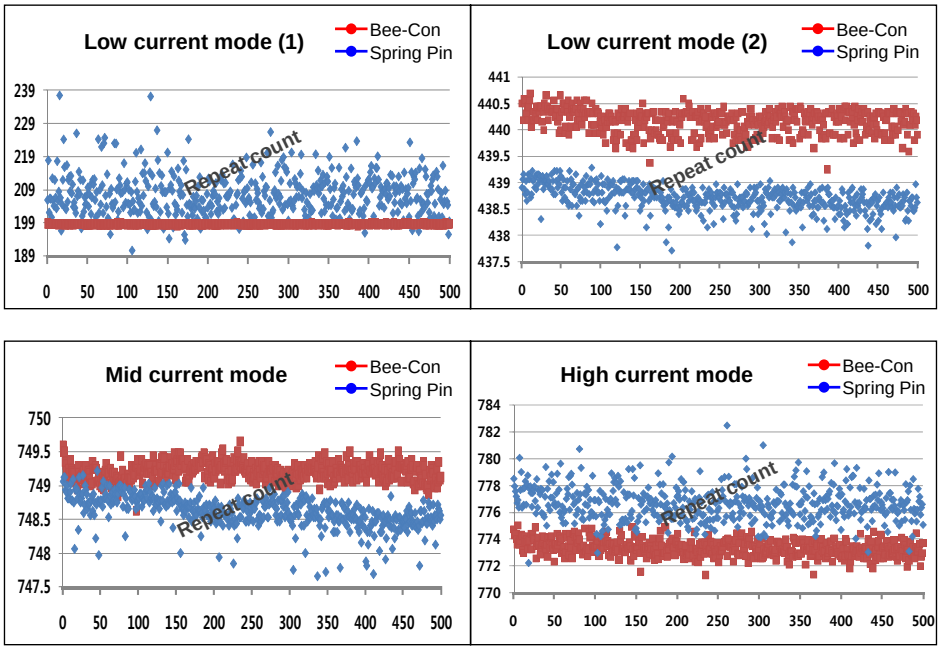






3. Customer Evaluation (Contact Test on WLCSP)

Repeatability Test
-Customer: Amkor
-PKG: WLCSP
-Ball counts: 24pin
-Ball pitch: 0.4mm
-Application: Power Management IC



4. Summary

-WLCSP pitch is getting smaller but still requires high current carrying capacity. This high current for downsized devices is one of the main challenges.

-Unique features include multipoint contact, micro-scrub for solder ball, and large internal contact surface for each plunger. This feature set is the solution for high current carrying capacity test for WLCSP.