BiTS 2010 Tutorial

ARCHIVE 2010

SOCKET RF CHARACTERIZATION LAB

by

Gert Hohenwarter, Ph.D.
President
Gatewave Northern, Inc.

ABSTRACT

This Tutorial is taught by Gert Hohenwarter of GateWave Northern, an industry expert on socket and interconnect characterization. In this tutorial he'll bring the electrical measurements lab to the classroom.

The material and demonstrations will be tailored for both the manufacturers of test sockets as well as the end user. The lab will start with a brief foundation of the relevant parameters and their importance in the final application. This will promote understanding of the basic concepts for electrical and non-electrical engineers alike.

With that knowledge gained various testing configurations will be discussed. Among those are traditional spring probe test arrangements as well as more complex BGA pin arrays. Pin pairs, differential and multi-port measurements will also be examined. Configuration specific issues such as parasitic inductance and capacitance of interfaces to the socket that affect socket application as well as testing are included in this discussion.

The lab will then cover various testing equipment used in the industry including inductance analyzers, time domain reflectometers and vector network analyzers. An accounting of each instrument's specific strengths, weaknesses and practical limitations is given.

A hands-on test section with scale models operating at low frequency for ease of use will allow for examination of specific configurations during the lab.

Finally, attendees will have the chance to analyze test reports and learn how to extract the most information for their specific application.

BiTS 2010 **Tutorial**

Who should have attended this Tutorial?

This tutorial offers a great learning environment for a wide range of workshop attendees. Those with a basic knowledge of the socket's electrical attributes will have the opportunity to step through all the measurement methods and gain an understanding of how the industry uses these results. Attendees already comfortable with these basic concepts will find both the practical demonstrations as well as the small classroom setting with an expert helpful to strengthening their electrical knowledge. Where else can you have 1:1 experience with an 18 year veteran in the field of signal integrity?

Socket RF Characterization Lab

2010 BiTS Tutorial

Gert Hohenwarter

GateWave Northern, Inc.

2010 BiTS Workshop
March 7 - 10, 2010

Objective of workshop

- Establish an outline of test socket characterization basics
  - for manufacturer
  - for end user
- Provide attendants with an understanding of test parameters, goals and procedures as well as test focus
- Outline equipment and capabilities
- Give hands-on scale model test opportunities

Approach

- Brief review of the relevant test parameters
  - basic concepts
  - importance in the final application
- Configurations
  - pin pairs, differential and multi-port measurements
  - test configurations
  - parasitic inductance and capacitance of interfaces
- Test equipment – some of its strengths, weaknesses and practical limitations
  - inductance/capacitance/impedance analyzers
  - time domain reflectometers
  - vector network analyzers
  - other
- Hands-on test section
  - select measurements on a scale model socket (low frequency operation)
- Analysis of a test report and how to extract the most information for a specific application

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Gert Hohenwarter

Education

Ph.D., University of Wisconsin, Madison
Superconducting microwave electronics
MSEE, University of Wisconsin, Madison
RF coupling of Josephson junctions in a Fabry-Perot resonator
Diplom -Ingenieur Elektrotechnik TU Braunschweig, Germany
X-Band microwave filters, oscillators

Professional

GateWave Northern, Inc.
RF design, models and measurement
Signal integrity consulting
HYPRES, Inc.
70 GHz interface to cryogenic electronics development
University of Wisconsin, Madison
Superconducting microwave electronics
SIEMENS, Munich
Microwave oscillator tuning and testing
Arthur Dieffenbach, Frankfurt, Germany
Electronics, ultrasound imaging

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Objective of test

- Goals of a test socket characterization by measurement
  - Provide feedback to manufacturer
    - Performance
    - Highlight need for potential improvement
    - Impact of design changes
    - Model verification
  - Provide info to end user
    - Performance prediction
    - Comparison with other products

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Details of a socket test

- Parameters of interest
  - Inductance
  - Capacitance
  - Impedance
  - Insertion loss / return loss
  - Crosstalk
- Explore impact of configuration
  - G-S
  - G-S-G
  - G-S-S-G
  - Checkerboard
  - Pogo test
  - Multi-port
  - 'Random'
- Outline process of characterizing a test socket
  - Time domain vs. frequency domain
  - Instrument function
  - Test fixtures
  - Relevance for test

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Parameters

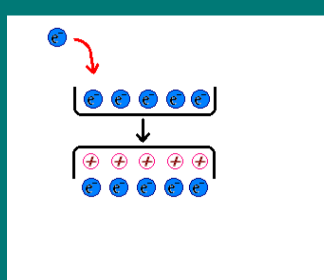
Standard:

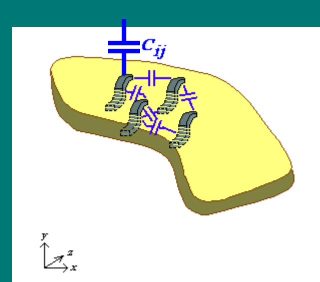
- Capacitance
- Inductance
- Impedance
- Delay
- Risetime
- Insertion loss
- Return loss
- Crosstalk

Optional:

- Eye diagrams
- Resistance
- Imax
- Leakage

Capacitance

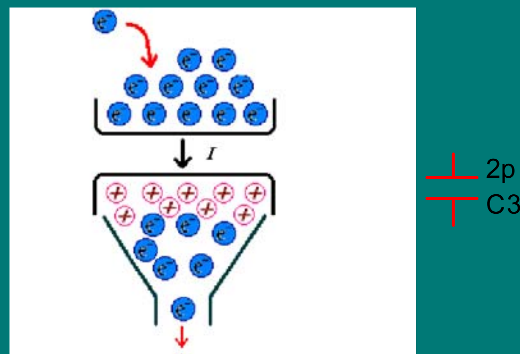




Charge accumulation on either side of a gap results in surplus charges of one kind on the respective side. An electric field exists in the gap. Residual conductivity will cause leakage when DC is applied.

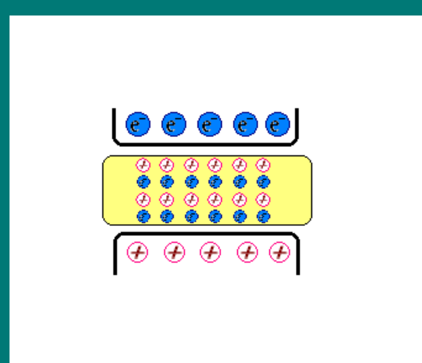
Capacitance exists from all pins to all pins. Generally, only the nearest neighbors are significant.

Capacitor



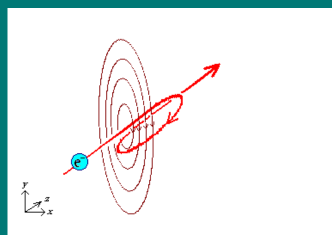
Capacitive (displacement) current: While charging a capacitor a current flows through it. The current is proportional to the rate of change of the voltage.

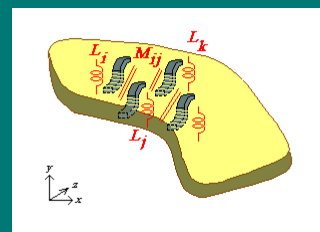
Permittivity



Matter contains charge that can align itself to the electric field lines, thereby enhancing the field (E). Loss occurs when this process occurs at elevated frequencies.

Inductance





Motion of charge is accompanied by a magnetic field. Just like in the case of the capacitor, the field is established by providing energy from a source.

Each pin contributes inductance. Mutual terms exist between all pins.

Only the nearest neighbors are relevant.

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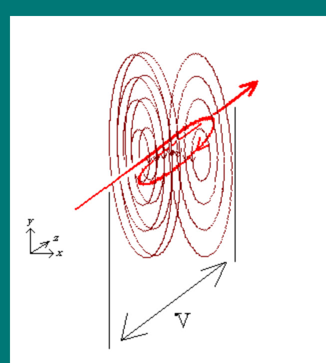
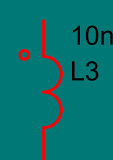
Inductor





While building up a magnetic field in an inductor, a voltage exists across the inductor's terminals. The rate of change of the current determines the voltage.

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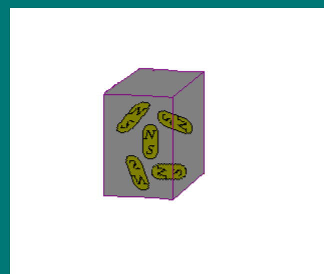
Permeability



Ferromagnetic material contains small dipoles that can align themselves with the magnetic field (H) and thus enhance it. This may be of significance in contacts with a large percentage of ferromagnetic materials such as Ni.

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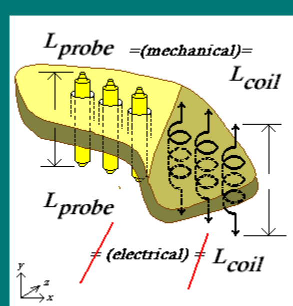
Inductance



Inductance directly impacts quality of power delivery on both ground and power connections.

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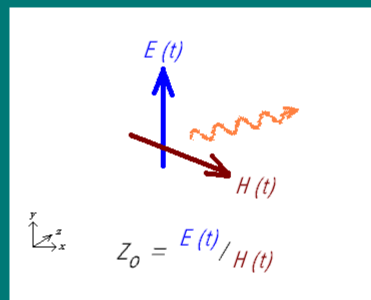
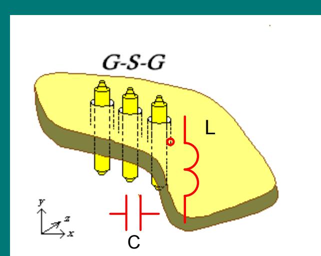
Impedance



The ratio of E and H is the characteristic impedance Z_O.

In the simplest equivalent circuit representation of a connection by one inductor and one capacitor the relative size of L and C determines the characteristic impedance of the interconnect according to $Z = \sqrt{(L/C)}$.

Capacitance & Inductance -> Impedance $Zo = \sqrt{(L/C)}$



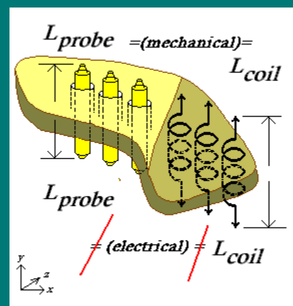
Socket impedance Zo depends primarily on:

Configuration of signals and grounds

Contact dimensions and material -> L

Dimensions and dielectric constant of the socket material -> C

Electrical Length $td = \sqrt{(L*C)}$

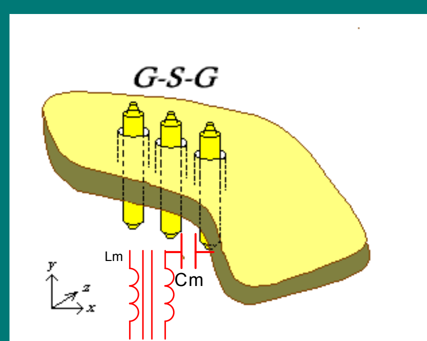


Socket electrical length td depends primarily on:

Contact length and material -> L

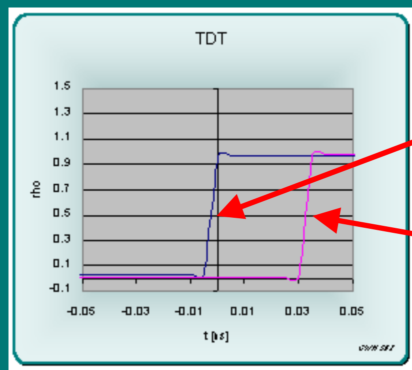
Dimensions and dielectric constant of the socket material -> C

Mutuals



- Mutual capacitance causes current to flow from a contact to its neighbors.
- Mutual inductance causes a voltage to appear on its conducting neighbors when a current flows in a pin.
- Crosstalk results as a consequence of either.

Time Domain Transmission - Delay td



at source

at load / DUT

A signal requires a finite amount of time to travel through a structure. In air it travels a distance of 1 mm (0.040”) in 3.3 ps. This time requirement increases if matter is encountered.

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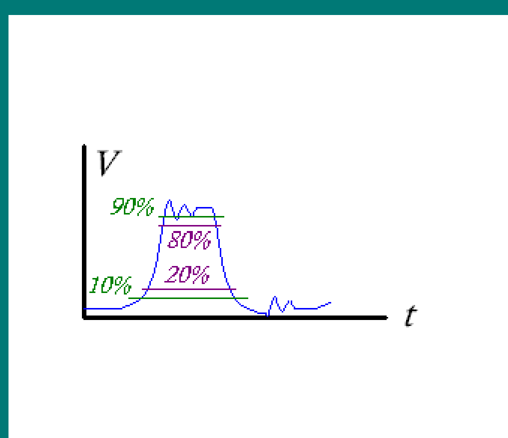
Risetimes



A risetime generally is taken from 10% - 90% of the total signal. In digital circuits 20% - 80 % may be more meaningful.

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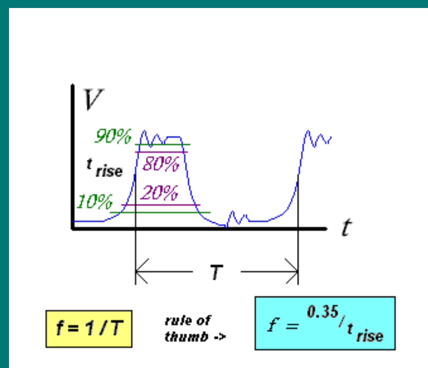
Operating Speed



Time and frequency are related and risetime can be associated with a maximum frequency of operation.

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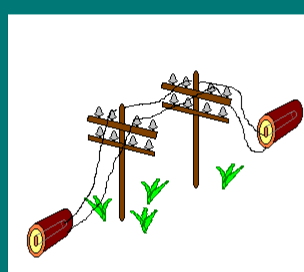
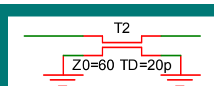
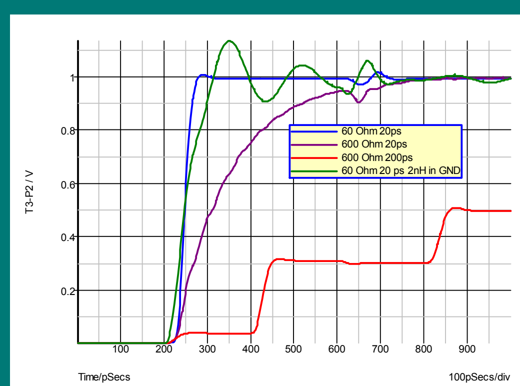
Importance of impedance and delay to the Signal Path Design







There is a need to provide a coherent and consistent signal propagation environment. The ground return path is vital.

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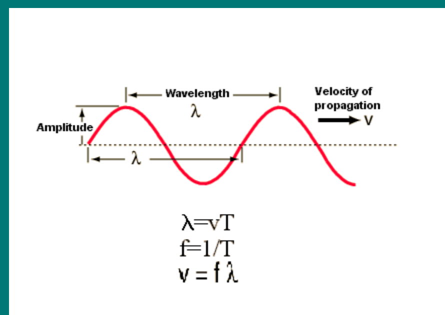
Wavelength



Example: At 10 GHz the wavelength in free space is 3 cm (about 1.25”). In matter it drops according to the square root of the dielectric constant.

Signal transmission must take note of the wavelength. Obstacles and structures of size greater than 1/10 of this wavelength need special consideration.

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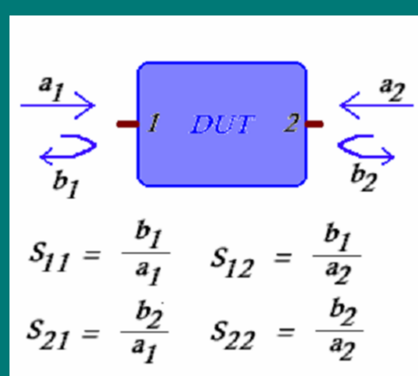
S-parameters



The scattering parameters are defined as the ratios of incident and reflected voltage wave amplitudes.

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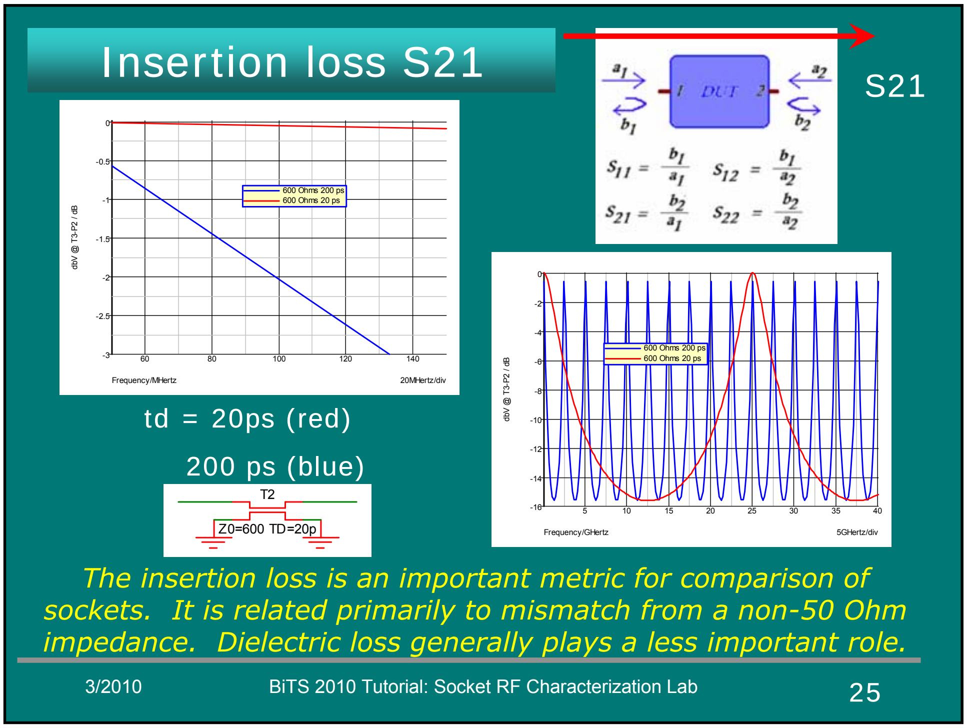
Insertion loss S21
S21
$S_{11} = \frac{b_1}{a_1}$ $S_{12} = \frac{b_1}{a_2}$
$S_{21} = \frac{b_2}{a_1}$ $S_{22} = \frac{b_2}{a_2}$
DUT
600 Ohms 200 ps
600 Ohms 20 ps
Frequency/MHertz
20MHertz/div
Frequency/GHertz
5GHertz/div
td = 20ps (red)
200 ps (blue)
T2
Z0=600 TD=20p
The insertion loss is an important metric for comparison of sockets. It is related primarily to mismatch from a non-50 Ohm impedance. Dielectric loss generally plays a less important role.
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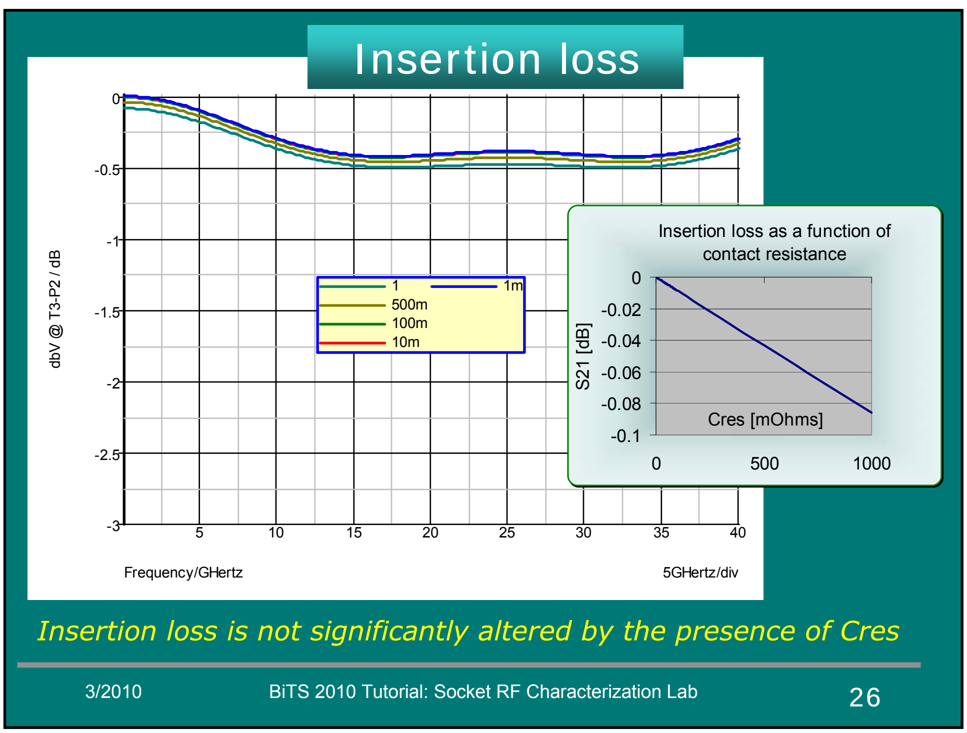
Insertion loss
dbV @ T3-P2 / dB
Frequency/GHertz
5GHertz/div
1
1m
500m
100m
10m
Insertion loss as a function of contact resistance
S21 [dB]
Cres [mOhms]
0
500
1000
Insertion loss is not significantly altered by the presence of Cres
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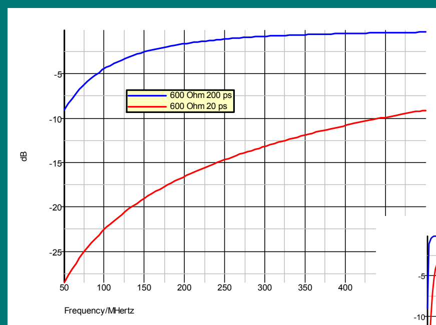
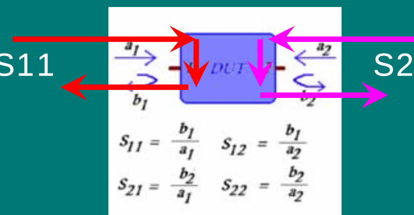
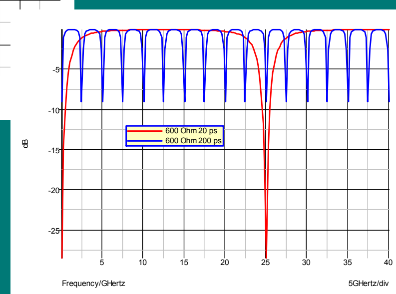
Return loss S11, S22





td = 20ps (red)

200 ps (blue)



The return loss is a metric for the comparison of sockets.

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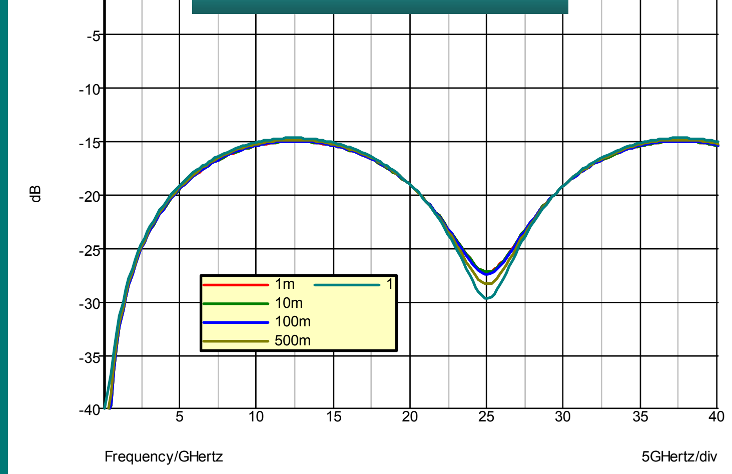
Return loss



Return loss is not significantly altered by the presence of Cres

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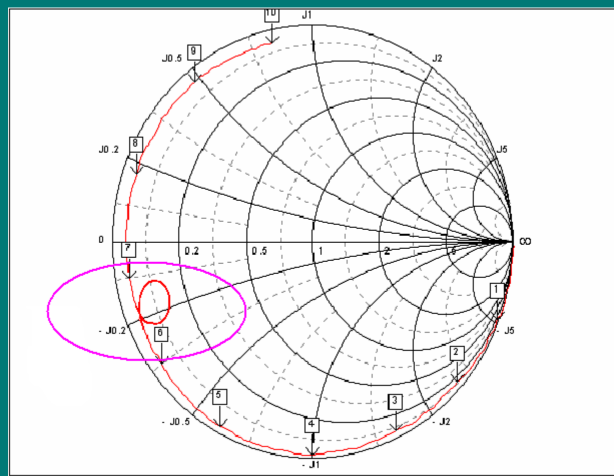
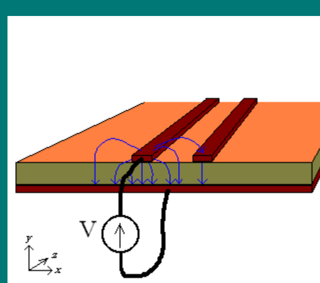
Smith Chart

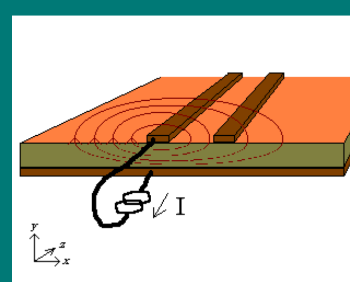


The Smith chart is a plot of the reflection coefficient in the complex plane. It readily reveals resonances in the system.

Crosstalk

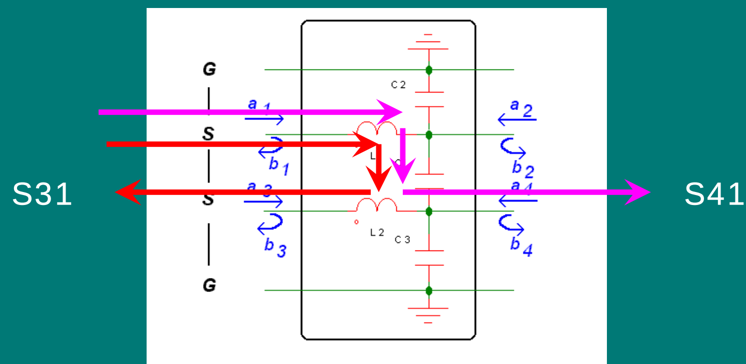


Electric field lines reach the adjacent trace and couple a portion of the signal into it.



Magnetic field lines overlap the adjacent trace and couple a part of the signal to it.

Crosstalk



Crosstalk exists in both forward and reverse directions. S31 and S41 must both be acquired. All ports must be terminated into 50 Ohms. Crosstalk is cumulative from multiple adjacent connections and may therefore have to be carefully managed.

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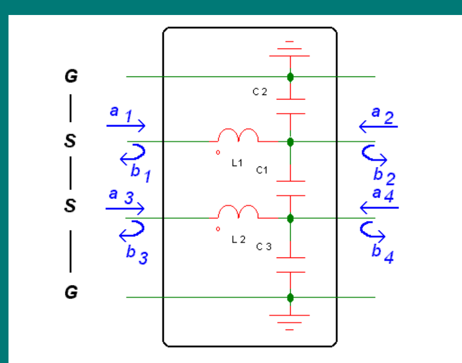
Differential Signaling



Differential signaling affords easier signal routing and handling and improved signal integrity. A four-port VNA is needed or 16 measurements with a two port VNA must be taken and properly processed.

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Pin Configurations

- S
- G-S
- G-S-G
- G-S-S-G
- Checkerboard
- Pogo test
- Multi-port
- ‘Random’

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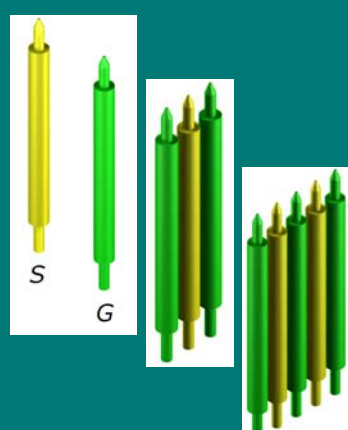
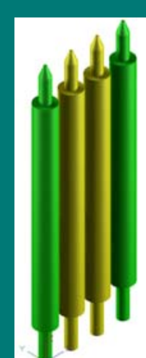
Linear array

G-S
G-S-
G



G-S-S-G



G-S-S-G testing
provides applicable info

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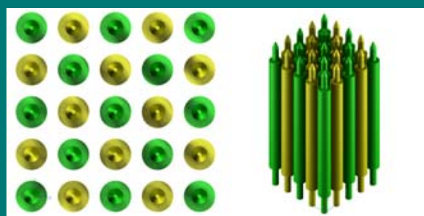
2D arrays

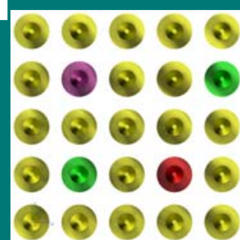
Checkerboard

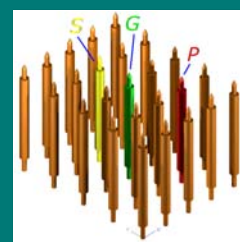


G-S-G and G-S-S-G testing provides good approximation (see slides on test configurations below)

Multi-port & 'random'

G-S-G and G-S-S-G testing provides approximate info Exact measurements/models require replication of the exact S/P/G configuration

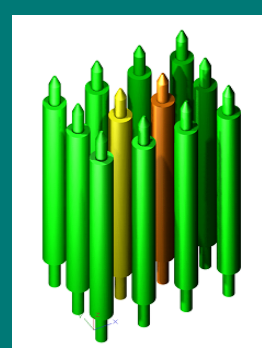




Test configurations

Typical test fixture configuration for single pin self inductance characterization. Return current flows through holder.

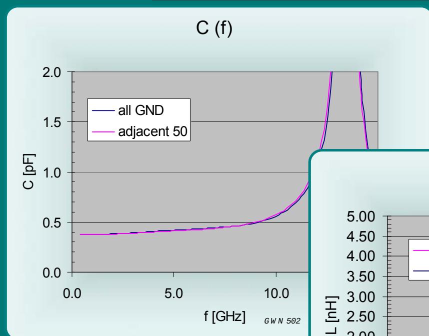
- Inductance value higher than in actual application.
- No capacitance info to nearest pins available.
- Limited upper frequency range.



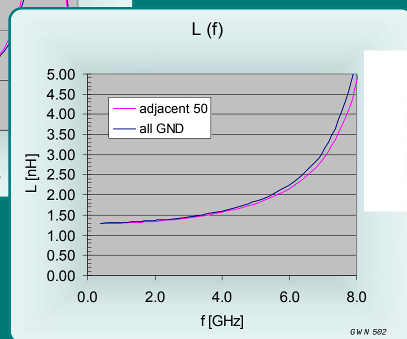
G-S-G / G-S-S-G spring probe test configuration (3 x 4). But…

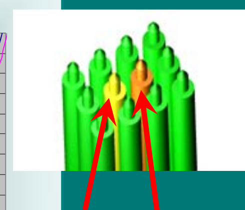
Is this a useful arrangement ?

Configurations-test L,C



Graphs show the impact of grounding one of the S pins in a G-S-S-G vs. connecting it to 50 Ohms:



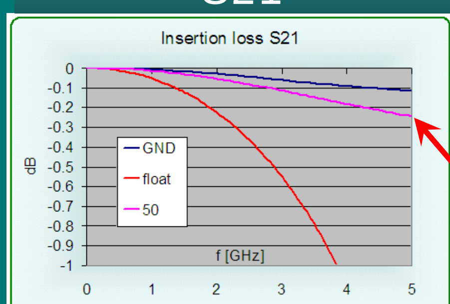


S G or 50Ω

No significant difference is noticeable – this provides a rationale for grounding all unused pins during test

Configurations-test S21

Graphs show the impact of floating one of the S pins in the array vs. connecting it to 50 Ohms or GND:

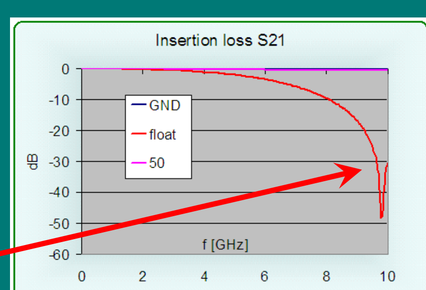


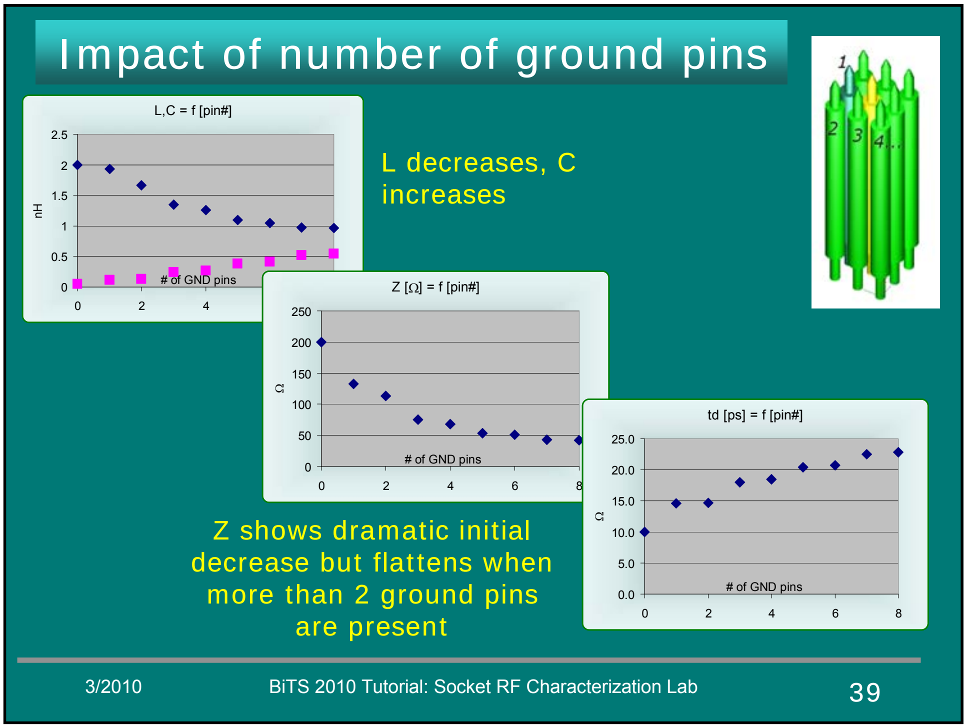
S21 to 5 GHz: Shows loss from 50 ohm loads

S G, 50Ω or float

S21 to 10 GHz:

Shows resonance when the signal frequency is such that the floating adjacent pin is ½ wavelength long




Impact of number of ground pins
L,C = f [pin#]
nH
# of GND pins
L decreases, C increases
Z [Ω] = f [pin#]
Ω
# of GND pins
td [ps] = f [pin#]
Ω
# of GND pins
1
2
3
4...
Z shows dramatic initial decrease but flattens when more than 2 ground pins are present
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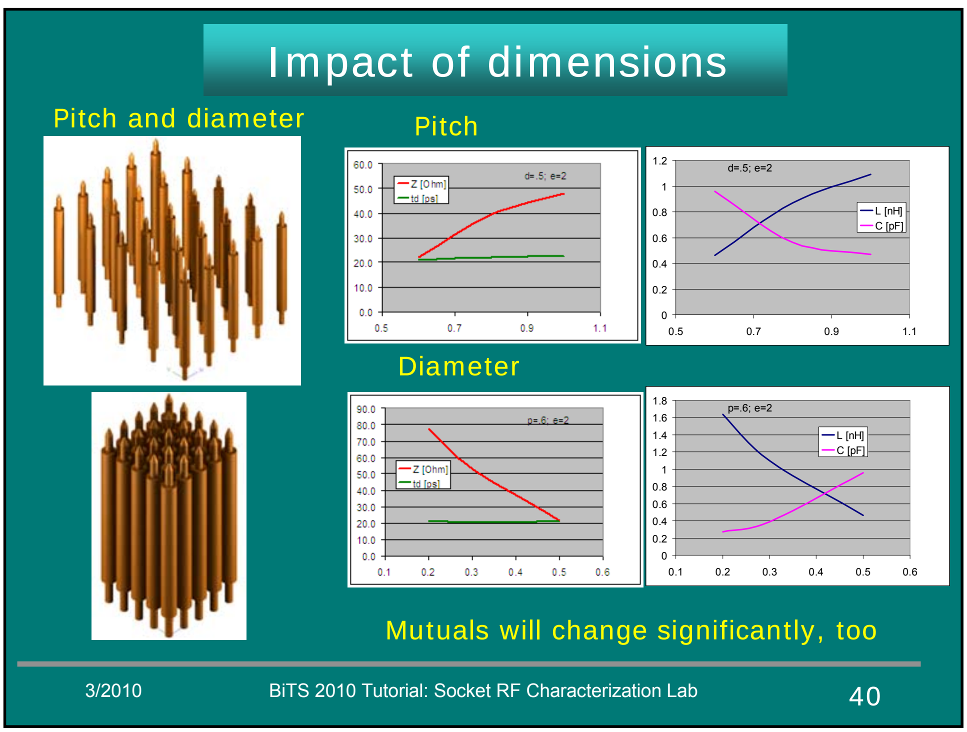
Impact of dimensions
Pitch and diameter
Pitch
Z [Ohm]
td [ps]
d=.5; e=2
L [nH]
C [pF]
Diameter
p=.6; e=2
Z [Ohm]
td [ps]
L [nH]
C [pF]
Mutuals will change significantly, too
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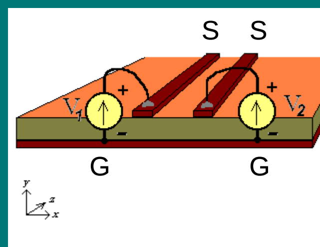
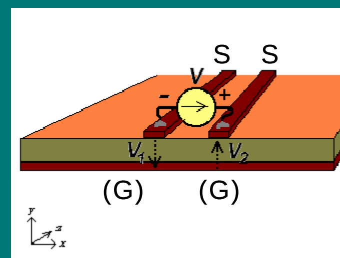
Single Ended vs. Differential Signaling

SE



Differential



A voltage is established between a signal line and ground. Two lines are shown, each being driven by one source.

A voltage is established between two signal lines. The ground (underside of the circuit board) serves merely as a reference. But…

G-S-S-G (S4P) test allows for extraction of differential parameters

Test equipment

- *Meters*
- *Impedance analyzers*
- *Time domain reflectometers*
- *Network analyzers*
  - *Scalar network analyzers*
  - *Vector network analyzers*
- *Custom built instruments*

L, C meters

- *Pros*
  - *Low to moderate cost*
  - *Simple operation*
  - *Little training required*

~100s pF min.

~ uH min.

~ sub pF min.

~ nH min.

- *Cons*
  - *Very low to low operating frequency*
  - *Mostly single frequency*
  - *High risk of obtaining erroneous/improper results*
  - *Range / accuracy limitations*
  - *Needs cal to apply to test configuration*
  - *Difficult to obtain 'unperturbed' measurement*

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Precision Z analyzers (L, C, R)

- *Pros*
  - *Measurement as a function of frequency*
  - *Up to ~ 3 GHz frequency range*
  - *Accurate measurement instrument*
    (configuration/test fixture influence notwithstanding)
- *Cons*
  - *Significant cost*
  - *Training required*
  - *Typically used for single contact measurement*
  - *Fixture and calibration required*
  - *Needs expertise to apply to specific test configuration*

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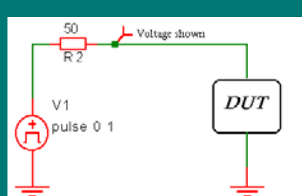
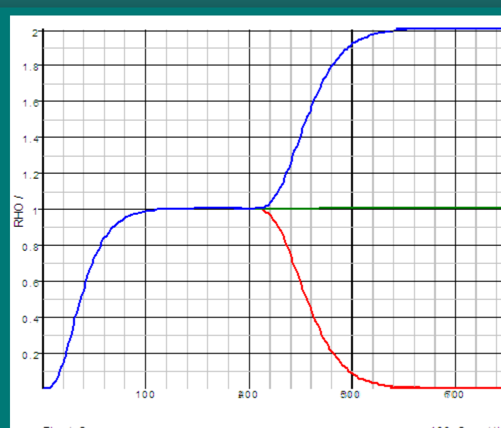
Time Domain Reflectometer

- *Pros*
  - *Relatively simple operation and calibration*
  - *Waveform visualization*
  - *True differential excitation possible (less important for passive devices, however)*
  - *S-parameter and parameter extraction software options available*
- *Cons*
  - *Moderate to high cost*
  - *Training required*
  - *Fixture and calibrators needed, but only short cables can be used*
  - *Needs expertise to apply to specific test configuration*
  - *Limited L,C accuracy if no S-parameter or added parameter extraction software option is used*
  - *Risk of 'overlooking' resonances if no S-parameter option*

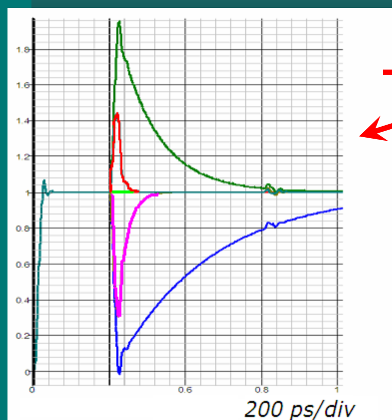
Time Domain Reflectometer Operation

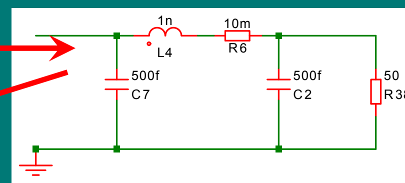




A step voltage is generated near t=0. The signal then propagates to the device under test (DUT).
The blue curve corresponds to an open circuit, the green one to a perfect 50 Ohm termination and the red one to a short circuit.

Time domain reflectometer characterization of interconnects





Sample circuit

Simulation of the TDR response for 1nH (red), 10 nH (green), 1 pF (pink) and 10 pF(blue) discontinuity

Time domain characterization of interconnects is based on the observation that the TDR waveform contains information about the discontinuities that the signal encounters.

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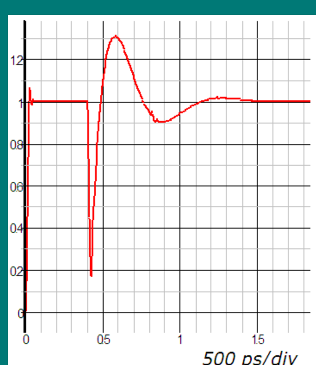
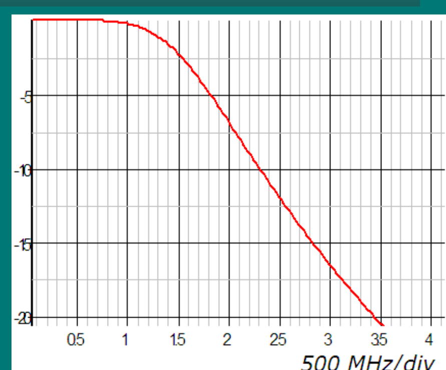
Time domain characterization of interconnects

V (rho)

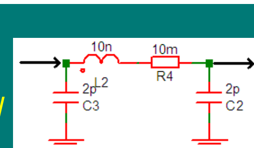


dB



Simulation of the TDR vs. VNA thru response for a LC Pi:

Time domain characterization does not reveal that the circuit "cuts out" above 1.5 GHz.



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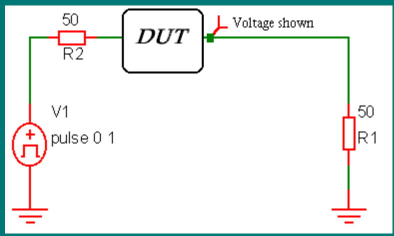
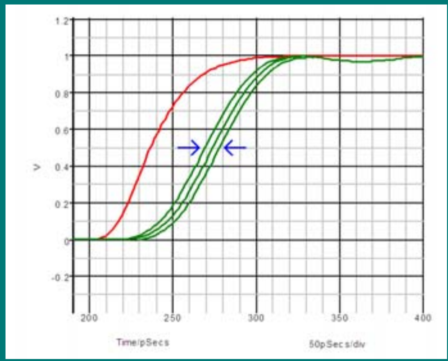
Time Domain Transmission



TDT circuit



The red curve is from the instrument into a perfect 50 Ohm load, the green curve is through a connector/socket into a 50 Ohm load. Skew is an important metric for multiple signal paths to a device under test (see blue arrows).

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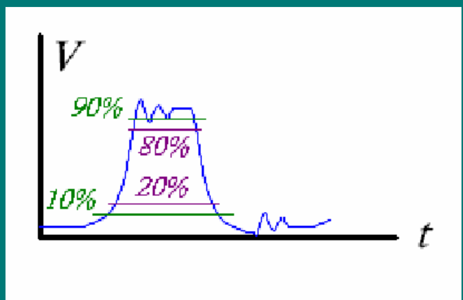
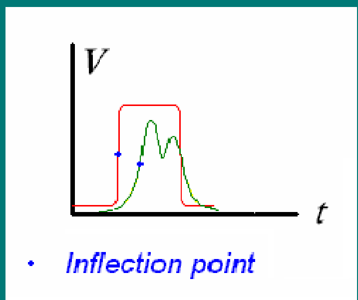
Risetime and delay





Risetime is generally defined from 10% - 90% of the total signal.
In digital circuits, however, 20% - 80 % may be more meaningful.

A 50% point cannot always be reliably identified. Thus, delay might be measured as the time between the inflection points of two signals.

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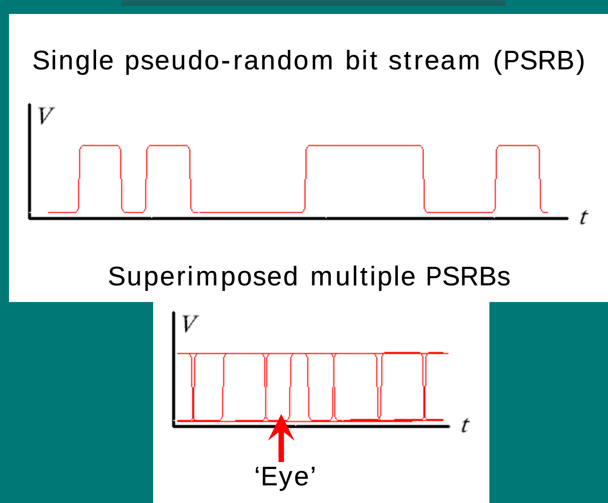
Time domain characterization of interconnects

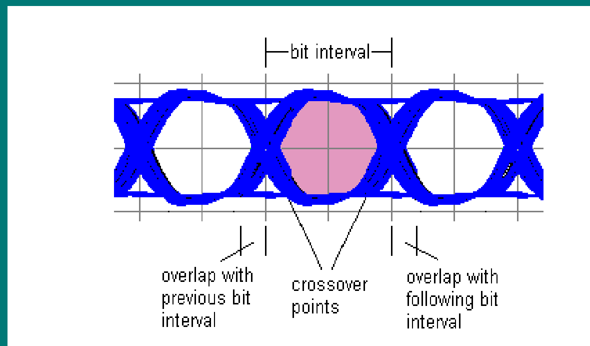
- *Advantages of time domain characterization are visualization of waveforms, lower cost instrumentation and less demanding measurement environments.*
- *Time domain characterization works well for large scale systems where crosstalk is not a major issue.*
- *A TDR provides a single pulse, an actual system operates with pulse trains. This can cause resonances not readily detected with TDR techniques.*
- *The TDR waveform contains decreasing amounts of energy at increasing frequencies. This will make accurate judgment of very high frequency performance more difficult or impossible.*
- *Long cables cannot be used with TDRs since signal attenuation and dispersion causes rapid deterioration of high frequency signal components.*

Eye Diagram



The eye diagram combines successive waveforms with different bit patterns.

Eye Diagram



The traces around the eye (purple region) broaden with deteriorating signal conditions. A receiver will be less and less able to distinguish the waveforms as the eye closes.
An eye diagram is an important tool to assess overall signal path performance. There is a high risk of not detecting resonances in the system path, however.
An eye diagram for a test socket alone is relatively meaningless.

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Eye diagram

- *The eye diagram serves as a system level tool to assess whether there will be reliable data transmission from source to receiver.*
-
- *Use of the eye diagram as a characterization tool for individual components is limited since component and model development are difficult.*

- *A meaningful eye diagram for a socket requires the knowledge of the interconnect parasitics inclusive those of the chip package and on-chip devices and connections.*

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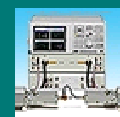
Vector Network Analyzer



- Pros
  - Highest frequency of operation
  - Very accurate
  - Time domain options available
  - Results readily interface with advanced software
- Cons
  - High cost
  - Training required
  - Fixture and relatively complex calibrators required
  - Needs expertise to apply to specific test configuration
  - No waveform visualization if time domain option not installed

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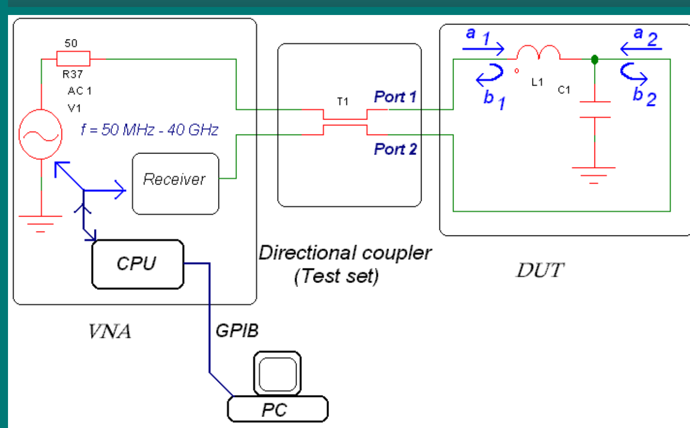
Vector Network Analyzer Operation



The vector network analyzer contains a swept frequency RF source and a synchronized phase sensitive receiver. Its output is fed to an internal CPU for data manipulation.

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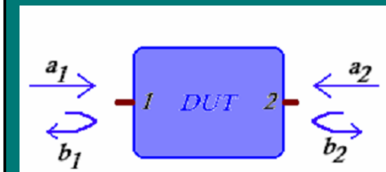
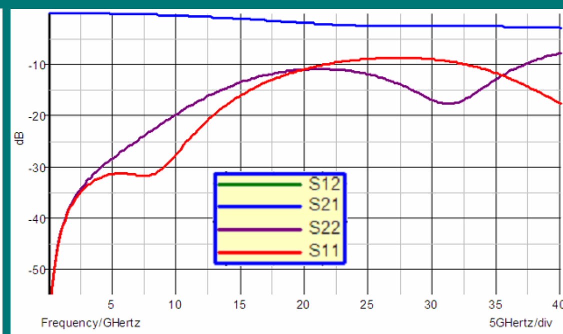
S-parameters



$$S_{11} = \frac{b_1}{a_1} \qquad S_{12} = \frac{b_1}{a_2}$$

$$S_{21} = \frac{b_2}{a_1} \qquad S_{22} = \frac{b_2}{a_2}$$



Socket model example

The scattering parameters are defined as the ratios of incident and reflected voltage wave amplitudes.

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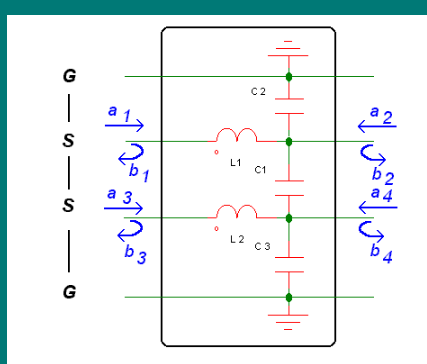
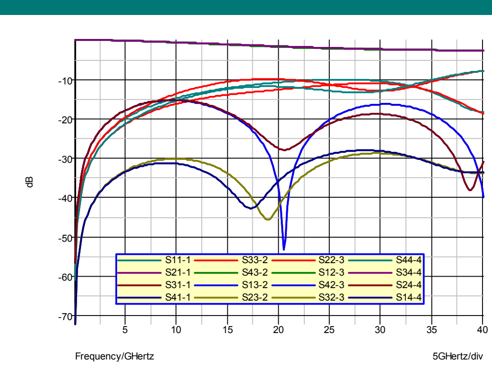
Differential Signaling





Differential signaling affords easier signal routing and handling and improved signal integrity. A four-port VNA is needed or 16 measurements with a two-port VNA must be taken. Measurements with more than 4 ports require even larger numbers of individual measurements.

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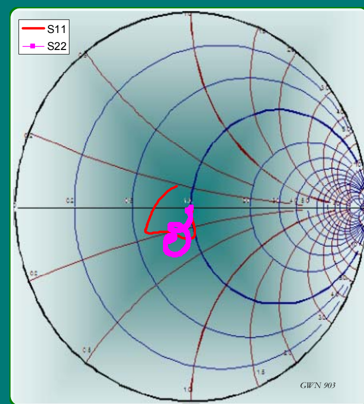
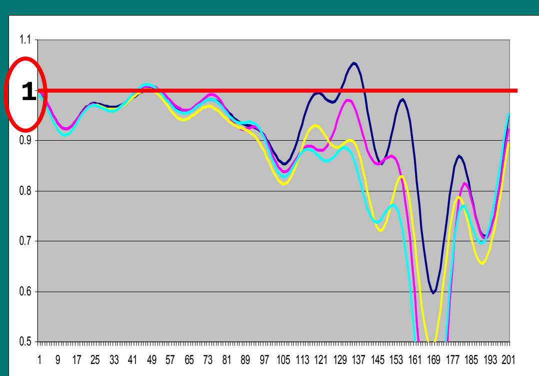
Smith Chart



The Smith chart is a plot of the reflection coefficient in the complex plane. S-parameters acquired with a VNA readily lend themselves to Smith chart representation. The Smith chart enables detection of even small resonances via "loops" in the response.

Passivity



A socket is passive – it does not generate any RF power. Therefore the total power detected coming from the socket (reflected and transmitted) must be less than that delivered. This test is best performed in the frequency domain with data acquired from a VNA.

Frequency Domain Analysis

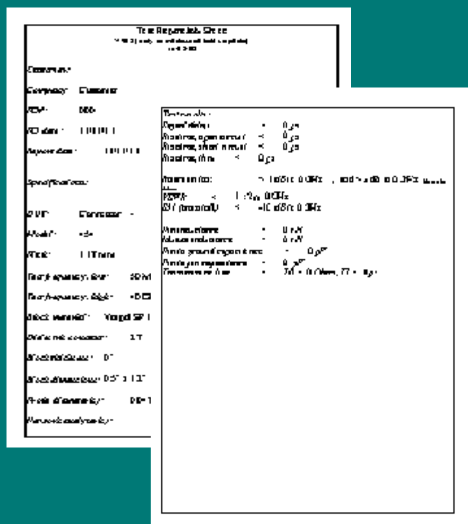
- *A vector network analyzer has a signal source that provides a constant signal level up to the highest frequencies. This distinguishes it from the step excitation in a time domain reflectometer that has a 1/over decay of high frequency components.*
- *Frequency dependent calibration allows the use of long cables between source and device under test without any loss of fidelity or accuracy. This is not possible with a time domain reflectometer since long cables cause significant attenuation of the already weak high frequency components.*
- *Use of sophisticated calibration techniques for the VNA make it the highest accuracy instrument available.*
- *Dataset extraction and processing for CAD and CAE systems is readily available.*
- *Time domain options are available for visualization of waveforms as in a time domain reflectometer.*

Socket testing

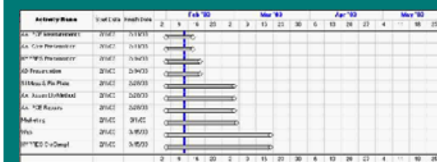
Electrical Testing

The process

Project Start



An important part of the test procedures is the proper documentation of tests, procedures and file tracking



Projects are mapped with job travelers

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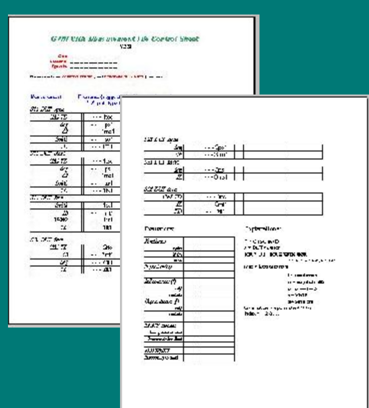
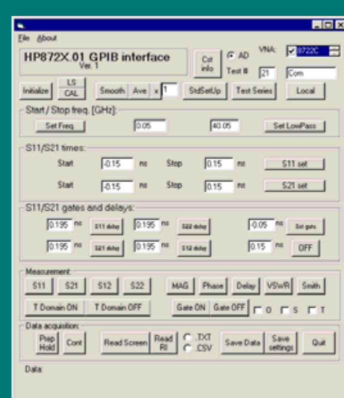
Measurement Tracking and File Control





Detailed travelers and specialized software are used to track measurement progress and file collection

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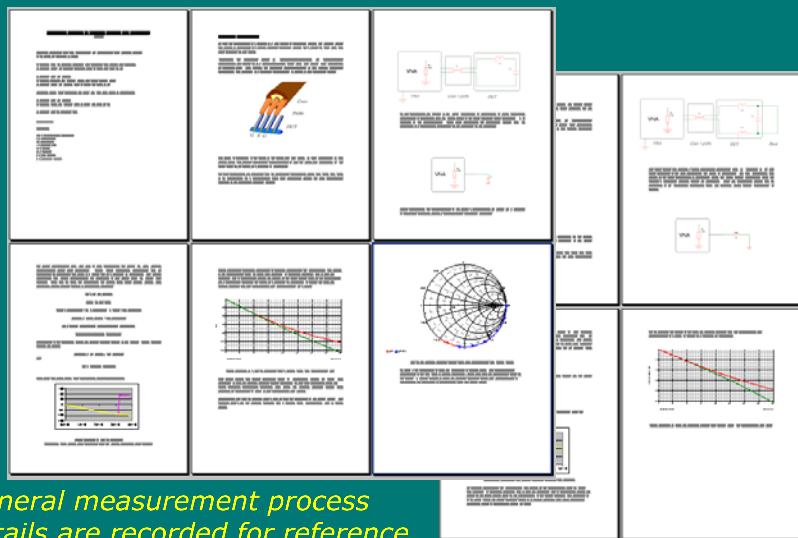
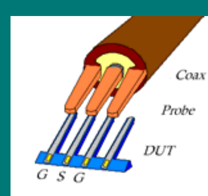
Measurement Process Documentation



General measurement process details are recorded for reference

Typical Test Arrangement



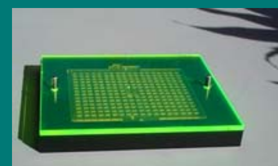
Most commonly used probing arrangements are G-S-G, G-S, and G-S-S-G

The physical arrangement impacts the outcome of the characterization. Likewise, the performance in the actual application is affected by the return current flow arrangement as well.

2 port measurements with DUT interfaces (if necessary, 4 port measurements are derived from the 2 port configuration)

Probes and Mechanical Interfaces

Pinplate for pogo pin tests (>0.25 mm pitch)



Testbed for an array of micro-contactors (wafer probing, 150 um pitch)

Coax microprobes to 0.013" dia.

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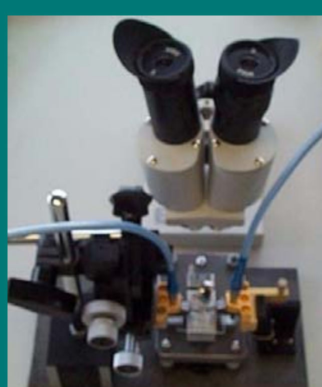
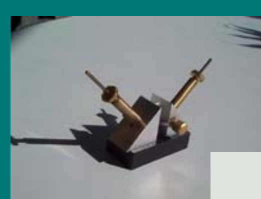
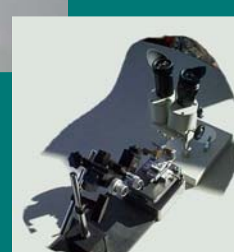
Probe Stations







Probe interfaces and stations are tailored to accommodate individual test requirements

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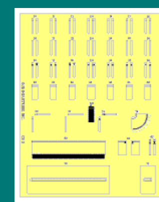
Measurement Calibration

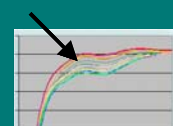
- End of coax with standard cal kits
- Standard probes with standard cal substrates



- Probes and fixture are deembedded
- Calibration through probe option (custom calibrators)
- Calibrators for system verification

- SOLT standard {TRL & TRM optional} calibrations

(The accuracy difference is generally negligible in the context of a typical parameter sensitivity to probe z-position and other factors)



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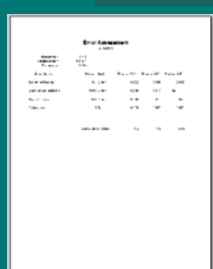
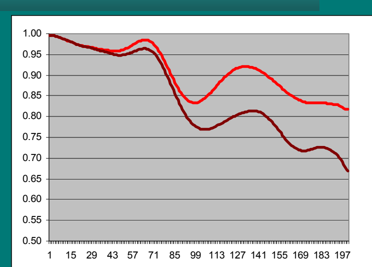
Measurement Validation



Error assessments are used as a tool to identify the type and significance of contributions to measurement uncertainty



In a passive system total power out must be equal or less than total power in (passivity).

Time gating is employed to eliminate the impact of multiple reflections from interfaces outside the valid time windows. Potential errors must be carefully considered, especially in the context of passivity and causality.

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Models

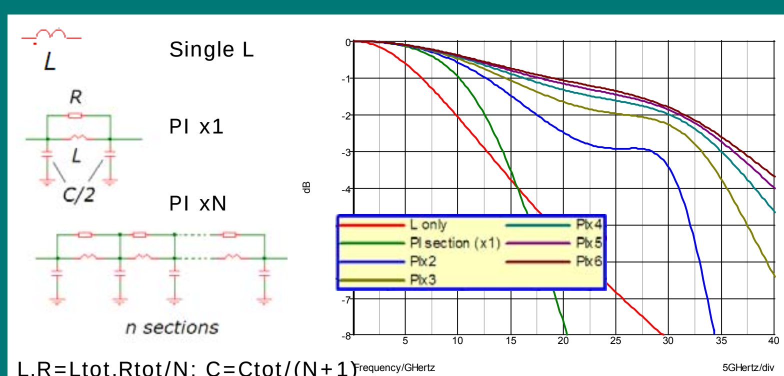
- *Extracted models for contacts and sockets using RLC model to quantify parasitics*
- *Equivalent transmission line circuits where applicable*
- *SPICE circuits and models*
- *Fitted multi-pole models (PSPICE, HSPICE)*
- *IBIS models*

.S2P / .S4P data files extracted from measured data, fitted and passivity plus causality enforced

```
****************************************
* Synthesis of real and complex poles *
****************************************

* Real pole n. 1
CS_1 NS_1 0 9.9999999999999998e-013
RS_1 NS_1 0 2.8637225251303093e+001
GS_1_1 0 NS_1 NA_1 0 3.5996764903480655e-001
GS_1_2 0 NS_1 NA_2 0 -3.7156227088373162e-001
*
* Real pole n. 2
CS_2 NS_2 0 9.9999999999999998e-013
RS_2 NS_2 0 2.8637225251303093e+001
GS_2_1 0 NS_2 NA_1 0 2.9856551462468101e-001
GS_2_2 0 NS_2 NA_2 0 2.8924876071699995e-001
*
* Complex pair n. 3/4
CS_3 NS_3 0 9.9999999999999998e-013
CS_4 NS_4 0 9.9999999999999998e-013
RS_3 NS_3 0 7.3043500212240986e+001
RS_4 NS_4 0 7.3043500212240986e+001
GL_3 0 NS_3 NS_4 0 1.2411980879163279e-001
GL_4 0 NS_4 NS_3 0 -1.2411980879163279e-001
GS_3_1 0 NS_3 NA_1 0 6.4019351899817778e-002
GS_3_2 0 NS_3 NA_2 0 -1.0610030831102265e-002
GS_4_2 0 NS_4 NA_2 0 6.2971137144757619e-002
*
```

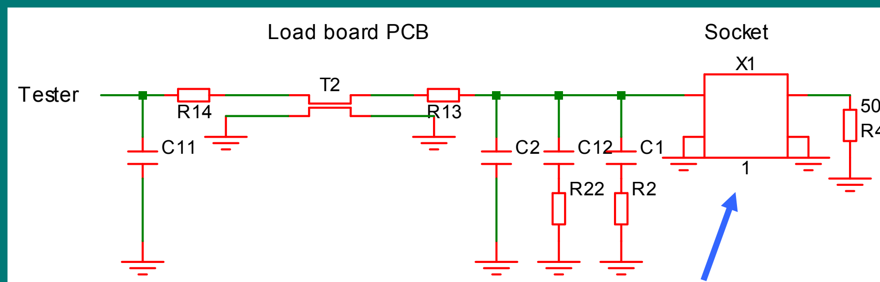

DUT Models



Device representation alternatives:
Single element vs. PI section vs. transmission line model

The lumped element single L model in this example loses its usefulness at fairly low frequencies, the Pix1 model above 5 GHz. A multi-element model mimics a transmission line representation.

From test head to DUT…



Socket parameters from measurement

There is a need to provide a coherent and consistent signal propagation environment. The ground return path is vital.

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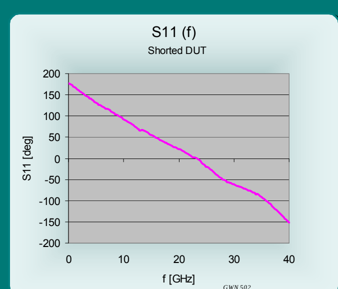
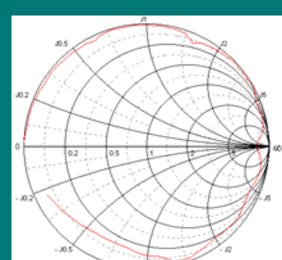
Measurement Example

S11 of a short circuited DUT



S11 phase of a BGA socket as a function of frequency for the short circuited case



S11 in the Smith chart for the short circuited case

Approximations:

A phase change of 14.3 deg/GHz corresponds to 1 nH (short ckt.)

A phase change of 34.8 deg/GHz corresponds to 1 pF (open ckt).

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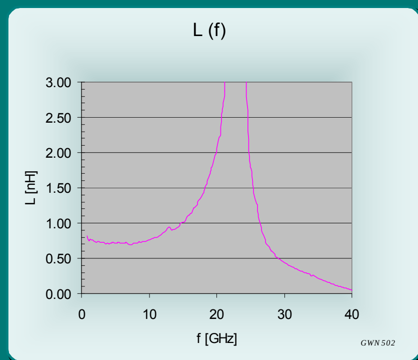
Measurement Evaluation
Inductance as a function of frequency



BGA socket inductance as a function of frequency

Above 8 GHz the inductance increases because the device physical length (2.5mm) becomes equal to 1/4 of the wavelength. A transmission line model must be used at higher frequencies.

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Test Lab

Socket 1:

@frequency:		MHz							
	L	C	Z	td	S11	S21	S22	S31	S41
GS									
GSG									
GSSG									
GSSG 50 Ohm									
GGGSGGG									
50 Ohm term Gs									

A select number of sample measurements will be taken and evaluated. All remaining and not measured numbers will be provided to participants after the lab.

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Test Lab

Z=	sqrt(L/C)
td=	sqrt(L*C)
L=	Z*td
C=	td/Z

Simple relations can be used to determine approximate socket parameters.
While determination of L and C from TDR measurements of Zo and t_d are possible, accuracy of this method is limited.
Nevertheless, the method may provide a simple means to get an approximation or comparisons of socket performance during development.

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Sample report – discussion of results

"Interposer Sample Test Report
1.00 mm pitch
Measurement and Model Results"

Test data from an interconnect (manufactured in-house) representative of a high performance socket

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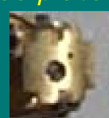
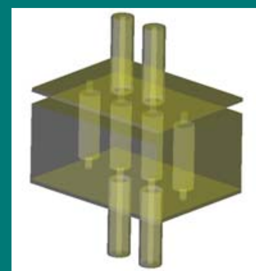
Typical arrangement base plate and DUT probe

Socket base plate example



DUT plate



G-S-S-G test arrangement with coax feeds

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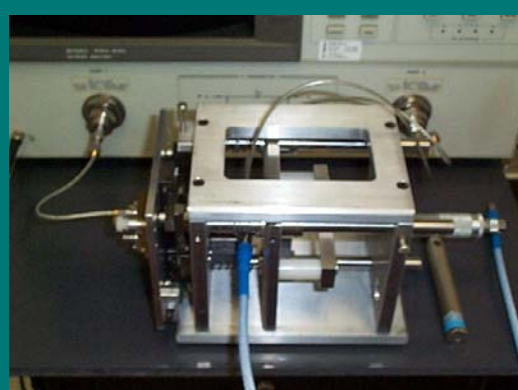
Test fixture



Typical example of a fixture with x, y and z control

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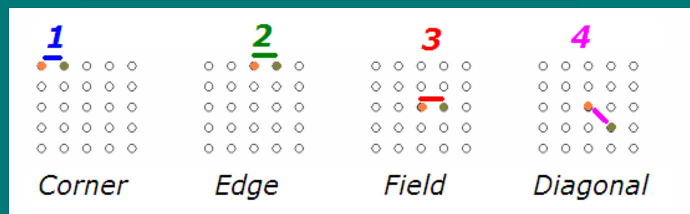
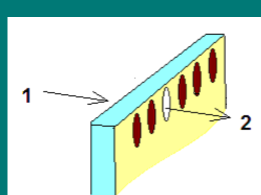
BGA Test Configuration



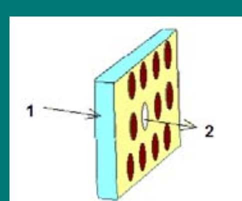
In a typical load board environment signal lines are terminated in 50 Ohms or are of relatively low impedance. Together with power and ground connections a reasonable approximation is to consider these pins to be effectively grounded. Only completely unconnected unused pins can be treated as open circuited.

A 5 x 5 array is thus a good test platform that allows for testing of a number of different configurations that give info about the performance to be expected on the final application.

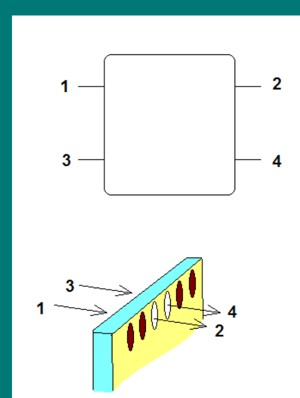
Test ports



Peripheral array

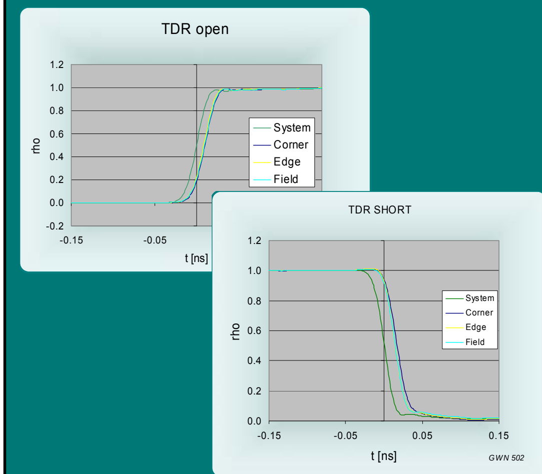


BGA, LGA



Single row – multi-row G-S-G and G-S-S-G configurations

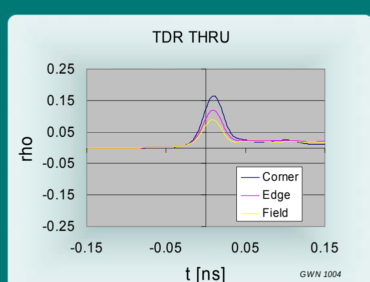
TDR signal from an OPEN and SHORT circuited interposer



Manufacturer:
End user:

- Fidelity
- Skew

TDR measurement into a 50 Ohm probe

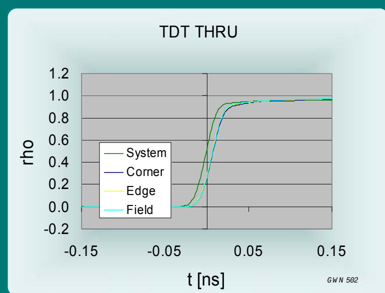


Manufacturer:
End user:

- 50 Ohm impedance (least deviation from straight line)

The thru TDR response shows primarily an inductive response. The peak corresponds to an impedance of 69.7, 63.5 and 59.8 Ohms for corner, edge and field, respectively

TDT (thru) measurement

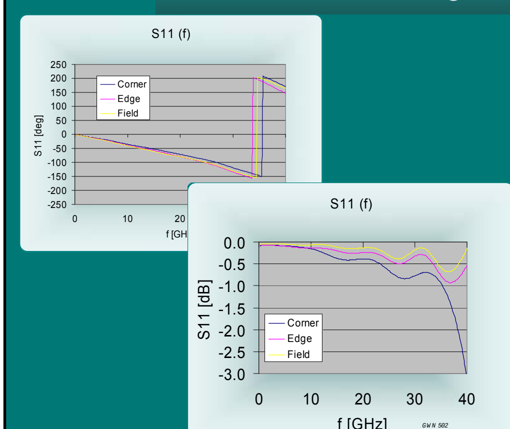


Manufacturer:
End user:

- Fidelity
- Skew

The TDT measurements for transmission show almost the same risetime from the pin array (10-90% RT = 31.5, 31.5 and 30.0 ps for corner, edge and field, respectively, the system risetime is 27.0 ps).

S11(f) for the open/short circuited signal pin

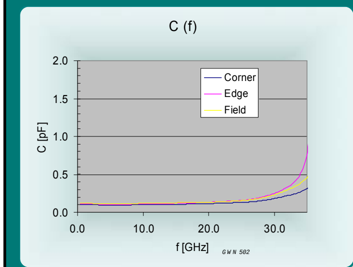


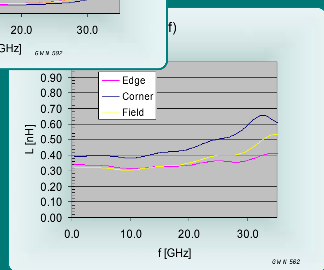
Manufacturer:
End user:

- Continuity of response
- Level of S11 and resonance free response

There are no aberrations in the response. The 360 degree jump is due to the network analyzer data presentation which does not allow for values greater than +/- 180 degrees.

L, C (f)





Manufacturer:

- Smooth response
- Overall values

End user:

- Frequency range, i.e. where is model no longer valid

The rise in capacitance/inductance toward 36 GHz is due to the fact that the pins form a transmission line with a length that has become a noticeable fraction of the signal wavelength.

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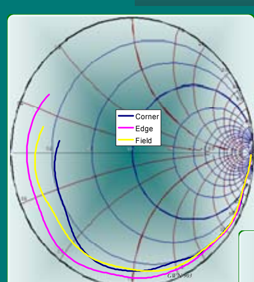
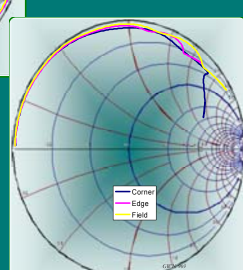
Reflections from the open/short circuited interposer



Open



Short

Manufacturer:
End user:

- Smooth response without any loops (resonances)

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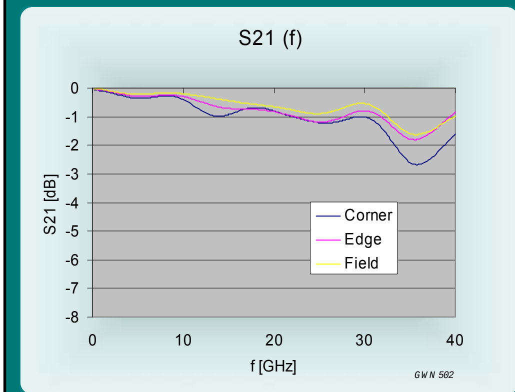
Insertion loss S21 (f)



Manufacturer:

- 1 dB point for comparison with competing products

End user:

- Overall response smoothness

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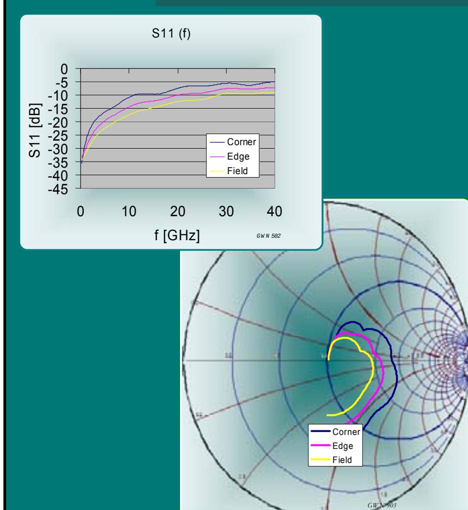
S11(f) for the thru measurement into a 50 Ohm probe



Manufacturer:
End user:

-20 dB point

- Reasonably smooth response
(deep dips are not necessarily detrimental)

- No loops in Smith chart up to desired operating frequency

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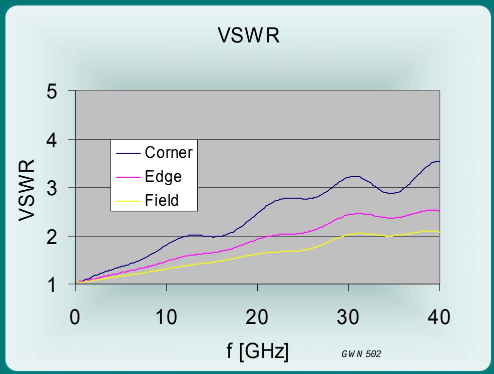
Standing wave ratio VSWR (f)



Manufacturer:
End user:

-Classic performance metric

The VSWR remains below 2 : 1 up to a frequency of 16.1, 21.5 and 29.5 GHz (corner, edge, field).

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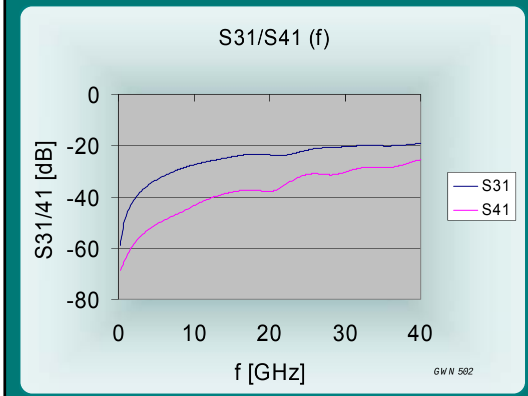
G-S-S-G crosstalk as a function of frequency



Manufacturer:

- Metric for specs or as competitive comparison (e.g. -20 dB point for S31 or S41)

End user:

-Comparison to other sockets (actual application may require different model)

The graph shows forward crosstalk from port 1 to port 4 (S41) and backward crosstalk from port 1 to the adjacent terminal (port 3, S31). The -20 dB point is reached at 36.9 GHz (S31) and not before 40.0 GHz (S41).

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GateWave Northern, Inc.

Interposer sample report

1.0 mm pitch

3/30/2009

Measurement results:

	Corner	Edge	Field	
Delay	7.5	7.5	7.5	ps
Risetime open	28.5	28.5	28.5	ps
Risetime short	31.5	28.5	28.5	ps
Risetime thru, 50Ω	31.5	31.5	30	ps
Insertion loss (1dB)	22.1	22.3	32.5	GHz
Insertion loss (3dB)	40.05	40.05	40.05	GHz
VSWR (2:1)	16.14	21.52	29.49	GHz

PI equivalent circuit component values:

Site	Cg=C1+C2		L1		R4	
Corner	0.105	pF	0.39	nH	1000	Ohms
Edge	0.113	pF	0.34	nH	800	Ohms
Field	0.120	pF	0.32	nH	800	Ohms
Diagonal	0.120	pF	0.32	nH	800	Ohms

It should be noted that there are 2 capacitors in the PI equivalent circuit. Each of them has half the value listed here.

Mutual component values:

Site	Cm		M	
Corner	0.007	pF	0.123	nH
Edge	0.006	pF	0.096	nH
Field	0.004	pF	0.056	nH
Diagonal	0.002	pF	0.022	nH

It should be noted that there are 2 capacitors in the PI equivalent circuit. Each of them has half the value listed here.

Transmission line equivalent circuit values:

Site	Zo		td	
Corner	69.7	Ω	7.5	ps
Edge	63.5	Ω	7.5	ps
Field	59.8	Ω	7.5	ps

The impedance listed is that observed in the time domain measurements. It is different than that calculated from the measured L,C parameters because of the limited time domain signal risetime.

Summary sheet

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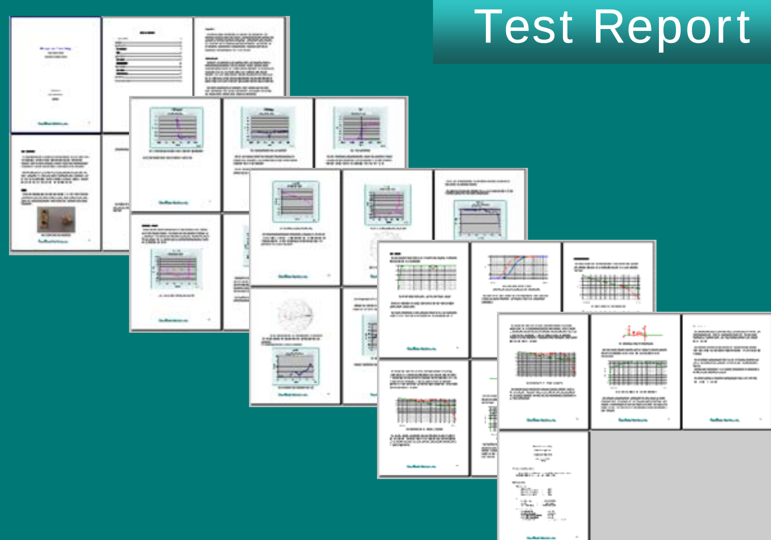
Test Report



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GateWave Northern, Inc.

Rf Property Measurement and Analysis
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- *Coaxial pogo pins*
- *Probe cards*
- *Contacts*
- *Sockets*
- *PCBs*

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