BiTS Burn-in & Test Socket Workshop 2010

TechTalk

ARCHIVE 2010

PCB DESIGN, FABRICATION AND ASSEMBLY

by

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ABSTRACT

This TechTalk will cover producing the printed circuits boards you want - from start (Design) to (Fabrication) finish (Assembly)".

With escalating electrical performance demands, the Printed Circuit Board is not only an essential part of a package test and/or burn-in solution, but has become an integral component for success. This TechTalk offers attendees an interactive, across the board examination of those PCBs sitting under your socket. The focus will be on learning about the challenges to properly select materials, layout, manufacture and assemble the PCB. In 'bringing the Printed Circuit Board shop to the 'classroom', a better understanding of the challenges you and your PCB vendors face is discussed.

First a brief history of the PCB or PWB (Printed Circuit/Wiring Board) industry will be covered, specifically in relation to the ATE industry. Next the talk will address the common challenges the industry deals with in the layout of a high yielding, yet lower volume process flow. Once designed, the discussion will cover the main cost and technical drivers of the PCB. Those being the pitch, layer count, board thickness and via drill hole diameter (to name but a few of the critical attributes of today's interface boards). Once built, the presentation will explain the assembly challenges and tricks that are required to complete the final PCB assembly.

Last, but certainly not least, the quality and performance characteristics you can demand of your supplier(s) will be analyzed. Even with today's boards becoming more crowded (with components) and pitch and pin counts driving attributes ever smaller, there are ways to verify and validate the quality of your interface boards with your suppliers. Attendees will learn how, with samples of data gathered over years of process development, characterization and verification.

PCB Design, Fabrication and Assembly

BiTS 2010 Tech Talk

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What you came here for…

- A little bit about PWB's
  - The marketplace
- Fabrication
  - The Attributes
  - Materials and more
  - The Process
- Assembly

Printed Circuit Boards

- A PWB consists of a non-conducting substrate (typically woven fiberglass with epoxy resin) upon which a conductive pattern or circuitry is formed.
- Wikipedia…A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, on a non-conductive substrate.

Marketplace

- 2007
  - US$50B
- 2012
  - US$76B
- US Market in 2007
  - US$13B
- ATE
  - US$.5B to US$1B (difficult to estimate)

What's in a name?

- PCB
- PWB
- DUT board, DIB, PIB, Load board, ATE board
- Interface Board
  - Between Device Under Test and Tester

Attributes

- Pitch
  - Device, line, space, hole to copper
- Layers
  - rows
- Hole Diameter
  - Function of device pitch
- Aspect Ratio
  - Ratio of thickness to hole diameter

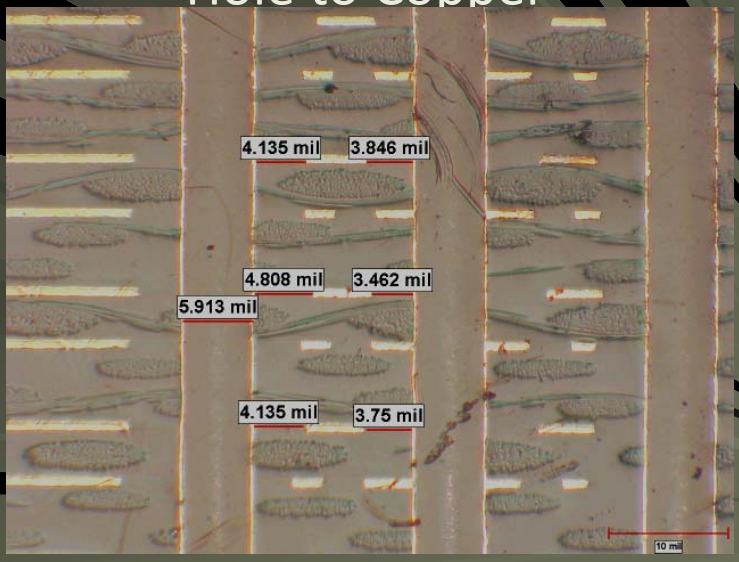
Attributes - Pitch

- Device Pitch
  - 1.0mm, 0.8mm, 0.5mm, 0.4mm ….
  - Translates to other attributes
    - Line width
    - Spacing
    - Dielectric spacing
    - Hole to copper feature dimensions

Pitch Translation

	1.0mm	0.8mm	0.5mm	0.4mm
Pad	0.76mm	0.66mm	0.35mm	0.3mm
Hole	0.37mm	0.3mm	0.15mm	0.1mm
Line	0.2mm	0.2/0.12	0.2/0.08	0.2/0.07
Hole2Cu	0.25mm	0.18mm	0.12mm	0.1mm
A/R	Low	Med.	High	Extreme

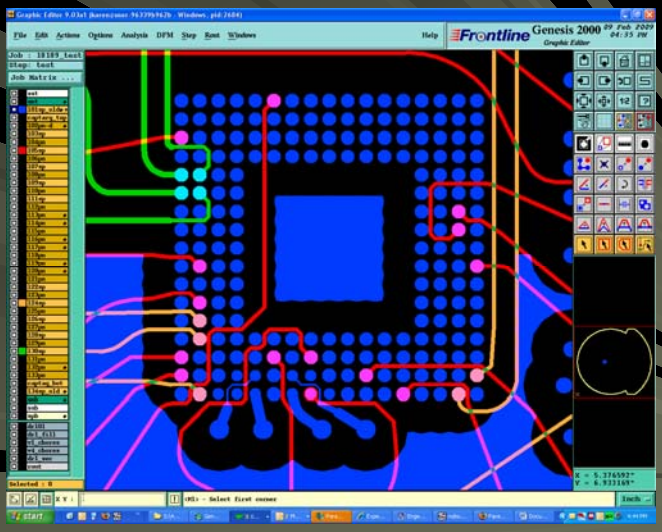
Hole to Copper



Attributes - Layers

- Rows = Signal Layers
- Signal Layers need ground planes
  - Impedance control
- Additional routing layers

Rows = Layers



Attributes – Hole Diameter

- Drill / Hole diameter
- Human hair
  - 0.04 to 0.25mm
- 0.1mm 'average'

Attributes – Aspect Ratio

- 1.0mm
  - 13:1
- 0.8mm
  - 16:1
- 0.5mm
  - 31:1
- 0.4mm
  - 47:1

Materials & More

- Wikipedia…A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, on a non-conductive ***substrate***.

Materials & More

- Laminate
  - Pre-preg
    - Glass cloth (woven)
    - Resin
  - Copper foil
    - Electrodeposited (ED)
      - 1 ounce per square foot (305g/M^2) (35 microns thick)
      - ½ ounce per square foot (153g/M^2) (17 microns thick)
      - ¼ ounce per square foot (80g/M^2) (9 microns thick)

Materials

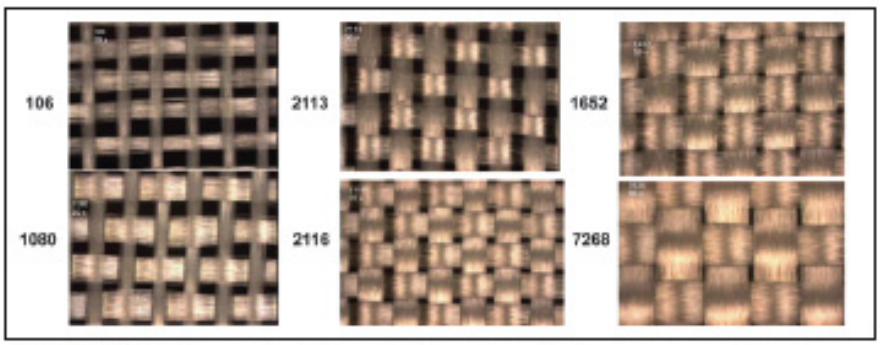
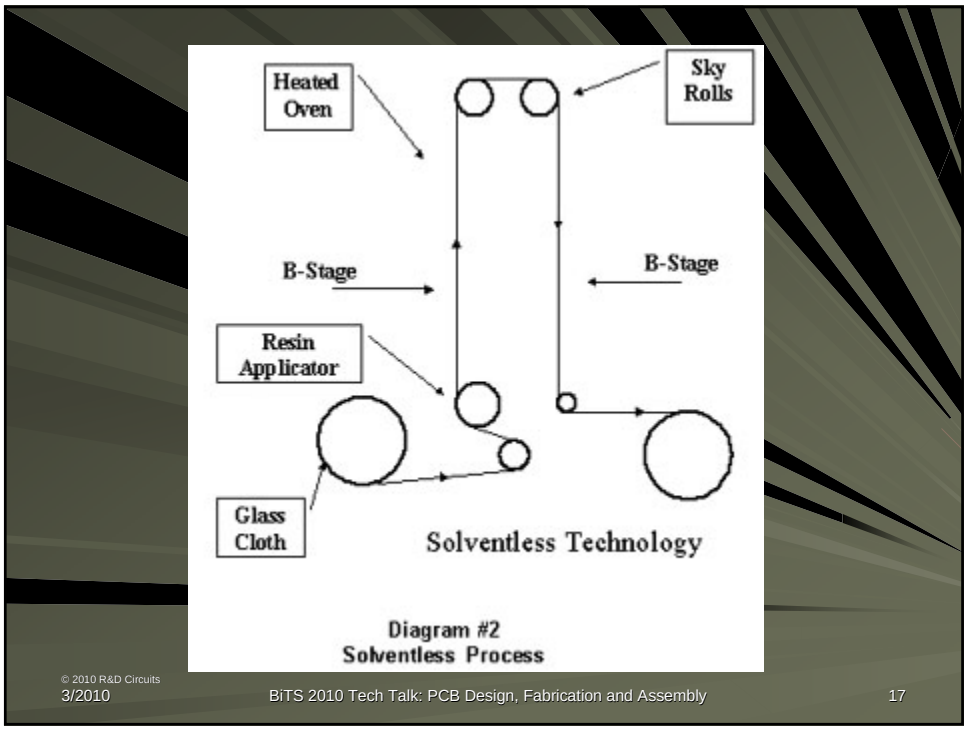


FIGURE 4. Different styles of glass laminate weaves. Photos courtesy of the isola group.



Laminates

- Fr-4
- Enhanced Fr-4's
- HF laminates
- Teflon
- Hybrids

Glass Styles

Style	Glass Dia.	Yarn Ct.	Yarn Pitch
106	1.4	56x56	17.9x17.9
1080	2.3	60x40	16.7x21.3
2113	2.9	60x56	16.7x17.9
2116	3.8	60x58	16.7x17.2
7628	6.8	44x32	22.7x31.3

Constructions

Thickness	Tolerance	Construction	Resin Content	E_r @ 1 MHz	E_r @ 10 GHz
0.008	0.001	1 7628	44.4%	4.55	4.12
0.008	0.001	2 2116	43.0%	4.54	4.11
0.008	0.001	1 2116 1 2113	48.6%	4.36	4.02
0.008	0.001	1 7629	42.6%	4.38	4.12

Constructions

- Know what you're getting
- Understand the implications
- Electrically insignificant?
- Mechanically significant

Material Properties

- Mechanical & Thermal
  - Peel strength
  - X-Y CTE
  - Z CTE
  - T_g
    - DSC
    - TMA
    - DMA

Material Properties

- Electrical
  - Dielectric Constant or
  - ε_r (or relative permittivity)
    - The dielectric constant is a ratio of the capacitance of a capacitor in which a particular insulating material is the dielectric, to the capacitance of the capacitor in which a vacuum is the dielectric.
  - Effective Permittivity

Inner Layer Imaging

- Photo-resist application
- UV Exposure
  - Film and collimated light
  - LDI or Laser Direct Imaging
    - Polymerizes photo-resist
  - Develop
    - Removal of non-polymerized resist

Inner Layer Imaging

Inner Layer Imaging

Inner Layer Etch

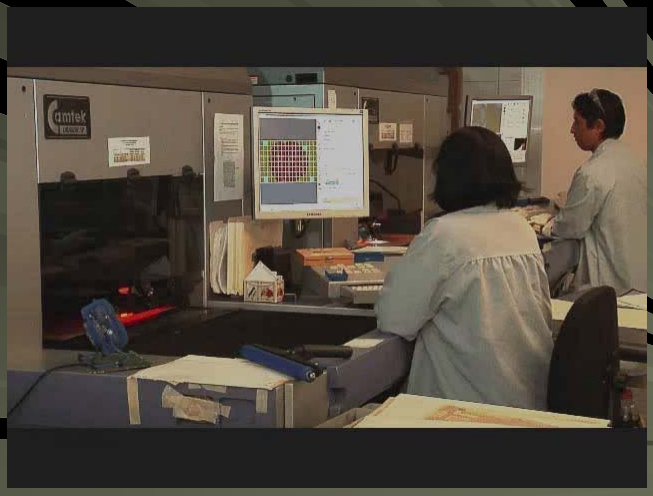
- Remove base copper
  - Non-polymerized area
  - Various chemistries available
    - Ammonia based
    - Cupric chloride based
- Resist removal (stripping)

Inner Layer Etch

AOI

- Post-Etch Punch
  - Registers all layers to optical targets
- Automated Optical Inspection
  - Data download from CAM
  - Core layer scanned
  - Compared to CAM data
  - Verification

AOI



Oxide Treatment

- Copper Surface Preparation
- Adhesion promoter
  - Added bond strength
- Reduced Oxide
  - Pink ring elimination
- Alternative Oxide
  - Variety of materials
  - Multiple or sequential laminations

Layup and Lamination

- Registration and stacking of cores
- Combines cores, pre-preg, Cu foil
- Pin lamination
  - Registration or layer to layer alignment
- Vacuum chamber
- Heat, pressure, time
- Controlled process window

- Stack up

Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type DK / DF
SM-1	0.0005		SM	Spray LPI	3.20 / 0.0000
L-1, TOP	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-2, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-3, PWR1	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-4, PWR2	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-5, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-6, SIG1	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-7, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-8, SIG2	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-9, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-10, SIG3	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-11, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-12, SIG4	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-13, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-14, SIG5	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-15, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-16, SIG6	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-17, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-18, PWR3	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-19, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-20, BOT	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
SM-2	0.0005		SM	Spray LPI	3.20 / 0.0000
	0.1517	Total Calc. Thickness			
	0.1520	Incl.Plating	+0.0152	-0.0152	
		After Lamination	+	-	

Drill/Rout Files: A: DR-1

Engenx® by Cimnet Systems, Inc. © 2002-2008

Drill

- Mechanical hole formation
  - 0.1mm
- Opto-mechanical positioning
  - Glass scales
- Real-time analysis
  - Diameter
  - Run-out
  - Broken bit
- Stub Drilling (back-drilling)

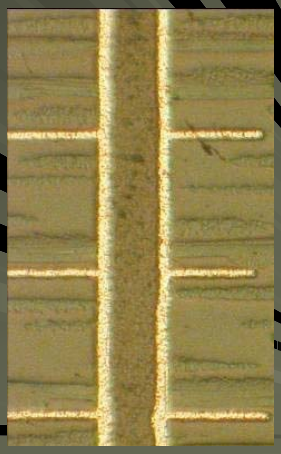
Drill

Drill

- Laser hole formation
  - Microvia's
    - Down to 25 micron
- Opto-mechanical positioning
- Blind via's
- Buried via's

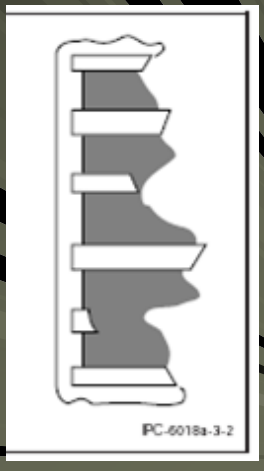
Hole Prep & Copper Plate

- Desmear
  - Removes epoxy smear from interconnects
  - Drilling operations
  - Chemical removal



Hole Prep & Copper Plate

- Etchback
  - Different from desmear
  - Removes epoxy from dielectric space
  - Glass etch
  - Three point connection
  - Some materials resistant to chemical removal



Hole Prep & Copper Plate

- Copper Deposition
- Seed layer
  - Prepares dielectric and interconnects for subsequent plating operations
  - 30-40 µ followed by copper plate
  - 75-125 µ to prep for imaging process
- Unfriendly chemistry
- Inherently unstable

Hole Prep & Copper Plate

- Carbon (Black Hole®)
- Graphite (Shadow®)
- Palladium
- Electroless Nickel (Ultra-Plate®)
- Conductive Polymer
- Non-Formaldehyde-Based Electroless Copper

Hole Fill

- Fill to create flat surface
  - Need for socket touchdown
- Vacuum assist
- Compressed air
  - Thru system & thru holes
- High aspect ratio
- Blind via's

Hole Fill

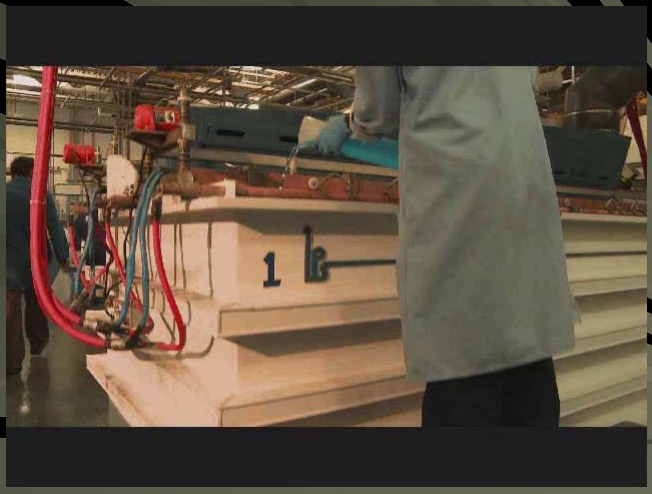
Outer Layer Imaging

- Reversed from inner layer imaging
- Plating resist, not etch resist
- Photo-resist application
- UV Exposure
  - Film and collimated light
  - LDI or Laser Direct Imaging
    - Polymerizes photo-resist
  - Develop
    - Removal of non-polymerized resist

Cu Ni Au Plating

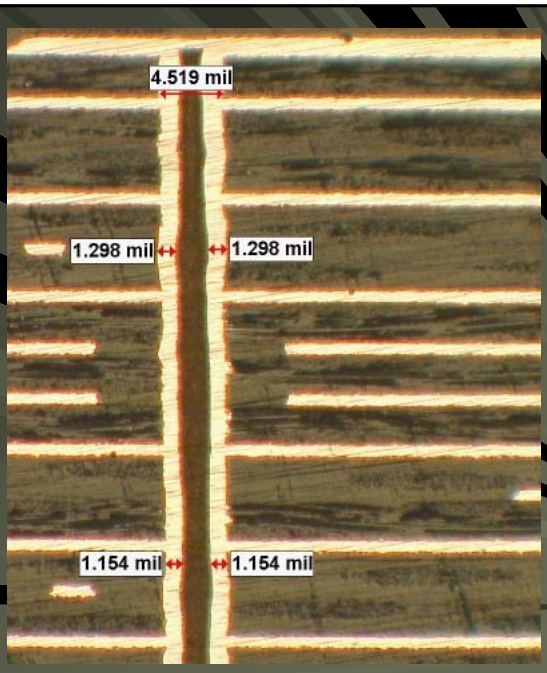
- Electroplating
  - Chemistry (electrolyte solution)
  - Power rectifier
    - Rectifier converts AC to DC
  - Anode (copper)
  - Cathode (PCB panel)

Cu Ni Au Plating



Cu Ni Au Plating

- 1 mil minimum thickness in holes
- Minimize surface buildup
- Aspect ratio
  - Thru holes and / or micro-via's
- Robust and survivable
- Etch Resist

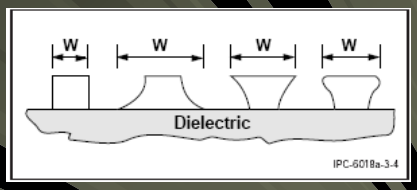


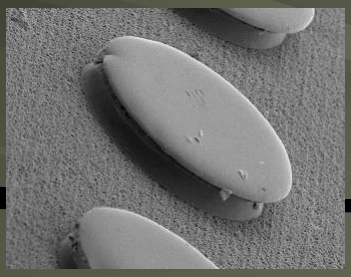
Outer Layer Etch

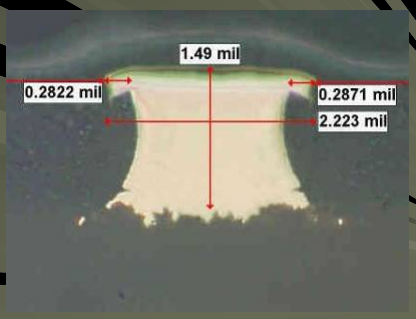
- Define the outer layer(s) pattern
  - Removal of base copper
  - Lines, pads, other features
  - Impedance control
- Nickel / Hard Gold typical ATE finish
- Etch factors and overhang
- Other finishes available

Outer Layer Etch

- Overhang
  - Depends on finish
  - 1:1 thickness
  - Surface thickness critical







Electrical Test

- Direct measurement for first board
- Indirect Measurement all others
  - Isolation and continuity
  - Capacitive or electromagnetic coupling
    - Broken trace = reduced coupling
    - Shorted trace = increased coupling
    - Trace to ground (↑ degree of confidence)
  - Adjacency analysis

Electrical Test

Soldermask

- Epoxy based coating
  - Available in colors and clear
- Surface protection
- Solder resist, as the name implies
- Identification

Soldermask

- Screen-flood
- Liquid Photo-imageable (LPI)
  - Spray coated
  - consistency
- Via Plugging
- Dry Film

Silkscreen

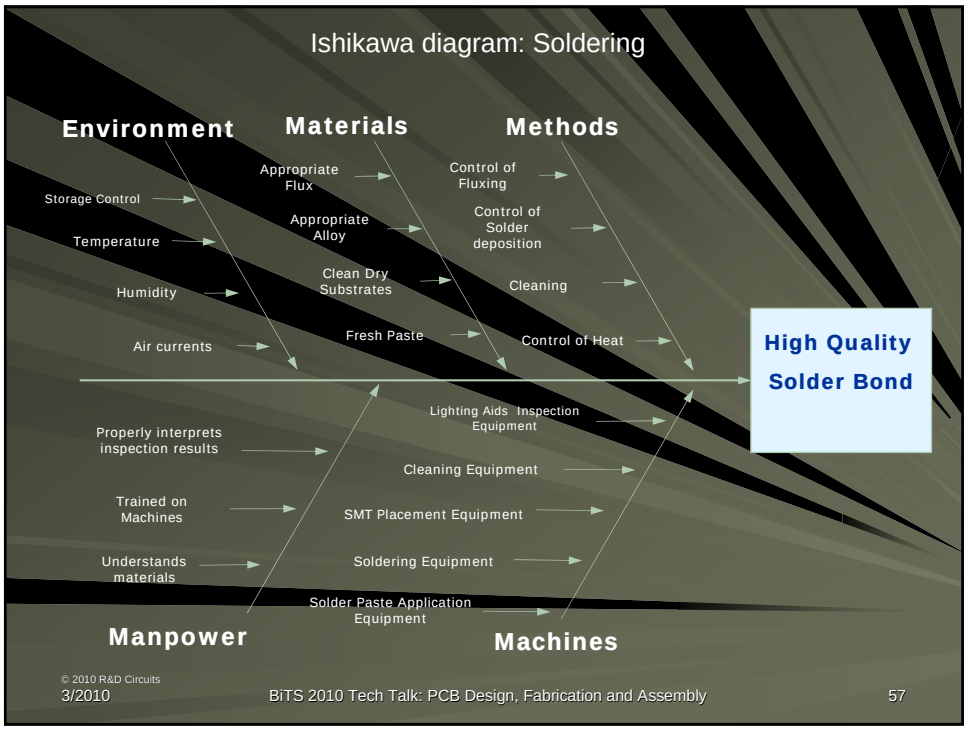
- Assembly nomenclature or legend
- Available Colors
- Product identification
- Screen print
- Inkjet

De-panelization

- Routing
- Secondary Drill
- Back / Stub Drill
- Counterbores / countersinks
- Slots

Final Inspection

- Visual and dimensional
  - Cosmetic defects
- Impedance Testing
- Cross sectioning
- Other measurements and certifications


Ishikawa diagram: Soldering
Environment
Materials
Methods
Storage Control
Temperature
Humidity
Air currents
Appropriate Flux
Appropriate Alloy
Clean Dry Substrates
Fresh Paste
Control of Fluxing
Control of Solder deposition
Cleaning
Control of Heat
High Quality Solder Bond
Properly interprets inspection results
Trained on Machines
Understands materials
Lighting Aids Inspection Equipment
Cleaning Equipment
SMT Placement Equipment
Soldering Equipment
Solder Paste Application Equipment
Manpower
Machines
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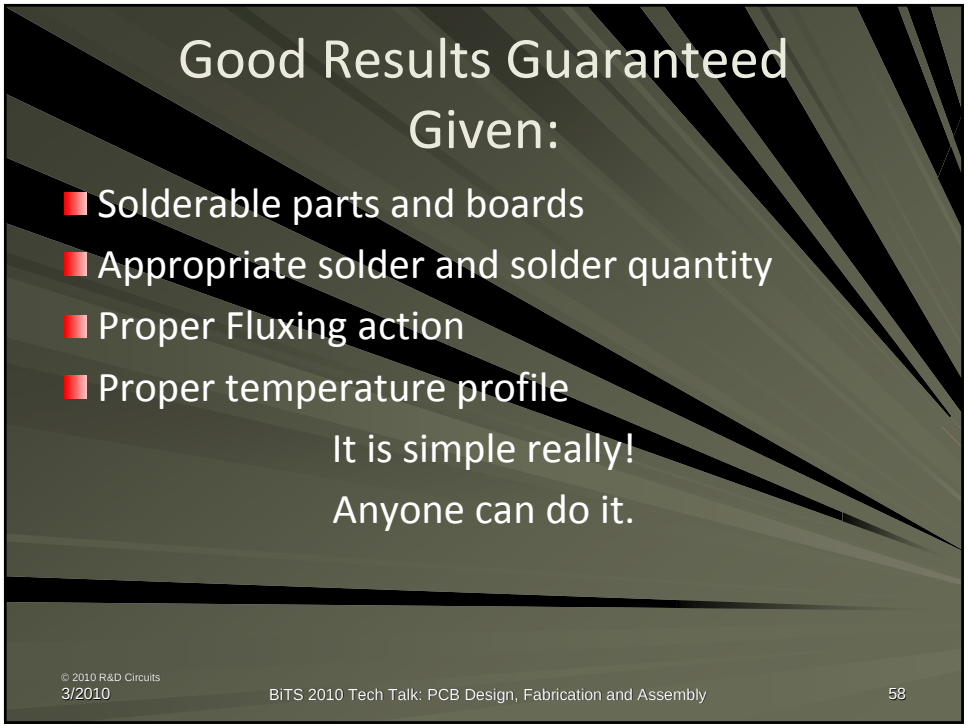
Good Results Guaranteed Given:
Solderable parts and boards
Appropriate solder and solder quantity
Proper Fluxing action
Proper temperature profile
It is simple really!
Anyone can do it.
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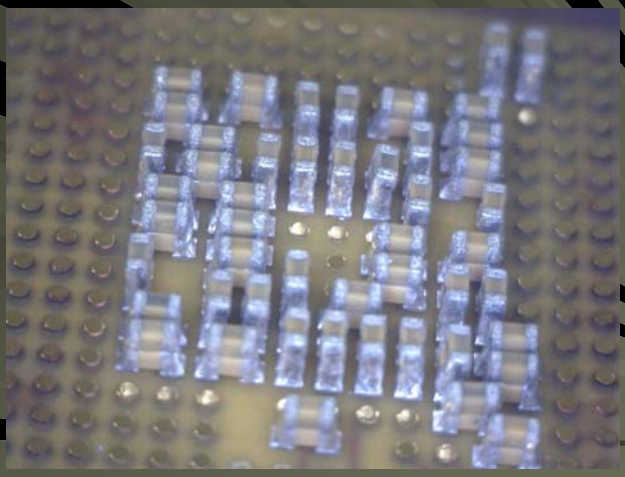
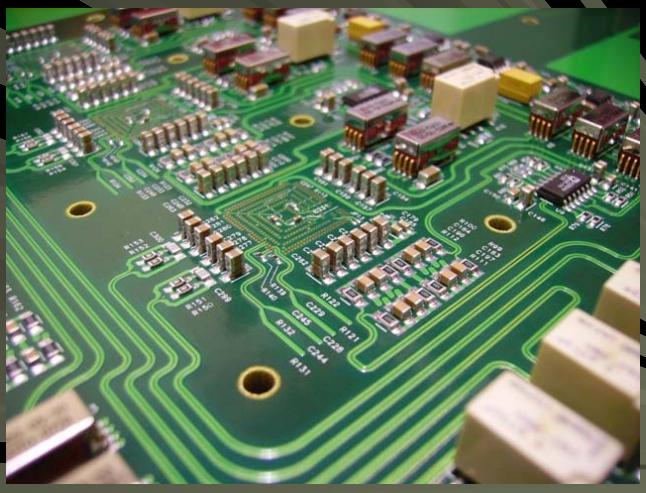
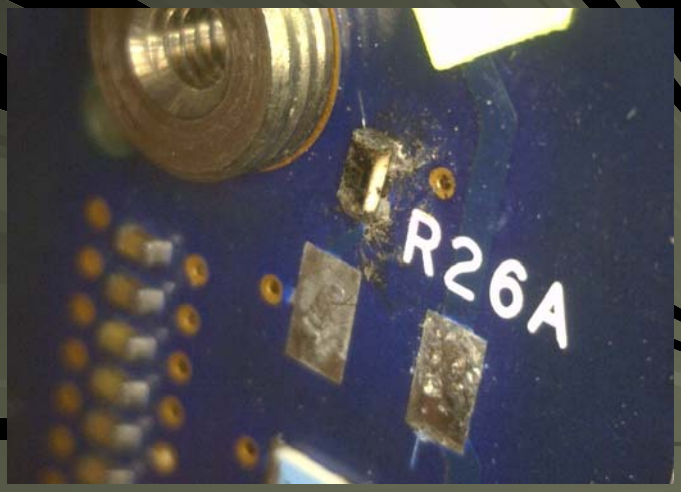
Easy Does it



Easy Does it



Or Not !!

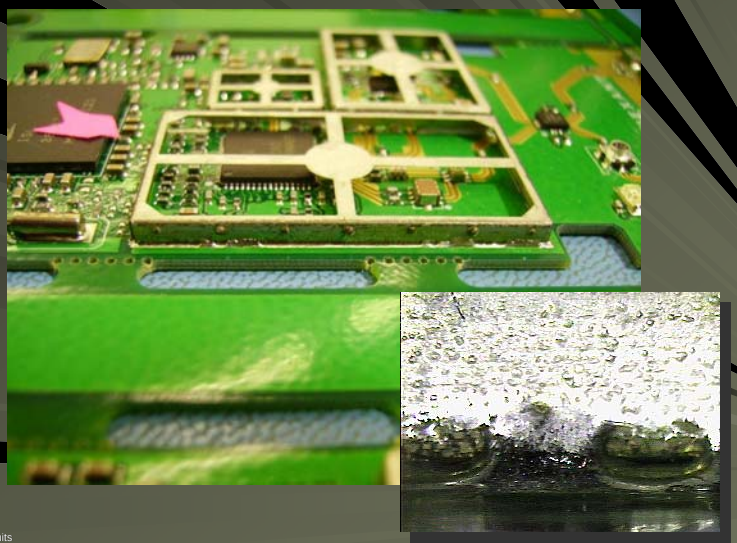


Or Not: Two

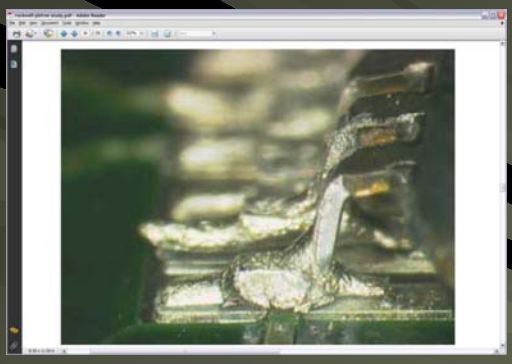
Materials

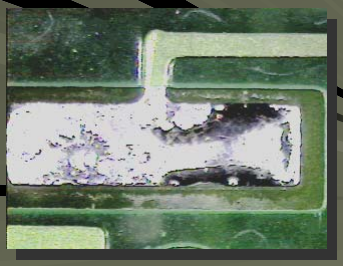
- Parts: J-STD-002
- Boards: J-STD-003
- Flux: J-STD-004
- Solder Paste: J-STD-005
- Solder: J-STD-006
  - Solvents: Must be compatible
    - Flux
    - Cleaning method
    - Parts

Non-solderable Parts



Non Solderable Board

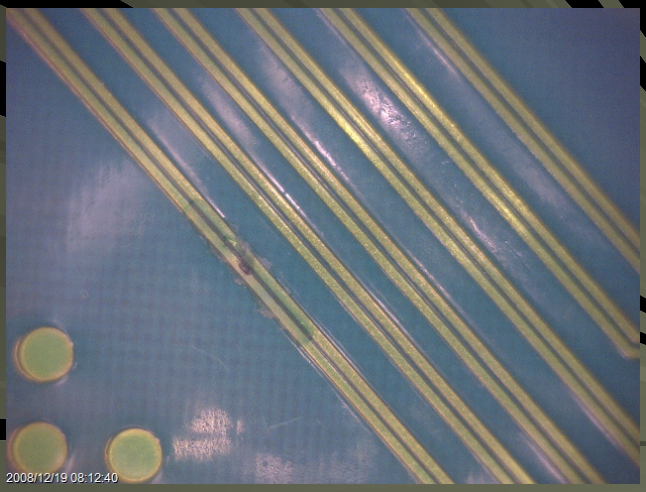




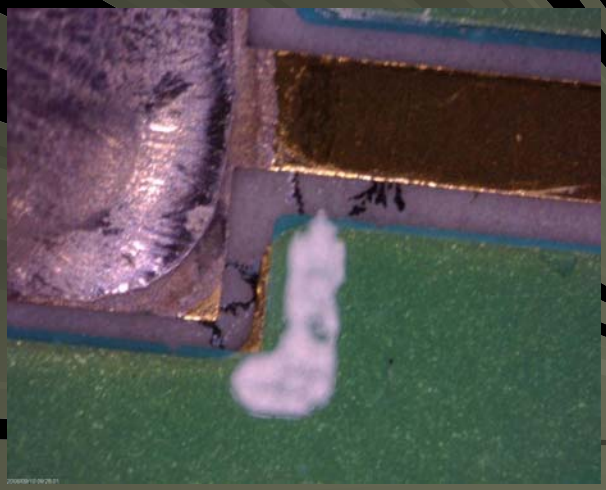
Flux Classification

- Low Activity
- Medium Activity
- High Activity
- All levels:
  - Halide activators
    - May produce metal salts
  - Non-halide activators
    - Less likely to produce corrosion

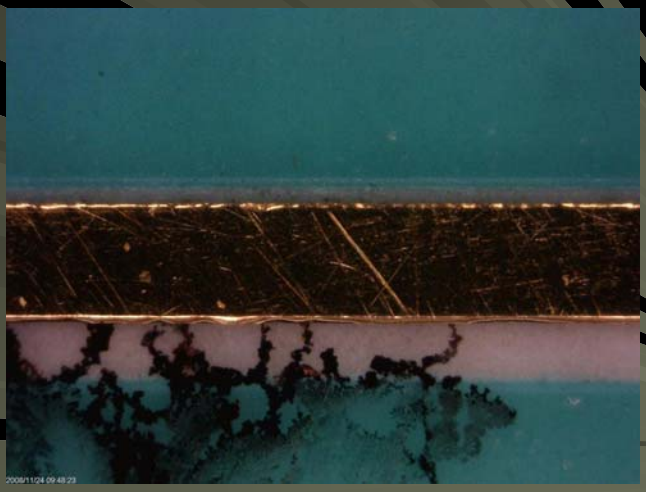
Corrosion: Flux Residue



Corrosion: Dendrite



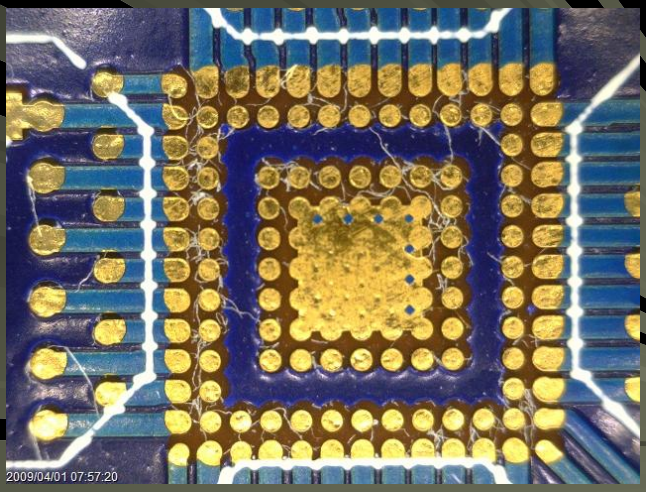
Corrosion : Dendrite two



Cleaning Materials

- Solvent based
- Water based
  - In any event cleaning is really happening when we remove the contaminated carrier of the dissolved flux.
    - Rinsing
    - Blow Drying
    - Extraction with absorbent material or force.

"Lint Free Wipes"



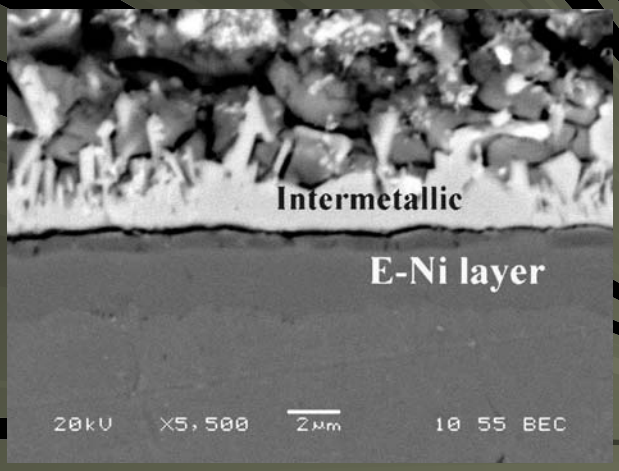
Solder

- Solder is not an adhesive
  - Not Adhesion,
    - attachment by mechanical means,
    - electrostatic forces, as in static electricity, hold the substances together
    - Van Der Waals forces that develop between molecules.
    - moisture-aided diffusion of the glue into the substrate, followed by hardening.

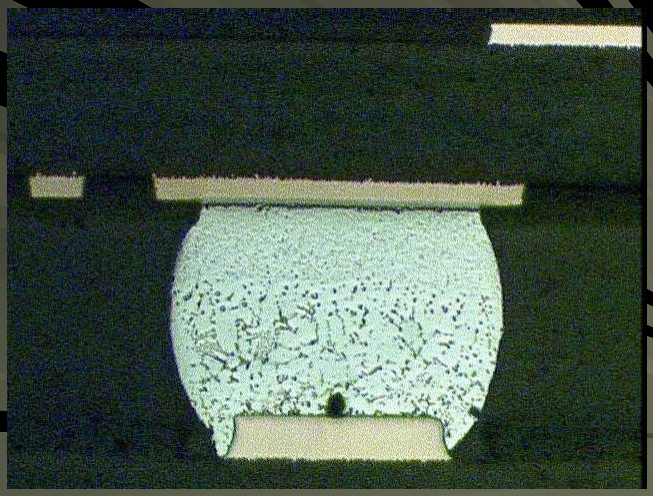
Solder

- Solder is not an adhesive
  - A process in which metals are joined by melting and flowing a filler metal, called solder, into the joint.
  - The solder is drawn into the joint by capillary action.
  - A portion of the metals to be joined are dissolved into the solder forming a metallurgical bond between the solder and metals to be joined.

Solder joint structure



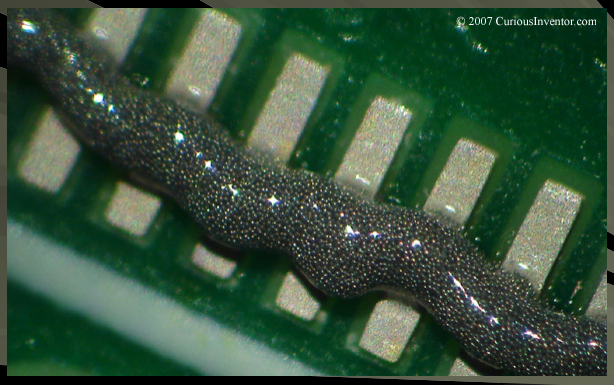
Pb-Free ball: SnPb Solder Diffusion



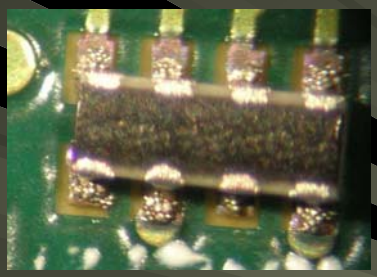
Solder Paste

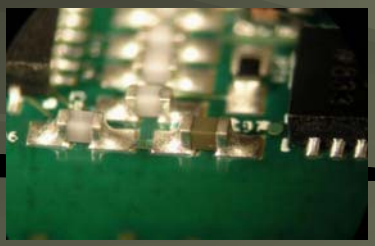
- A mixture of snake oil and solder:
  - Thixotropy
    - The property of certain gels or fluids that are thick (viscous) under normal conditions, but flow (become thin, less viscous) over time when shaken, agitated, or otherwise stressed.
  - Rheology
    - The study of the flow of matter: mainly liquids but also soft solids or solids under conditions in which they flow rather than deform elastically.

Solder Paste



Solder Paste Failure





- Powder oxidized

Flux unable to reduce and permit "normal" behavior of solder. Coalescing of powder into a single fillet capable of wetting to the board and component terminations

Methods - Machines

- Solder Paste Deposition – Fluxing
  - Printing or Dispensing
- Soldering
  - Reflow or Hand
- Cleaning
  - Hand or Machines
- Inspection
  - Visual or Automated

Home Sweet Home

Stencil Printing

Dispensing

Component Placement

- Manual
- Automated

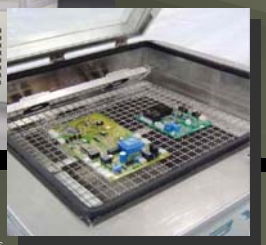
Automatic Component Placement

MYDATA®

Split-Axis Movement

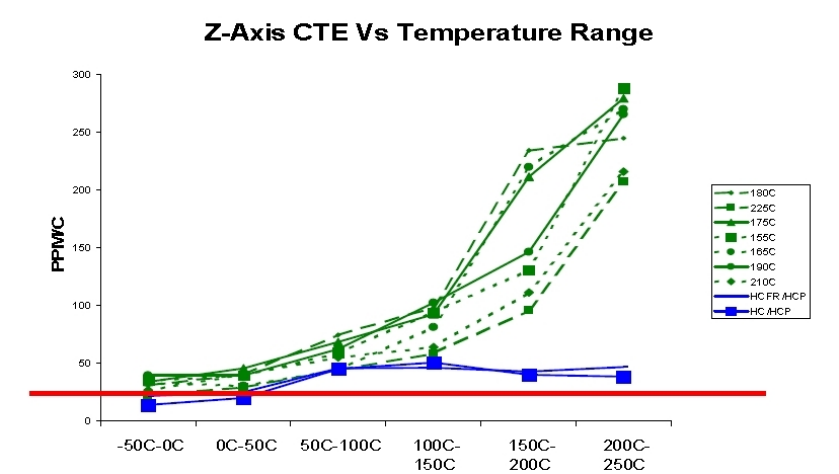
Reflow Soldering

- Convection and IR
- Vapor Phase



Hand Soldering

Why did I break my board?



Hand Cleaning

Batch Cleaning

In-Line Cleaning

Vapor Phase Cleaning

Inspection -Visual

- Standard Stereo Microscopes
- Ring lamps
- Mag rings probably not adequate
- Machine vision

Manpower

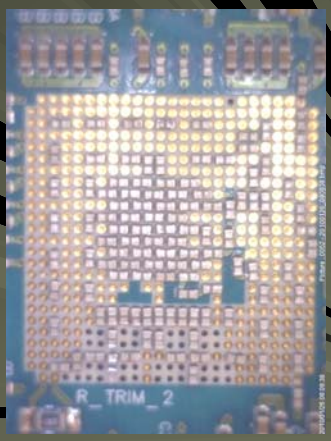
- Certification
- Training
- Education

Environment

- Temperature
- Humidity
- ESD

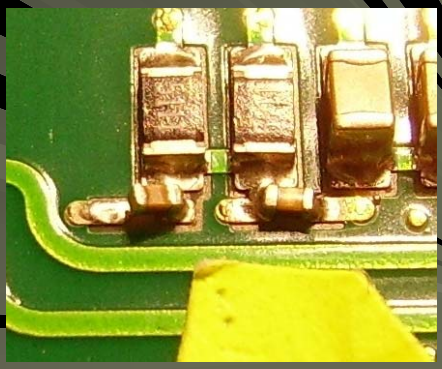
Design for Assembly

- Design is a series of compromises
  - Component Density
  - Laminate Materials
  - Layout
  - Component Selection

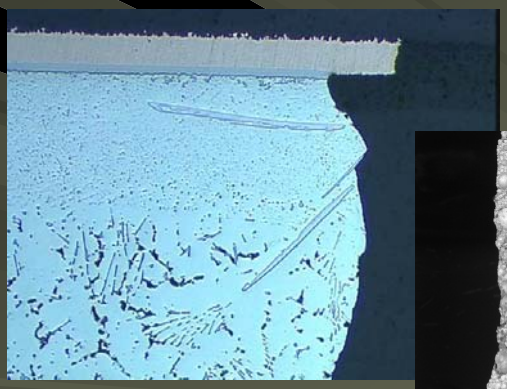


Surface Tension

- copper land patterns causing problems

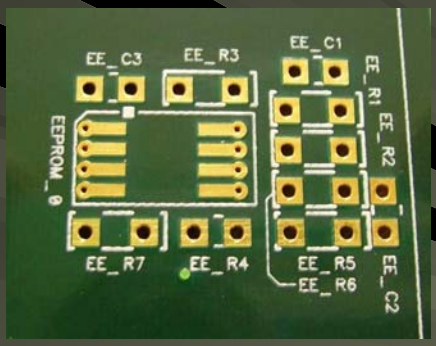


Gold Embrittlement



- Gold in excess of about 4% of Solder

PTH and SMT Land Pattern



- Design NO-NO
  - Solder will drain down the hole leaving no solder fillet

Board Damage

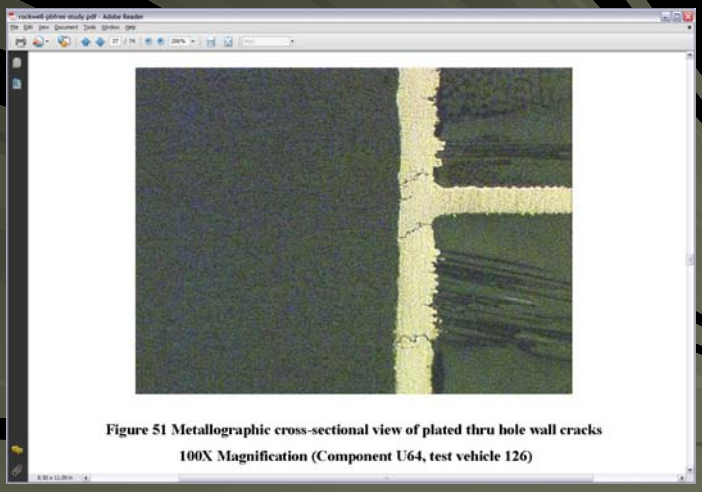
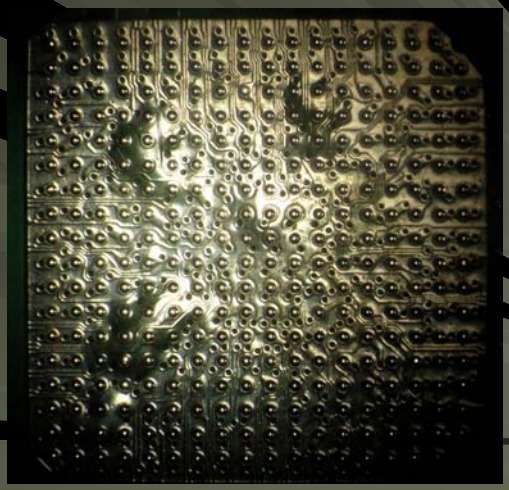


Figure 51 Metallographic cross-sectional view of plated thru hole wall cracks
100X Magnification (Component U64, test vehicle 126)

Moisture Sensitive



Review

- Overview of the Assembly Process
- Using traditional Fish Bone Diagram
  - Materials
  - Methods
  - Machines
  - Manpower
  - Environment

ATE Directions

- New devices?
- New chip manufacturing technology?
  - Flexibility
  - Scalability
  - Performance
  - Support
  - Cost

Manufacturing Challenges

- Flexibility
  - Variety of platforms
  - Range of pin counts
  - Pitch
  - Multi-site
  - Process capabilities

Manufacturing Challenges

- Scalability
  - Manufacturing capability
    - Board to board
    - Lot to lot
  - Multi-site
  - High pin count

Manufacturing Challenges

- Performance
  - Wider range of materials
  - Controlled process
    - Impedance
  - Lot controls

Manufacturing Challenges

- Support
  - Vendor stability
  - Vendor knowledge
  - Vendor process capability

Manufacturing Challenges

- Cost
  - Layer counts (thicker boards?)
  - Aspect ratio
  - Line and space requirements
  - Hole to copper dimensions
    - Pitch
  - Reliability
  - DfA

Sample Review

- We have prepared and have available for review, a series of process panels representing each of the process steps we reviewed during today's presentation. We can review and discuss any questions you may have.

R&D Circuits

- Founded in 1969
- Privately Owned & Operated
- ~$15M in Sales, FY09
- Full Turn-Key Supplier
  - Design - Layout
  - Fabrication
  - Assembly
  - Sockets, Contactors, Interconnects

R&D Circuits Locations

- Mesa, AZ – Design Center
- South Plainfield, NJ – PWB Fabrication
- Allentown, PA – PWB Assembly
- Singapore – Sales and Support, Asia
- Penang, Malaysia