BiTS 2010 **Session 2**

ARCHIVE 2010

SMARTER PCB DESIGN

Impact of Parasitic Resonances on Load Board Performance
Gert Hohenwarter—GateWave Northern, Inc.

The Importance of the Signal Return Path
Zaven Tashjian—Circuit Spectrum, Inc.
Kevin Hoffmann—Development/Test/SI

Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards
Erkan Acar, Tim Swettlen—Intel Corporation

Spring Probe PCB Pad Wear Analysis
Valts Treibergs, Chris Cuda—Multitest

COPYRIGHT NOTICE

The papers in this publication comprise the proceedings of the 2010 BiTS Workshop. They reflect the authors' opinions and are reproduced as presented , without change. Their inclusion in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.

There is NO copyright protection claimed by this publication or the authors. However, each presentation is the work of the authors and their respective companies: as such, it is strongly suggested that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.

All photographs in this archive are copyrighted by BiTS Workshop LLC. The BiTS logo and 'Burn-in & Test Socket Workshop' are trademarks of BiTS Workshop LLC.

Impact of Parasitic Resonances on Load Board Performance

Gert Hohenwarter
GateWave Northern, Inc.

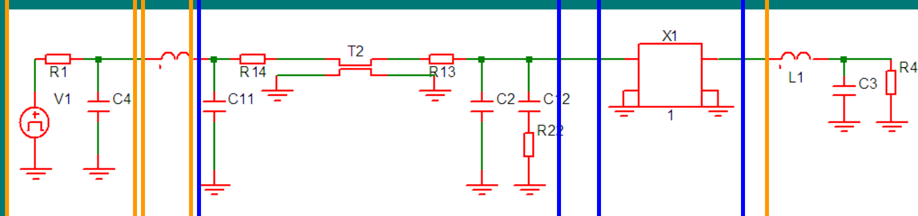
2010 BiTS Workshop
March 7 - 10, 2010

Objective

- Examine socket performance as a function of compression level and grounding conditions
- Identify sources of parasitic resonances
- Present socket measurements in the presence of resonances
- Develop performance prediction for load board signal path
- Assess significance of observed changes for final application

3/2010 Impact of Parasitic Resonances on Load Board Performance 2

Signal path model



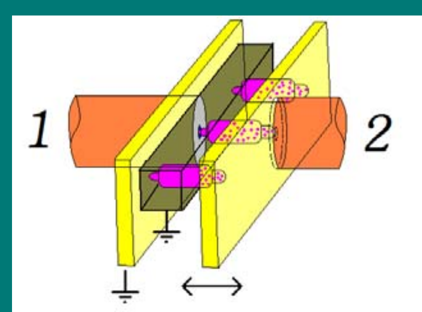
Tester | PCB | Socket | DUT

Cabling and connector

Resonances can occur in all individual parts or between components

3/2010 Impact of Parasitic Resonances on Load Board Performance 3

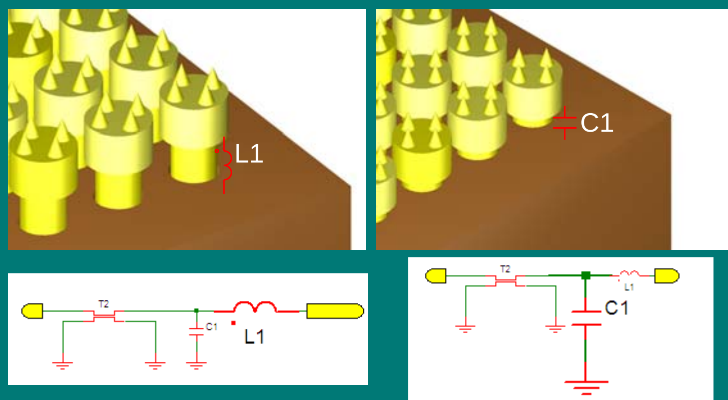
Contact parasitics as a function of displacement (compression level)



Assembly 1 and socket are fixed, assembly 2 moves

3/2010 Impact of Parasitic Resonances on Load Board Performance 4

Series inductance and shunt capacitance



Varying positions result in different values of parasitic parameters in the equivalent circuit

3/2010 Impact of Parasitic Resonances on Load Board Performance 5

Some sources of series inductance and shunt capacitance

Parasitic inductance can occur due to

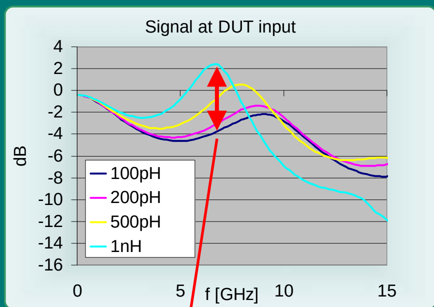
- Contact construction (thin portion of contact sticking out)
- Package construction (internal routing, bond wires)
- Die layout and trace routing

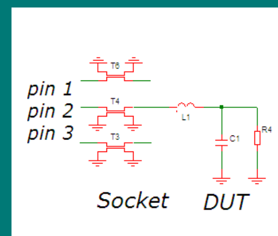
Parasitic capacitance can occur due to

- PCB layout (pad size)
- Package construction (pad size)
- Die layout (routing)
- Device input capacitance

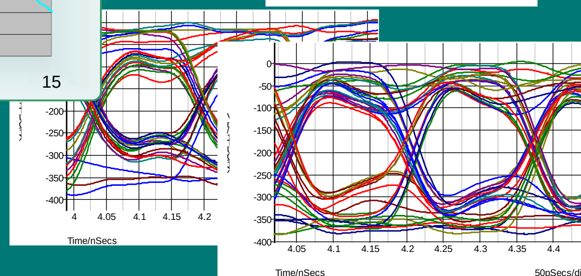
3/2010 Impact of Parasitic Resonances on Load Board Performance 6

Simulated voltage for a socket sample with varying L



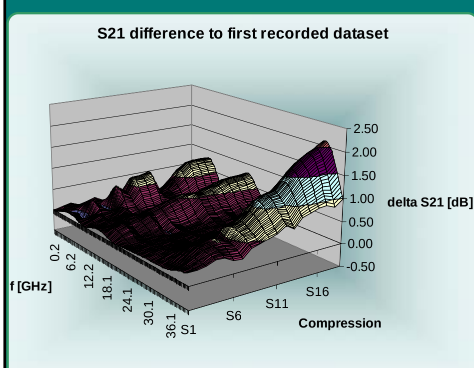


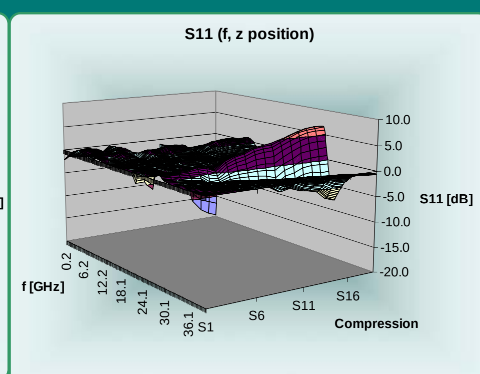
up to 6 dB difference



The load (device under test – DUT) is assumed to be non-50 Ohms. This can cause a resonant peaking of the voltage.

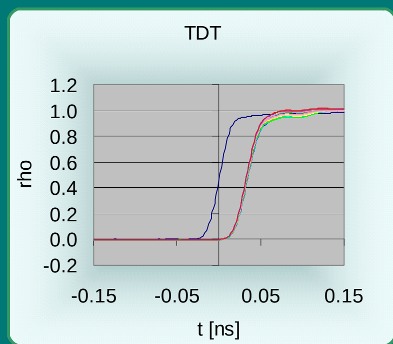
Measured insertion loss (S21) and return loss (S11) for a socket sample with varying z compression

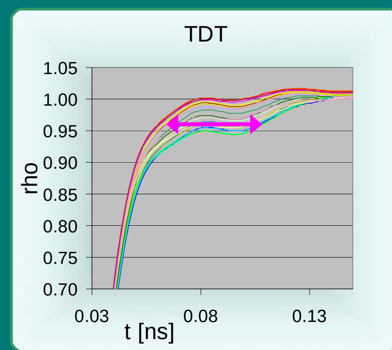




Insertion loss (into 50 Ohms) changes by 0.7 dB at low frequencies and up to 2 dB at high frequencies.

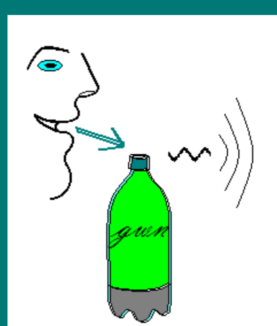
Measured time domain transmission of a step through a socket with varying z compression



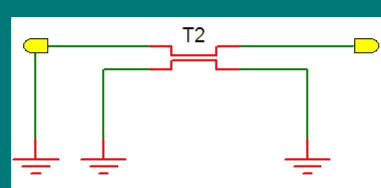


While overall change appears small, a plateau appears at the end of the signal transition. If the overall signal level is near a transition voltage, significant timing error can occur.

Resonances

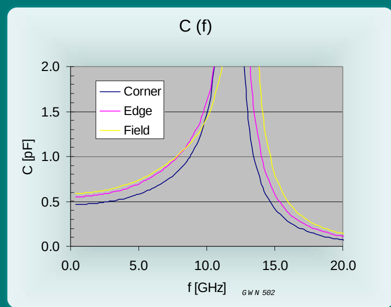


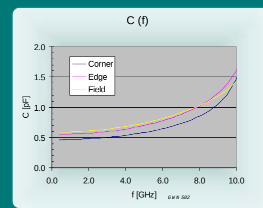
Helmholtz resonator

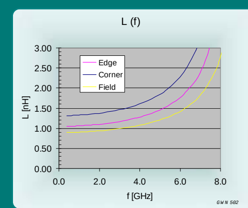


Transmission line, open on one end, shorted on the other (quarter-wavelength transformer)

λ/4 transformer







Example – 4mm probe

fres=c/{4*L*sqrt(ε)}; Zin/Zo = Zo/ZL

3/2010 Impact of Parasitic Resonances on Load Board Performance 11

Some sources of resonances

PCB:

- Coupling to unterminated or mismatched adjacent lines
- Strong internal routing discontinuities, vias
- Mismatched tester interconnects and sockets

Socket:

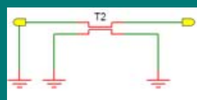
- One sided unterminated (open ckt.) pins
  - Unused GND or power connection on PCB or on DUT side
  - Signal N/C

DUT:

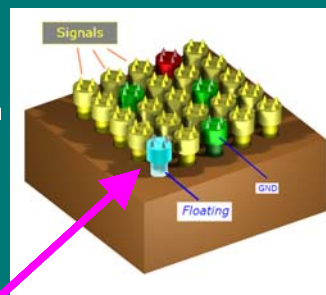
- Package design
- Die layout (routing), coupled stub routes
- Termination (mismatch, open)
- Failed circuitry

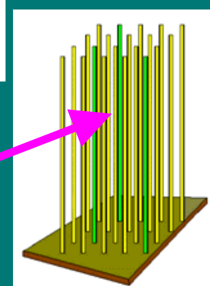
3/2010 Impact of Parasitic Resonances on Load Board Performance 12

Resonances



Transmission line, open on one end, shorted on the other

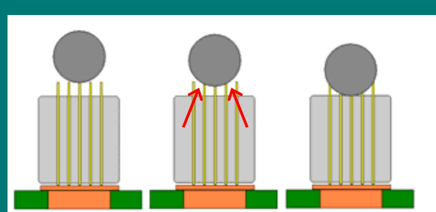


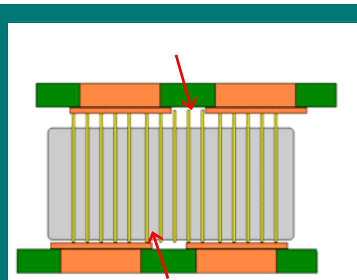


Opportunities for open/short circuited transmission lines exist

3/2010 Impact of Parasitic Resonances on Load Board Performance 13

Configuration dependence on overdrive and alignment





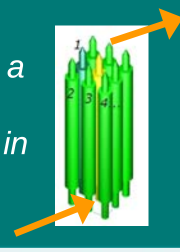
If not properly configured, interconnects with multiple parallel conductors can potentially contribute to resonances.

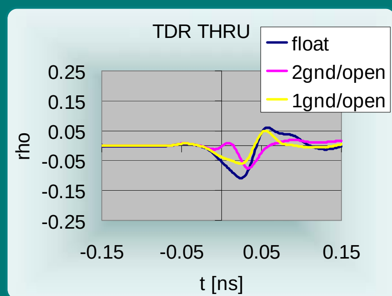
Insertion loss S21 measurement for 3 different displacements

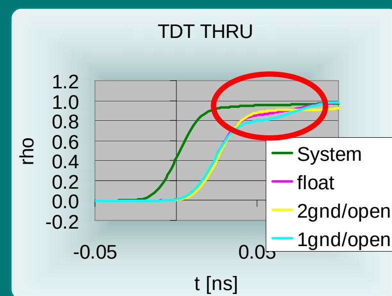
3/2010 Impact of Parasitic Resonances on Load Board Performance 14

Consequences of an open/short pin

Measured time domain signals sent through a contact array (on yellow pin) show some changes as a result of an open/short pin (1) in the assembly:

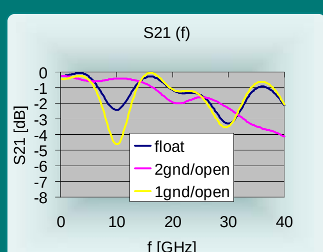


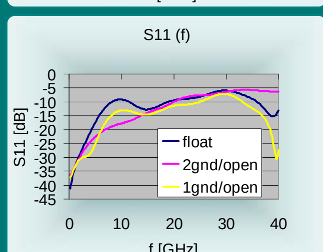


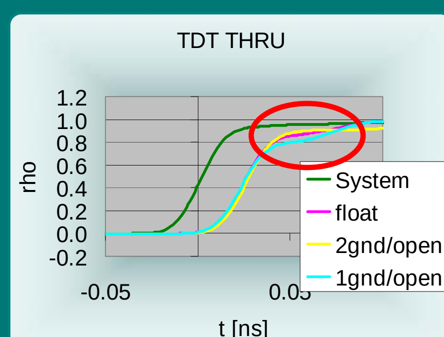


3/2010 Impact of Parasitic Resonances on Load Board Performance 15

Consequences of an open/short pin



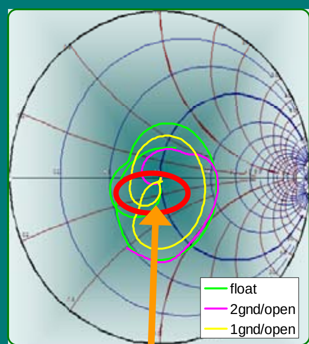


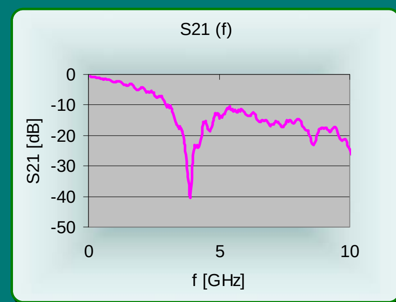


Measured socket responses show dips/peaks (S21/S11) and 'plateaus' in a transmitted step voltage

3/2010 Impact of Parasitic Resonances on Load Board Performance 16

Consequences of an open/short pin



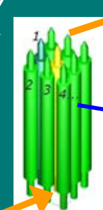


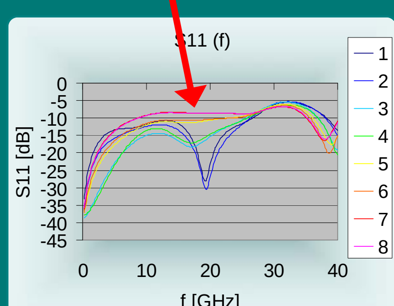
The Smith chart shows resonances in the connection as a small loop

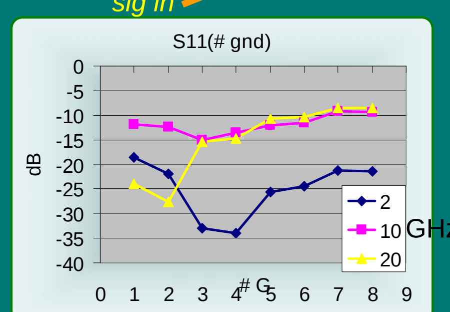
Measured insertion loss S21 of a load board with a parasitic resonance

Return loss (S11) performance with varying grounding

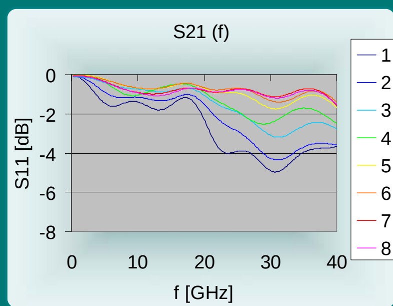
The 'resonances' observed here are not readily observable in the insertion loss S21 but merely frequencies where a perfect match is obtained. If there is no significant change in S21 at this frequency they are not necessarily detrimental to system performance.

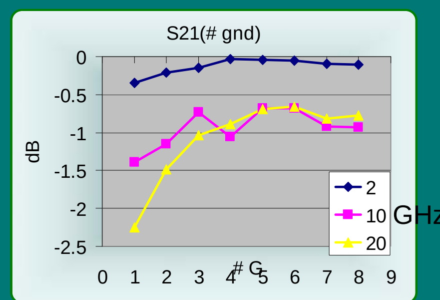






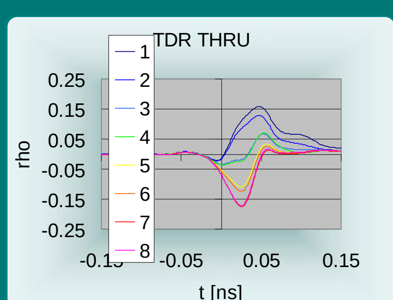
Insertion loss (S21) performance with varying number of ground connections

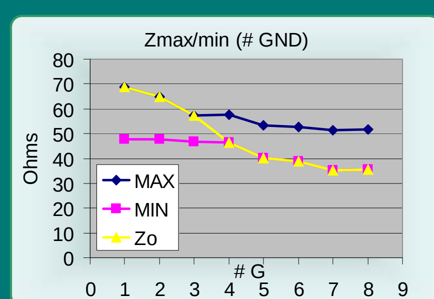




3/2010 Impact of Parasitic Resonances on Load Board Performance 19

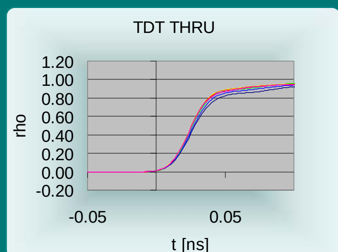
Time domain performance measurement with varying grounding conditions

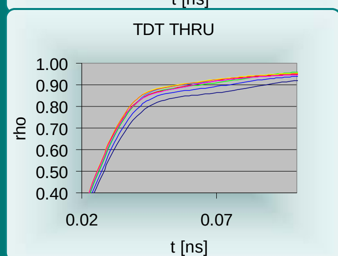


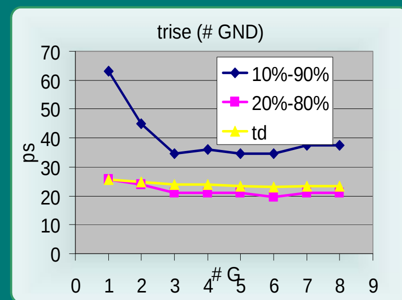


3/2010 Impact of Parasitic Resonances on Load Board Performance 20

Time domain performance measurement with varying grounding conditions

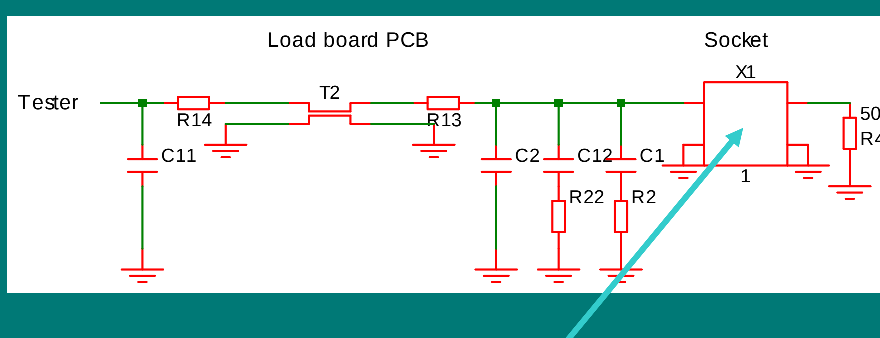






Only the 10%/90% rise time shows a noticeable dependence on the number of ground pins.

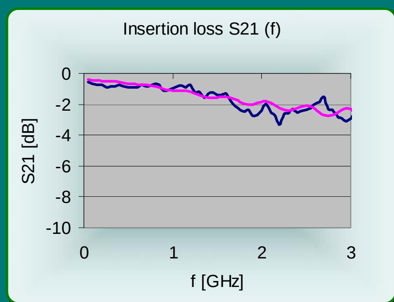
Equivalent circuit for signal path models



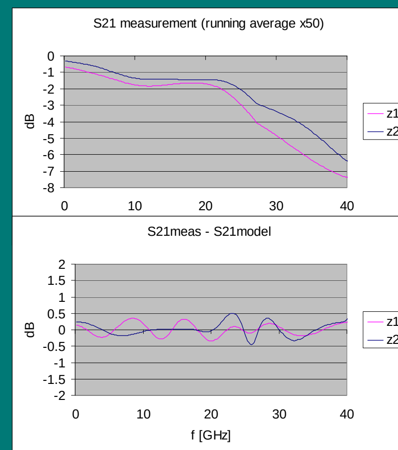
Socket parameters from measurement, converted to a multi-pole SPICE model

Model performance verification (measurement vs. simulation verification)

PCB only



Socket only (two diff. z values)

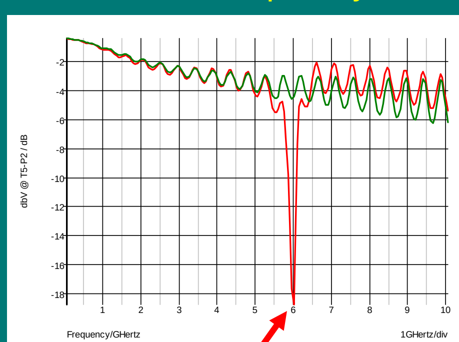


PCB simulation results (pink) compare favorably with the measurement results (blue).

Measurement results (top) are only given as a reference and averaged to make unidentifiable

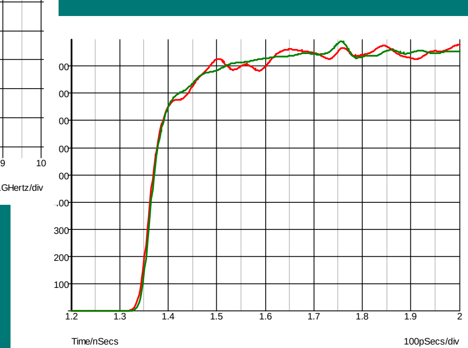
3/2010 Impact of Parasitic Resonances on Load Board Performance 23

Impact of resonance on load board time and frequency domain performance



Insertion loss model

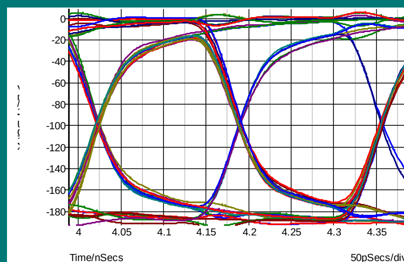
6 GHz

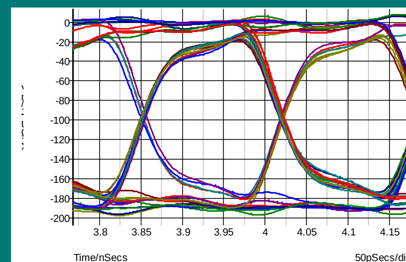


Transmitted step model

3/2010 Impact of Parasitic Resonances on Load Board Performance 24

Eye diagram change due to an adjacent pin open/short resonance





no resonance

resonance

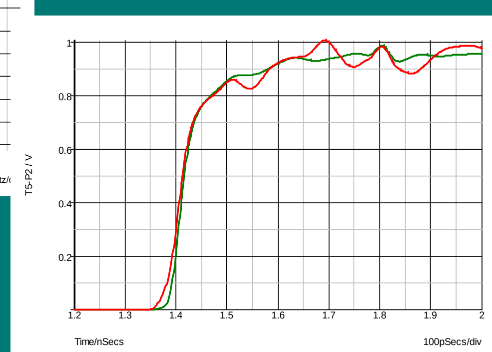
There is little impact from a 6 GHz resonance on a load board eye diagram at 6 Gbps

3/2010 Impact of Parasitic Resonances on Load Board Performance 25

Impact of resonance on load board time and frequency domain performance

Insertion loss model

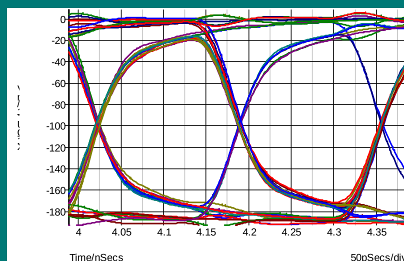
3 GHz



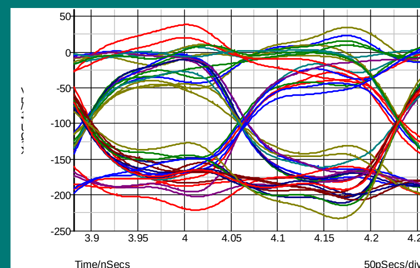
Transmitted step model

3/2010 Impact of Parasitic Resonances on Load Board Performance 26

Eye diagram change due to an adjacent pin open/short resonance



no resonance



resonance

Noticeable degradation of a load board eye diagram (6Gbps) from a 3 GHz resonance

Conclusion

- Parasitic resonances can have severe impact on system operation and thereby potentially limit test yield.
- Individual assessment is needed since grounding configurations are case specific.
- Simple load board models allow for prediction of resonance effects and their consequences.
- Eye diagrams show that good performance at certain frequencies is available even in the presence of resonances.
- Conversely, eye diagrams may miss “dangerous resonance” conditions at frequencies other than that used.

The Importance of the Signal Return Path

Zaven Tashjian
President, Circuit Spectrum, Inc.

Kevin Hoffmann
Consultant, Development/Test/SI

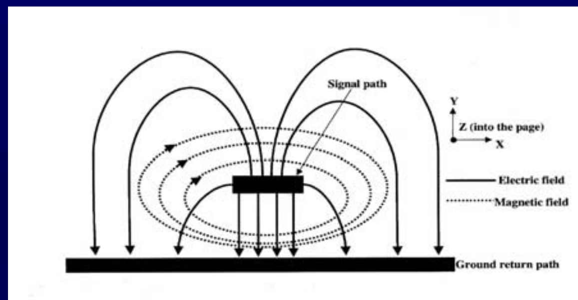
2010 BiTS Workshop
March 7 - 10, 2010

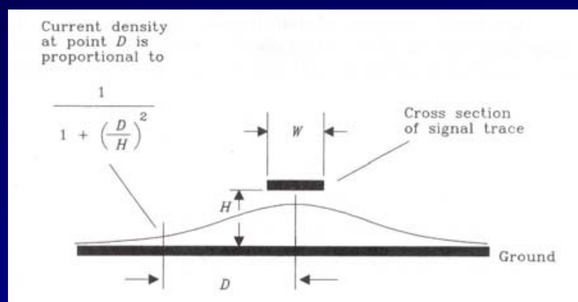
Agenda

- The realities of digital signal transmission in PCB's
- Modeling and simulation tools help predict behavior
- Use of S-parameters (S11/S22, S12/S21) and TDR to characterize 2-port systems
- Illustration with PCB via transitions
- A simple, but important, lesson from an SMA launch
- Correlation between simulation data and empirical data

3/2010 The Importance of the Signal Return Path 2

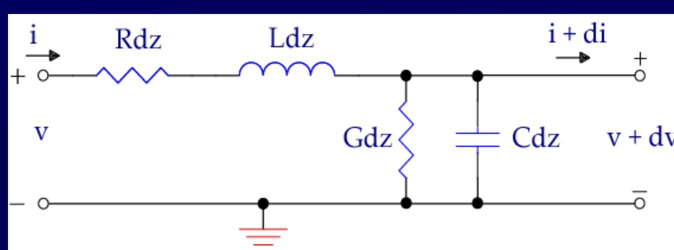
The Need for 3D Electromagnetic Field Solver





3/2010 The Importance of the Signal Return Path 3

RLGC Model for Incremental Length dz



$$\frac{dv}{dz} = -L\frac{di}{dt} - R\,i$$

$$\frac{di}{dz} = -C\frac{dv}{dt} - G\,v$$

3/2010 The Importance of the Signal Return Path 4

Portion of Touchstone File for Socket Pin

(Courtesy Johnstech International)

```
!     GWN .S2P test data output file                G-S-G configuration

!     S11          S21          S12          S22
!     symbol       freq-unit    parameter-type    data-format keyword      impedance-ohms

#     GHz    S      MA     R      50
1.99E-01     1.23E-02     -9.85E+00    9.97E-01     -1.57E+00    0.996765505 -1.573792    0.001721621 -5.35E+01
3.99E-01     1.26E-02     -1.44E+01    9.97E-01     -2.35E+00    0.9966806   -2.351074    0.002240738 -6.36E+01
5.98E-01     1.32E-02     -2.09E+01    9.97E-01     -3.51E+00    0.996607061 -3.511597    0.003177961 -7.59E+01
7.97E-01     1.40E-02     -2.67E+01    9.96E-01     -4.67E+00    0.996469637 -4.670654    0.004165134 -8.32E+01
9.96E-01     1.49E-02     -3.20E+01    9.96E-01     -5.82E+00    0.99639086  -5.820068    0.005169833 -8.84E+01
1.20E+00     1.60E-02     -3.65E+01    9.96E-01     -6.97E+00    0.996175577 -6.966797    0.006201268 -9.26E+01
1.39E+00     1.72E-02     -4.06E+01    9.96E-01     -8.10E+00    0.995880755 -8.102539    0.007246971 -9.61E+01
1.59E+00     1.86E-02     -4.40E+01    9.95E-01     -9.23E+00    0.995474948 -9.23291     0.008310535 -9.91E+01
1.79E+00     2.01E-02     -4.71E+01    9.95E-01     -1.04E+01    0.995085047 -10.35352    0.009381353 -1.02E+02
1.99E+00     2.18E-02     -4.97E+01    9.95E-01     -1.15E+01    0.994622776 -11.46973    0.010462344 -1.04E+02
2.19E+00     2.35E-02     -5.21E+01    9.94E-01     -1.26E+01    0.994069926 -12.57422    0.011545228 -1.07E+02
2.39E+00     2.54E-02     -5.42E+01    9.93E-01     -1.37E+01    0.993417017 -13.66699    0.012643156 -1.09E+02
```

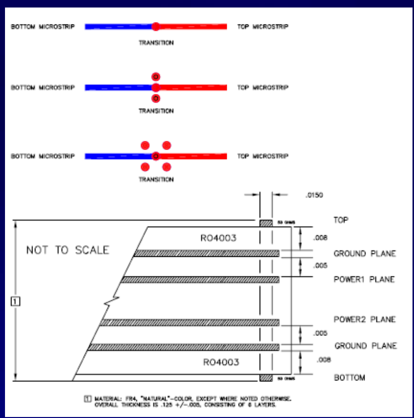
Bandwidth claims are valid only if test conditions are stated (GSG)

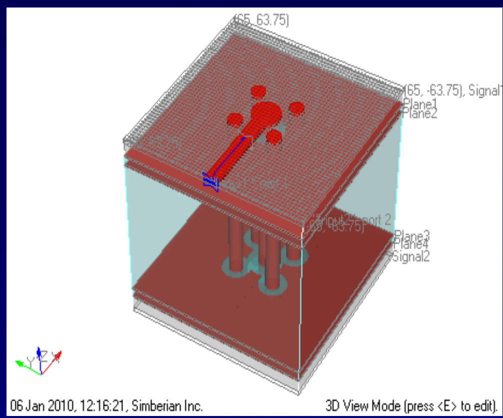
3/2010 The Importance of the Signal Return Path 5

Microstrip Lines with Via Transitions

From CAD

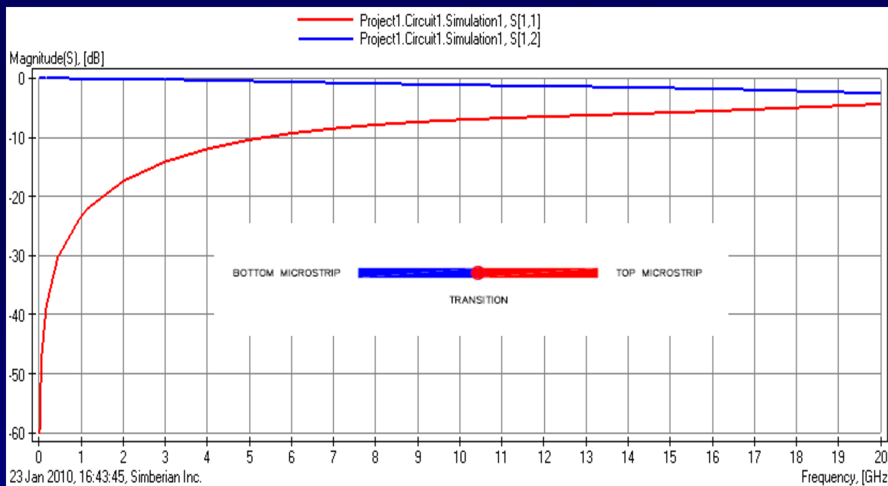
Modeling by Simbeor





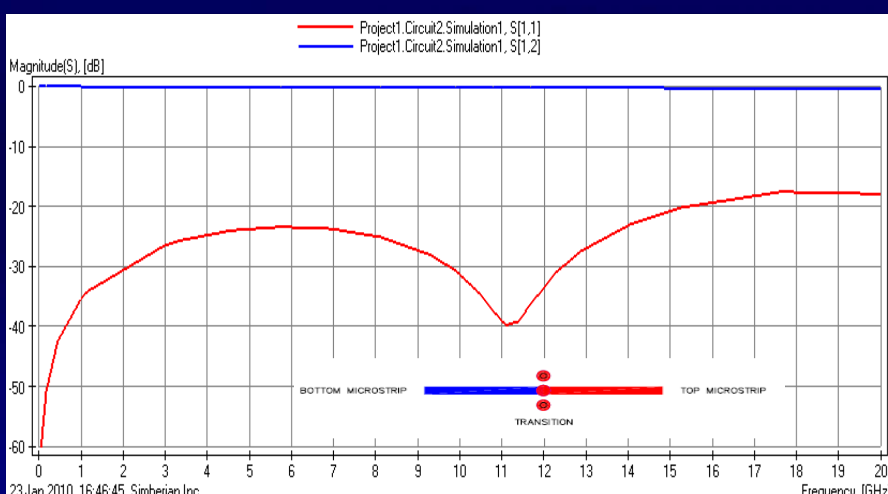
3/2010 The Importance of the Signal Return Path 6

Signal Via with no Ground Vias



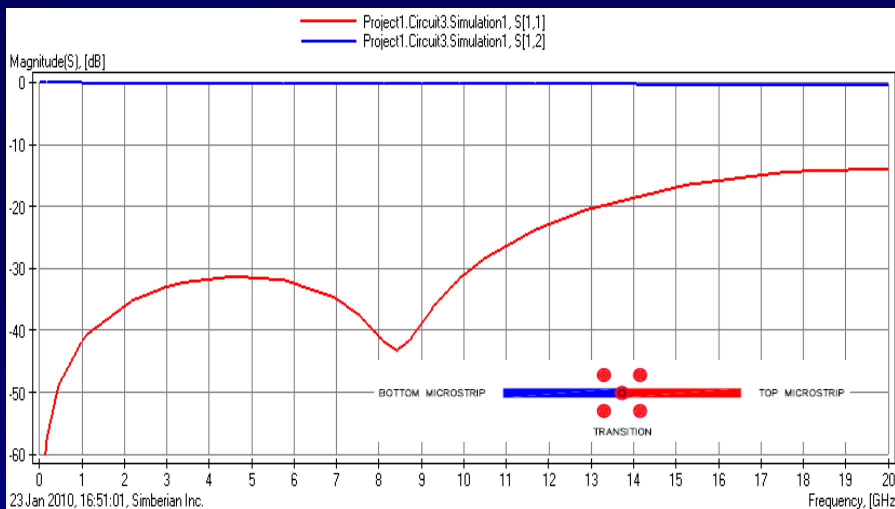
3/2010 The Importance of the Signal Return Path 7

Signal Via with Two Ground Vias



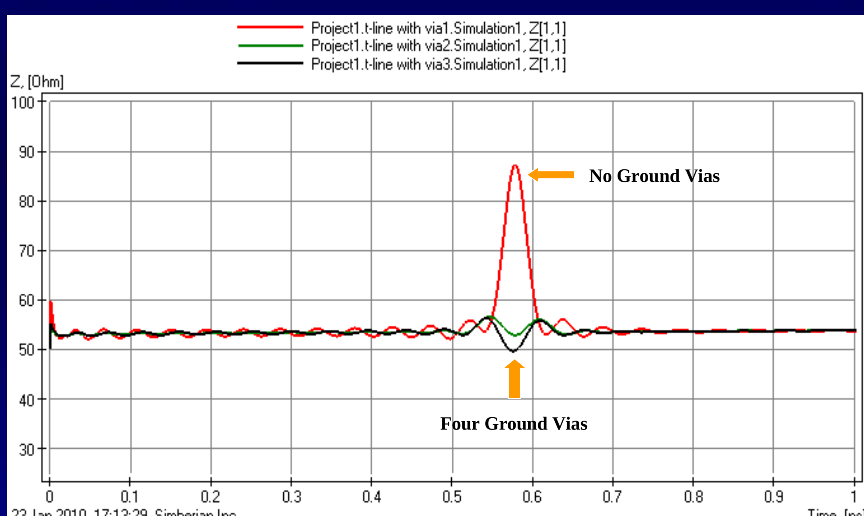
3/2010 The Importance of the Signal Return Path 8

Signal Via with Four Ground Vias



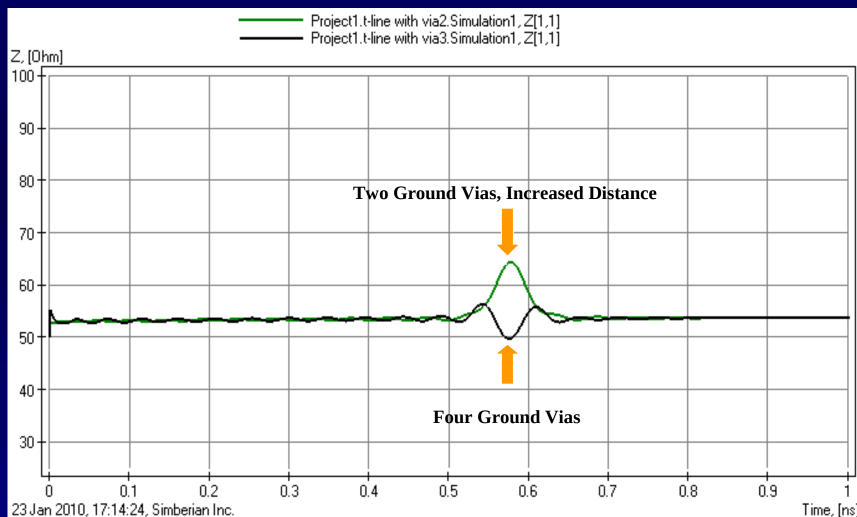
3/2010 The Importance of the Signal Return Path 9

TDR Data for the Three Via Patterns



3/2010 The Importance of the Signal Return Path 10

TDR Data for Two Via Patterns



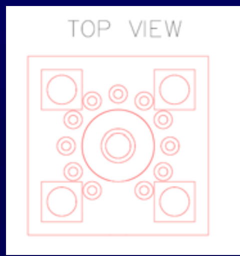
3/2010 The Importance of the Signal Return Path 11

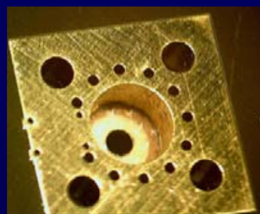
SMA Signal Launch through PCB

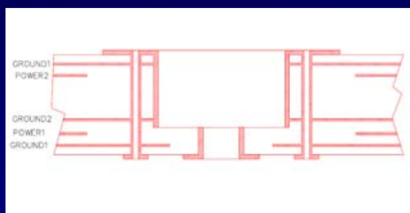
- SMA flange-mount connector launch
- Two cases - one with a poor return path and one with an improved configuration
- Simulation results from a 2D tool
- Simulation results from a 3D EM solver
- Measured data from a test coupon using VNA
- S-parameters show performance versus frequency

3/2010 The Importance of the Signal Return Path 12

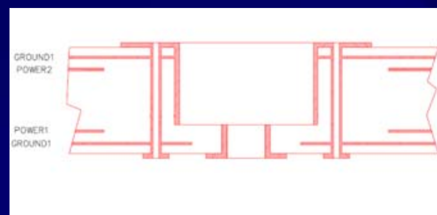
SMA Launch







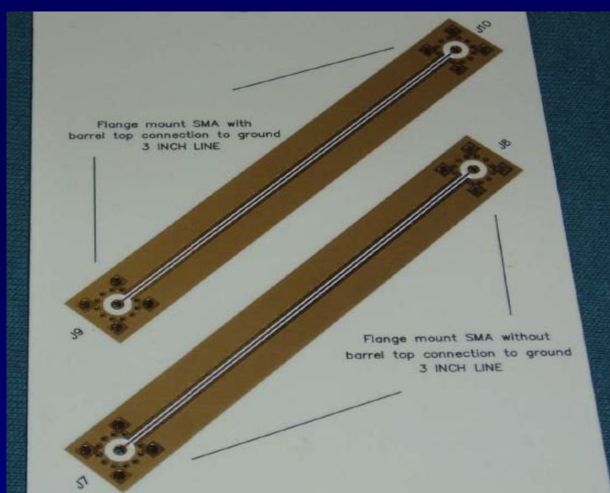
Improved Signal Return Path



Poor Signal Return Path

3/2010 The Importance of the Signal Return Path 13

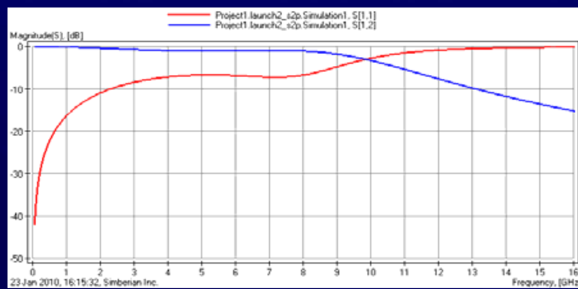
SMA Launches with Co-planar Microstrips



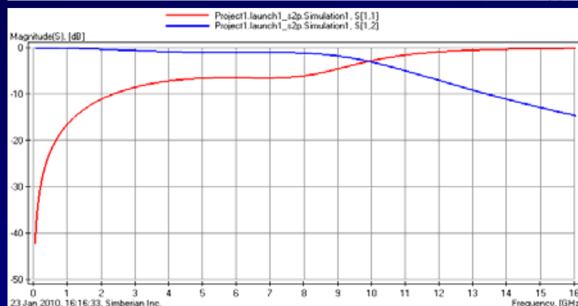
3/2010 The Importance of the Signal Return Path 14

Results from 2D Modeling Tool

Improved Path

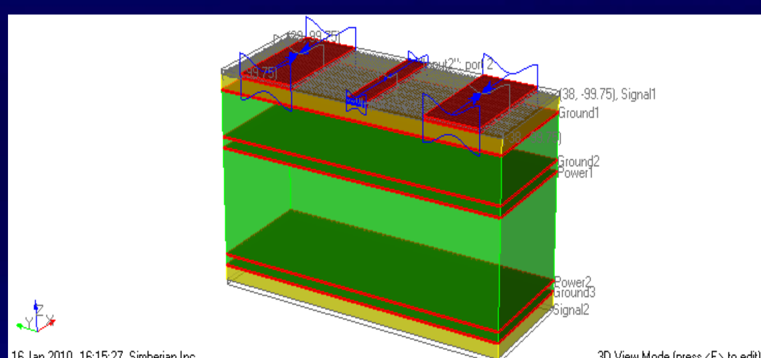


Poor Path



3/2010 The Importance of the Signal Return Path 15

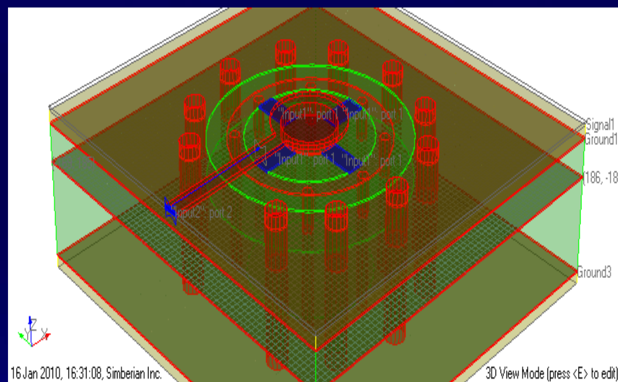
Transmission Line Simulation Geometry



- Microstrip T-Line with co-planar ground
- Reduced ground width to minimize simulation

3/2010 The Importance of the Signal Return Path 16

Launch Geometry: Poor Return



Circuitous signal return path

Launch Geometry: Improved Return

Direct path from Ground1 to Ground2 afforded by adding a plane to the design

VNA and Test Coupon

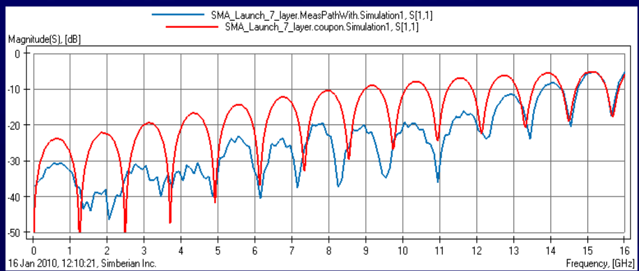
Agilent
E8722ES

The VNA provides measured responses over a frequency range (S-parameters) that can be saved in a Touchstone file format, allowing importing into a simulator for comparison

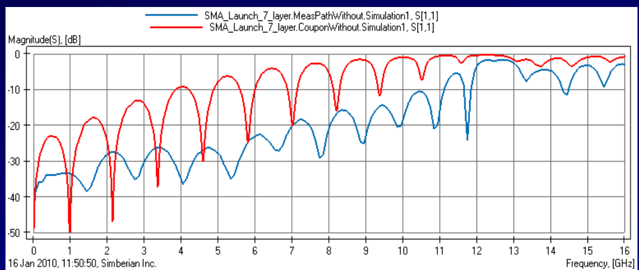
3/2010 The Importance of the Signal Return Path 19

S11 - Return Loss

Improved
Path



Poor
Path

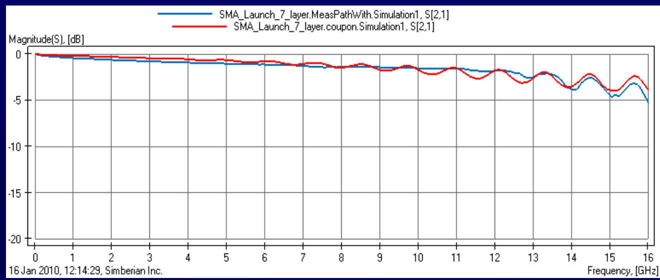


Measured response in blue, simulated in red

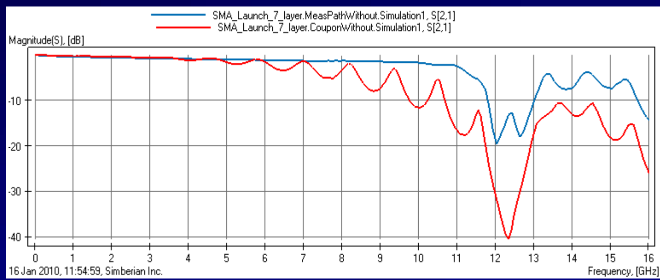
3/2010 The Importance of the Signal Return Path 20

S21 - Insertion Loss

Improved Path



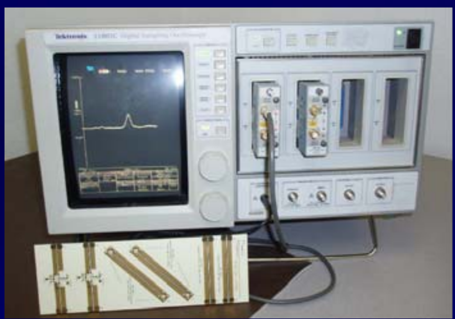
Poor Path



Measured response in blue, simulated in red

3/2010 The Importance of the Signal Return Path 21

TDR Scope and Test Coupon



Tektronix 11801C

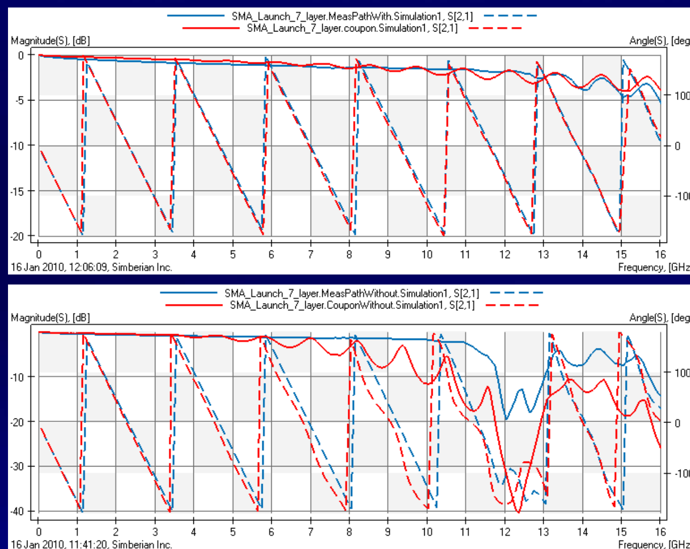
Improved path in green, poor path in purple

3/2010 The Importance of the Signal Return Path 22

S21 - Magnitude & Phase Comparison

Improved Path

Poor Path



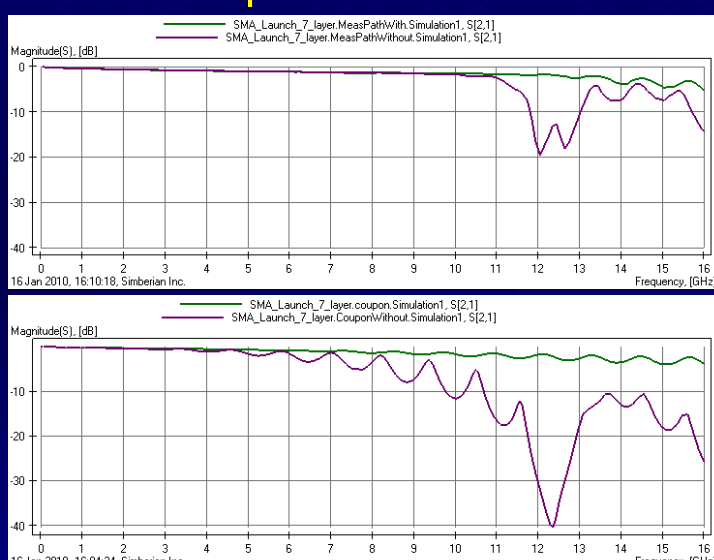
Measured response in blue, simulated in red

3/2010 The Importance of the Signal Return Path 23

S21 - Improved vs Poor

Measured Data

Simulation Data



Improved path in green, poor path in purple

3/2010 The Importance of the Signal Return Path 24

Conclusions

- For signal transitions through a PCB, the nature of the return path will affect performance
- Comparison of simulated and measured results shows good correlation of general behavior
- Improving the return path takes a design that is usable to 3.2 Gbps and extends it to 10 Gbps

3/2010 The Importance of the Signal Return Path 25

Acknowledgement

The authors wish to thank Yuriy Shlepnev, Ph.D., President, Simberian Inc., for his valuable help and generous support throughout the process of creating this presentation.

3/2010 The Importance of the Signal Return Path 26

Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards

Erkan Acar and Tim Swettlen
Intel Corporation

2010 BiTS Workshop
March 7 - 10, 2010

Motivation

- Kudos for achieving aspect ratios of 30+:1
  - Very impressive manufacturing
  - But very costly trend to continue down this trend
  - There are ways to better designs
    - Use design ingenuity
- Lower cost through thinner PCBs

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 2

Outline

- Motivation
- ATE PCB Manufacturing
  - High aspect ratio
  - Routing density
  - Cost
- Stripline Structures
- Using Power-Ground-Signal stack-up
- Simulation and Measurement Results
- Conclusion

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 3

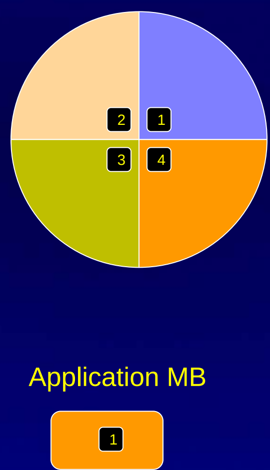
ATE PCB’s

- Shorter electrical paths
- Standard interconnects

- Longer paths
- Additional interconnects

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 4

ATE PCB's



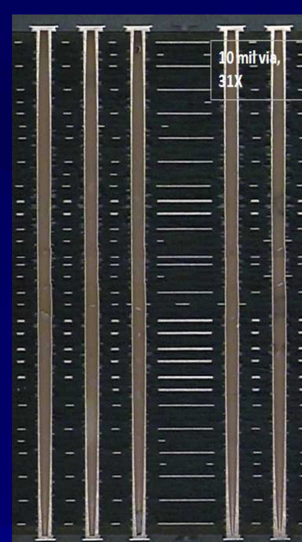
- Multiple devices
- Fixed size
- Mechanically rigid
- Increased leadtime

These limits have driven the PCB thicknesses up. Boards greater than 0.250" thick are not rare.

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 5

Via style

- Internal routing layers
  - Required to meet routing density
- Any layer change requires a via
  - PTH vias are preferred
- In a thick design, these vias push the manufacturing limits with their high aspect ratios
  - Bigger drills
  - Plating process
  - Yield

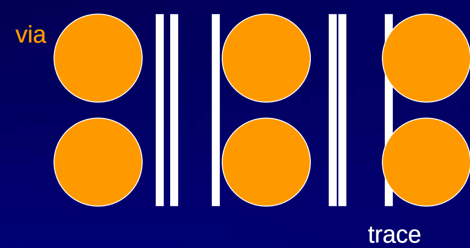


Courtesy of Harbor Electronics

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 6

Routing and Breakout Density

- Larger via drill bits
  - Reduced space for signal breakout
- Challenging to meet routing density



3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 7

Potential Solution Options

- Use advanced via technologies
  - Microvias
  - Good for only a number of internal layers
- Use sequential lamination
  - Multiple books can be fabricated and laminated
  - Increased lead time
  - Higher overall cost
- Reduce board thickness
  - Easier said than done

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 8

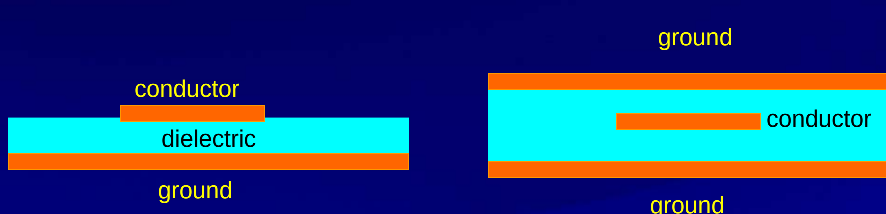
Board Thickness Reduction

- Eliminates the need for higher aspect ratios
- Improved performance
  - Reduced electrical length
  - Shorter via stubs
- Several ways to reduce board thickness
  - Reduce routing layer count
    - Appealing, but requires sacrifice in performance
- Use a Ground-Signal-Power stack-up
    - Another look into PCB transmission lines

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 9

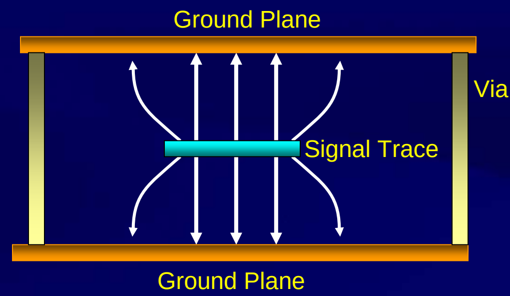
PCB Transmission Lines

- Transmission lines are created to transmit signals point to point
  - Microstrip
  - Stripline
    - Common in multi-layer ATE boards



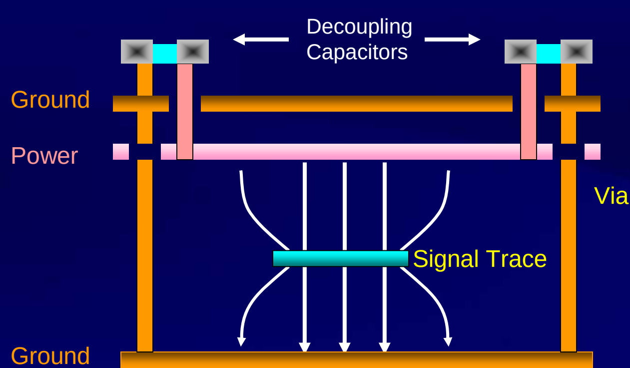
3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 10

Stripline Background

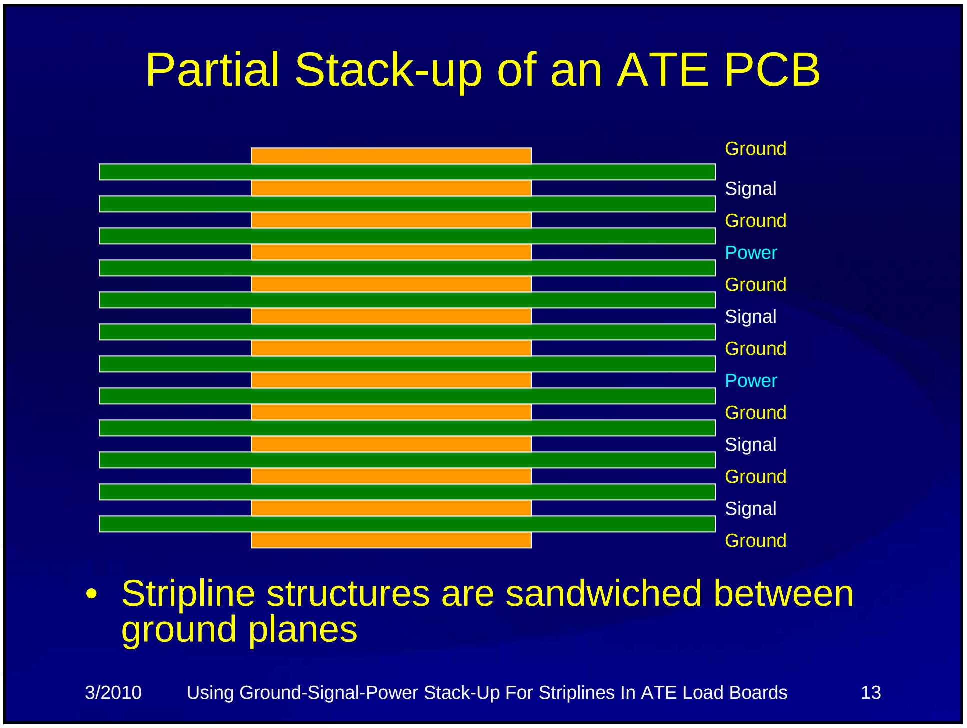


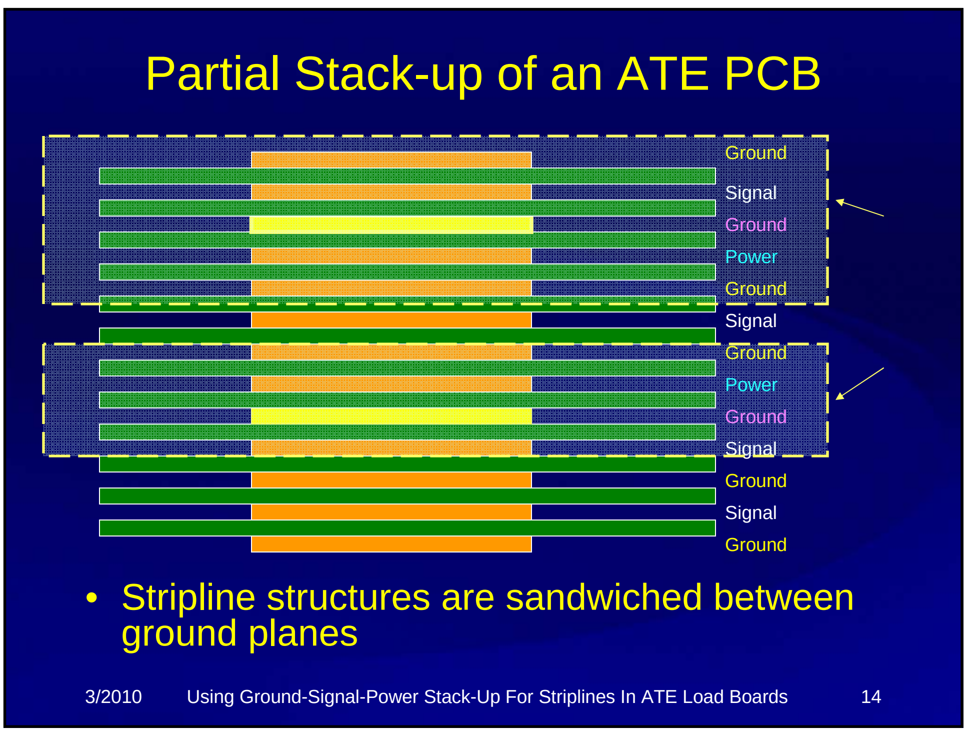
- The signal trace is sandwiched between ground planes
  - Stitched through vias
- Immune to outside noise
- Fabrication is much more complex compared to microstrip
- Used in multi-layer PCBs

Ground-Signal-Power Stack-up

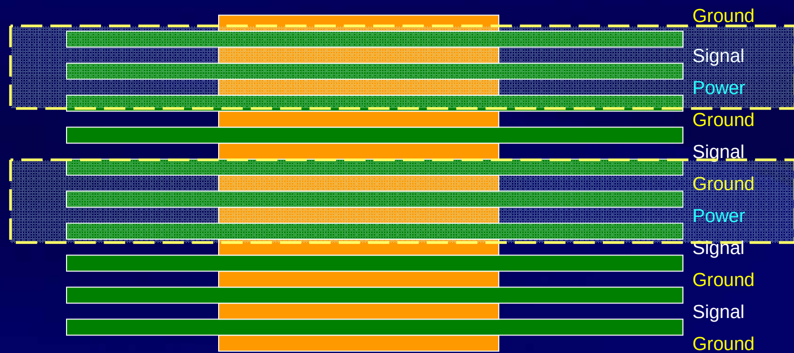


- The signal trace is sandwiched between a ground and a power plane
  - Stitched through decoupling capacitors


Partial Stack-up of an ATE PCB
Ground
Signal
Ground
Power
Ground
Signal
Ground
Power
Ground
Signal
Ground
Signal
Ground
• Stripline structures are sandwiched between ground planes
3/2010
Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards
13


Partial Stack-up of an ATE PCB
Ground
Signal
Ground
Power
Ground
Signal
Ground
Power
Ground
Signal
Ground
Signal
Ground
• Stripline structures are sandwiched between ground planes
3/2010
Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards
14

Partial Stack-up of an ATE PCB

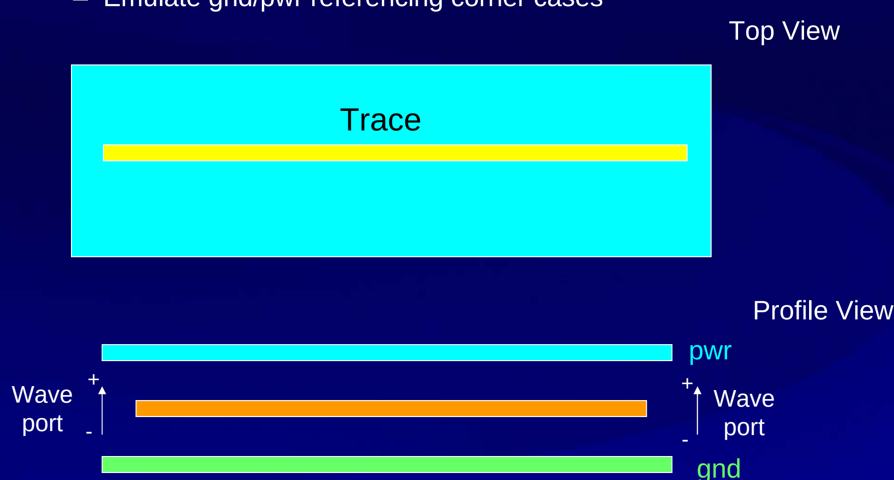


- The layer count and board thickness can be reduced in this way
  - 36 layers → 22 layer
  - 250mil → 185mil
- Several challenges that do not apply to ordinary striplines

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 15

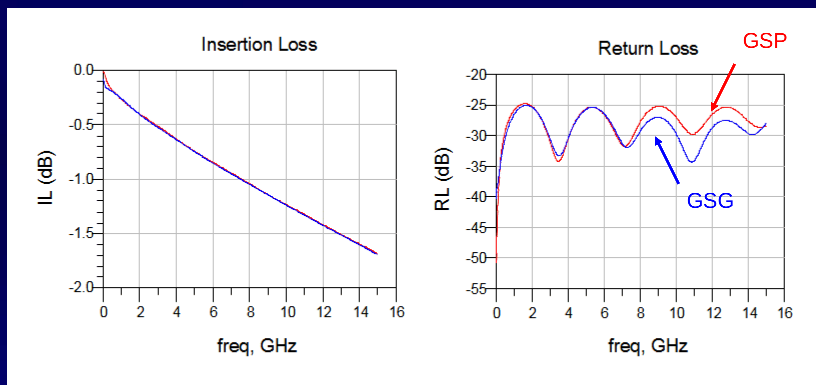
Simulation

- 3D EM simulation
  - Emulate gnd/pwr referencing corner cases



3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 16

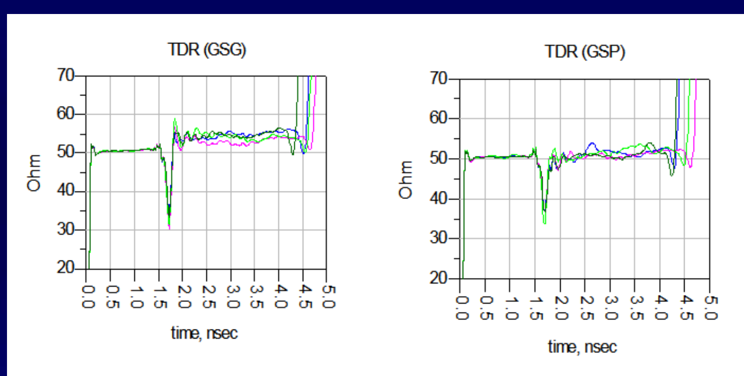
Simulation Results



- Insertion and return loss do not show a significant difference

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 17

Measurements



- Comparison of TDR responses
  – No significant difference between GSG and GSP

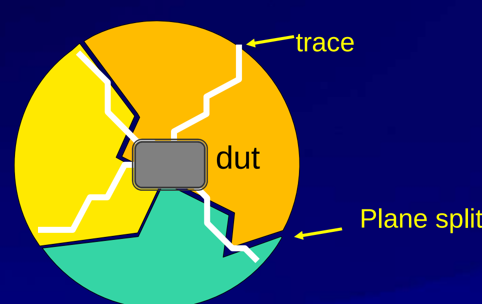
3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 18

GSP Design Issues

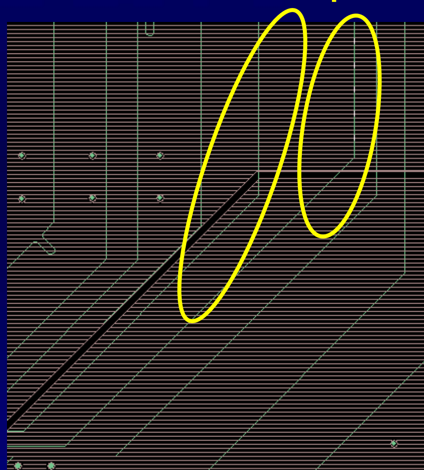
- Power plane splits
  - Different potentials on the same layer
- DC leakage on the signal
  - Parasitic capacitances may change the DC level of the signal
- Power Supply Noise/Resonance

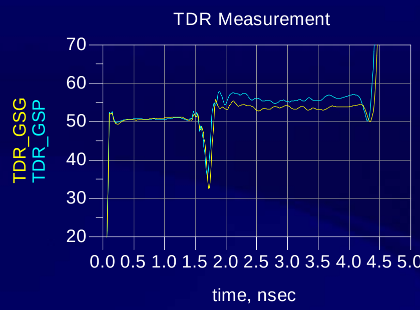
Split Power Planes

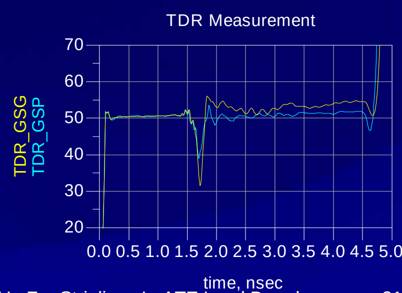
- Multiple power nets can share the same layer
  - Split power plane
- Signals may cross plane splits



A Real Example







No significant difference between TDR profiles of GSG and GSP!

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 21

Conclusion

- Conservative design practices are pushing limits of PCB manufacturing capabilities
- Simple changes such as GSP stack-ups can reduce manufacturing complexity without impacting the performance
- Ideal supplier builds to performance specs not physical specs
  - More focus on design and layout for manufacturing

3/2010 Using Ground-Signal-Power Stack-Up For Striplines In ATE Load Boards 22

Spring Probe PCB Pad Wear Analysis

Valts Treibergs
Chris Cuda

ECI Interface Products
Harbor Electronics, Inc.

2010 BiTS Workshop
March 7 - 10, 2010

BiTS Burn-in & Test Socket Workshop
multitest

Presentation Agenda

- ATE PCB Loadboard Considerations
- Pad Wear-out Test Setup And Methodology
- Pad Wear Vs. Spring Probe Tips
  - Results
- Pad Wear Vs. Surface Finish
  - Results
- Pad Wear Due To Probe Chatter
  - Results
- Summing It All Up
- Missing Pieces & Next Steps

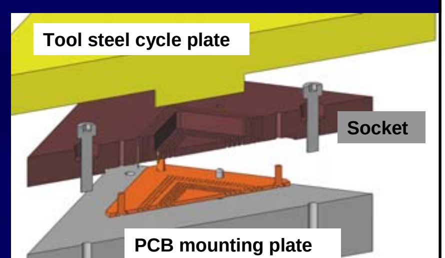
ATE PCB Loadboard Considerations

- ATE PCBs are a significant cost contribution to a test cell:
  - $500 - $10,000 for the bare board, plus components assembly up to $10,000 for the most complex designs
- It is thought that most ATE boards see in excess of 4 million socket cycles – roughly an order of magnitude over typical socket contact life expectations
- MYTH or FACT? More gold on socket pads means longer life

03/2010 Spring Probe PCB Pad Wear Analysis 3

Pad Wear-out Test Setup

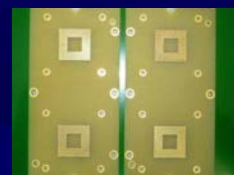
- Cycle test fixture
  - Probe cross-section designed for each probe style
  - Multiple probe styles can be accommodated in one setup
  - Hardened tool steel cycle plate that hardstops on top of socket fixture
  - High-speed pneumatic cycling apparatus



03/2010 Spring Probe PCB Pad Wear Analysis 4

Pad Wear-out Test Setup

- Standardized PCB outline
  - .8mm pitch offset-via on BGA grid, .125” thick PCB
  - Manufactured at Harbor Electronics using same equipment and processes as standard ATE boards
  - Pads finish plating per experiment
  - PCB pads shorted for SEM analysis compatibility



03/2010 Spring Probe PCB Pad Wear Analysis 5

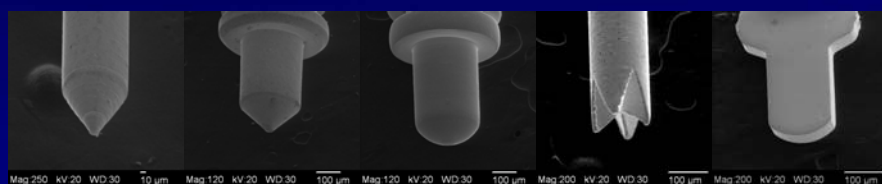
General Pad Wear-out Test Methodology

1. New probes loaded in test fixture – tip condition photographed
2. PCB pads optically photographed – new
3. Cycle to 1 million fixture actuations
4. Probes replaced – some positions not repopulated
5. PCB pads optically photographed @ 1M
6. Cycle to 2 million actuations
7. PCB pads optically photographed @ 2M
8. SEM analysis: SE images of pads and marks, EDS analysis through marks @ 1M and 2M
9. Scoring and ranking - comparison

03/2010 Spring Probe PCB Pad Wear Analysis 6

Pad Wear Vs. Spring Probe Tips

- Standard Au/Ni plated PCB pads (1.27 µm Au over 5 µm Ni)
- 5+ probe tips: spear, conical, spherical, crown, radiused-flat
- 3 probe styles:
  - CSP5 (35g) – double-ended conventional probe
  - BTM080(28g) – machined 2-piece probe – external spring
  - MER050(30g) – flat technology probe
- Fully preloaded to the PCB**

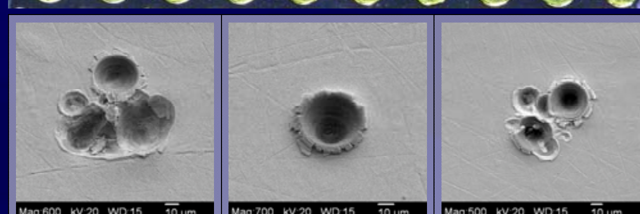


SPEAR CONICAL SPHERICAL CROWN RADIUS-FLAT

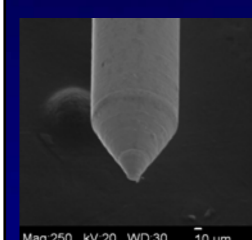
03/2010 Spring Probe PCB Pad Wear Analysis 7

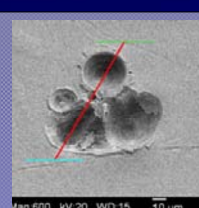
Spear Tip Results 2M (1.27 µm Au)

- Extreme divoting
- Exposed copper foil

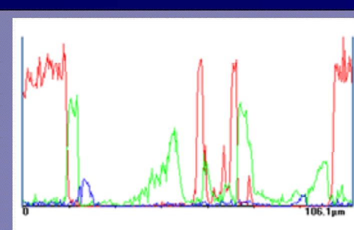


Pad 1 (2M) Pad 6 (1M) Pad 10 (2M)





Line - 1
Number Points - 359
Line Lenght - 106.1µm

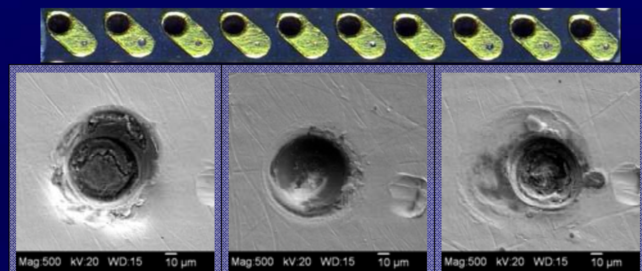


03/2010 Spring Probe PCB Pad Wear Analysis 8

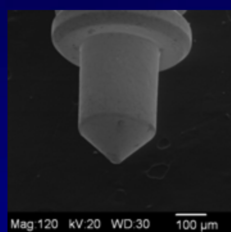
Paper #4

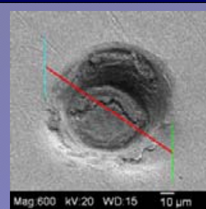
Conical Tip Results 2M (1.27 µm Au)

- Extreme divoting
- Exposed copper foil

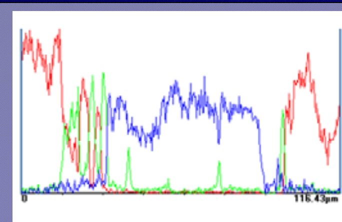


Pad 2 (2M) | Pad 6 (1M) | Pad 9 (2M)



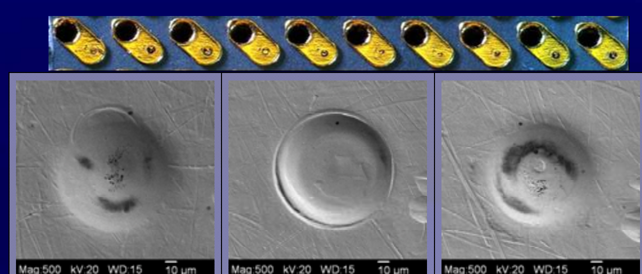


Line - 1
Number Points - 394
Line Lenght - 116.43µm

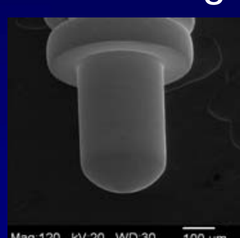


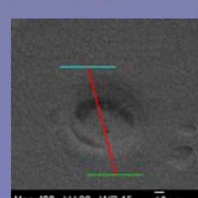
Spherical Tip Results 2M (1.27 µm Au)

- Radiused dimple
- No exposed copper foil
- Some burnishing

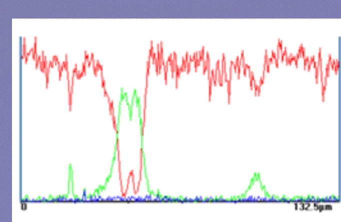


Pad 2 (2M) | Pad 4 (1M) | Pad 9 (2M)



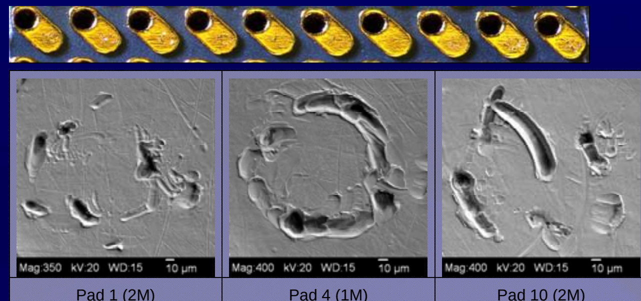


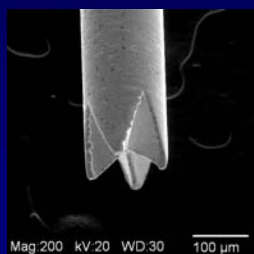
Line - 1
Number Points - 299
Line Lenght - 132.5µm

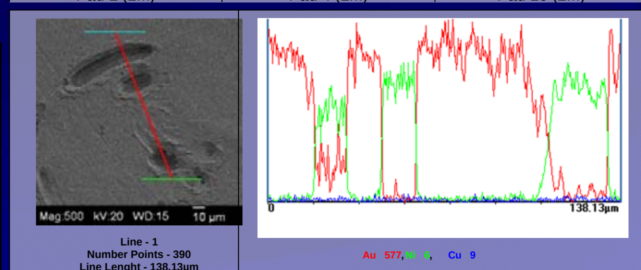


Crown Tip Results 2M (1.27 µm Au)

- Smeared gold
- No exposed copper foil
- Some burnishing
- Exposed nickel



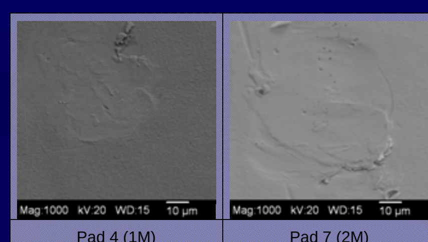


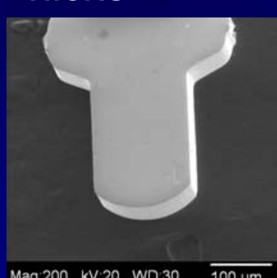


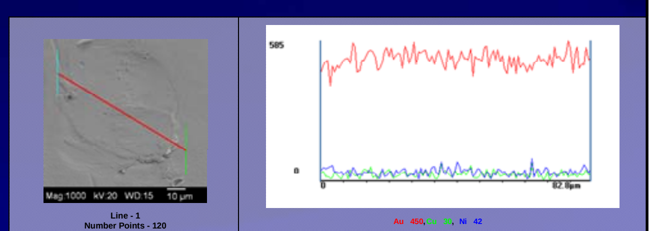
03/2010 Spring Probe PCB Pad Wear Analysis 11

Radius-flat Results 2M (1.27 µm Au)

- Smeared gold
- No exposed copper foil
- Some burnishing
- No exposed nickel







03/2010 Spring Probe PCB Pad Wear Analysis 12

Probe Tips – Severity Results

Tip	SPEAR		CONICAL		SPHERICAL		CROWN		R-FLAT	
	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu
SEVERITY	2	2	3	3	1	1	2	1	0	0
SCORE	4		6		2		3		0	

Winners!

Table Legend (Severity Score):
None (0): No material detected
Slight (1): Traces of exposed material on 10% of pad contact area or less
Moderate (2): Exposed material up to 50% of pad contact area
Severe (3): Exposed material – damaged pads > 50% of contact area

03/2010 Spring Probe PCB Pad Wear Analysis 13

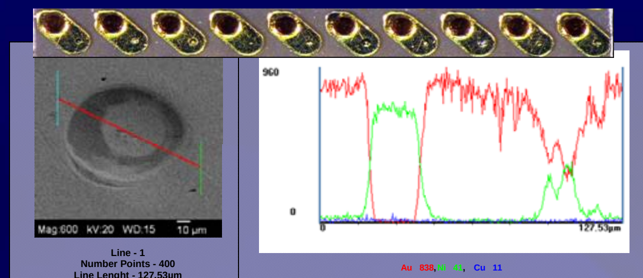
Pad Wear Vs. Surface Finish

- 2 PCB plating recipes:
  - 1.27 µm Au over 5 µm Ni
  - .75 µm Au over 5 µm Ni
- 5 probe tips: spear, conical, spherical, crown, radius-flat
- 3 probe styles:
  - CSP5 (35g) – double-ended conventional probe
  - BTM080(28g) – machined 2-pc probe – external spring
  - MER050(30g) – flat technology probe
- Fully preloaded to the PCB

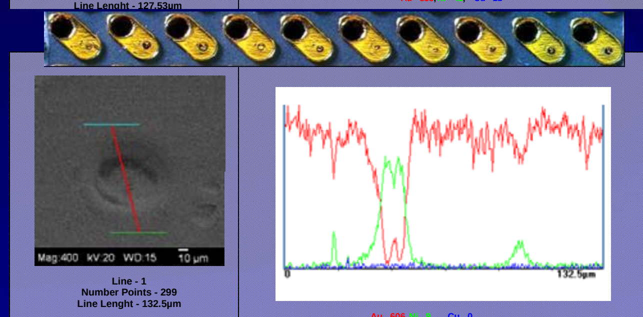
03/2010 Spring Probe PCB Pad Wear Analysis 14

Spherical Tip Results 2M

.75 µm Au
- Some exposed Ni
- Burnishing
- No exposed Cu



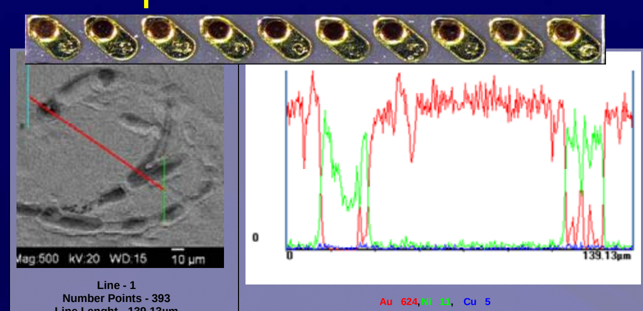
1.27 µm Au
- Some exposed Ni
- Burnishing
- No exposed Cu



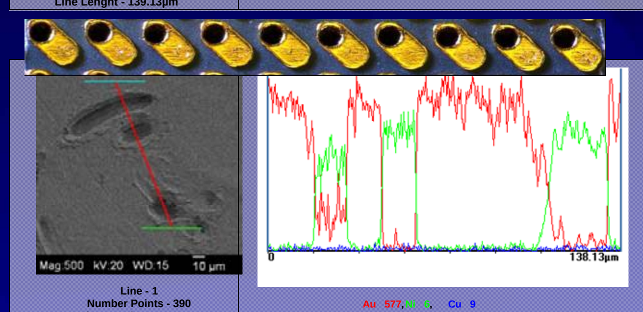
03/2010 Spring Probe PCB Pad Wear Analysis 15

Crown Tip Results 2M

.75 µm Au
- Some exposed Ni
- Smearing
- No exposed Cu



1.27 µm Au
- Some exposed Ni
- Smearing
- No exposed Cu

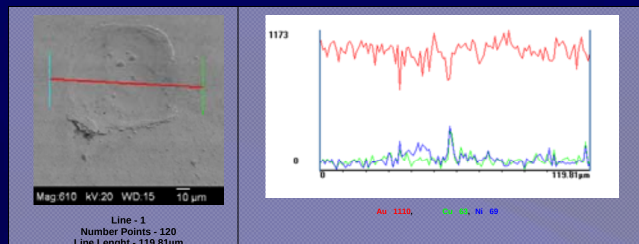


03/2010 Spring Probe PCB Pad Wear Analysis 16

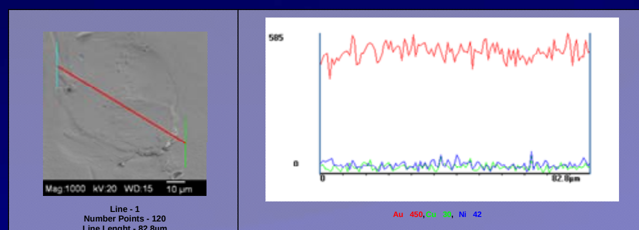
Paper #4

Radius-flat Results 2M (.75µm Au)

.75 µm Au
- Some exposed Ni
- Smearing
- No exposed Cu



1.27 µm Au
- Some exposed Ni
- Smearing
- No exposed Cu



03/2010 Spring Probe PCB Pad Wear Analysis 17

PCB Au Thickness – Severity Results

TIP / PCB	SPEAR		CONICAL		SPHERICAL		CROWN		R-FLAT		PCB SCORE
	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	
.75 µm Au	3	1	3	3	2	1	2	1	1	0	17
1.27 µm Au	2	2	3	3	1	1	2	1	0	0	15

Table Legend (Severity Score):
None (0): No material detected
Slight (1): Traces of exposed material on 10% of pad contact area or less
Moderate (2): Exposed material up to 50% of pad contact area
Severe (3): Exposed material – damaged pads > 50% of contact area

03/2010 Spring Probe PCB Pad Wear Analysis 18

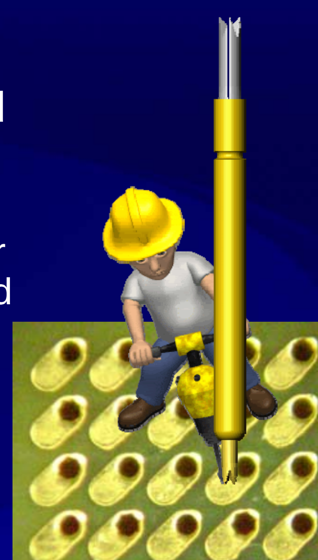
Final Box Score

TIP / PCB	SPEAR		CONICAL		SPHERICAL		CROWN		R-FLAT		PCB SCORE
	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	Ni	Cu	
.75 µm Au	3	1	3	3	2	1	2	1	1	0	17
1.27 µm Au	2	2	3	3	1	1	2	1	0	0	15
TIP SCORE	8		12		5		6		1		

03/2010 Spring Probe PCB Pad Wear Analysis 19

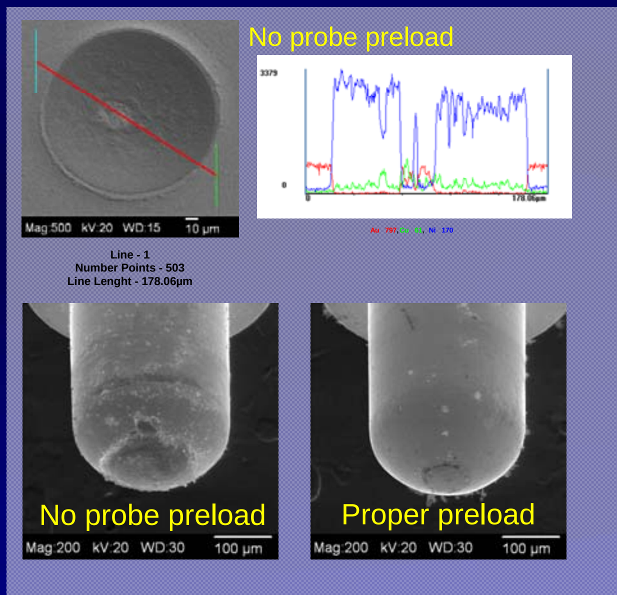
Pad Wear Due To Probe Chatter

- Not all PCB wear is due to 'normal' probe use
- Probe 'chatter' can be caused by a number of different conditions:
  - Improper socket design (little or no preload) or probe goes solid
  - Socket body bowing
  - Loose or improperly installed fasteners
  - Poorly toleranced probes or socket housings



03/2010 Spring Probe PCB Pad Wear Analysis 20

Pad Wear Due To Probe Chatter



- Spherical probe tip
- 1.27µm Au PCB
- Severe base material exposure
- Abrasion of probe tip

03/2010 Spring Probe PCB Pad Wear Analysis 21

Summing It All Up

- PCB pad wear-out is a costly issue
- PCB pad wear can be minimized by:
  – Specifying spherical or radius-flat probe tip geometries for socket pins
  – Insure that socket pin preload is maintained to minimize probe chatter
- Gold thickness on PCB pads does not have a significant impact on board longevity
  – However, future PCB finishes may significantly improve pad life

03/2010 Spring Probe PCB Pad Wear Analysis 22

Missing Pieces & Next Steps

- This study does not address these contact interfaces to PCB pads:
  - Blade-type contacts
  - Bare spring contacts
  - Rocking-type rigid contacts
  - Elastomeric style interconnects
- Determine the relationship between physical wear mechanisms to electrical contact performance
- Temperature effects of all wear mechanisms
- Optimizing PCB surface finishes for maximum life

03/2010 Spring Probe PCB Pad Wear Analysis 23