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LOW COST, SMALL FORM FACTOR PACKAGING

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ABSTRACT

While size reduction and performance improvement are often the drivers of new package and interconnect solutions, cost reduction strategies have become an even more critical factor to further enable continued profitability through challenging times. Although those times are hopefully (albeit temporarily) behind us, many companies large and small have adopted strategies to reduce package, interconnect and test cost. This presentation paper will look at leading package trends driven by cost reduction.

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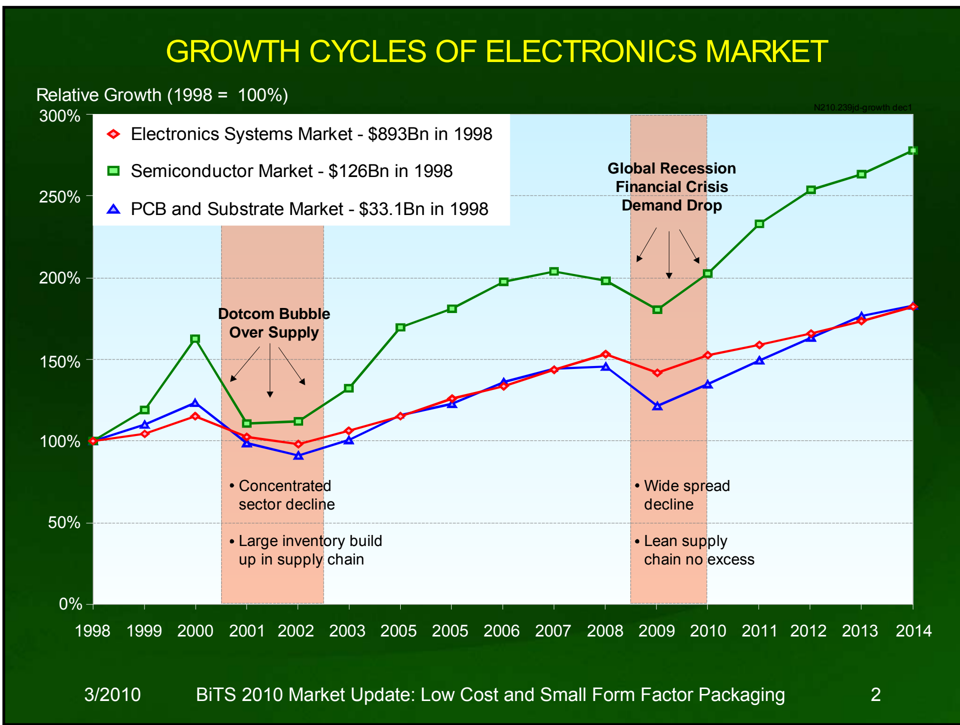

WHY LOW COST PACKAGES?

- Cost Reduction is always a priority, but industry downturns increase the stress put into cost reduction strategies
- Various approaches can be applied
  - Raw Material Cost (e.g. Copper vs. Gold wire)
  - Package Size Reduction (QFN/DFN, tighter pitch FBGA, WL-CSP)
  - Outsourcing and Regional Shifts
  - Efficiency Improvements (throughput, strip test, etc)

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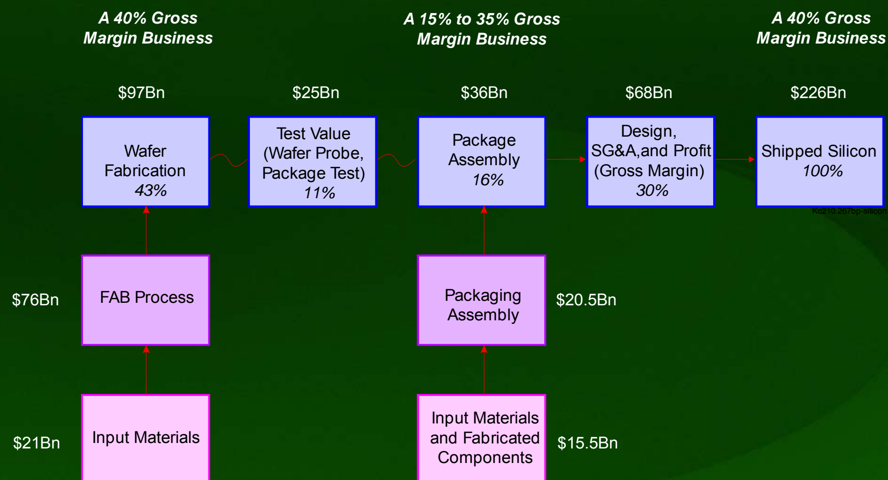

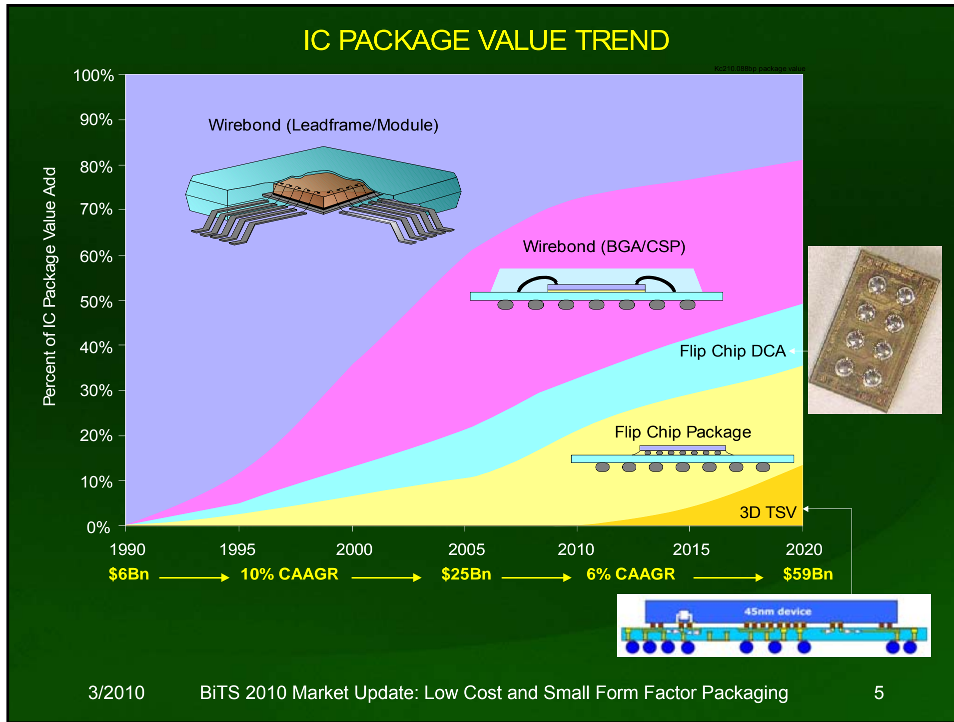
IC PACKAGE VALUE TREND
Percent of IC Package Value Add
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
Wirebond (Leadframe/Module)
Wirebond (BGA/CSP)
Flip Chip DCA
Flip Chip Package
3D TSV
1990
1995
2000
2005
2010
2015
2020
$6Bn
10% CAAGR
$25Bn
6% CAAGR
$59Bn
45nm device
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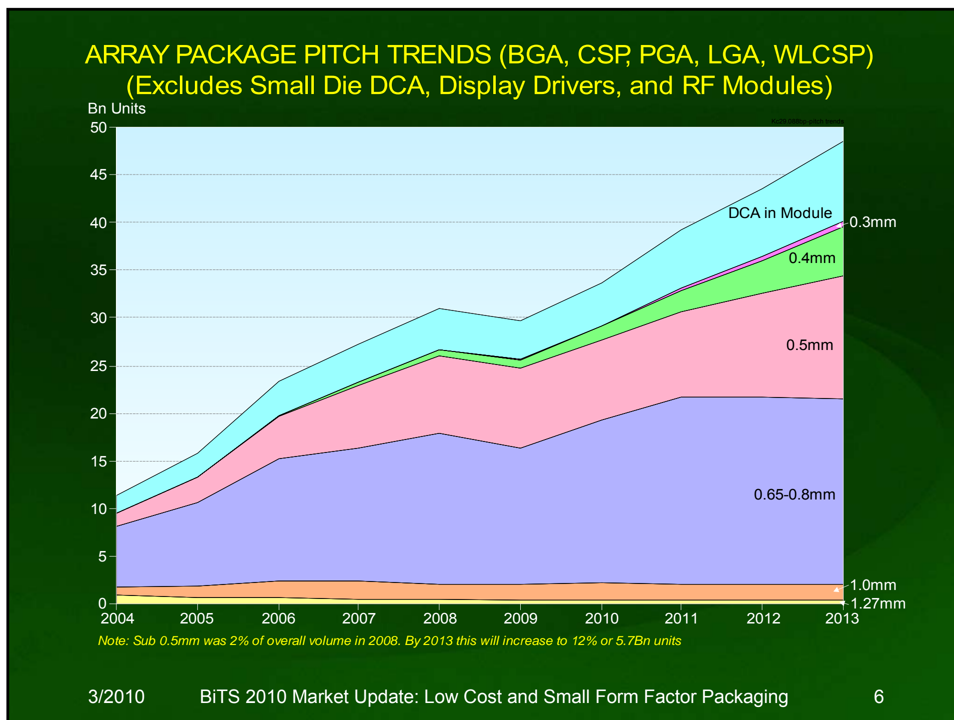
ARRAY PACKAGE PITCH TRENDS (BGA, CSP, PGA, LGA, WLCSP)
(Excludes Small Die DCA, Display Drivers, and RF Modules)
Bn Units
50
45
40
35
30
25
20
15
10
5
0
DCA in Module
0.3mm
0.4mm
0.5mm
0.65-0.8mm
1.0mm
1.27mm
2004
2005
2006
2007
2008
2009
2010
2011
2012
2013
Note: Sub 0.5mm was 2% of overall volume in 2008. By 2013 this will increase to 12% or 5.7Bn units
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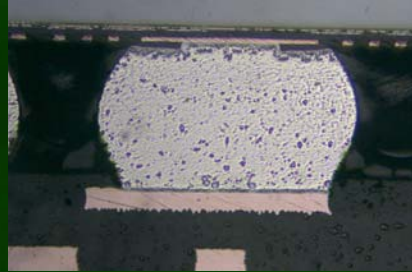
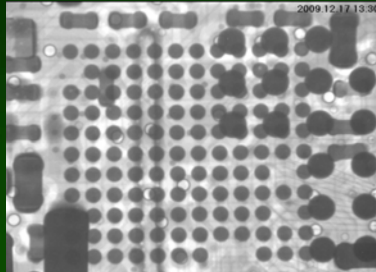
TI WiLink™ 6.0

210.1/085bp

- Single chip WLAN (b/g/n), Bluetooth, and FM Tx/Rx
- Found as WLCSP in Motorola Droid
  - Mounted on main board, underfilled
  - 5.0 x 4.6mm die size
  - 0.4mm pitch
  - 126 balls (near full array)
- One metal layer redistribution





Photos source: Prismark/Binghamton University

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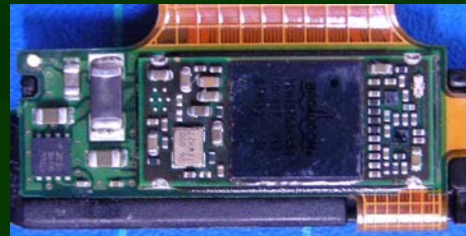
WLCSP SOLUTION IN APPLE iPod TOUCH

79.10/283bp

- WLAN/Bluetooth/FM Radio (FM not enabled)
- Broadcom BCM4325 WLAN/BT/FM
- WLCSP – 6.4 x 5.7mm
- 320 SnAg bumps at 250µm pitch
- Ceramic filter, crystal
- 52 SMT parts
- 1.0cm^2 PCB area mounted on rigid-flex



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99.1/085bp

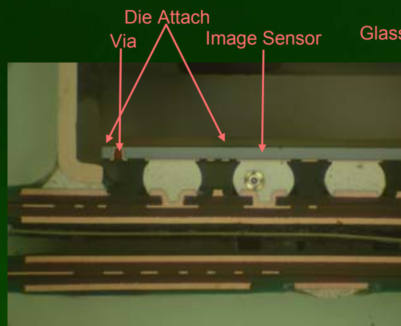
RECENT WLCSP APPLICATION EXAMPLES

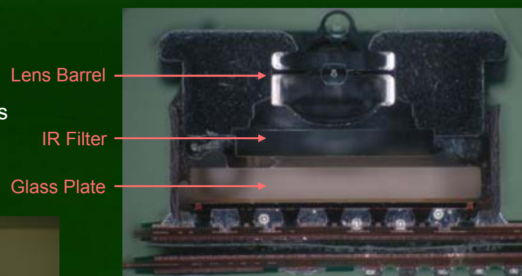
Mobile Phone	Total Wafer CSP	WLCSP Applications	Comments
Palm Pre	10	ESD/EMI, EEPROM, Bluetooth, WLAN	6 – 25 I/O on board WLAN, BT, EEPROM on module
Panasonic P901i TV	7	ESD/EMI, analog/power, other?	Up to 5mm die with 119 I/O at 0.4mm pitch
LG KM900 Arena	3	ESD/EMI, GPS	4.7mm, 64 I/O at 0.4mm pitch
Apple iPhone 3GS	6	ESD/EMI, Bluetooth, WLAN, GPS	Up to 4.7mm die with 69 I/O at 0.4mm pitch on board, 6.4 x 5.7mm die at 320 I/O on module
Panasonic P905i	6	Transceiver, Bluetooth, power, TV tuner (two chips), GPS	5 die use copper post tech, up to 185 I/O at 0.4mm pitch
Nokia 6220 Classic	7	ESD/EMI, power, other?	Up to 5mm die
Nokia N95	8	EMI/ESD, analog, Bluetooth, FM radio	Up to 4mm die with 47 I/O at 0.5mm pitch
Nokia N97	8	EMI/ESD, GPS, WLAN, analog	Up to 4.4mm on module (104 I/O) Up to 3.5mm die on board (61 I/O)

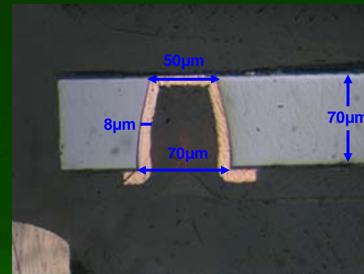
210.8/371PL

TOSHIBA TCM9000MD VGA MODULE USING TSV

- Image sensor die
  - 25 balls at 0.5mm pitch
  - 2.8 x 3.3mm
  - 70µm thick
  - 125µm thick attach to glass
  - 350µm thick glass







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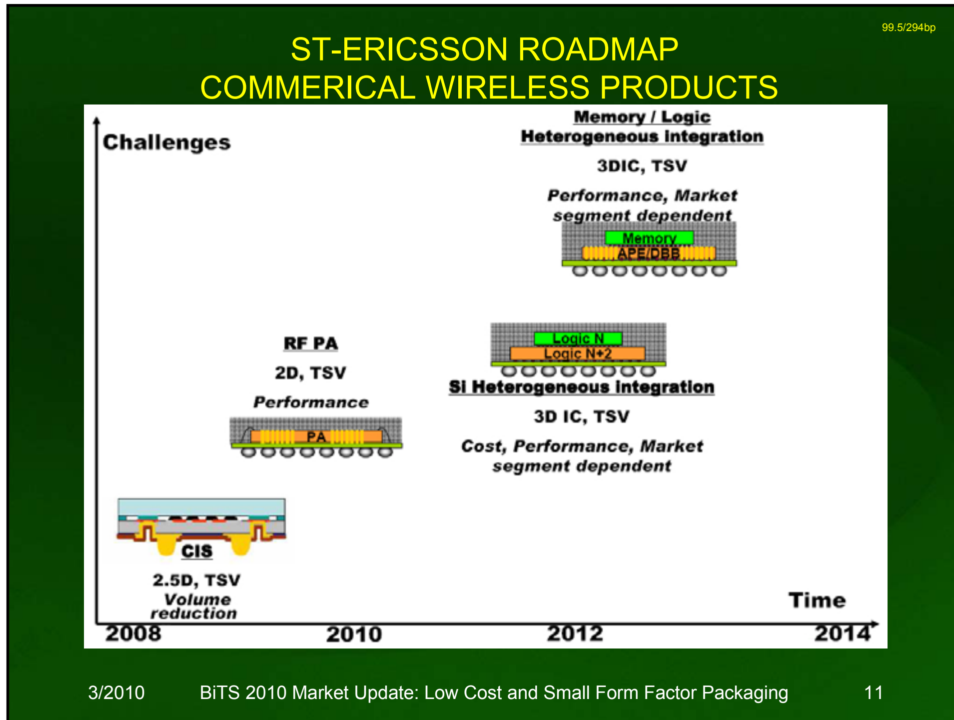

210.1/141bp

COPPER WIRE BONDING DRIVING FORCES

- Lower cost metal
  - Most attractive for thick gold wire (33µm – 50µm)
  - 90% to 95% material cost savings depending on diameter
- Higher thermal and electrical conductivity
- Other driving forces
  - Stiffer wire/less wire sweep for longer bonds with thin diameter wire
  - Higher current capability
  - Can use existing wire bonders with conversion kits

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COPPER WIRE ENABLES LOWER COST

Leadframe and CSP Examples

- No argument that copper wire is lower cost than gold wire. Two example products and differences between copper and gold wire are shown below:

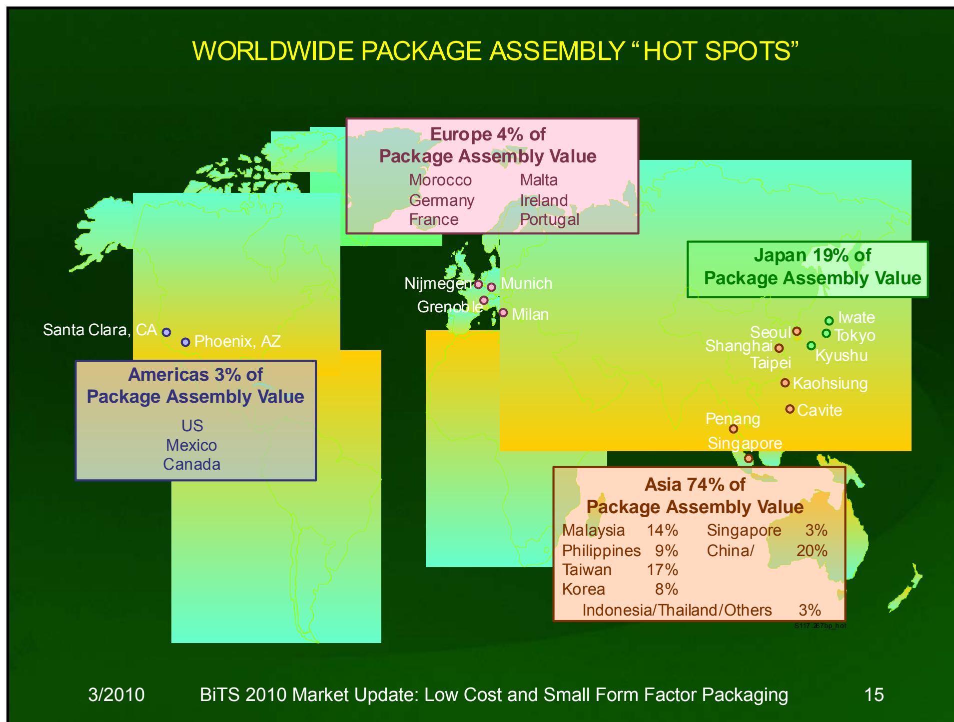
SO-14 (33µm wire)		
	Cu Wire	Au Wire
Wire Cost	0.1¢	1¢
Wire Bonding Cost	0.6¢	0.5¢
Other Package Costs	1.1¢	1.1¢
Total Cost (not price)	1.8¢	2.6¢
Total Savings: 0.8¢ or 30%		

350 FBGA (20µm wire)		
	Cu Wire	Au Wire
Wire Cost	3¢	13¢
Wire Bonding Cost	17¢	15¢
Other Package Costs	37¢	37¢
Total Cost (not price)	57¢	65¢
Total Savings: 8¢ or 12%		

- Savings with copper wire as a percent of package are more pronounced with thicker wire, not more wires.
- Concerns with yield are less noticed with low I/O, low-value devices.

COPPER WIRE BOND STATUS

- In 2009, copper represented 4% to 5% of all bonding wire by length, up from < 1% in 2006
- This is expected to reach 15% or more by 2014
- Driving applications are power discretes (i.e., power transistors, rectifiers, thyristors), “power/logic mixed signal devices”, and now logic and memory
- Justification
  - Lower cost than thick gold
  - Faster bonding than aluminum
  - Possibility to do corners easily (unlike aluminum)
  - Possibility to place function under pads (unlike aluminum)
- However, copper wire may be slow to penetrate mainstream IC market as the following items are addressed:
  - Yield parity with gold
  - Establish comprehensive reliability database
  - Pad structure compatibility
  - Qualification risk and expense mitigated



CONCLUSIONS

- Semiconductor companies always searching for cost reduction strategies
- Various approaches can and have been applied
  - Copper vs. Gold wire, Lower cost EMC, laminate, etc
  - Smaller packages such as QFN/DFN, tight pitch FBGA, and WL-CSP as bare die
  - Outsourcing and Regional Shifts – Asia already dominates, but continued growth in China, India, Philippines and Vietnam
  - Efficiency Improvements (throughput, strip test, etc) are never sufficient
- 3D/TSV approaches are still searching for cost effective test
  - Pitches approach 50um
  - Test before die to die or die to wafer assembly often required

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