BiTS Burn-in & Test Socket Workshop 2010 **Invited Speaker**

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RISING TO THE 3D TSV TEST CHALLENGE: WILL YOU BE READY?

by

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ABSTRACT

3D integration is not a novel concept. Veterans in the industry will tell you it's been around for 20 years. In fact many 3D integration configurations, such as package-on-package (PoP) configurations, stacked die interconnected with wirebond or flip chip, and other 3D wafer-level packaging (WLP) technologies that utilize the existing WLP supply chain such as fan-out WLP, Freescale's redistributed chip package (RCP), and Infineon's eWLB; are already being manufactured in volume. While these configurations have most assuredly posed challenges to the test community, the technology proving to be most elusive is naturally the newest kid on the block: 3D ICs stacked using through silicon via (TSV) interconnects.

However, while test solutions are high on the list of limitations yet to be overcome, experts agree that such deficiencies won't slow down market adoption of 3D TSVs, and that when the time comes, solutions will be available. Indeed, one giant step towards assuring this is communication between the manufacturing and test communities, and in turn, an increased awareness in the test community of what the challenges are, and what issues they'll be asked to solve.

As such, this talk will offer a brief overview of the 3D roadmap, the technology benefits of 3D TSV adoption, the test obstacles TSV stacking presents, R&D efforts addressing these solutions thus far, alternatives being suggested, and other information to help you decide if your company should take up the gauntlet.

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Rising to the 3D TSV Test Challenge: Will You be Ready?

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2010 BiTS Workshop
March 7 - 10, 2010

Agenda

- How I became Queen of 3D
- Defining 3D
- 3D Roadmaps
- 3D TSV: the new kid on the block
- The role of test in 3D TSVs

Queen of 3D?

Who says?

Queen of 3D

- Where I got the name
- I'm NOT an engineer
- I'm a JOURNALIST focused on 3D integration and packaging
- Information here gathered at various 3D events, from the true 3D experts.

3D 101: A review

- Basic Truths:
  - 3D has been around for 30 years (Lee Smith at Amkor)
  - 3D integration refers to architecture.
  - TSV alone is NOT 3D – it ENABLES 3D.

3D 101: A review

- Why 3D?
  - Performance
  - Form factor
  - Cost benefits
  - Board real estate
  - Wafer real estate

3D 101: A review

- 3D Packaging vs. 3D Silicon
  - 3D Packaging already in volume production
  - 3D silicon – TSV and non-TSV approaches
- 3D comes in many varieties
  - 3D PoP
  - 3D SiP
  - 3D WLP
  - 3D ICs
  - 3D SICs

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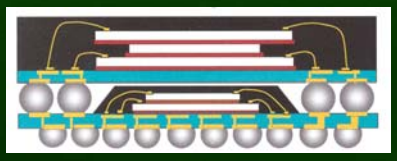
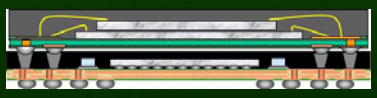
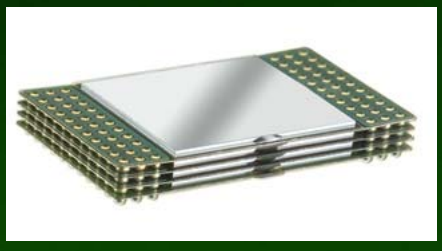
3D Packaging Examples



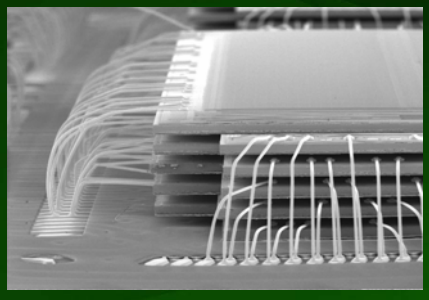
Traditional PoP



TMV PoP Source: Amkor



µPILR-Memory_PoP-Stack Source: Tessera



Wire bond die stacks Source: STMicro

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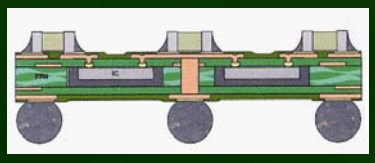
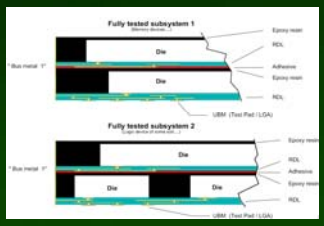
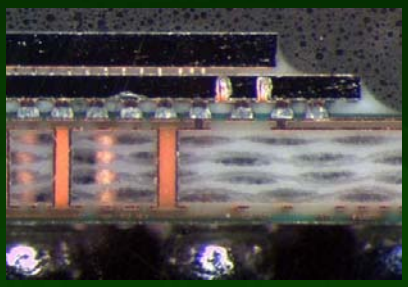
3D WLP Modules



Embedded die – RF module Source: Imbera



WF DOD Source; 3D plus



3D eEWLB Source: ST Ericsson

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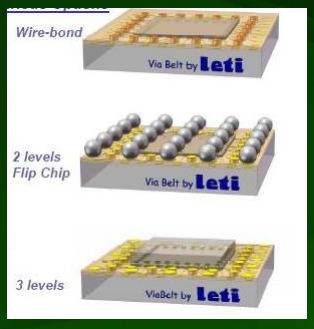
3D NON TSV Stacks

Edge connection Source: Vertical Circuits

In Production



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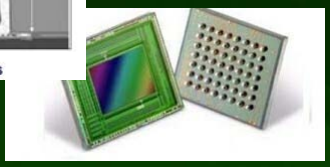
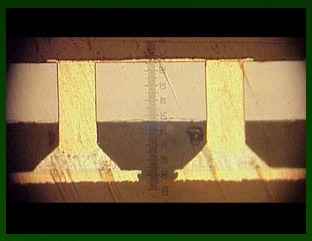
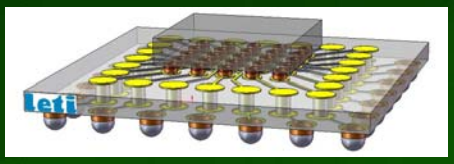
2.5D TSV Applications

CMOS image Sensors





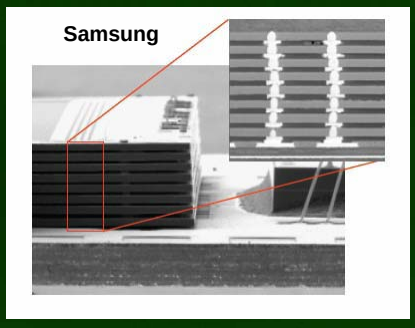
Silicon Interposers



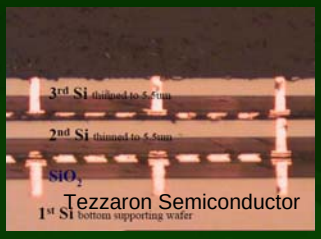
Source: ALLVIA

Source: Leti

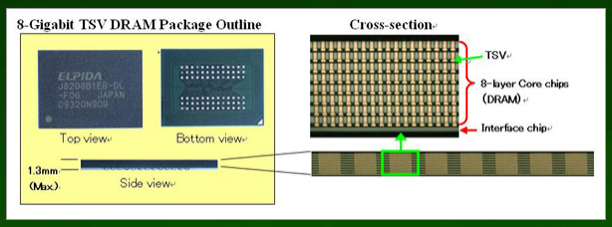
3D TSV Stacks



3D Memory Stacks



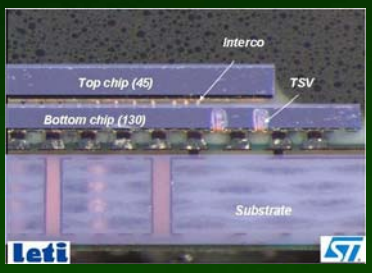
Tezzaron Semiconductor



3D Heterogeneous Demonstrators

• IMEC DRAM on logic demonstrator (2009)

Source: IMEC



Leti 45nm chip on 130nm chip

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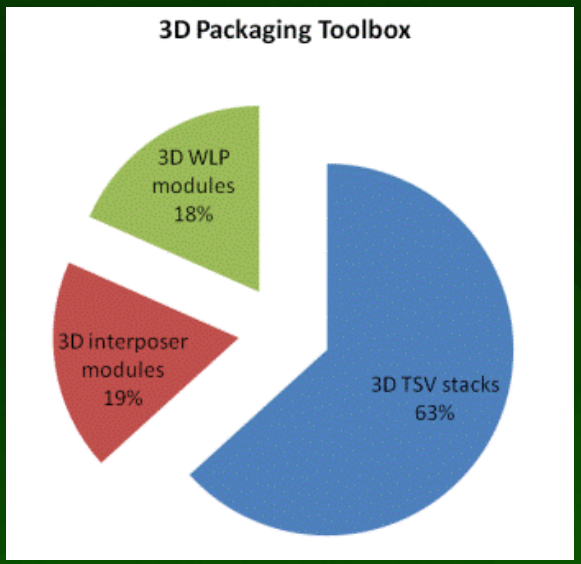
3D Roadmaps

According to Yole Developpment, How things will look by 2013.

Despite a worldwide economic recession, the R&D activity linked to 3D companies has reached "unprecedented levels."



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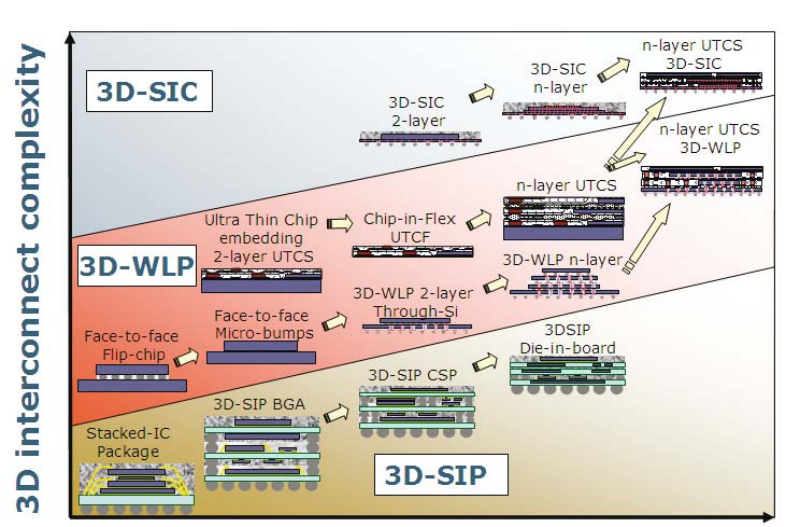
3D Roadmaps



IMEC's roadmap for 3D technology

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Limitations to TSV Adoption

The experts agree, while there are variations, these three issues still stand out:

- **Design Tools are still lacking**
  - **Progress is well underway here**
- **Thermal solutions must be developed**
  - **Not a show stopper – and some see thermal advantages to TSVs**
- **Test issues must be addressed and resolved**

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Test: The TSV Black Hole

- If there's work being done in the test community, not much information is being circulated to the manufacturing community
- Current test methodologies won't work with TSV stacks
  - Contact testing (probe cards) damage TSV wafers
  - Probing doesn't scale
- Known Good Die or at least Pretty Good Die are needed for suitable yields.
- Do we test each strata or the whole stack?

Test: The TSV Black Hole

- New processes mean new defects to be tested for.
- Thin wafers and pads on both sides will need testing
- Current probe technolgies are not effective on tight-pitch TSVs (5-10 micron)

Will We Be Ready?

Al Crouch says NO!

"For electronic greeting cards, maybe, but for high end applications, test and quality concerns are high and product introductions and lifetimes are short."

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TSV Test Solutions

- New Test Flow
  - Test both before and after bond
- Built in self test (BIST)
- Repair and Redundancy
- Clean partitioning
- Scan to edge
- Design for Test solutions
- Use iJTAG to permit testing TO the TSV interface before assembly

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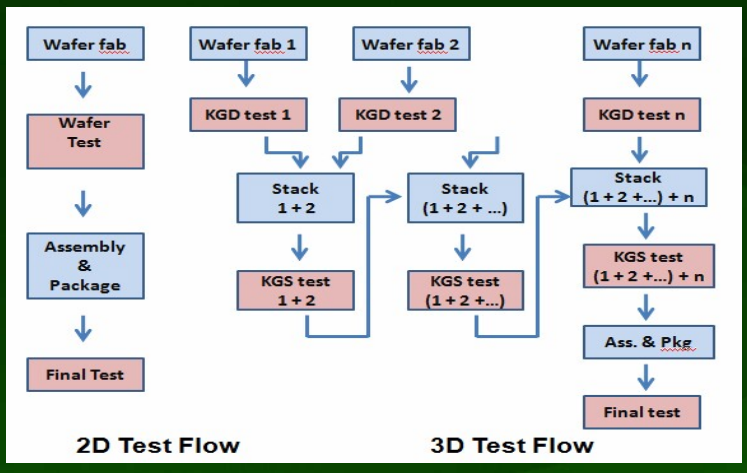
Tezzaron's Bi-Star

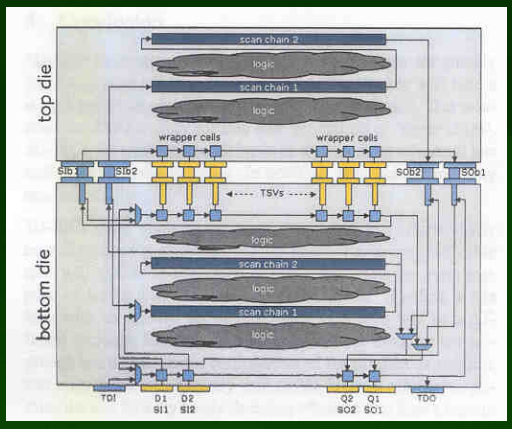
- Improves yield of highly parallel structures such as memory
- Basis: integration of intelligent self test, self repair
- Performs greater level of testing than normally available during normal chip or wafer level testing
- Bi-STAR™tests and compares >300,000 nodes or bits/clock cycle; more than 1,000 times faster than can be achieved by any external memory tester

2D vs 3D Test Flow



Sources: Erik Jan Marinssen of IMEC via P. Garrou, Perspectives from the Leading Edge

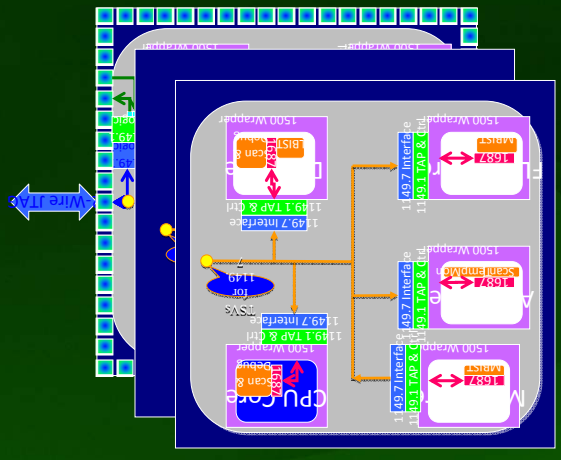
2D vs 3D Test Flow



Sources: Erik Jan Marinssen of IMEC via
P. Garrou, Perspectives from the Leading Edge

Embedded Solution

The block diagram shown here shows how the 1149.7 and P1687 standards could be implemented in a 3D chip package. (Source: ASSET's ScanWorks platform)



Summary

•3D Integration comes in many flavors. One is right for you.
•TEST is an area of critical concern that must be addressed.
•The community has been made aware, and the rumblings of activity can be heard
• 3D spells opportunity for those tenacious enough to pick up the gauntlet.

References

P. Garrou, Ph.D; 3D IC Integration: Status and Overview.; proc. 3-D Architectures for Semiconductor Integration and Packaging Burlingame CA; DEC 2009; *3-D IC Test, Perspectives from the Leading Edge,* December 8, 2009; http://www.semiconductor.net/blog/Perspectives_From_the_Leading_Edge/29137-3_D_IC_Test.php

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P. Franzon, Ph.D.; Creating 3D Specific Systems: A 10 Step Program; proc. 3-D Architectures for Semiconductor Integration and Packaging Burlingame CA; DEC 2009

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