ARCHIVE 2009

WHAT'S THAT THING UNDER MY SOCKET?

by

Tom Bresnan
Sales Manager
R&D Circuits

ABSTRACT

That 'thing' under your socket is a Printed Circuit Board (PCB) – a critical part of your packaged test and/or burn-in solution. This tutorial's scope offers attendees an across the board examination of those Printed Circuit Boards sitting under your socket. The focus is on learning about the attributes, materials and processes required to produce the PCB's used as test interface boards. In 'bringing the Printed Circuit Board shop to the tutorial hall', a better understanding of the challenges you and your PCB vendors face is attained.

A brief history of the PCB or PWB (Printed Circuit/Wiring Board) industry is covered, specifically in relation to the ATE industry. Next detailed discussions on pitch, layer count, board thickness and via drill hole diameter (to name but a few of the critical attributes of today's interface boards) on manufacturability and cost is explored. Additionally, the many options currently available for materials, and how those options may be shrinking (as is device pitch!) are examined.

That is followed by a detailed explanation of the PWB manufacturing process - from raw materials through finished product, including new visual aids and a hands-on exhibit of a PWB in all its process stages.

Last, but certainly not least, the quality and performance characteristics you can demand of your supplier(s) are analyzed. Even with today's boards becoming more crowded (with components) and pitch and pin counts driving attributes ever smaller, there are ways to verify and validate the quality of your interface boards with your suppliers. You'll learn how, with samples of data gathered over years of process development, characterization and verification.

BiTS 2009 — Burn-in & Test Socket Workshop

Tutorial 2

Who should have attended this tutorial?

Test Engineers & technicians (and others) who want more detailed knowledge of just what a printed circuit board is (and isn't) will find this an excellent tutorial on Printed Circuit Board design and manufacturing. This is a rare opportunity where attendees, whose work in the test and burn-in arena would benefit from a deeper understanding of Printed Circuit Board technology, can participate in a concentrated tutorial covering such a key topic area, and come away with a new-found understanding of PCB technology capabilities and limitations.

What's That Thing Under My Socket?

…and how is it made?

Tom Bresnan
Sales Manager, R&D Circuits

2009 BiTS Workshop Tutorial
March 8 - 11, 2009

March 8, 2009

- Born on this date
  - Oliver Wendell Holmes – SC Justice – 1841
  - Mickey Dolenz – 1945
  - Jim Rice – Boston Red Sox – 1953
  - Gary Numan – Cars – 1958
  - Jason Elam – NFL kicker – 1970
  - Nanette Pearson – Miss America – 1996

March 8, 2009

- Died on this date
  - – Nat Gordon – “last pirate”? – 1862
  - – Millard Fillmore – 13^{th} President – 1874
  - – William Howard Taft – 27^{th} President – 1930
  - – John F. Bothwell – Freckles – Our Gang – 1967

March 8, 2009

- Dog licenses become law in NY – 1894
- IRS begins ‘operations’ – 1913
- Pan Am begins operations – 1927
- International Women’s Day – 1945
- Groucho, Chico, Harpo – 1957
- Casey Stengel – HOF induction – 1966
- Goodyear Blimp – first flight – 1972

What you came here for…

- A little history of PWB's
  - The evolution
  - The marketplace
- The Attributes
- Materials and more
- The Process
- Manufacturing Challenges
- Process Verification

Printed Circuit Boards

- A PWB consists of a non-conducting substrate (typically woven fiberglass with epoxy resin) upon which a conductive pattern or circuitry is formed.
- Wikipedia…A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, on a non-conductive substrate.

Some evolution info.

- 1950's
  - Patent 2,756,485 July 31, 1956 (process of assembling electrical circuits)
  - Single-sided circuitry
- 1960's – 1970's
  - Double-sided circuitry

Some more evolution info.

- 1980's
  - Multilayers and surface mount
- 1990's
  - Double-sided assembly

Marketplace

- 2007
  - US$50B
- 2012
  - US$76B
- US Market in 2007
  - US$13B
- ATE
  - US$.5B to US$1B (difficult to estimate)

What's in a name?

- PCB
- PWB
- DUT board, DIB, PIB, Load board, ATE board
- Interface Board
  - Between Device Under Test and Tester

Attributes

- Pitch
  - Device, line, space, hole to copper
- Layers
  - rows
- Hole Diameter
  - Function of device pitch
- Aspect Ratio
  - Ratio of thickness to hole diameter

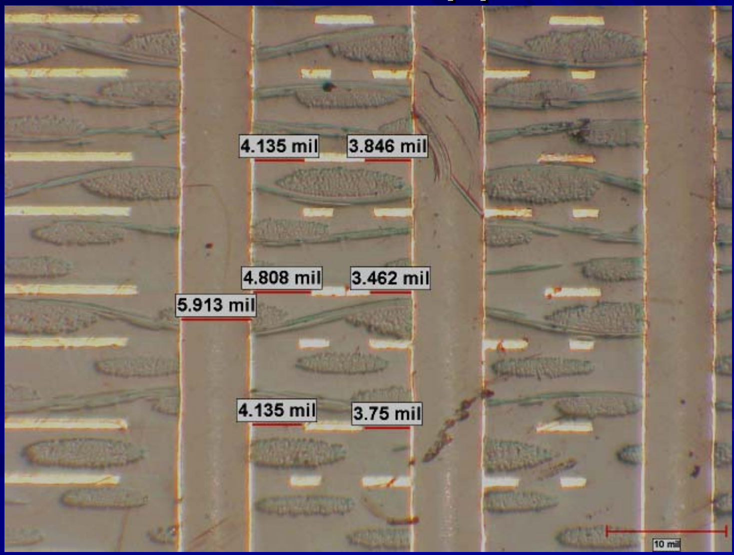
Attributes - Pitch

- Device Pitch
  - 1.0mm, 0.8mm, 0.5mm, 0.4mm ….
  - Translates to other attributes
    - Line width
    - Spacing
    - Dielectric spacing
    - Hole to copper feature dimensions

Pitch Translation

	1.0mm	0.8mm	0.5mm	0.4mm
Pad	0.76mm	0.66mm	0.35mm	0.3mm
Hole	0.37mm	0.3mm	0.15mm	0.1mm
Line	0.2mm	0.2/0.12	0.2/0.08	0.2/0.07
Hole2Cu	0.25mm	0.18mm	0.12mm	0.1mm
A/R	Low	Med.	High	Extreme

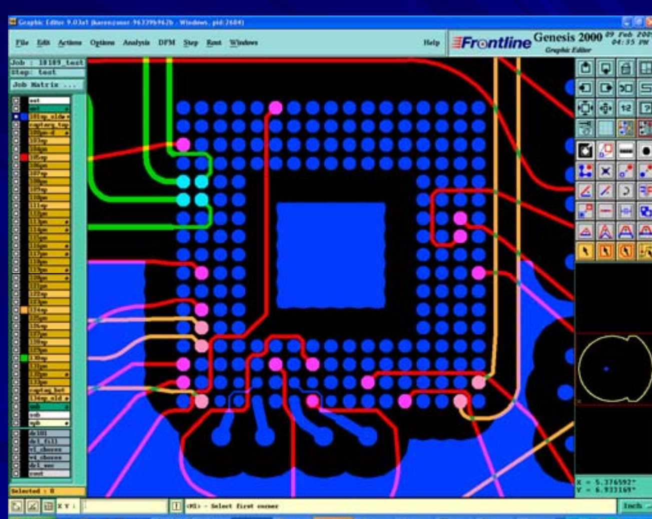
Hole to Copper



Attributes - Layers

- Rows = Signal Layers
- Signal Layers need ground planes
  - – Impedance control
- Additional routing layers

Rows = Layers



Attributes – Hole Diameter

- Drill / Hole diameter
- Human hair
  - 0.04 to 0.25mm
- 0.1mm ‘average’

Attributes – Aspect Ratio

- 1.0mm
  - 13:1
- 0.8mm
  - 16:1
- 0.5mm
  - 31:1
- 0.4mm
  - 47:1

Materials & More

- Wikipedia…A printed circuit board, or PCB, is used to mechanically support and electrically connect electronic components using conductive pathways, on a non-conductive ***substrate***.

Materials & More

- Laminate
  - Pre-preg
    - Glass cloth (woven)
    - Resin
  - Copper foil
    - Electrodeposited (ED)
      - 1 ounce per square foot (305g/M^2) (35 microns thick)
      - ½ ounce per square foot (153g/M^2) (17 microns thick)
      - ¼ ounce per square foot (80g/M^2) (9 microns thick)

Materials

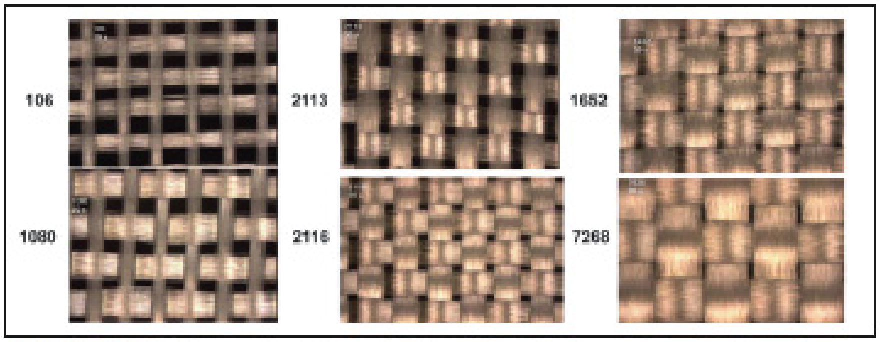
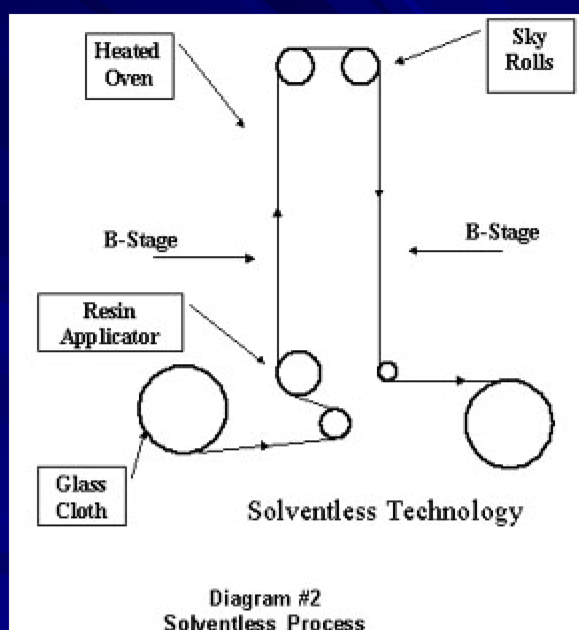


FIGURE 4. Different styles of glass laminate weaves. Photos courtesy of the isola group.



Laminates

- Fr-4
- Enhanced Fr-4's
- HF laminates
- Teflon
- Hybrids

Glass Styles

Style	Glass Dia.	Yarn Ct.	Yarn Pitch
106	1.4	56x56	17.9x17.9
1080	2.3	60x40	16.7x21.3
2113	2.9	60x56	16.7x17.9
2116	3.8	60x58	16.7x17.2
7628	6.8	44x32	22.7x31.3

Constructions

Thickness	Tolerance	Construction	Resin Content	E_r @ 1 MHz	E_r @ 10 GHz
0.008	0.001	1 7628	44.4%	4.55	4.12
0.008	0.001	2 2116	43.0%	4.54	4.11
0.008	0.001	1 2116 1 2113	48.6%	4.36	4.02
0.008	0.001	1 7629	42.6%	4.38	4.12

Constructions

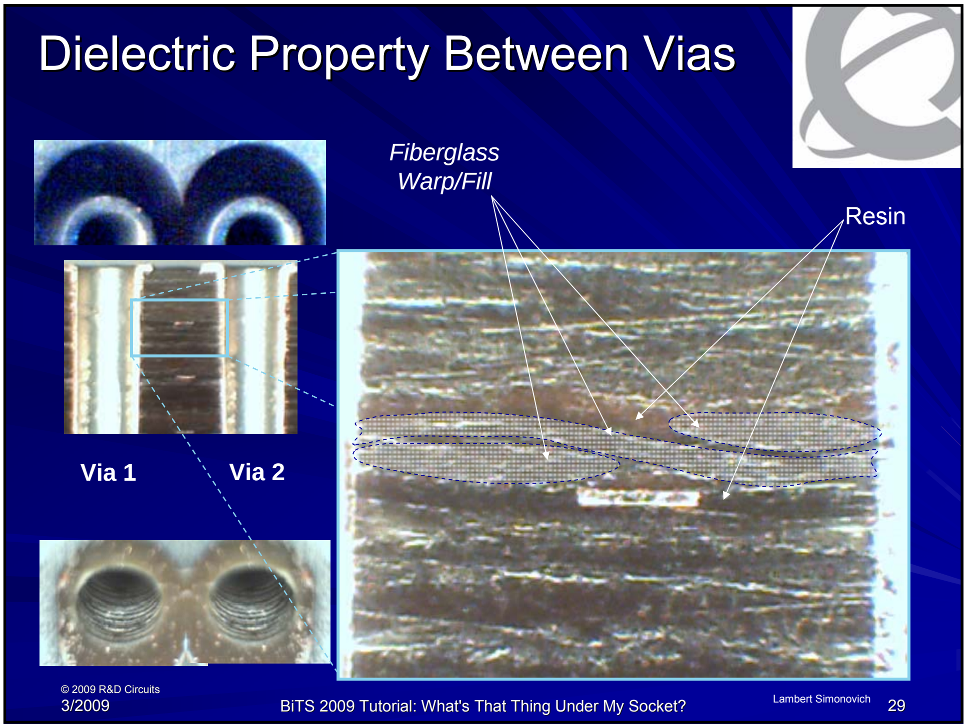
- Know what you're getting
- Understand the implications
- Electrically insignificant?
- Mechanically significant

Material Properties

- Mechanical & Thermal
  - Peel strength
  - X-Y CTE
  - Z CTE
  - T_g
    - DSC
    - TMA
    - DMA

Material Properties

- Electrical
  - Dielectric Constant or
  - ε_r (or relative permittivity)
    - The dielectric constant is a ratio of the capacitance of a capacitor in which a particular insulating material is the dielectric, to the capacitance of the capacitor in which a vacuum is the dielectric.
  - Effective Permittivity


Dielectric Property Between Vias
Fiberglass
Warp/Fill
Resin
Via 1
Via 2
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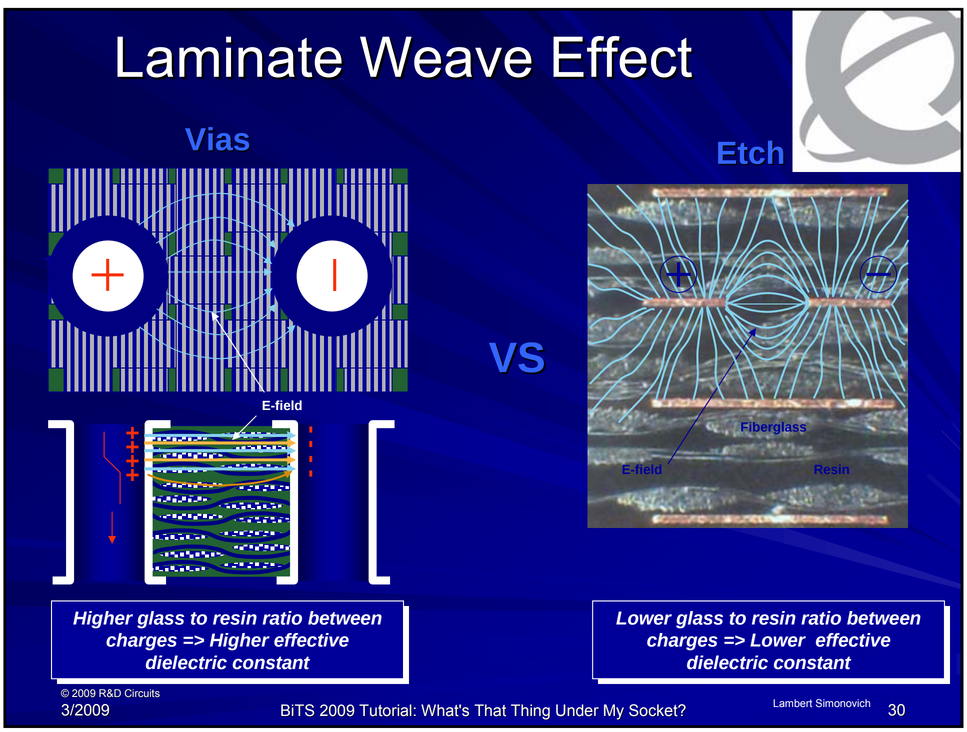
Laminate Weave Effect
Vias
Etch
VS
E-field
Fiberglass
E-field
Resin
Higher glass to resin ratio between charges => Higher effective dielectric constant
Lower glass to resin ratio between charges => Lower effective dielectric constant
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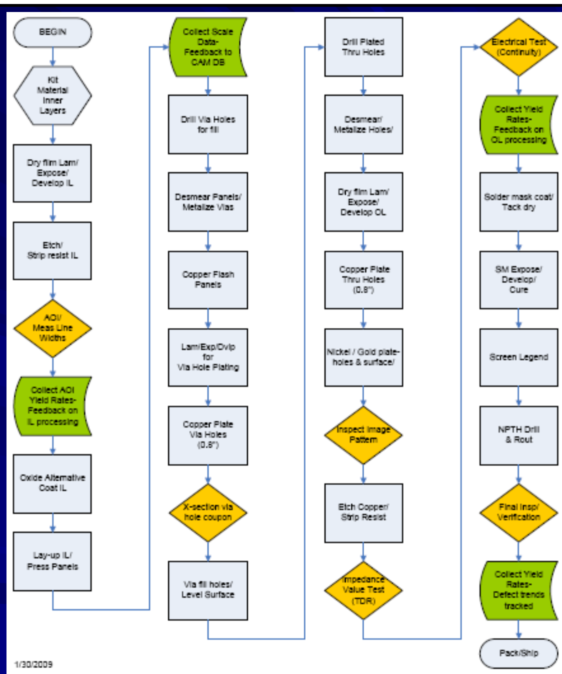
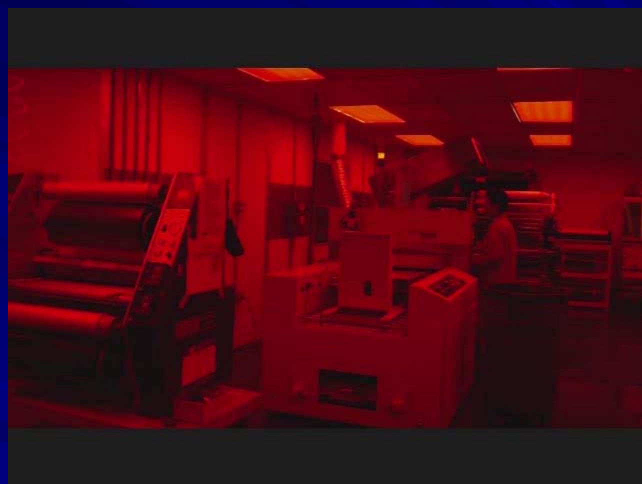


Inner Layer Imaging

- Photo-resist application
- UV Exposure
  - Film and collimated light
  - LDI or Laser Direct Imaging
    - Polymerizes photo-resist
  - Develop
    - Removal of non-polymerized resist

Inner Layer Imaging



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Inner Layer Imaging

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Inner Layer Etch

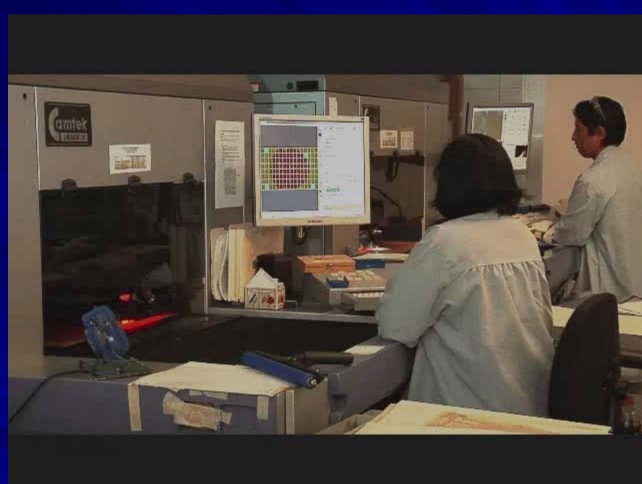
- Remove base copper
  - Non-polymerized area
  - Various chemistries available
    - Ammonia based
    - Cupric chloride based
- Resist removal (stripping)

Inner Layer Etch

AOI

- Post-Etch Punch
  – Registers all layers to optical targets
- Automated Optical Inspection
  – Data download from CAM
  – Core layer scanned
  – Compared to CAM data
  – Verification

AOI



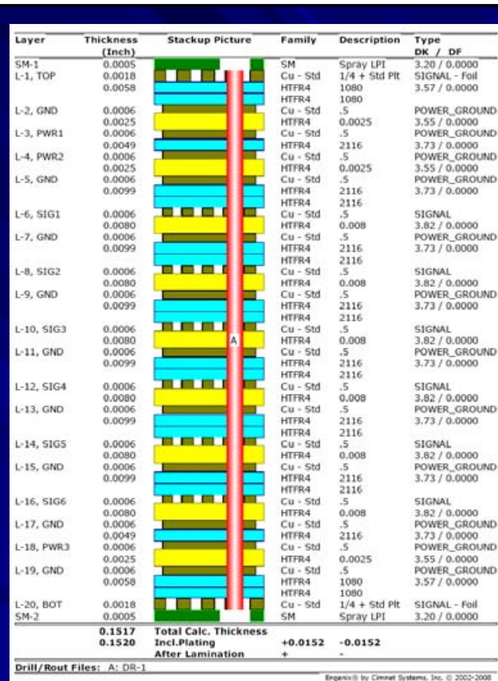
Oxide Treatment

- Copper Surface Preparation
- Adhesion promoter
  - Added bond strength
- Reduced Oxide
  - Pink ring elimination
- Alternative Oxide
  - Variety of materials
  - Multiple or sequential laminations

Layup and Lamination

- Registration and stacking of cores
- Combines cores, pre-preg, Cu foil
- Pin lamination
  - Registration or layer to layer alignment
- Vacuum chamber
- Heat, pressure, time
- Controlled process window

- Stack up



Layer	Thickness (Inch)	Stackup Picture	Family	Description	Type DK / DF
SM-1	0.0005		SM	Spray LPI	3.20 / 0.0000
L-1, TOP	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-2, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-3, PWR1	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-4, PWR2	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-5, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-6, SIG1	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-7, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-8, SIG2	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-9, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-10, SIG3	0.0006		Cu - Std	.5	SIGNAL
	0.0080	A	HTFR4	0.008	3.82 / 0.0000
L-11, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-12, SIG4	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-13, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-14, SIG5	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-15, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0099		HTFR4	2116	3.73 / 0.0000
			HTFR4	2116	
L-16, SIG6	0.0006		Cu - Std	.5	SIGNAL
	0.0080		HTFR4	0.008	3.82 / 0.0000
L-17, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0049		HTFR4	2116	3.73 / 0.0000
L-18, PWR3	0.0006		Cu - Std	.5	POWER_GROUND
	0.0025		HTFR4	0.0025	3.55 / 0.0000
L-19, GND	0.0006		Cu - Std	.5	POWER_GROUND
	0.0058		HTFR4	1080	3.57 / 0.0000
			HTFR4	1080	
L-20, BOT	0.0018		Cu - Std	1/4 + Std Plt	SIGNAL - Foil
SM-2	0.0005		SM	Spray LPI	3.20 / 0.0000
	0.1517	**Total Calc. Thickness**			
	0.1520	**Incl.Plating**	**+0.0152**	**-0.0152**	
		After Lamination	**+**	**-**	

Drill/Rout Files: A: DR-1

Drill

- X-ray panel inspection
  - Scale and skew
  - Every panel, every layer
- Database capture
  - History and future use

Drill

- Mechanical hole formation
  - 0.1mm
- Opto-mechanical positioning
  - Glass scales
- Real-time analysis
  - Diameter
  - Run-out
  - Broken bit
- Stub Drilling (back-drilling)

Drill

- Tool Capacity – 250
- Positioning Speed – 1,180 IPM
- Feed Rate – 4-500 IPM
- Retract Rate – 4-1,000 IPM
- Positioning Feedback - .0005mm (.00002”)
  - Glass scale
- Positioning Accuracy +/-.005mm (.0002”)
- Spindle Speed – 15,000 to 125,000 RPM

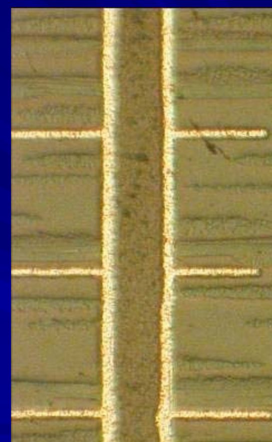
Drill

Drill

- Laser hole formation
  - Microvia's
    - Down to 25 micron
- Opto-mechanical positioning
- Blind via's
- Buried via's

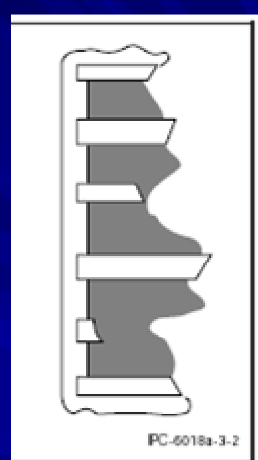
Hole Prep & Copper Plate

- Desmear
  - Removes epoxy smear from interconnects
  - Drilling operations
  - Chemical removal



Hole Prep & Copper Plate

- Etchback
  - Different from desmear
  - Removes epoxy from dielectric space
  - Glass etch
  - Three point connection
  - Some materials resistant to chemical removal

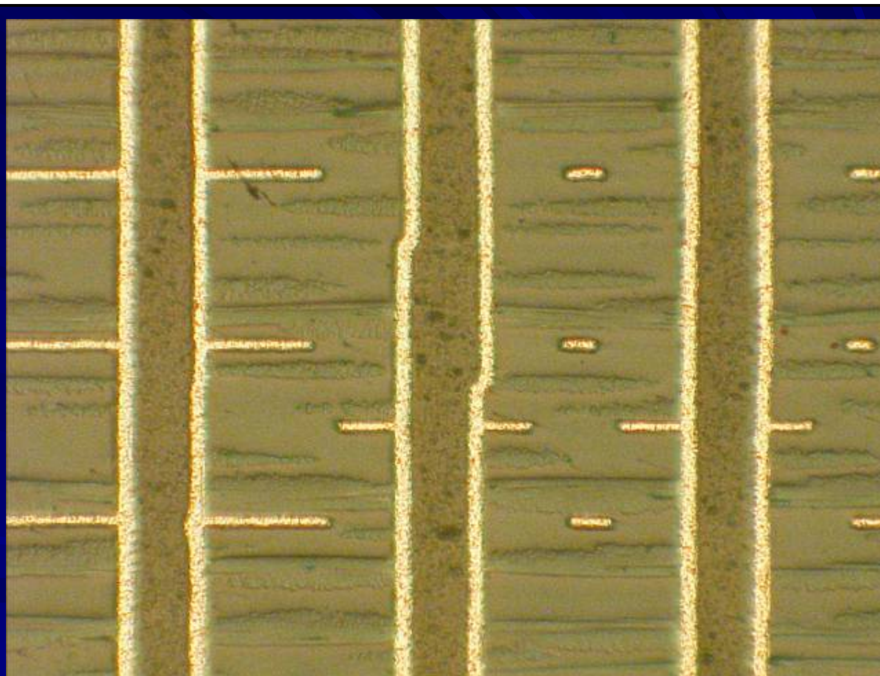


Hole Prep & Copper Plate

- Copper Deposition
- Seed layer
  - Prepares dielectric and interconnects for subsequent plating operations
  - 30-40 µ followed by copper plate
  - 75-125 µ to prep for imaging process
- Unfriendly chemistry
- Inherently unstable

Hole Prep & Copper Plate

- Carbon (Black Hole®)
- Graphite (Shadow®)
- Palladium
- Electroless Nickel (Ultra-Plate®)
- Conductive Polymer
- Non-Formaldehyde-Based Electroless Copper



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Hole Fill

- Fill to create flat surface
  - Need for socket touchdown
- Vacuum assist
- Compressed air
  - Thru system & thru holes
- High aspect ratio
- Blind via's

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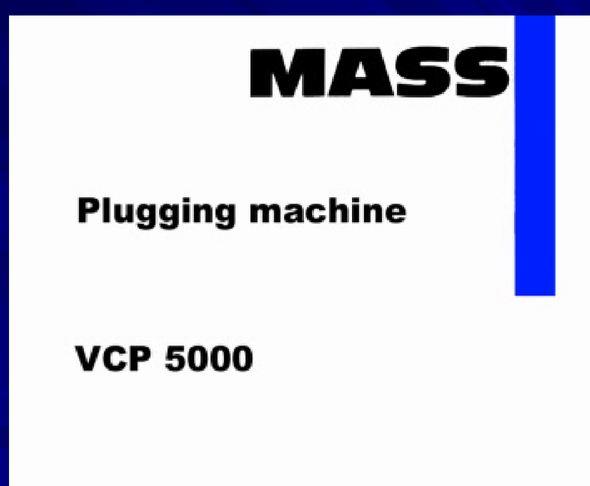
Hole Fill

Hole Fill (2)

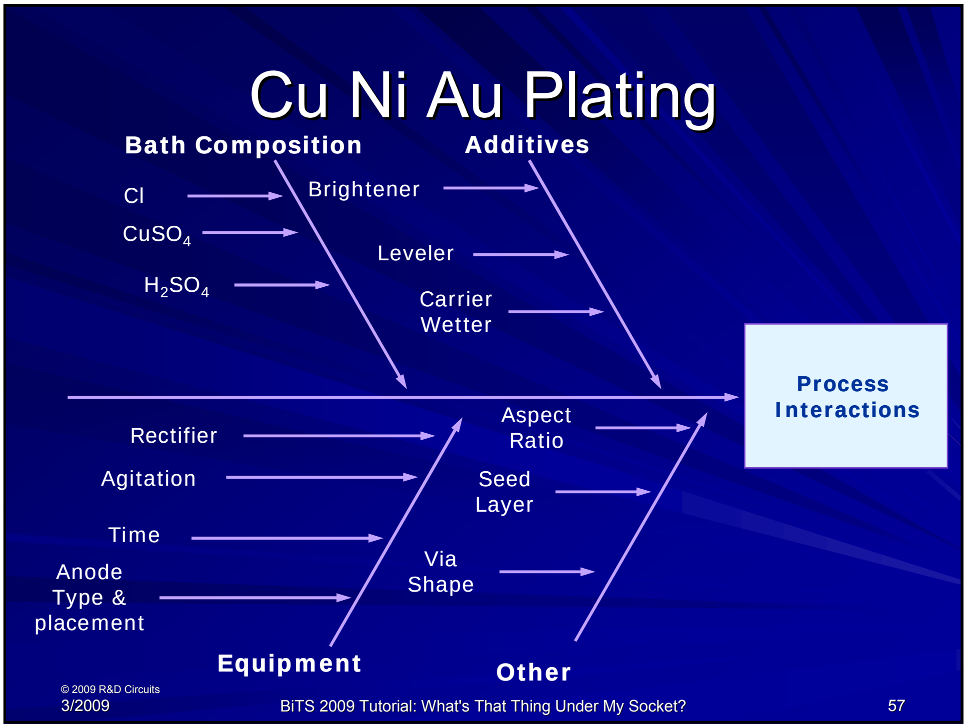


Outer Layer Imaging

- Reversed from inner layer imaging
- Plating resist, not etch resist
- Photo-resist application
- UV Exposure
  - Film and collimated light
  - LDI or Laser Direct Imaging
    - Polymerizes photo-resist
  - Develop
    - Removal of non-polymerized resist

Cu Ni Au Plating

- Electroplating
  - Chemistry (electrolyte solution)
  - Power rectifier
    - Rectifier converts AC to DC
  - Anode (copper)
  - Cathode (PCB panel)


Cu Ni Au Plating
Bath Composition
Additives
Cl
CuSO4
H2SO4
Brightener
Leveler
Carrier Wetter
Process Interactions
Rectifier
Agitation
Time
Anode Type & placement
Aspect Ratio
Seed Layer
Via Shape
Equipment
Other
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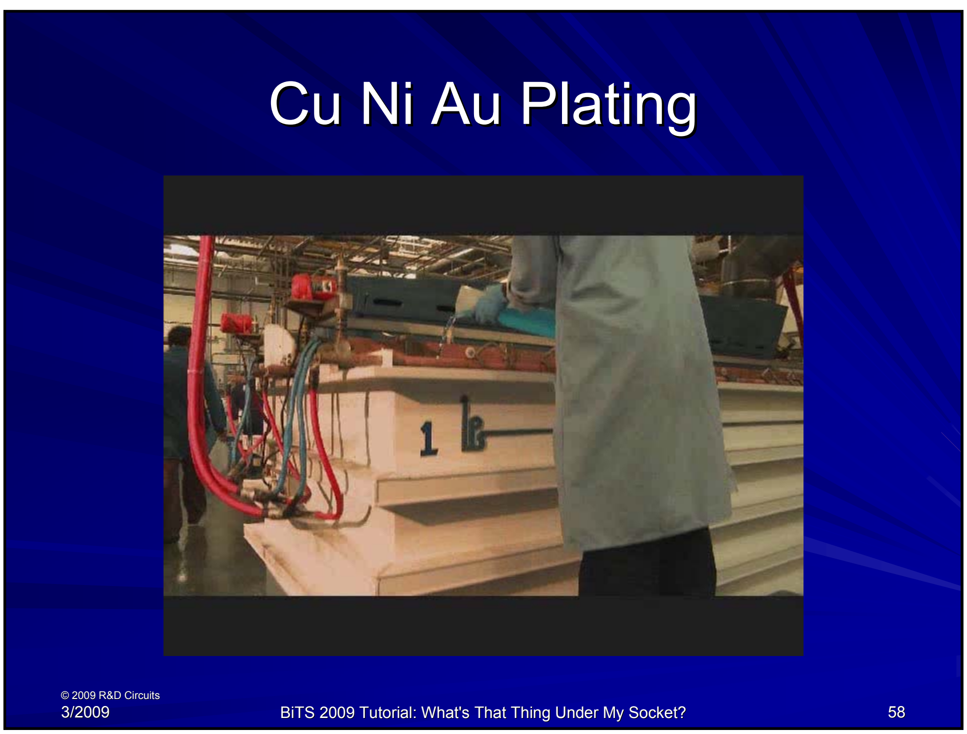
Cu Ni Au Plating
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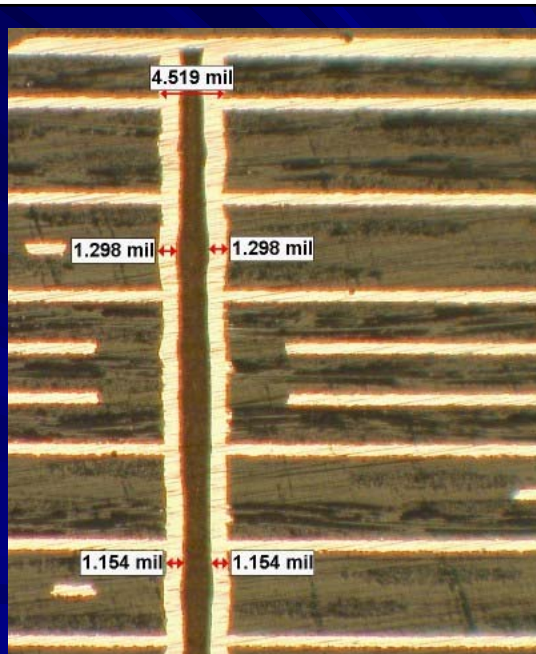
Cu Ni Au Plating

- 1 mil minimum thickness in holes
- Minimize surface buildup
- Aspect ratio
  - Thru holes and / or micro-via's
- Robust and survivable
- Etch Resist

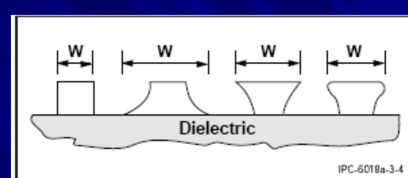


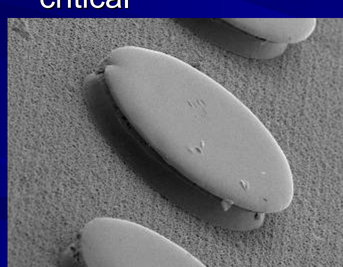
Outer Layer Etch

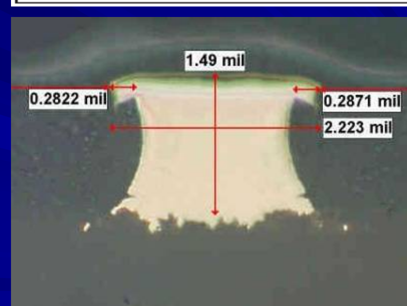
- Define the outer layer(s) pattern
  - Removal of base copper
  - Lines, pads, other features
  - Impedance control
- Nickel / Hard Gold typical ATE finish
- Etch factors and overhang
- Other finishes available

Outer Layer Etch

- Overhang
  - Depends on finish
  - 1:1 thickness
  - Surface thickness critical







Electrical Test

- Direct measurement for first board
- Indirect Measurement all others
  - Isolation and continuity
  - Capacitive or electromagnetic coupling
    - Broken trace = reduced coupling
    - Shorted trace = increased coupling
    - Trace to ground (↑ degree of confidence)
  - Adjacency analysis

Electrical Test

Soldermask

- Epoxy based coating
  - Available in colors and clear
- Surface protection
- Solder resist, as the name implies
- Identification

Soldermask

- Screen-flood
- Liquid Photo-imageable (LPI)
  - Spray coated
  - consistency
- Via Plugging
- Dry Film

Silkscreen

- Assembly nomenclature or legend
- Colors available
- Product identification
- Screen print
- Inkjet

De-panelization

- Routing
- Secondary Drill
- Back / Stub Drill
- Counterbores / countersinks
- Slots

Final Inspection

- Visual and dimensional
  - Cosmetic defects
- Impedance Testing
- Cross sectioning
- Other measurements and certifications

ATE Directions

- New devices?
- New chip manufacturing technology?
  - Flexibility
  - Scalability
  - Performance
  - Support
  - Cost

Manufacturing Challenges

- Flexibility
  - Variety of platforms
  - Range of pin counts
  - Pitch
  - Multi-site
  - Process capabilities

Manufacturing Challenges

- Scalability
  - Manufacturing capability
    - Board to board
    - Lot to lot
  - Multi-site
  - High pin count

Manufacturing Challenges

- Performance
  - Wider range of materials
  - Controlled process
    - Impedance
  - Lot controls

Manufacturing Challenges

- Support
  - Vendor stability
  - Vendor knowledge
  - Vendor process capability

Manufacturing Challenges

- Cost
  - Layer counts (thicker boards)
  - Aspect ratio
  - Line and space requirements
  - Hole to copper dimensions
    - Pitch
  - Reliability

Process Verification

- IST = Interconnect Stress Test
- Determines overall PCB reliability
- Test copper interconnect and materials
- IPC approved Test Method
- Wide industry acceptance

Process Verification

- IST Defined
  - IST = Interconnect Stress Testing
  - Thermal Cycles by Electrically Heating an IST Test Coupon
  - Continuously Measures Resistance of Circuits During Cycle
  - 10% Increase in Resistance is Failure –Test Stops in Seconds

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Process Verification

- IST Process
  - Select and Fabricate a Representative Coupon
  - Prescreen Coupons and Select a Test Sample
  - Precondition – Simulate Assembly & Rework on Tester
  - Test Coupons by Thermal Cycling to Failure (10%)
  - Determine the Exact Failure Location (Thermal Camera)
  - Failure Analysis for the Root Cause and Latent Failure Modes
  - Evaluate Data, Rank Variables, Draw Conclusions

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Process Verification

- IST Coupon – Representative Design
  - Test Vehicle Engineered for Sensitivity
  - Testing Copper Interconnections and Material
  - Finds Barrel Cracks, Interconnect Separation, Delamination

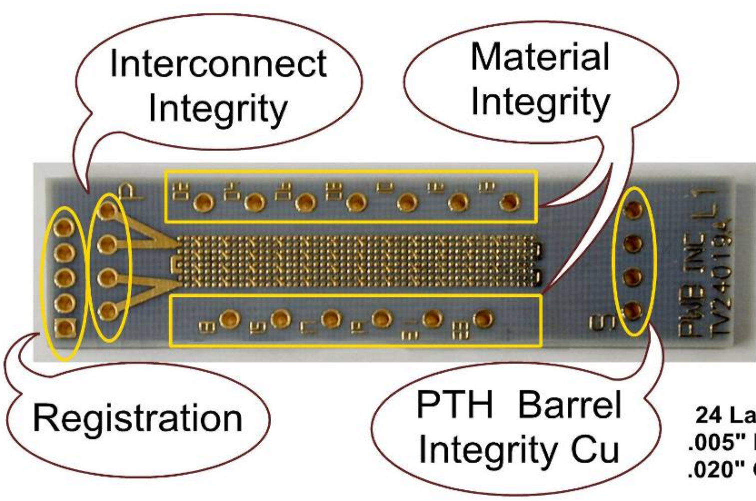
Process Verification

- Hardware - IST Testing Machine
  - Six Individually Controlled Test Heads
  - Automated – Preconditioning and Testing – 5 Minute/Cycle
  - Testing Any Temperature – Ambient to 300°C

Process Verification

- Software
  - Automated Control of Heating and Cooling
  - Continuous Measurements of Environment and Product
  - Automated Report Generation

IST Coupon - TV24019

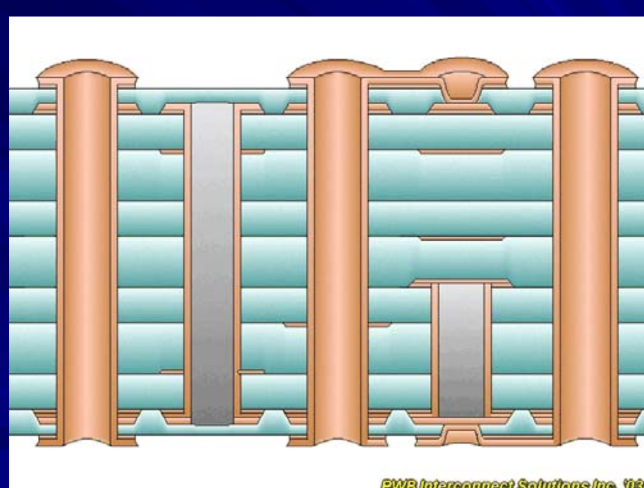


24 Layer
.005" PTH
.020" Grid

Hardware and Software

3/2009 BiTS 2009 Tutorial: What's That Thing Under My Socket? 83

Thermal Cycling – Cross Section Animation



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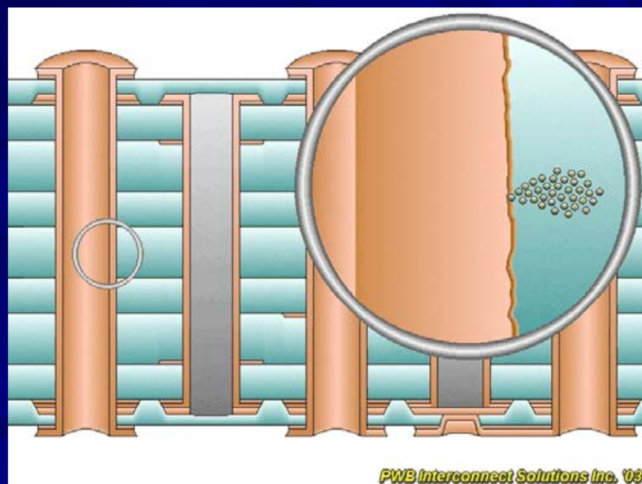
IST Metal Fatigue – Metal Fatigue Animation



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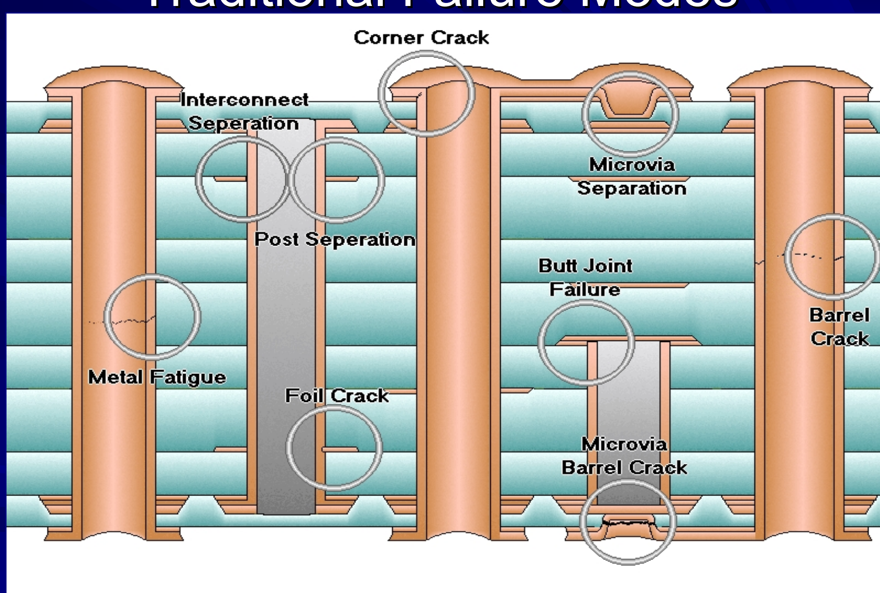
Traditional Failure Modes



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Sample Review

- We have prepared and have available for review, a series of process panels representing each of the process steps we reviewed during today's presentation. We can review and discuss any questions you may have.

R&D Circuits

- Founded in 1969
- Privately Owned & Operated
- ~$16M in Sales, FY08
- Full Turn-Key Supplier
  - Design - Layout
  - Fabrication
  - Assembly
  - Sockets, Contactors, Interconnects

R&D Circuits Locations

- Mesa, AZ – Design Center
- South Plainfield, NJ – PWB Fabrication
- Allentown, PA – PWB Assembly
- Singapore – Sales and Support, Asia