BiTS Burn-in & Test Socket Workshop 2009

Distinguished Speaker

ARCHIVE 2009

BREAKING TRADITIONAL BOUNDARIES - OUR INDUSTRY CHALLENGES AT TEST

by

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ABSTRACT

Success in the semiconductor market is never predictable but it always involves being faster, cheaper or better than your competition. This maxim holds especially true when it comes to microprocessor test. While Moore's Law has spawned a profusion of product features and functions through ever cheaper and abundant transistors, it has left test with increasing complexity and cost. Additionally, market forces necessitate ever-smaller form factors as mobile products become ubiquitous. This combination of shrinking geometry, increasing bandwidth and expanding features creates a confluence of mechanical, electrical and thermal challenges that run head-on into a severely cost constrained environment in the midst of an economic downturn.

Meeting these stringent technical challenges while providing cost effective solutions, requires a collaborative response from the whole industry. Customers and suppliers alike. An outlook on the key technology drivers, leadtime, and total test costs, as well as what can be done between the suppliers and customers, to accelerate improvements beyond normal evolution, will be shared with the audience.

Breaking Traditional Boundaries – OUR Industry Challenges at Test

Navid Shahriari

Director - Sort/Test Technology Development

2009 BiTS Workshop
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Agenda

- *Key Messages*
- *The Environment*
- *Test Challenges*
- *Test Innovations Required*
- *Call To Action*

Key Messages

- Moore's Law is Alive and Well
  - It all comes together at the test interface
- Expect the Rate of Change to Accelerate
  - Business, Electrical, Thermal, and Package Handling
- Cost & Cycle Time Continue to Challenge the Industry
  - We must work together to meet the future needs

Thank You To The Industry

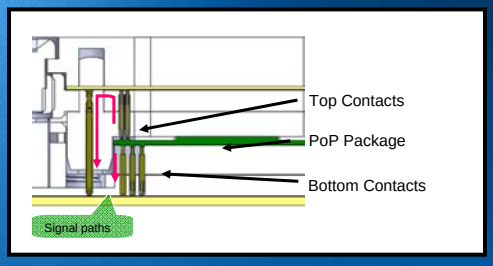
For many years of excellent support. We could not do what we do without you!

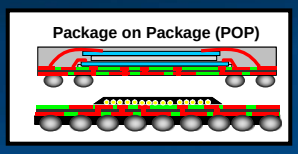
We have relied heavily on many of you to solve our most pressing test interface challenges

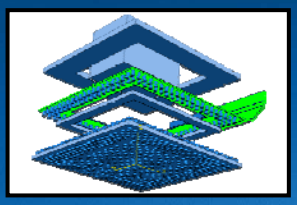
Together, We Have Created Great Solutions

A Couple Of Examples:

Low Cost Test Topside Contact







Good Solutions Starting to Emerge in the Industry

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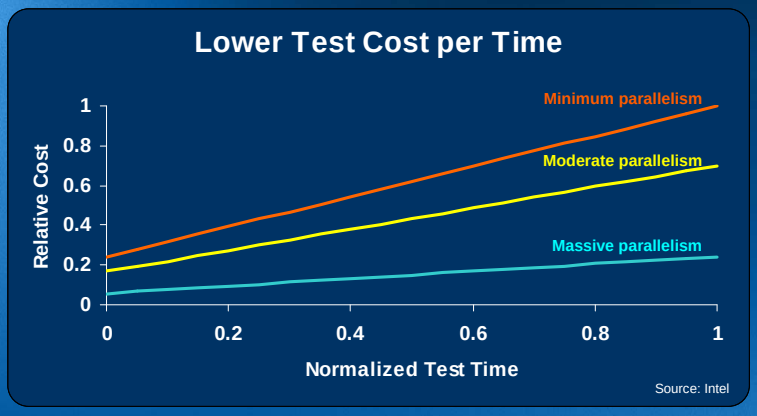
Cost Reduction by Increased Parallelism



Increased Parallelism Drives Lower Test Costs

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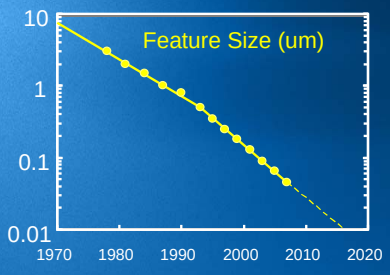
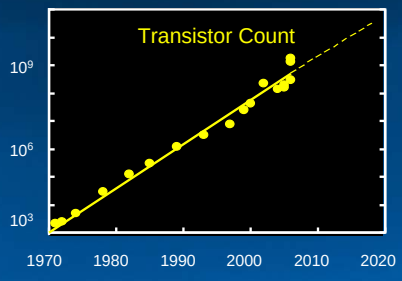
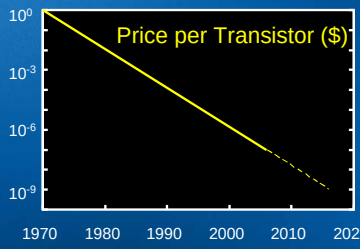
The Environment Continues To Get More Complex

Technology Innovations Continue to Sustain Moore's Law





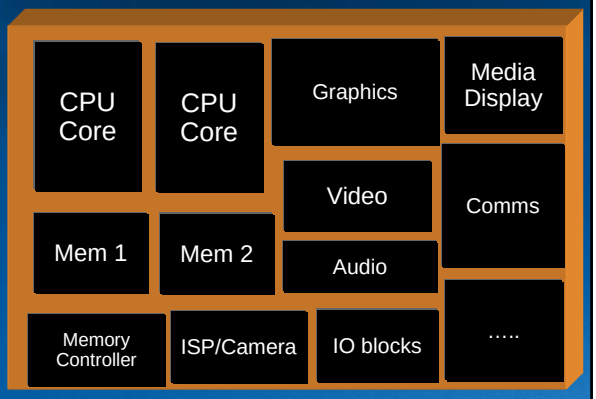


More transistors, increased performance, lower cost

Source: Intel

Growing Complexity In Design

–Advanced CPU
–Multiple heterogeneous programmable cores
–Complex subsystems (e.g., Video, Graphics)
–High bandwidth/ throughput IOs
–Multiple comms



New Levels of HW Integration and Complexity

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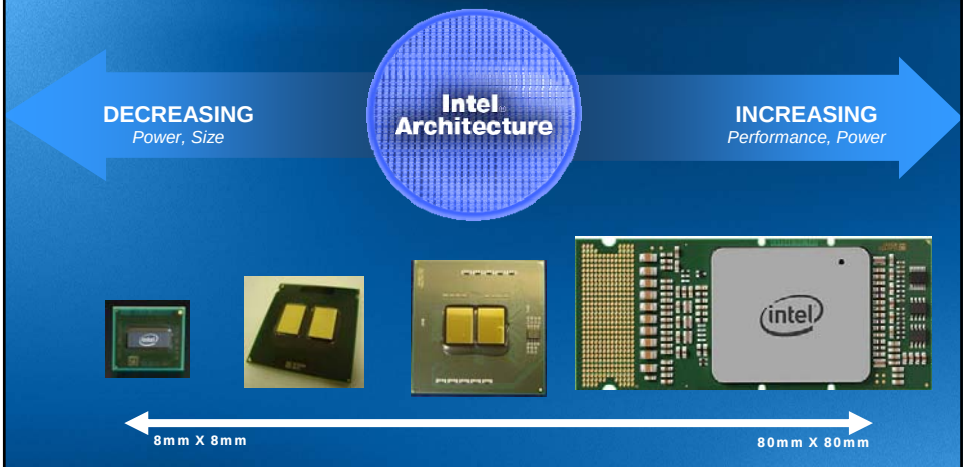
Packaging Multiplies the Challenges at Test



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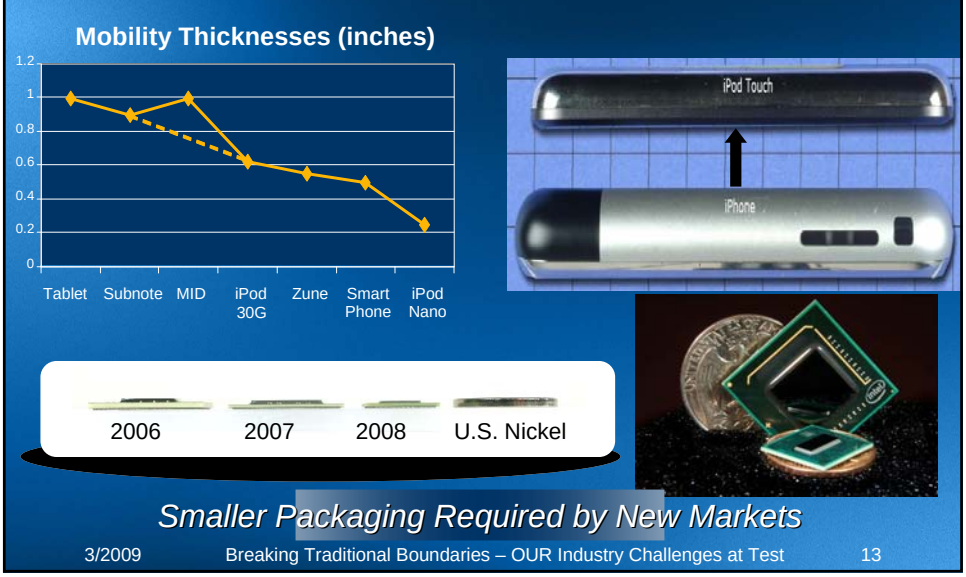
Miniaturization drives Z-reduction



Smaller Packaging Required by New Markets

Cost Pressures Increase

	2008 Avg. Market Price	2012 Avg. Market Price
Desktop PC	$726	$566
Mobile PC	$1,009	$701
Ultra Mobile PC	$1,095	$693
Net Books	$329	$152
Mobile Internet Device	$335	$135

Source IDC & ABI Research

Future Growth Markets Require Lower Cost Structure

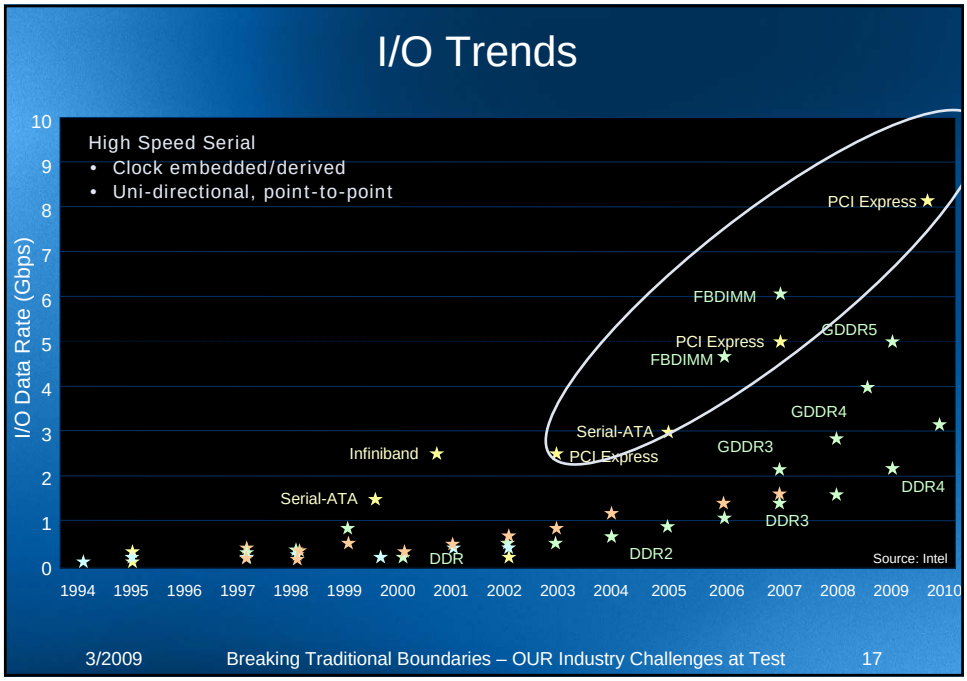
New Customers, New Expectations
1999-2009

Corporate Road Warrior c. 1999
700 MHz
10-15W CPU pwr
9.5M transistors
5-6 lbs
$1849

Classmate PC, 2007
1.6 GHz
<2W CPU pwr
47M transistors
2.8 lbs
$449

Test Challenges Continue To Multiply

Is Industry Innovation Keeping Up?


I/O Trends
High Speed Serial
• Clock embedded/derived
• Uni-directional, point-to-point
I/O Data Rate (Gbps)
PCI Express
FBDIMM
PCI Express
FBDIMM
GDDR5
GDDR4
Serial-ATA
PCI Express
GDDR3
Infiniband
DDR4
Serial-ATA
DDR3
DDR
DDR2
Source: Intel
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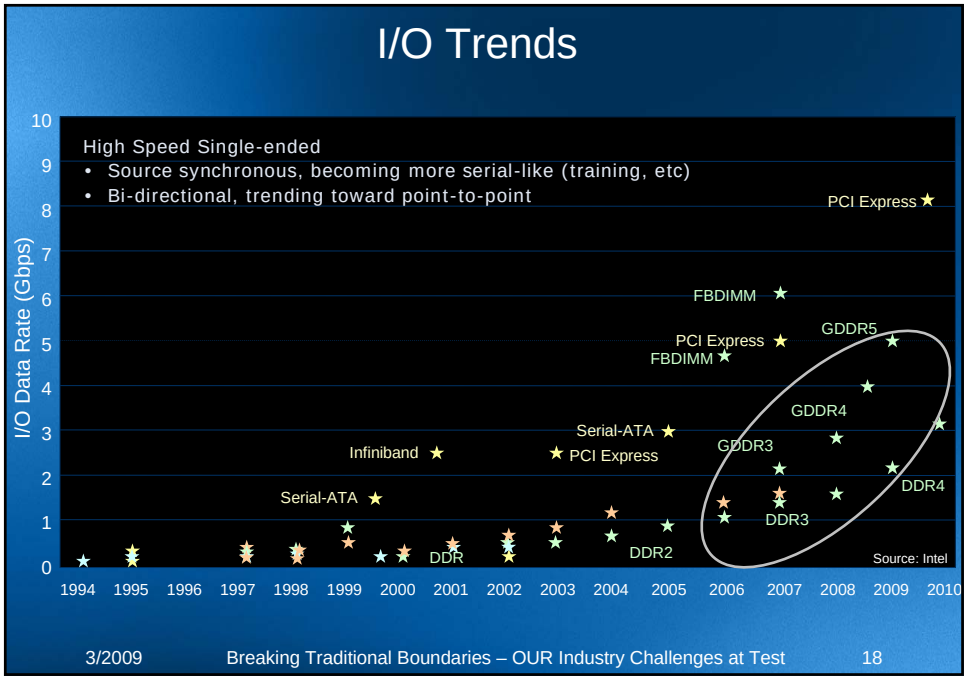
I/O Trends
High Speed Single-ended
• Source synchronous, becoming more serial-like (training, etc)
• Bi-directional, trending toward point-to-point
I/O Data Rate (Gbps)
PCI Express
FBDIMM
PCI Express
FBDIMM
GDDR5
GDDR4
Serial-ATA
PCI Express
GDDR3
Infiniband
DDR4
Serial-ATA
DDR3
DDR
DDR2
Source: Intel
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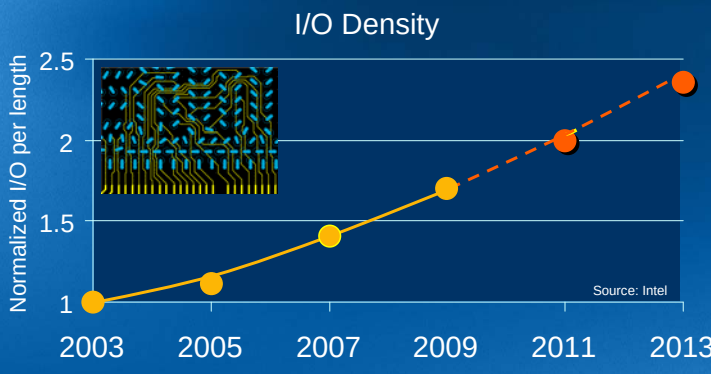
Channel Density Continues to Rise



Density Impacts Substrate Routing

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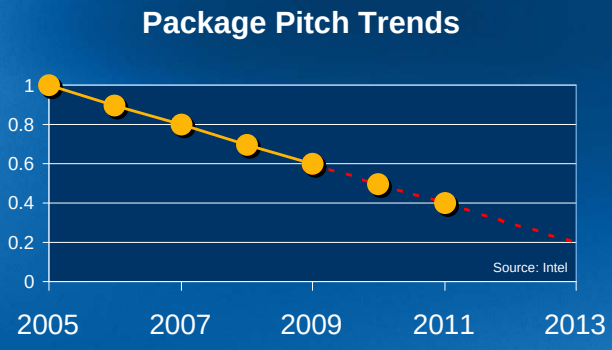
Pitch continues to shrink



Higher Density, Smaller Footprint Means Tighter Pitch

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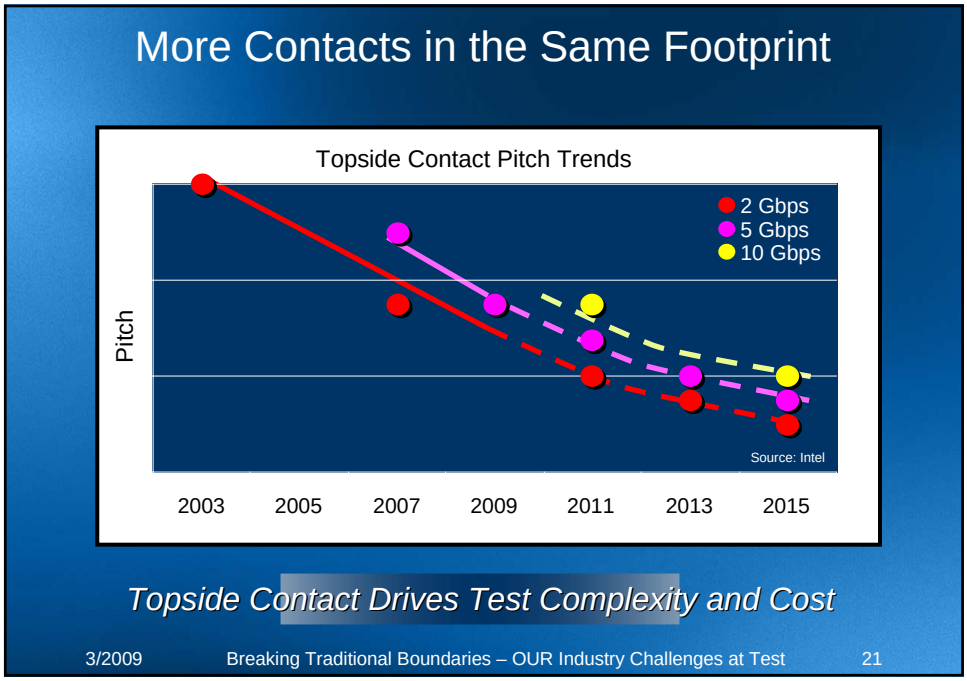
More Contacts in the Same Footprint
Topside Contact Pitch Trends
2 Gbps
5 Gbps
10 Gbps
Pitch
Source: Intel
2003
2005
2007
2009
2011
2013
2015
Topside Contact Drives Test Complexity and Cost
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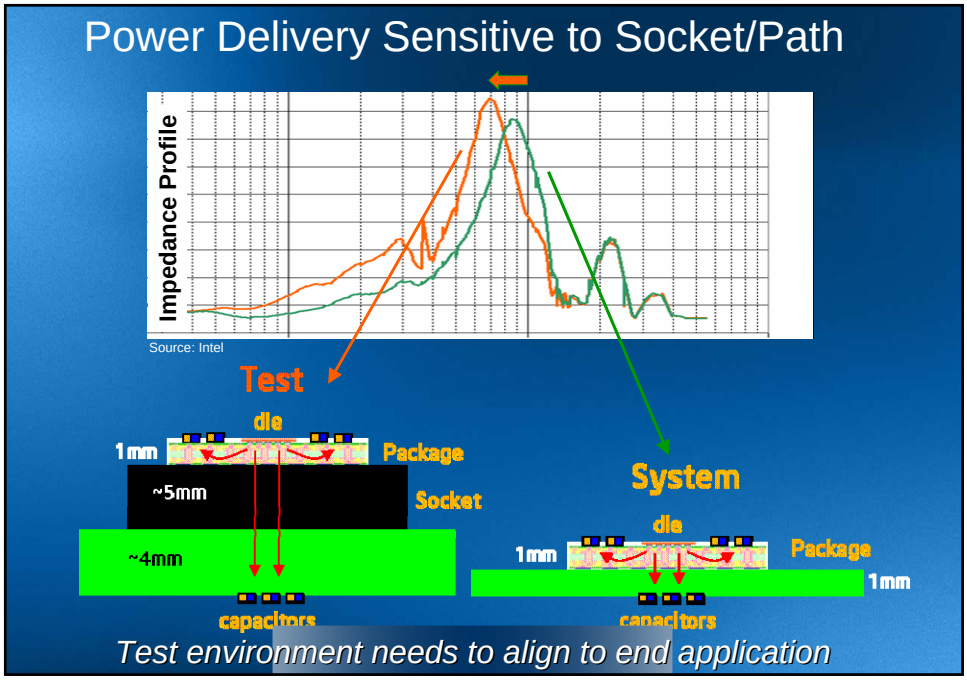
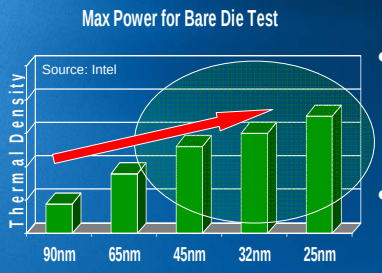
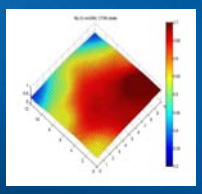

Power Delivery Sensitive to Socket/Path
Impedance Profile
Source: Intel
Test
die
1mm
Package
~5mm
Socket
~4mm
capacitors
System
die
1mm
Package
1mm
capacitors
Test environment needs to align to end application

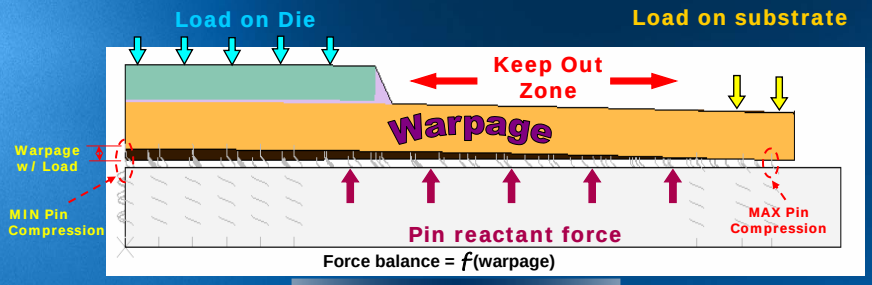
Test Thermal Challenge



- Silicon scaling results in higher thermal density
- Bare die brings major thermal control challenges
  - Fast transients
  - Spatial uniformity

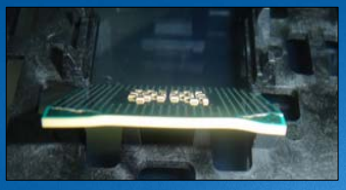


Thin package handling



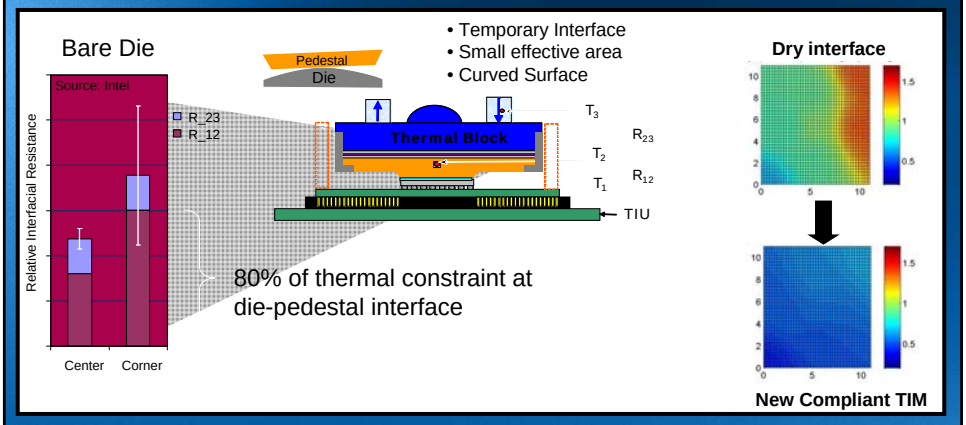
Any Test induced damage is unacceptable

Die cracking



Package damage

Bare Die Thermals: Focus on Die-Pedestal Interface



Better Test Thermal Interface Materials are Needed

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We Need To Do Much More

Call to Action

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Reduce Complexity

- Very Few Pre-competitive Standards
  - Each piece of tooling is custom built
- No Fully Integrated Test Solutions Off-the-Shelf
  - We have to manage many interfaces and suppliers
- Too Many New Solutions for the same Old Problems

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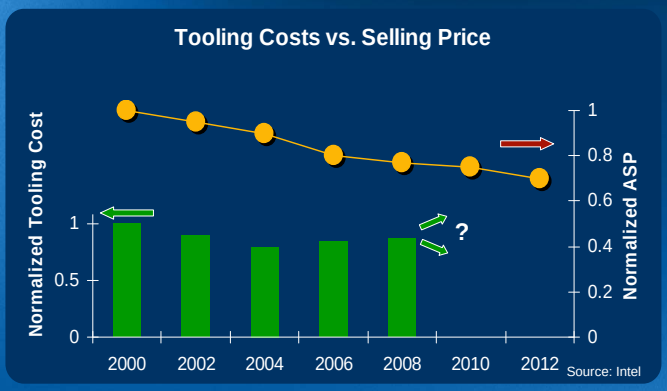
Cost Reduction



Tooling Costs must go down in parallel to platform costs

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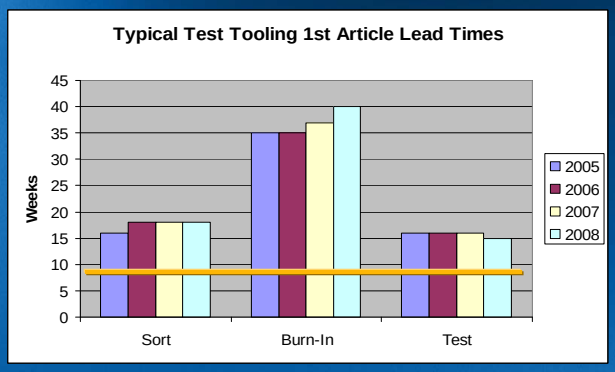
Need Improvement in Lead-time



- Package form-factor is a competitive advantage
- Quick-turn test tooling is a differentiator

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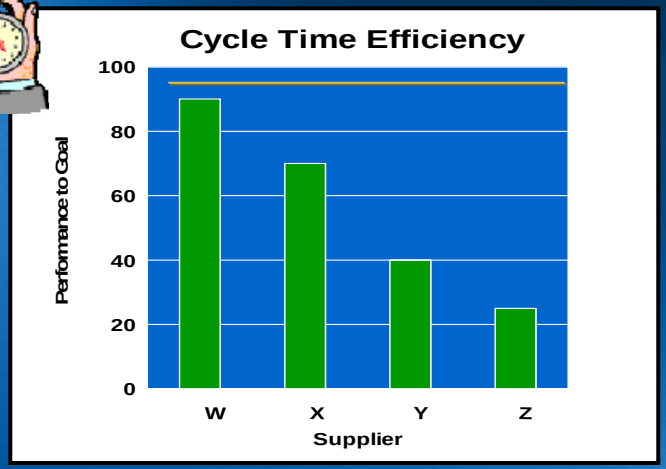
You Improve What You Measure



Need to improve cycle times efficiency!

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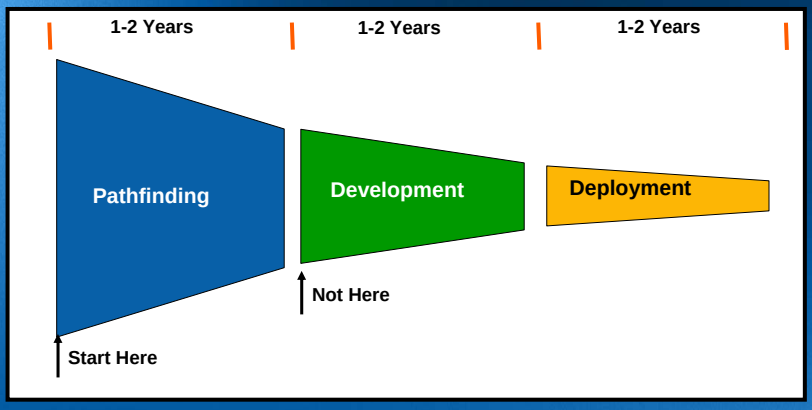
Engage Early



Invest in Roadmap Opportunities and Accept the Risks Required to Innovate

Summary

- Moore's Law is alive and well
  - Technical challenges continue to multiply
- The Rate of Innovation Needs to Increase
  - Need to reduce costs and cycle times
  - We need total solutions instead of many pieces
- Engage early… Develop pre-competitive standards to allow for industry level collaboration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