2009 **Session 4**

ARCHIVE 2009

PCBs – More Than Just Boards

Tuning a PCB/Contactor System to Your Device
Ryan Satrom—Everett Charles Technologies

A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations
Bob Jemison—RJI Technical Sales

Advances in Plating Technology, Reliable High Aspect Ratio Holes
Thomas N. Bresnan—R&D Circuits

COPYRIGHT NOTICE

The papers in this publication comprise the proceedings of the 2007 BiTS Workshop. They reflect the authors' opinions and are reproduced as presented , without change. Their inclusion in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.

There is NO copyright protection claimed by this publication or the authors. However, each presentation is the work of the authors and their respective companies: as such, it is strongly suggested that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.

All photographs in this archive are copyrighted by BiTS Workshop LLC. The BiTS logo and 'Burn-in & Test Socket Workshop' are trademarks of BiTS Workshop LLC.

TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE

Ryan Satrom
Everett Charles Technologies

2009 BiTS Workshop
March 8 - 11, 2009

Introduction

- Tuning involves modifying components, including the contactor, on PCB to optimize performance
- For many RF devices, the signal path requires tuning, and the contactor is a critical part of this path
- The inclusion of a contactor in an interface presents additional challenges to tuning

Agenda

This presentation will:

- Describe the importance of tuning
- Provide an introduction to tuning concepts
- Present a tuning example
- Show the effect of contactor on tuning
- Provide two solutions for tuning the signal path, including the contactor
- Propose future direction

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 3

Importance of Tuning

- Tuning components on your PCB will affect the performance of your device
- Adding a contactor will degrade key parameters, such as gain and power, up to ~10dB
- Proper tuning allows test of device, not interface
- Outcome: with accurate tuning, test results will reflect actual device performance

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 4

Importance of Tuning

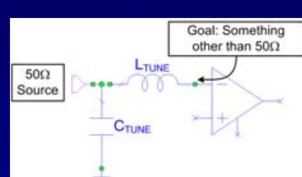
Poor tuning causes a series of problems:

- Complete test failure - decrease in performance will cause test to fail
- Moderate to significant drop in yield - typical performance much closer to failure limits, causing yield to drop
- Lower bottom line – invalid failures cost money, profits decrease

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 5

Tuning

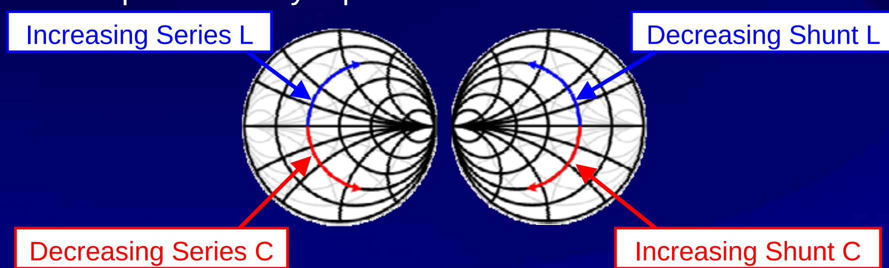
- Definition: optimization of the components in a system for maximum performance of an amplifier for a specific device frequency
- Involves modifying the components (L, C, PCB traces, contactor)
- Goal: Transform the impedance at the specific device frequency for optimal performance
  - Tuning is for narrow-band performance
  - Broad-band performance is unimportant



3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 6

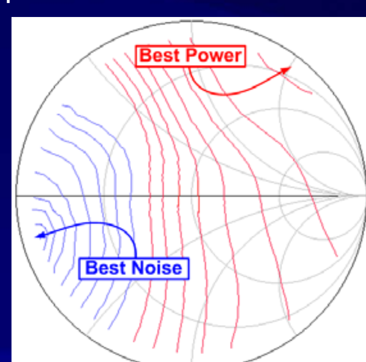
Smith Chart

- A graphical representation of impedance (Z) and admittance (Y, the inverse of impedance)
- Modifying component values changes the impedance and its corresponding location on the Smith Chart
- The ideal electrical performance an impedance represented by a point on the Smith Chart:



Determining a Good Match

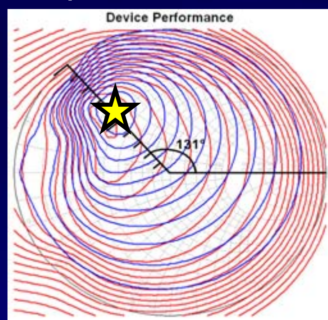
- Optimum device performance is often determined by taking load-pull measurements*
  - Load-pull measurements provide a compromise between two or more device parameters
  - Optimum impedance is chosen as a trade-off between specified parameters which are critical for given amplifier
  - Gain, Noise Figure, Power, and Efficiency are the most common measured parameters

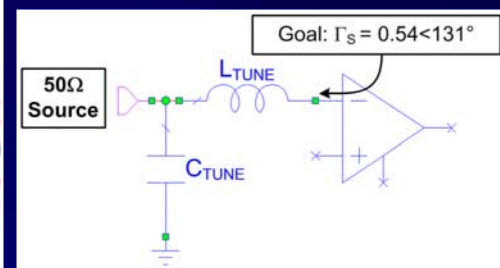


*Other methods can be used but that discussion is beyond the scope of this presentation

Tuning Example – No Contactor

- Device: Amplifier @ 2.4GHz
- Optimum source reflection : Γ_S=0.54<131°

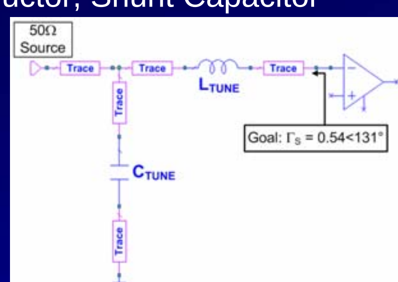




•Red Contours: Power - Max Power = 20dB
•Blue Contours: Efficiency (PAE) - Max Efficiency

Tuning Example – No Contactor

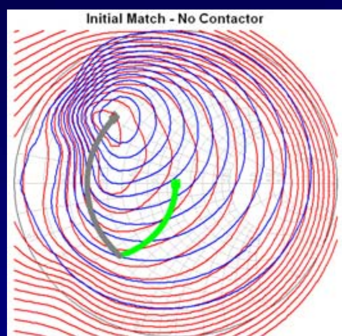
- Goal: Convert 50Ω (Γ=1) into Γ_S optimum performance
- Method: Use LC network below
  - PCB traces also included in path
  - Contactor will be added later
- Modify two variables to match impedance
  - Series Inductor, Shunt Capacitor



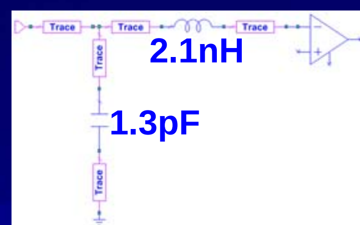
Tuning Example – No Contactor

Tuning Match

- 1st Step : Start at center (50Ω)
- 2nd Step : 1.3pF Capacitor with adjacent trace
- 3rd Step : 2.1nH Inductor with adjacent trace



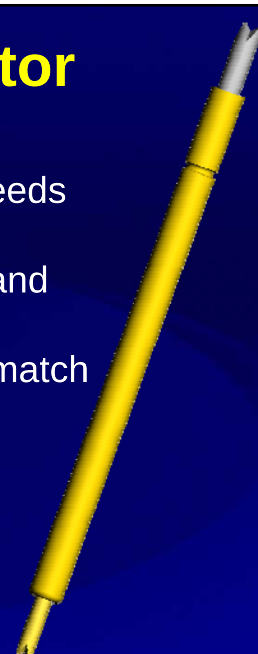
Results
Power = 19.0dB



3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 11

Adding a Contactor

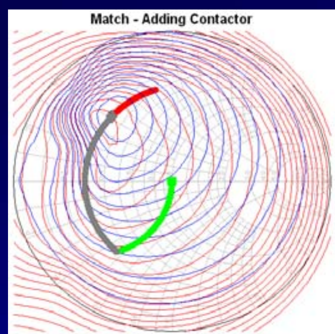
- Contactors
  - Will always affect match and needs to be considered
  - May require component value and placement modifications
- Two main parameters that affect match
  - Electrical length of probe
  - Loop inductance (strongly influenced by signal / ground proximity)



3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 12

Results – Adding a Contactor

- BTM050 added to signal path
  - Pin Length = 2.49mm
  - Loop Inductance = 0.87nH



- 1.3pF Capacitor
- 2.1nH Inductor
- BTM050 Contactor

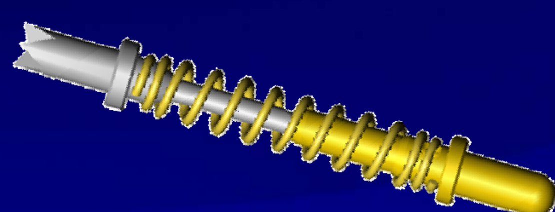
	Power
No Contactor	19.0dB
BTM050	16.1dB

Components will be added or adjusted to improve performance

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 13

Results – Adding a Contactor

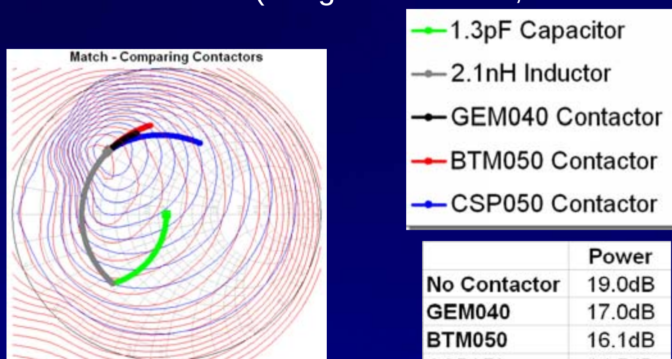
- Drop in power often does not correlate to contactor bandwidth specification
  - Power (no contactor) – power (w/ BTM050) = 19dB-16.1dB
  - Specified BTM050 contactor loss @ 2.4 GHz = 0.2dB
  - Change in power = 2.9dB – *Adjustments are needed!*
- Due to presence of non-linear circuitry (amplifier)



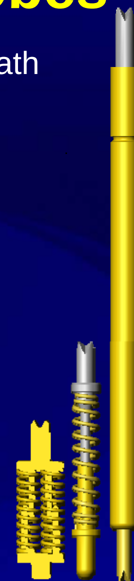
3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 14

Results – Comparing Probes

- Three different technologies added to signal path
  - GEM040 (Length = 1.54mm; L = 0.55nH)
  - BTM050 (Length = 2.49mm; L = 0.87nH)
  - CSP050 (Length = 6.45mm; L = 1.79nH)



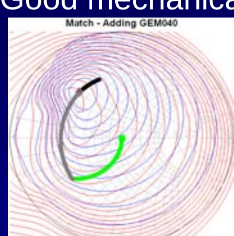
	Power
No Contactor	19.0dB
GEM040	17.0dB
BTM050	16.1dB
CSP050	14.5dB



3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 15

Using a High-Performance Probe

- Minimizes undesired movement on Smith Chart
- Increases likelihood of achieving good match
- GEM040 probe
  - Minimal length (1.54mm)
  - Minimal loop inductance
    - 0.45nH (0.4mm), 0.55nH (0.5mm)
  - Good mechanical integrity

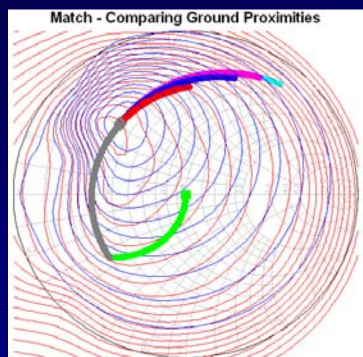


	Power
No Contactor	19.0dB
GEM040	17.0dB

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 16

Results – Comparing Ground Proximity

- Increased distance to ground = increased path length = increased inductance
- Plot compares four different distances
  - 0.5mm, 1mm, 1.5mm, 2mm



- BTM050 GS 0.5mm
- BTM050 GS 1.0mm
- BTM050 GS 1.5mm
- BTM050 GS 2.0mm

	Config	Proximity	Power
No Contactor	--	--	19.0dB
BTM050	GS	0.5mm	14.5dB
BTM050	GS	1mm	11.0dB
BTM050	GS	1.5mm	8.2dB
BTM050	GS	2mm	6.7dB

Up to **12dB** loss in power!

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 17

Solutions for Optimized Design

Two solutions for implementing good design:

1) Trial & Error
   - Benefits – Can occur after design/fab phase
   - Challenges – Optimal solution may not be achieved
2) Simulation
   - Benefits – Can produce most accurate results
   - Challenges – Requires PCB, contactor, and device expertise/models; must occur during design phase

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 18

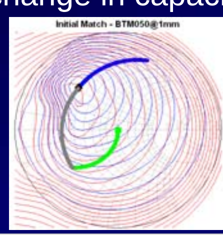
Solution #1 – Trial & Error

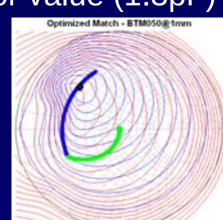
- Change L and C until acceptable results achieved
- Performance can be achieved but is least desirable option
  - Trial & Error allows for minor design changes, but is too late to make component placement changes
  - Non-ideal engineering practice – difficult to improve designs without understanding why changes are being made

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 19

Solution #2 - Simulation

- Use simulation to offset contactor parasitics
- Example #1 – No PCB Re-design
- BTM050@1mm (G-S Configuration)
  - Remove inductor (replace with 0Ω resistor)
  - No change in capacitor value (1.3pF)





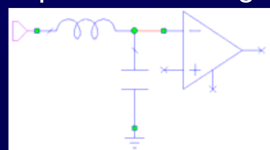
	Power
Initial Layout	11.0dB
After Component Change	16.9dB

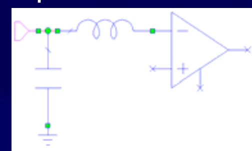
5.9dB change!

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 20

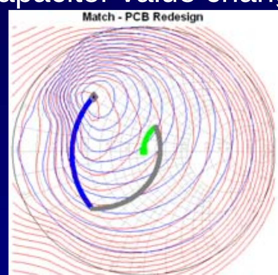
Solution #2 - Simulation

- Example #2 – Change PCB Component Placement





- Inductor changed to 1.5nH
- Capacitor value changed to 1.5pF



	Power
Initial Layout	11.0dB
PCB Redesign	19.0dB

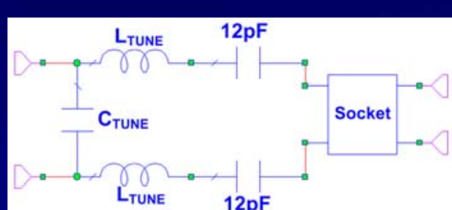
8dB change!

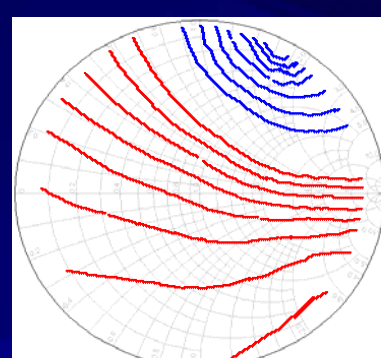
3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 21

Integrating Simulation and Measurement

Project Description

- Existing contactor solution was replaced with GEM040
- Components must be modified to account for new contactor
- Replacing longer probe with short probe still requires tuning
- Goal: modify PCB components to match or exceed performance of existing, functioning solution





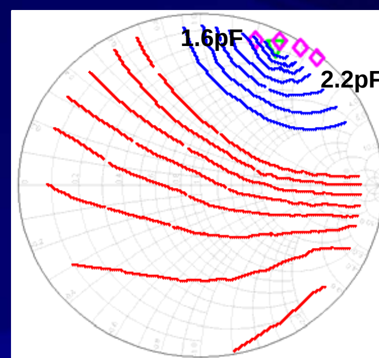
3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 22

Integrating Simulation and Measurement

- Existing Solution: L_{TUNE} = 3.0nH; C_{TUNE} = 1.2pF
- GEM040 Solution:
  - Leave L_{TUNE} unchanged (3.0nH)
  - Sweep C_{TUNE} from 1.6pF to 2.2pF

Measurement Results

Socket Type	L_{SERIES}	C_{SHUNT}	GAIN	NF
Existing Solution	*3.0nH*	*1.2pF*	*35.42 dB*	*3.20 dB*
GEM040	3.0nH	1.6pF	33.37 dB	3.52 dB
GEM040	*3.0nH*	*1.8pF*	*35.00 dB*	*3.51 dB*
GEM040	3.0nH	2pF	32.12 dB	3.71 dB
GEM040	3.0nH	2.2pF	29.96 dB	3.43 dB



3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 23

Vision for the Future

- Contactor/PCB Vendors
  - Provide expertise on contactor and PCB performance (and modeling)
- Device Manufacturers
  - Provide device characteristics, including device models and/or load-pull measurements
- Work together to simulate and design future PCBs and tuning networks
- Improve performance and yield for future products

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 24

Summary

- The contactor presents challenges to tuning a test interface
  - Adds inductance and electrical length
  - Changes the impedance the source sees
- It is important to minimize the effect of the contactor
  - Trial & Error – can work, but usually not the most accurate
  - Simulation
    - Provides the opportunity to offset the contactor prior to design
    - More difficult but can be most accurate

3/2009 TUNING A PCB/CONTACTOR SYSTEM TO YOUR DEVICE 25

A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations

Bob Jemison
RJI Technical Sales

2009 BiTS Workshop
March 8 - 11, 2009

The Challenge

The #1 question asked today is

"What can you do to lower my day-to-day burn-in board costs? "

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 2

The Challenge

Where can you cut costs?

- Buy cheaper sockets?
- Less expensive materials?
- Board fabrication?
- Electrical components?
- Board interconnect?

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 3

Here's the real question

"How can I reduce the cost of manufacturing burn-in boards in order to lower my day-to-day operating costs?"

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 4

Burn-in Board Challenge

Burn-in platforms vary greatly

Different platforms = different BIB profiles

Note: This paper applies to those BIB applications where customers have larger board outlines, higher I/O requirements and increasing power needs

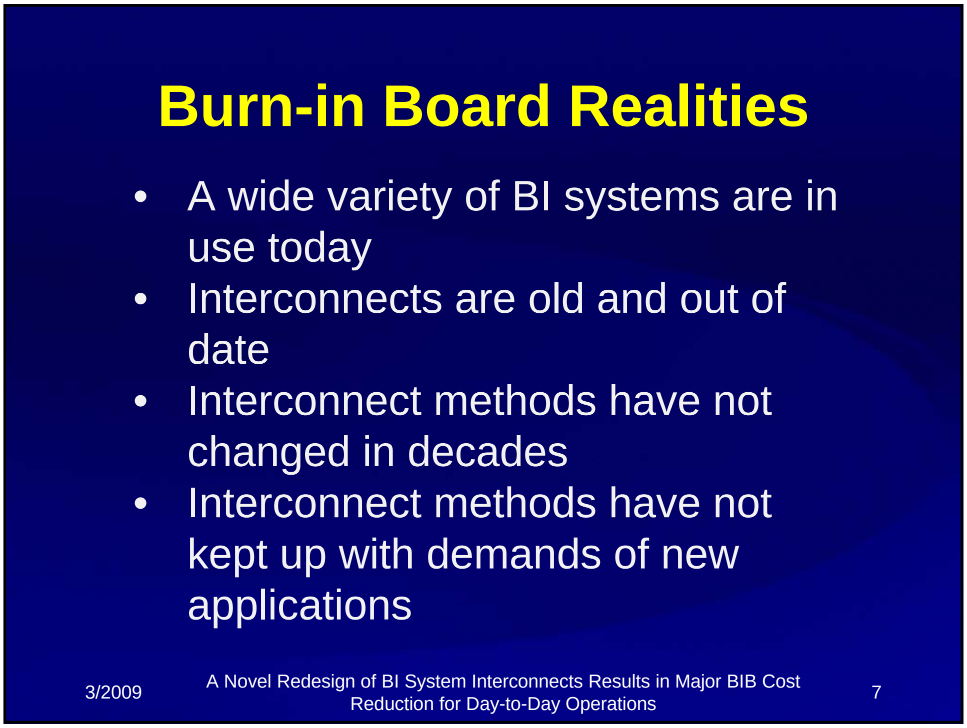
3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 5

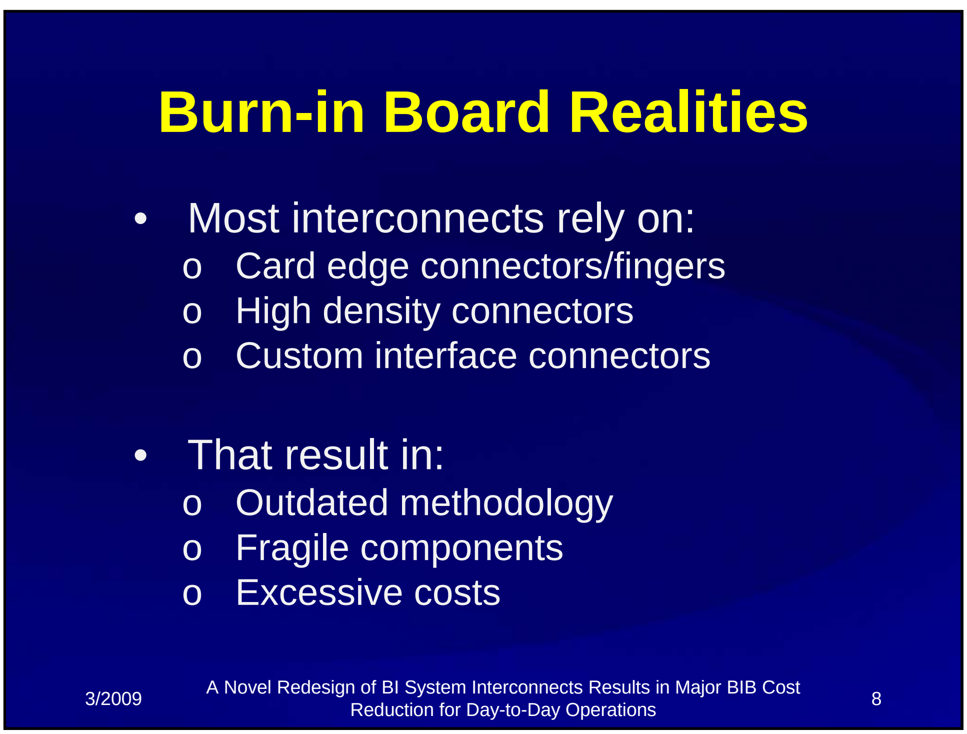
Burn-in Board Interconnects

Typical BIB interconnects

These boards represent typical applications

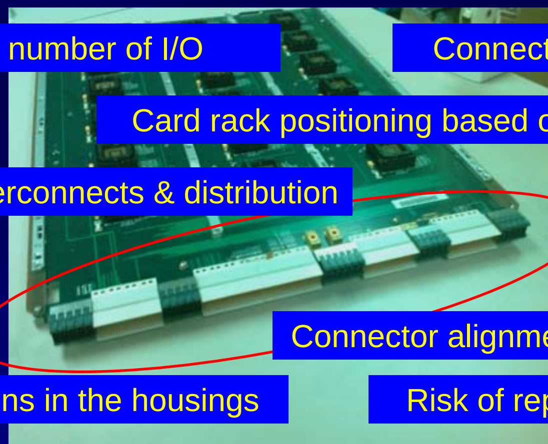
3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 6


Burn-in Board Realities
• A wide variety of BI systems are in use today
• Interconnects are old and out of date
• Interconnect methods have not changed in decades
• Interconnect methods have not kept up with demands of new applications
3/2009
A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations
7


Burn-in Board Realities
• Most interconnects rely on:
o Card edge connectors/fingers
o High density connectors
o Custom interface connectors
• That result in:
o Outdated methodology
o Fragile components
o Excessive costs
3/2009
A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations
8

BIB Interconnect Issues

Let's review one example

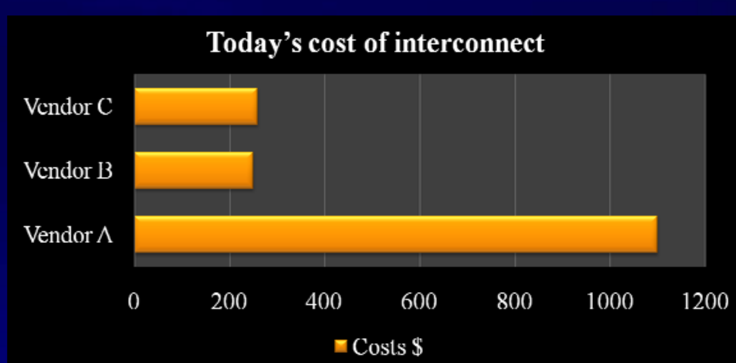


- Large number of I/O
- Connector costs
- Card rack positioning based on edges
- Power interconnects & distribution
- Connector alignment issues
- Fragile pins in the housings
- Risk of repairs

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 9

Interconnect Costs

Typical interconnect costs for 3 profiles



Cost per BIB for interconnect portion only

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 10

An innovative solution is …

… to eliminate of all interconnect hardware from the burn-in board

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 11

An Innovative Solution

We must address the following issues:

- Reduce the cost of the interconnect
- Introduce a more robust interconnect
- Eliminate alignment issues
- Allow for high density of contacts
- Plan for high power requirements

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 12

An Innovative Solution

Let's break it down into 4 steps

1) Provide a suitable contact to use for the interconnect
2) Provide a suitable interconnect housing to hold the contacts
3) Provide a method for implementation
4) Provide a cost comparison

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 13

An Innovative Solution

Step 1 – Select a suitable contact

- Contact that is suitable for burn-in applications
- Place a large number of contacts in a small space
- Must be a robust contact
- Ability to repair/replacement

Solution: Plastronics H-pin®

H-Pin is a registered trademark of Plastronics

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 14

An Innovative Solution

Step 1 – Selection criteria

- Working travel: 0.80 mm
- Contact force: 30 gr
- Current carrying: 4 amp
- Mechanical life: 50000 cycles

77 Series

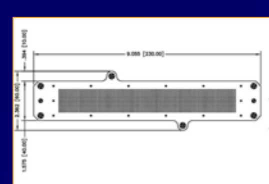
3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 15

An Innovative Solution

Step 2 - Determine a suitable housing

- Method to contain the contacts selected
- need to package a high pin count in a limited space
- Works in burn-in environment
- Ability to repair
- Be a one-time cost to burn-in

Solution: Interconnect pin block



3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 16

An Innovative Solution

Step 2 – Pin block for the interconnect

Approximately 2000 pins in 11 sq inches

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 17

An Innovative Solution

Step 3 – The implementation

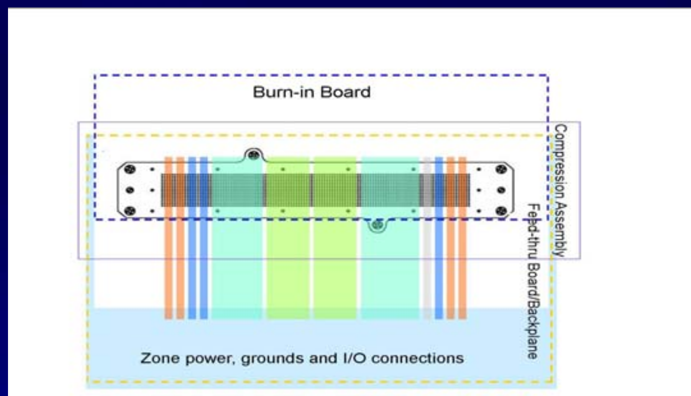
- Board to board interconnect
- One time implementation in the burn-in system
- Designed to work in this burn-in environment
- Suitable for new systems or in-house applications

Choice: A board to board interconnect suitable for a rack based burn-in environment

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 18

An Innovative Solution

Step 3 – The implementation

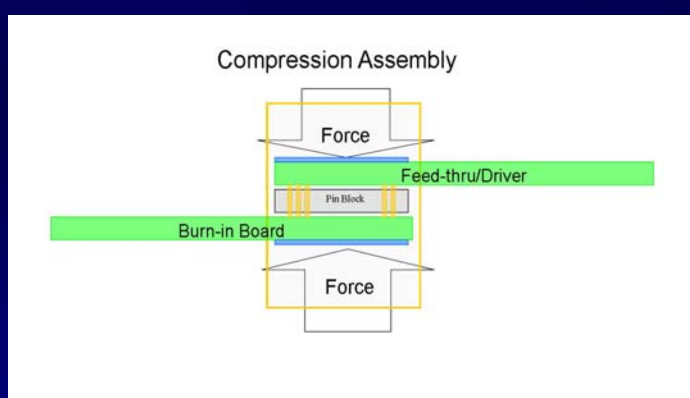


Typical power and I/O distribution

3/2009 | A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations | 19

An Innovative Solution

Step 3 – The implementation



View showing the stack up of all major components

3/2009 | A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations | 20

An Innovative Solution

Burn-in board requires the following:

All I/O connections are reduced to pad locations to match the pin block

No connectors are required on the burn-in board

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 21

An Innovative Solution

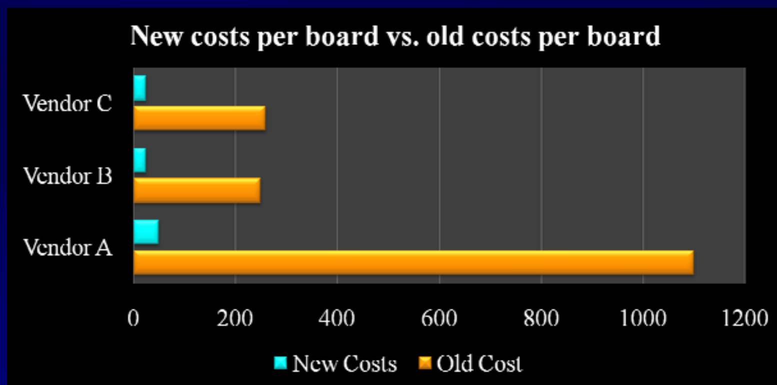
The burn-in system requires the pin block

- Pin block stays with the system
- One time investment in the burn-in system
- Day-to-day BIB costs are reduced

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 22

Interconnect Solution Costs

Step 4: Interconnect costs



Cost per BIB for interconnect portion only

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 23

Annual Cost Savings

BIB Profile	Old $ Per Board	New $ Per Board	Boards per Project	Savings Per Project	Annual Savings
A	1100	50	10	10500	630000
B	250	25	10	2250	135000
C	260	25	10	2350	141000

1) Annual cost savings is based on 60 projects of 10 boards each

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 24

Applications

Methods can be applied

Most BI system interconnects are outdated

New methods can be adapted to both new and old burn-in systems

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 25

Conclusion

- New methods are available for use
- Users must invest in new methods
- One-time system improvements acceptable
- Major cost savings are possible

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 26

Thank you

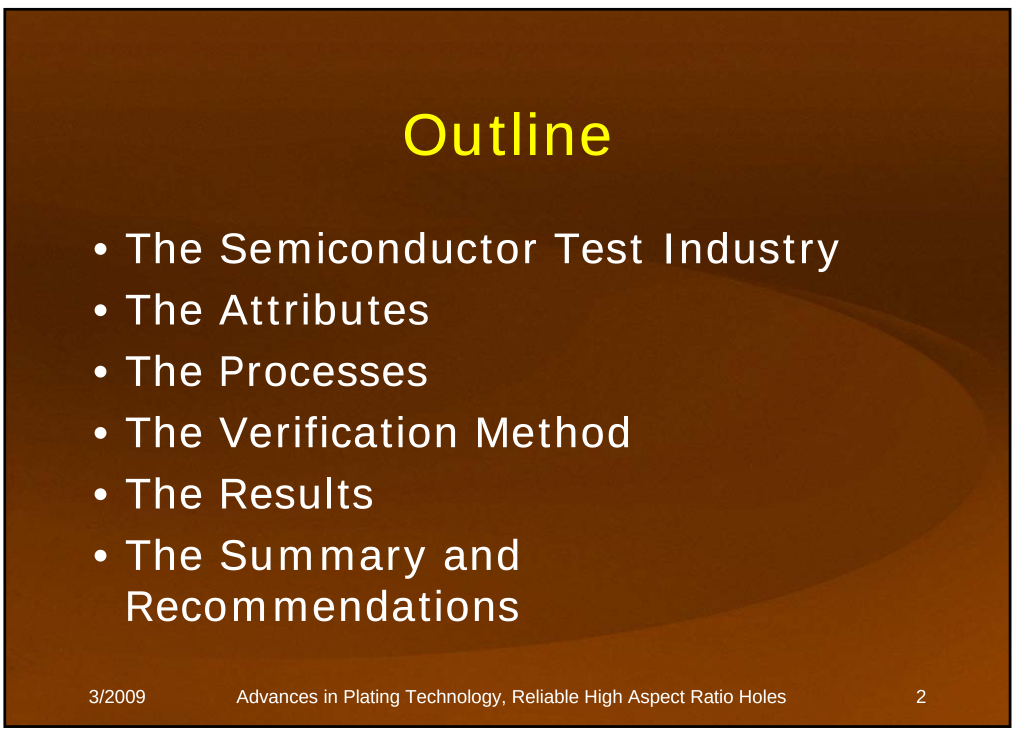
Our contributors include:

Bob Jemison, VP/GM, RJI Technical Sales
bjemison@rjisales.com

David Pfaff, COO, Plastronics Socket Company
Brad Mounsey, President, Stresstest, Inc.
Afshin Nouri, President, Contech Solutions
Thomas Allsup, President, Anida Technologies

3/2009 A Novel Redesign of BI System Interconnects Results in Major BIB Cost Reduction for Day-to-Day Operations 27


Advances in Plating Technology,
Reliable High Aspect Ratio Holes
Tom Bresnan
R&D Circuits
2009 BiTS Workshop
March 8 - 11, 2009


Outline
• The Semiconductor Test Industry
• The Attributes
• The Processes
• The Verification Method
• The Results
• The Summary and Recommendations
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
2

Semiconductor Test

- Fine Pitch Devices / Package Test
  - 0.5mm BGA
  - 0.4mm BGA
  - 0.3mm BGA
- Elevated Temperature Testing
  - 4 to 8 hours

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 3

Semiconductor Test

- Temperature cycling for characterization
  - -40°C to +125°C
- Package Verification

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 4

The ATE Industry

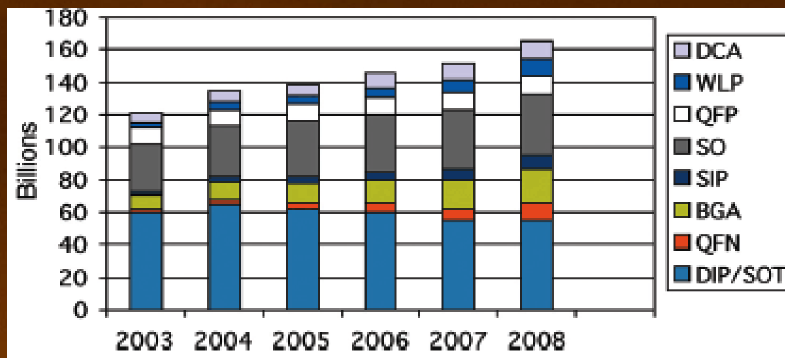


Table 1. Worldwide Semiconductor Package Volume

iNEMI Roadmap

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 5

The ATE Industry

- Packaged Device Testing
- 1.0mm – early 1990's
- 0.8mm – 0.65mm – late 1990's
- 0.5mm – 2000's
- 0.4mm – 2007
- 0.3mm – 2009
- 0.2mm – 2011

Int'l Tech Roadmap
for Semiconductors

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 6

High Aspect Ratio's

- Unique Board Geometries
  - Over-sized, not your usual 18 x 24 panel
  - Thick
    - 3.2mm minimum to > 6.4mm

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 7

High Aspect Ratio's

- Unique Board Geometries
  - Small holes
    - Mechanically drilled
    - 150 micron and less (100 micron currently)
  - High Aspect Ratio
    - 31:1 to > 45:1

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 8

Why These are Unique

- Attributes
- One of a Kind
- Thermal Extremes
- Continuous Use Environment

The Requirements

- The Tolerance Budget – 0.5mm
  - 0.5mm [0.0197] pitch
  - 150 micron [0.006] drill diameter (31:1)
  - 350 micron [0.0137] hole wall to hole wall
  - 100 micron [0.004] line width
  - 250 micron [0.0098] remaining / 2 =
  - 125 micron [0.00485] hole to circuit!

The Requirements

- The Tolerance Budget – 0.4mm
  - 0.4mm [0.0157] pitch
  - 100 micron [0.004] drill diameter (47:1)
  - 300 micron [0.0117] hole wall to hole wall
  - 75 micron [0.003] line width
  - 220 micron [0.0087] remaining / 2 =
  - 110 micron [0.00435] hole to circuit!

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 11

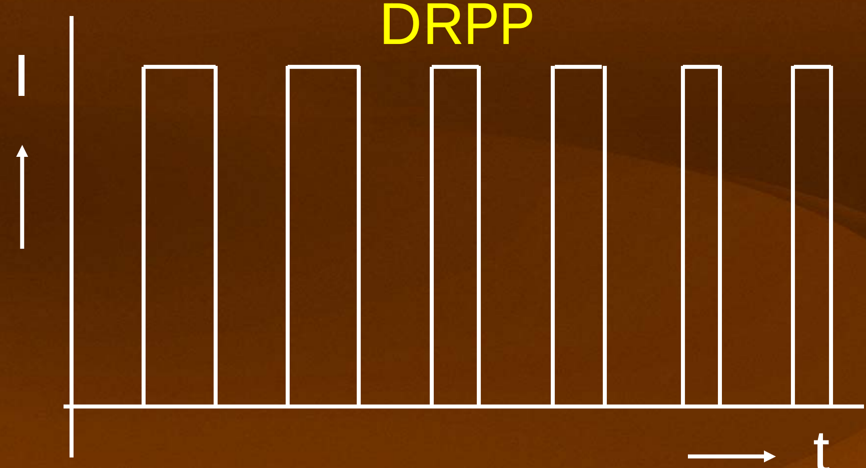
Registration on a 0.5mm Board

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 12

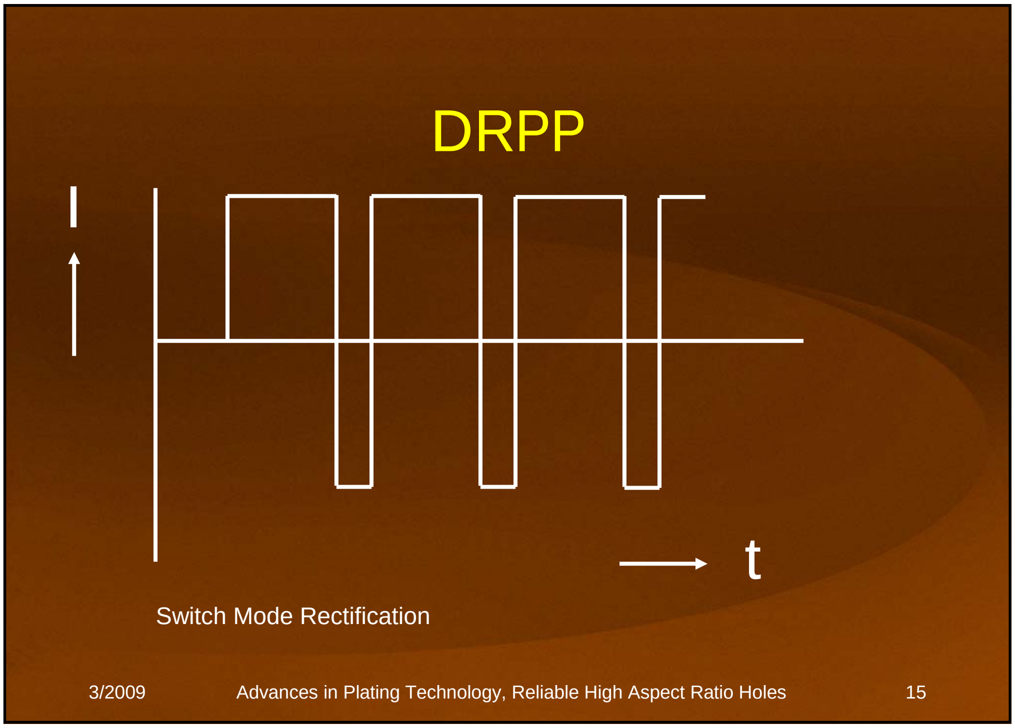
Plating Techniques

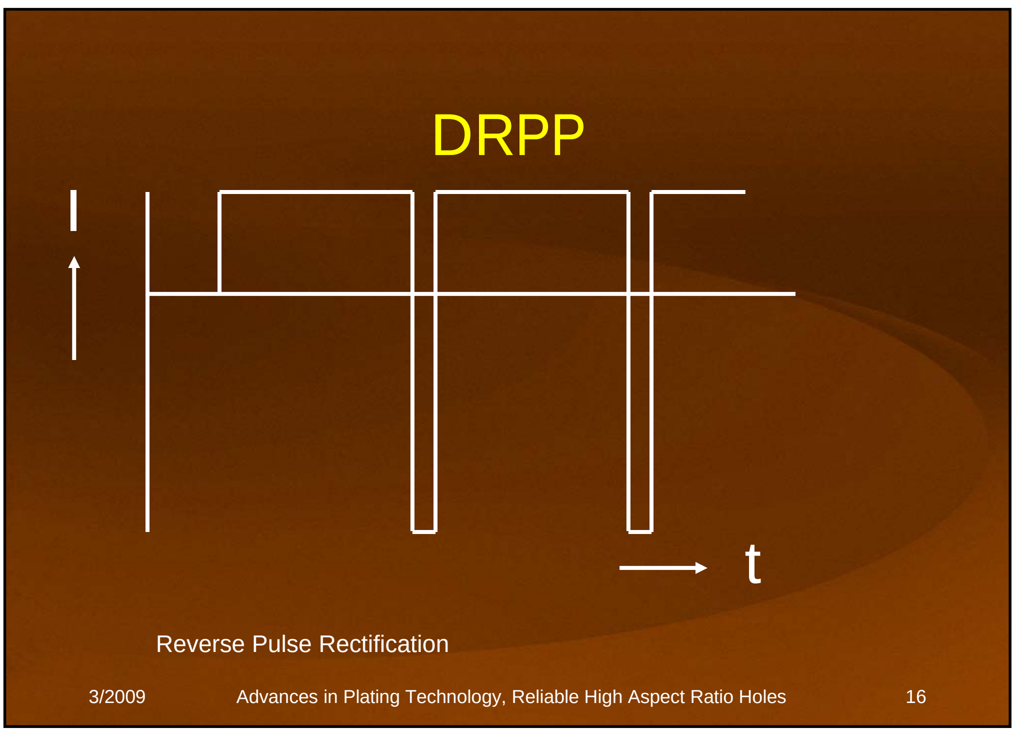
- High Aspect Ratio
- Cleaning (debris)
- Desmear / Hole Wall Prep
- Deposition
- Develop Resist
- Pattern Plate
- Nickel / Gold!

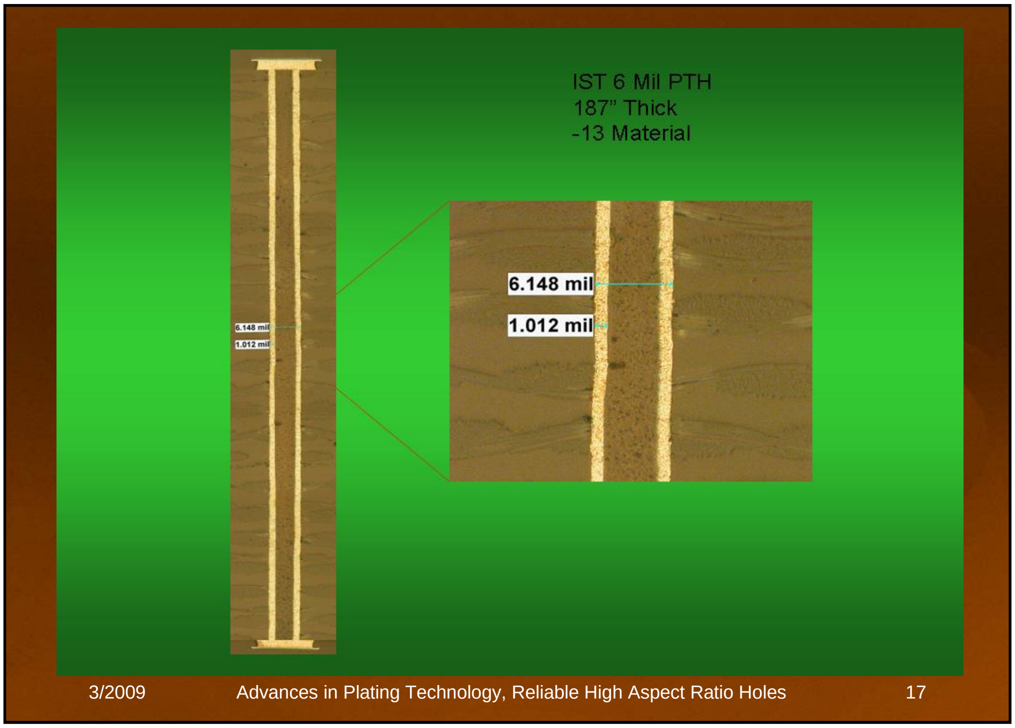
DRPP

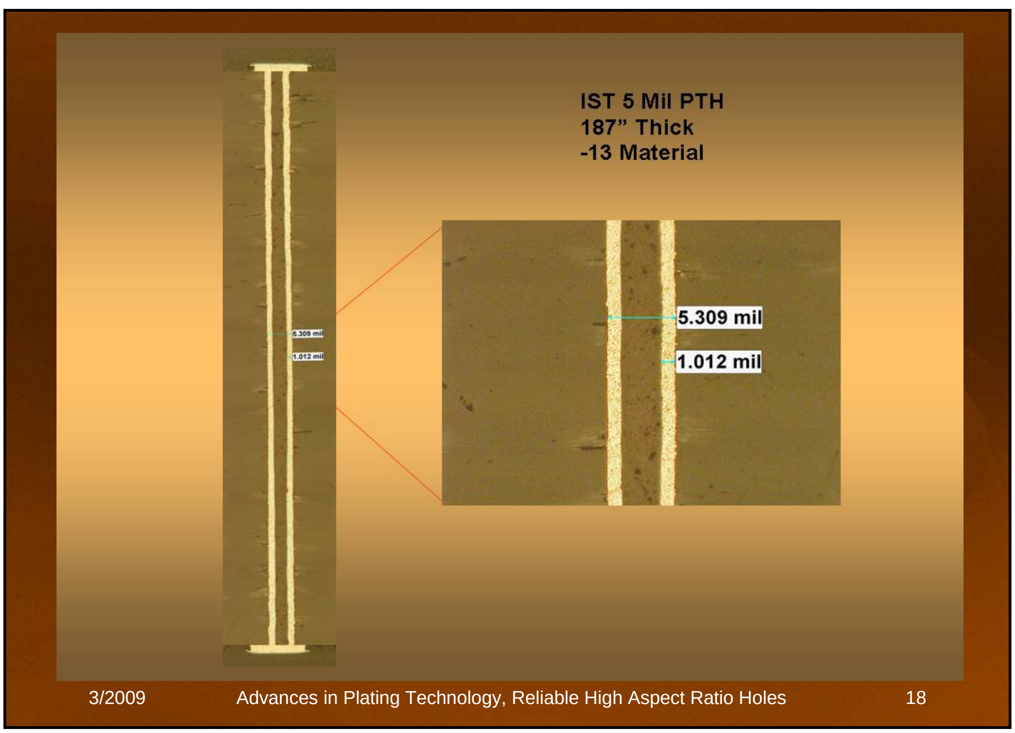


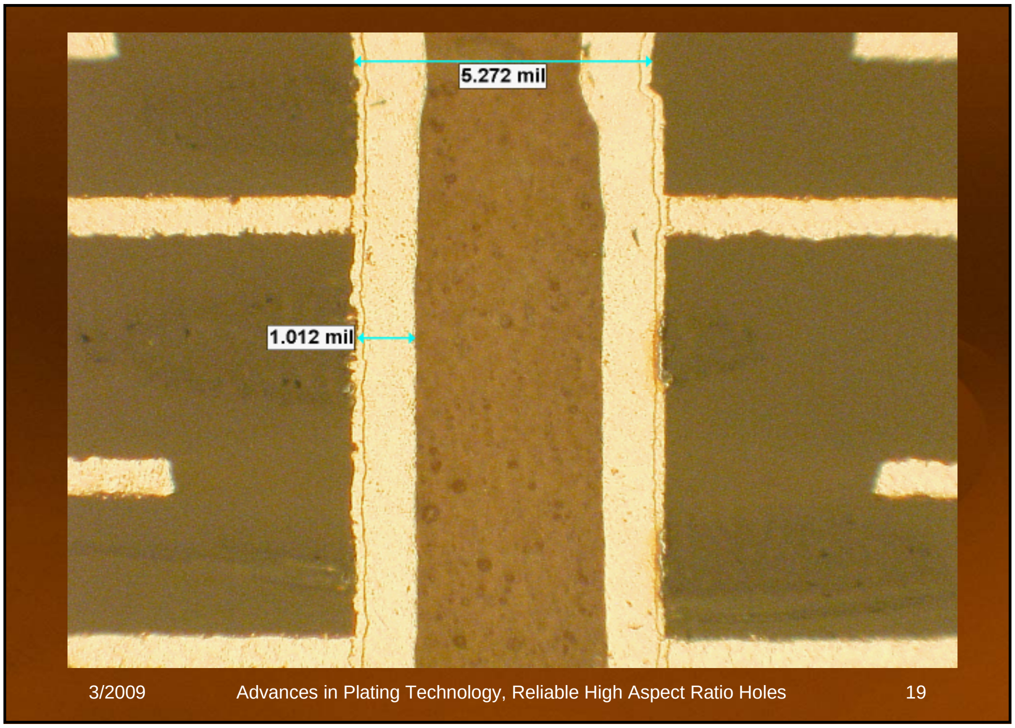
Pulse Rectification

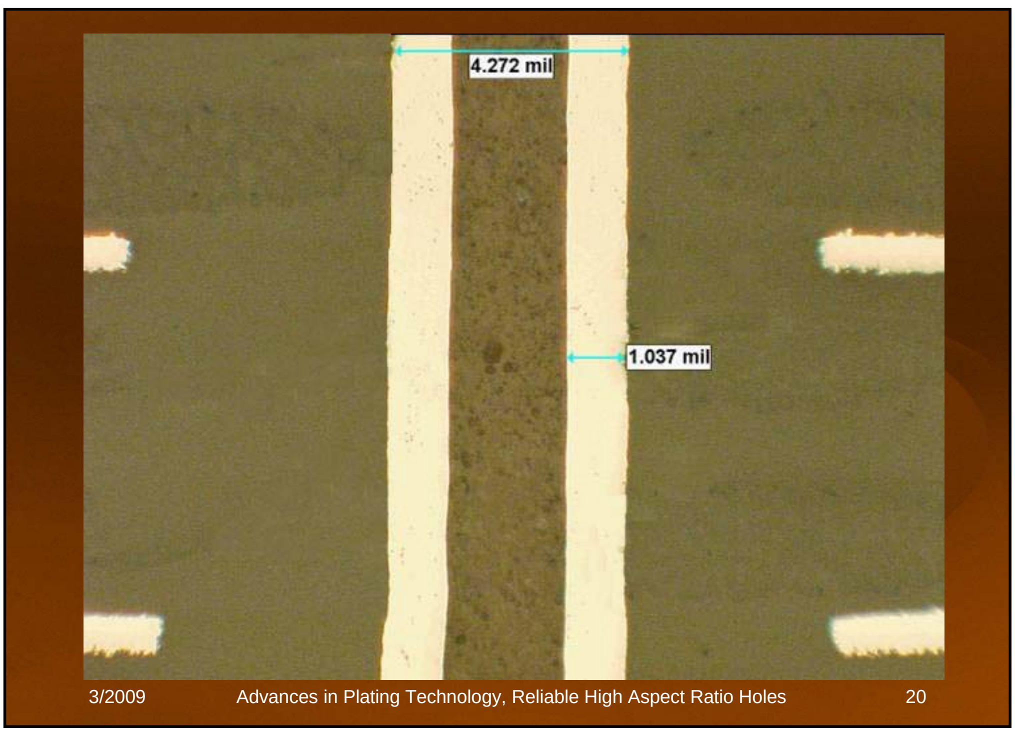

DRPP
I
t
Switch Mode Rectification
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
15


DRPP
I
t
Reverse Pulse Rectification
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
16


IST 6 Mil PTH
187" Thick
-13 Material
6.148 mil
1.012 mil
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
17


IST 5 Mil PTH
187" Thick
-13 Material
5.309 mil
1.012 mil
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
18


5.272 mil
1.012 mil
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
19


4.272 mil
1.037 mil
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
20

IST PWB Reliability Testing

- I.S.T. = Interconnect Stress Test
- Determines overall reliability of PWB
- Tests Copper Interconnection AND Material
- IPC Approved Test Method
- Industry Wide (Customer) Acceptance

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 21

I.S.T. Defined

- Interconnect Stress Test
  - Thermal Cycles by Electrically Heating an IST Test Coupon
  - Continuously measures resistance of the circuits during cycle
  - 10% Increase in Resistance is Failure – Test Stops in Seconds

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 22

I.S.T.

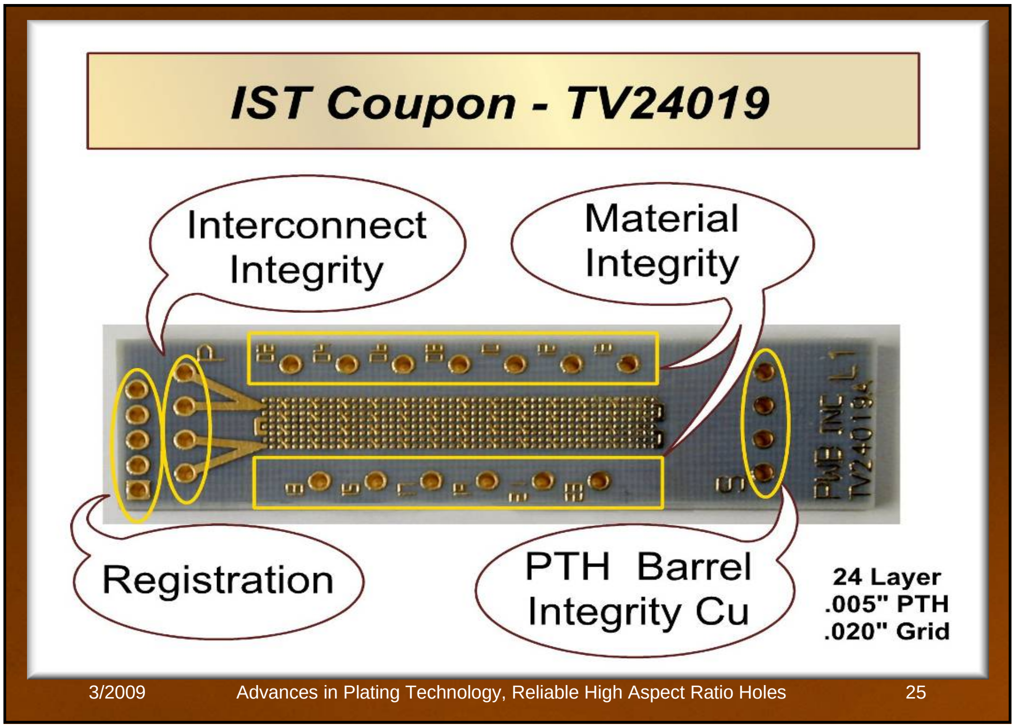
- Primary Objectives
  - Reduce Time to Results
  - Reduce Cost
  - Repeatability and Reliability
  - Automation of Testing and F/A

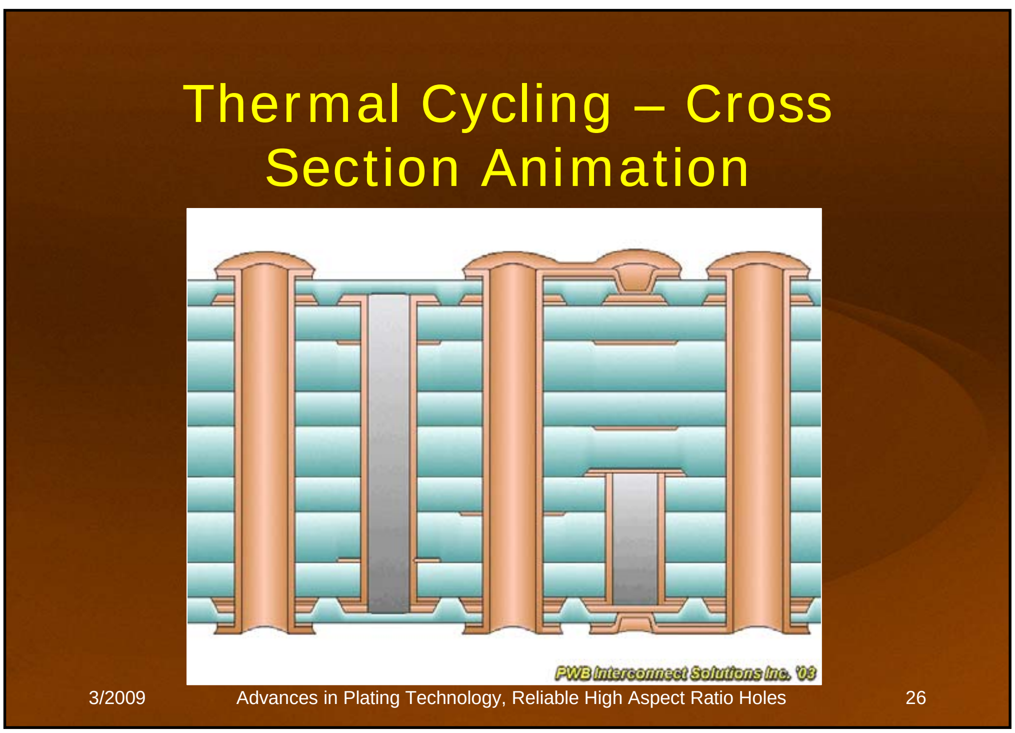
3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 23

IST

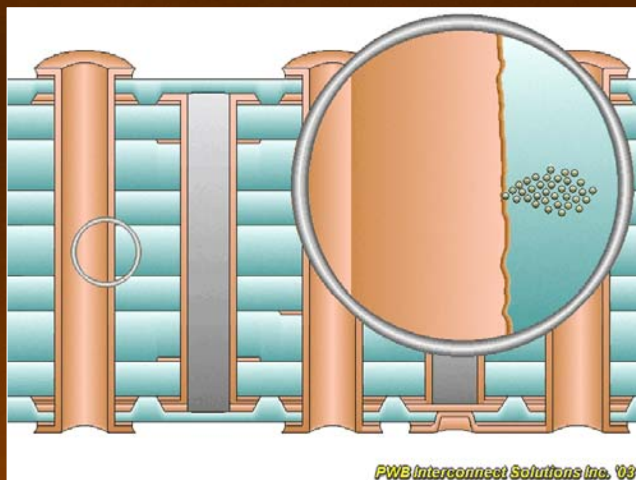
- Micro-sectioning vs. I.S.T.
  - Low # of holes / high number of holes
    - 1 degree vs. 360 degree
      - Circumference of all connections
  - Go / NoGo vs. quantifying severity
  - Poor vs. Excellent Repeatability
  - Not operator dependent
  - Visual criteria vs. Electrical criteria

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 24


IST Coupon - TV24019
Interconnect Integrity
Material Integrity
Registration
PTH Barrel Integrity Cu
24 Layer
.005" PTH
.020" Grid
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
25

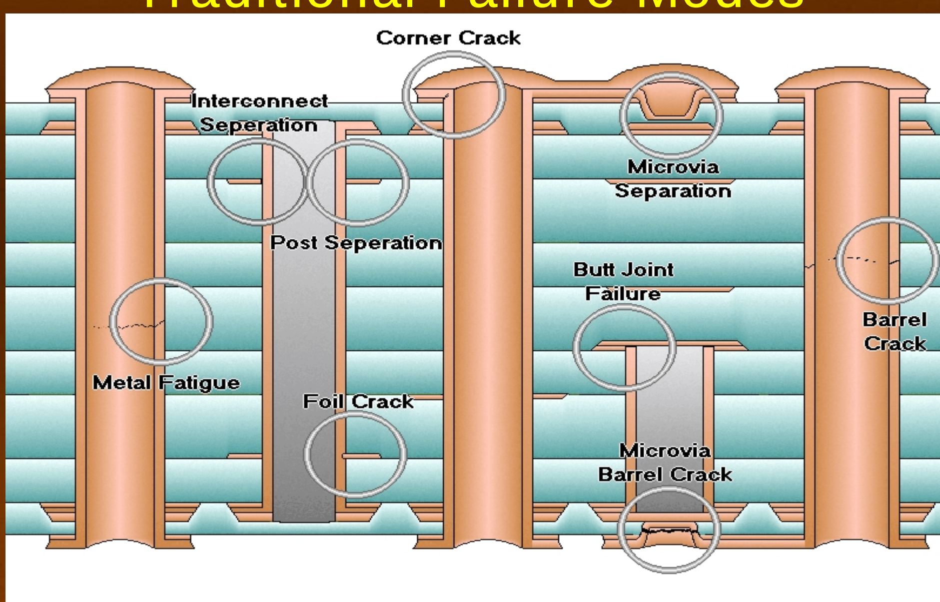

Thermal Cycling – Cross Section Animation
PWB Interconnect Solutions Inc. '03
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
26

IST Metal Fatigue – Metal Fatigue Animation



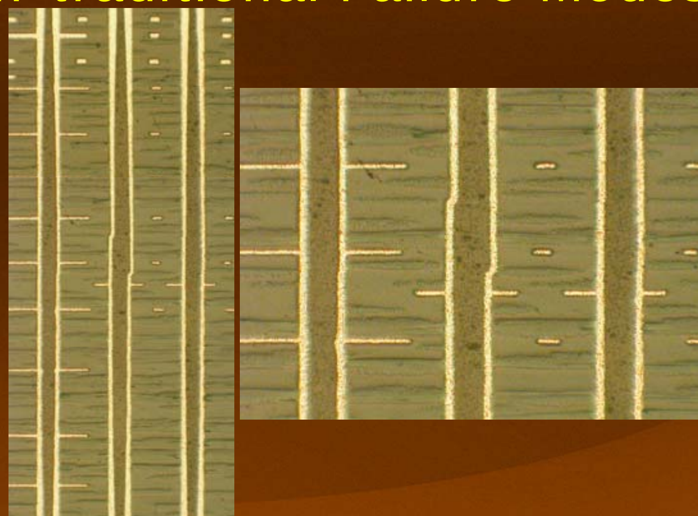
3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 27

Traditional Failure Modes



3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 28

Non-traditional Failure Modes?



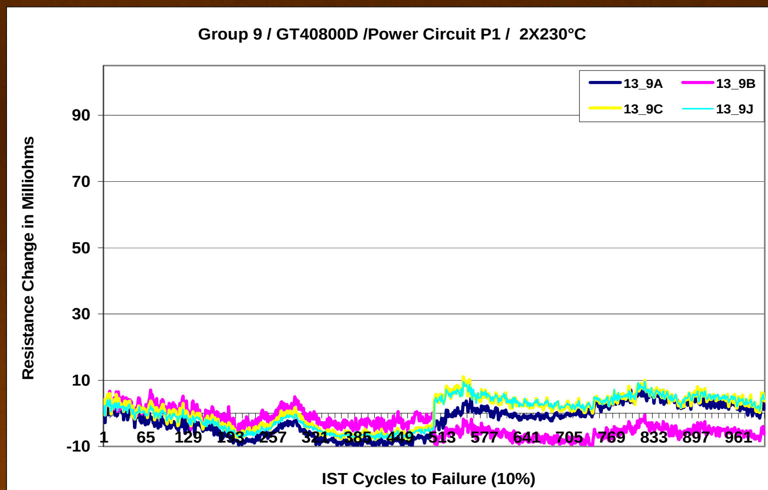
Some Data

IST Data – J07_1898

IST Cycles to Failure – S/N 9 – 2X230° C

IST Cycles to Failure - S/N 9 - 2X230°C					
COUPON	**P1**	**% P1**	**S1**	**% S1**	**Results**
13_9A	1000	0.1	1000	0.2	Accept
13_9B	1000	-0.5	1000	-1	Accept
13_9C	1000	0.4	1000	-0.4	Accept
13_9J	1000	0.4	1000	0.1	Accept
Mean	**1000.0**	**0.1**	**1000**	**-0.3**	
StDev	0.0	0.4	0.0	0.6	
Min	1000.0	-0.5	1000	-1.0	
Max	1000.0	0.4	1000	0.2	
Range	0.0	0.9	0	1.2	
Coef Var	**0%**		**0%**		

Graphing the Results



3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 31

Some more Data

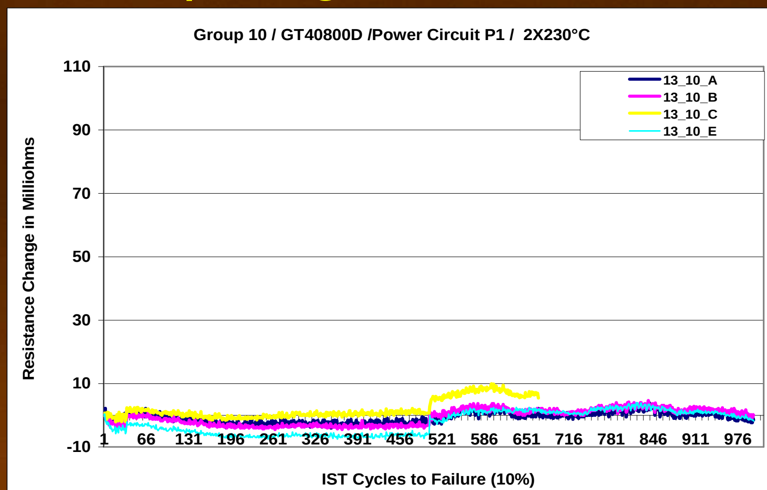
IST Cycles to Failure – S/N 10 – 2X230° C

IST Cycles to Failure - S/N 10 - 2X230°C

COUPON	P1	% P1	S1	% S1	Results
13_10_A	1000	-0.1	1000	1.8	Accept
13_10_B	1000	0	1000	3.1	Accept
13_10_C	N/A	0.6	669	10	S1
13_10_E	1000	-0.1	1000	2.1	Accept
Mean	1000.0	0.1	917	4.3	
StDev	0.0	0.3	165.5	3.9	
Min	1000.0	-0.1	669	1.8	
Max	1000.0	0.6	1000	10.0	
Range	0.0	0.7	331	8.2	
Coef Var	0%		18%		

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 32

Graphing the Results



3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 33

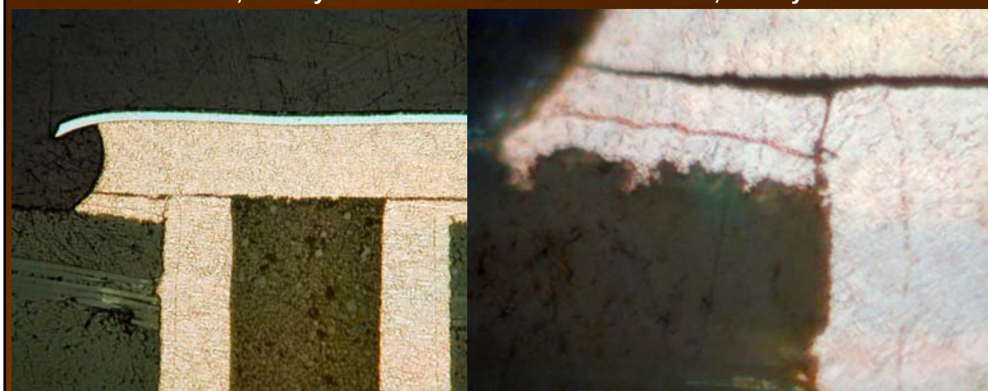
The Cause?

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 34

The Real Failure

XS# 3811, Coupon 13-10C - 2X230° C - Failed S1, 699 Cycles

XS# 3811, Coupon 13-10C - 2X230° C - Failed S1, 699 Cycles

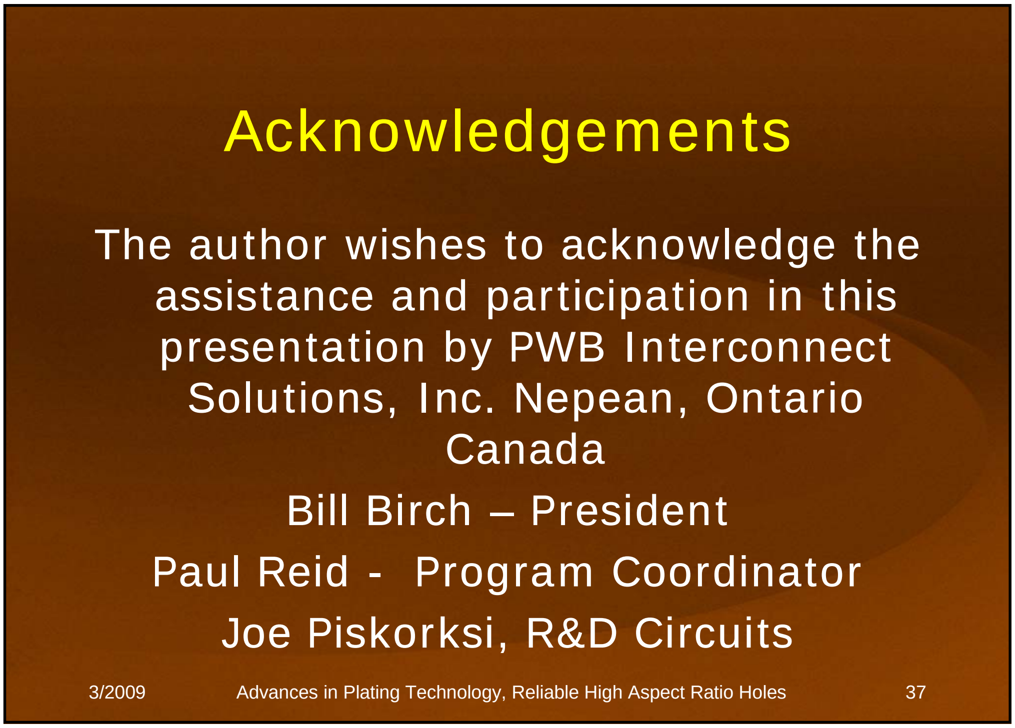


3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 35

Summary

- The Semiconductor Test Industry
- The Attributes
- The Processes
- The Verification Method
- The Results
- The Recommendations

3/2009 Advances in Plating Technology, Reliable High Aspect Ratio Holes 36


Acknowledgements
The author wishes to acknowledge the assistance and participation in this presentation by PWB Interconnect Solutions, Inc. Nepean, Ontario Canada
Bill Birch – President
Paul Reid - Program Coordinator
Joe Piskorksi, R&D Circuits
3/2009
Advances in Plating Technology, Reliable High Aspect Ratio Holes
37