BiTS Burn-in & Test Socket Workshop 2009

Session 3

ARCHIVE 2009

ADVENTURES IN TEST & BURN-IN OPERATIONS

Parallel Logic Test Interface Solutions

YH Jeon, Sang-Il Kwon—TSE
Gary Westendorf, Chris Mack—Pragmatics

CID: A New Breakthrough Solution For Contactor Hardware Tracking

Jonathan Mondero—Texas Instruments Philippines
Kevin Tiernan, Mike Guenther—Texas Instruments Houston
Eugene Batilo—Everett Charles Technologies – STG Singapore

Mechanical Reliability Test as Part of Final Test of a Packaged Chip

Che-Yu Li, Tia Korhonen—Che-Yu Li & Co.
Tim Wooden—Protos Electronics
SM Low—ADE Technologies

Substrate Bias: Application in Final Test and Burn-in of High-Power CPU's

Max Paransky—Texas Instruments

Parallel Logic Test Interface Solutions

YH Jeon, TSE
Sang-Il Kwon, TSE
Chris Mack, Pragmatics
Gary Westendorf, Pragmatics

2009 BiTS Workshop
March 8 - 11, 2009

Contents

- Welcome & Introductions
- Why We Chose This Subject
- Enabling Technologies
- Logic / SOC Test Interfaces
- Fan-Out Methodologies
- Fan-Out Signal Performance
- Considerations
- Conclusion

3/2009 Parallel Logic Test Interface Solutions 2

Paper #1

Why We Chose This Subject…

- Lessons learned from years of producing high parallel memory & MCP test interfaces are being applied to production Logic / SOC testing.
- Economics often require Logic / SOC production test without new capital spending on ATE.
- The real estate inside parallel test interfaces can be utilized to expand ATE resources.
- There are more Logic / SOC devices emerging that require high volume production.

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Enabling Technologies

- Increasing density ATE PEs & interconnects.
- DFT/BIST/SCAN reduces ATE I/O requirements.
- Logic load boards are transitioning to parallel test interfaces with real estate for fan-out circuitry & additional DUT power supplies.
- Advancements in lithography & packaging provides denser, smaller Logic / SOC devices that can be handled by memory test handlers.

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One-Piece PCB Logic Load Board

- Planarity & contact issues
- Poor thermal performance
- Limited real estate for additional circuitry
- PCB size limitations for high parallelism
- PCB aspect ratio limitations for fine pitch applications
- Costly PCB design & layout costs for high density & high speed performance
- PCB yield & cost issues for high density & performance
- Very limited repair & maintenance options

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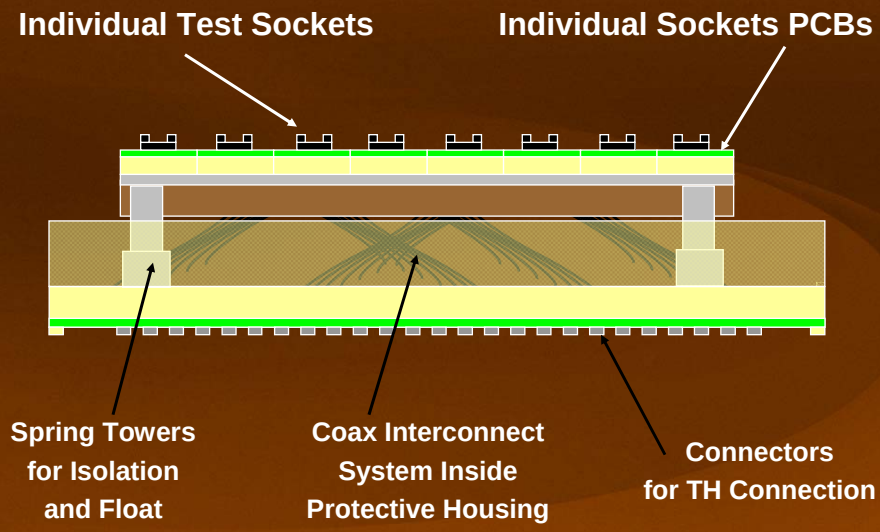
New Test Interface Technology

- Extensive real estate for additional circuitry
- Excellent tri-temp thermal performance
- Excellent planarity & contact
- Excellent impedance control
- Small PCB size
  - Enables high parallelism
  - Reduces PCB yield loss
  - Improves aspect ratio for fine pitch applications
- Modular structure provides repair options

16 DUT
800MHz

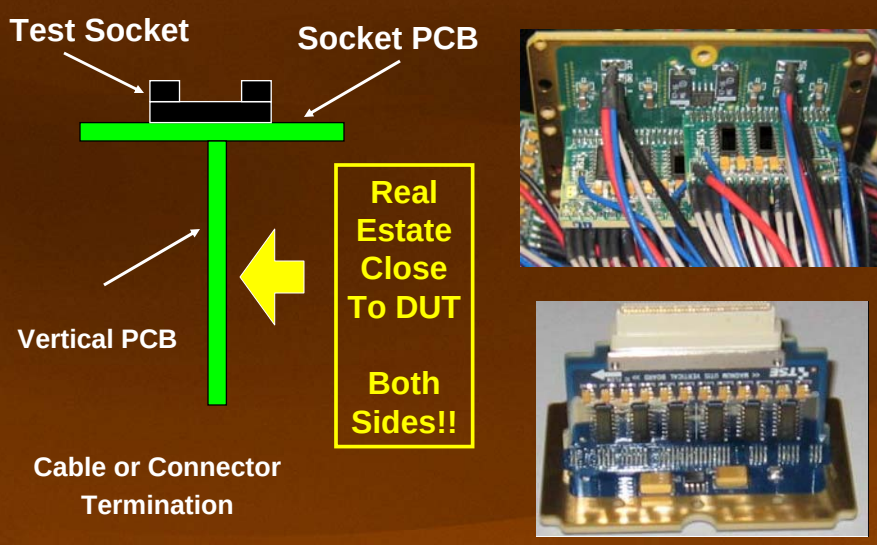
3/2009 Parallel Logic Test Interface Solutions 6

Structure of New Logic Test Interface

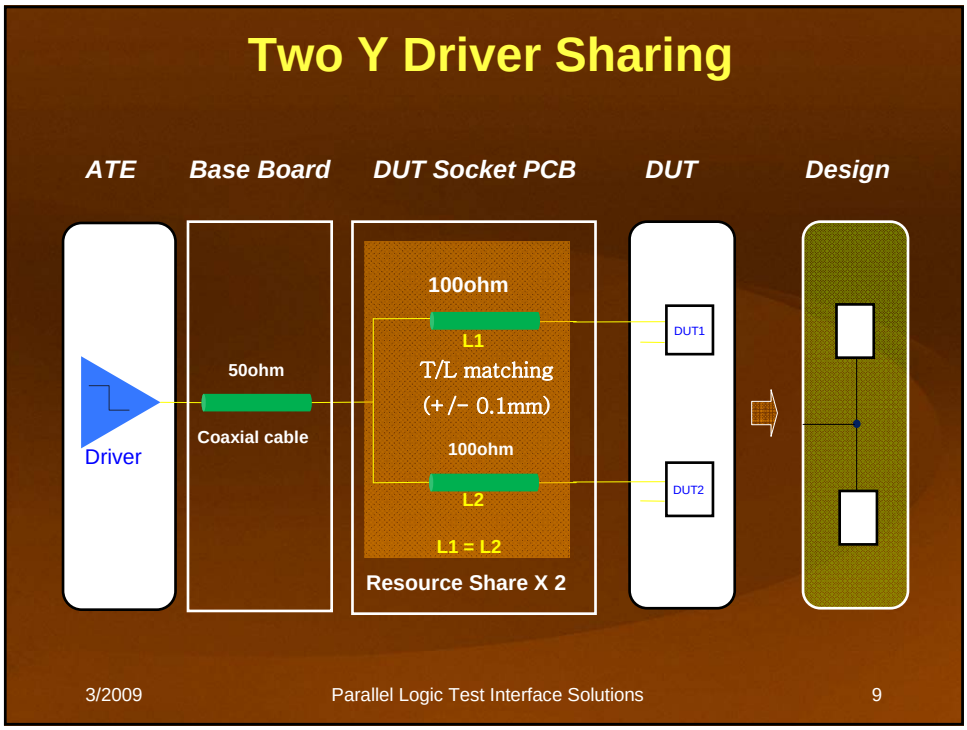


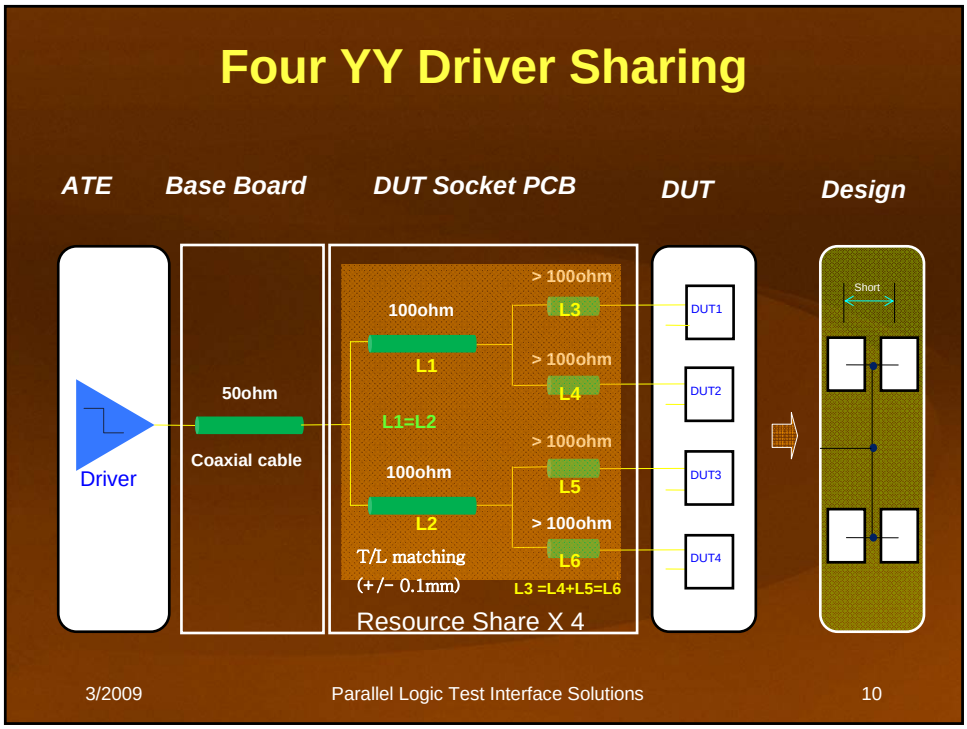
3/2009 Parallel Logic Test Interface Solutions 7

Structure of New Logic Test Interface



3/2009 Parallel Logic Test Interface Solutions 8


Two Y Driver Sharing
ATE
Base Board
DUT Socket PCB
DUT
Design
Driver
50ohm
Coaxial cable
100ohm
L1
T/L matching
(+/− 0.1mm)
100ohm
L2
L1 = L2
Resource Share X 2
DUT1
DUT2
3/2009
Parallel Logic Test Interface Solutions
9


Four YY Driver Sharing
ATE
Base Board
DUT Socket PCB
DUT
Design
Driver
50ohm
Coaxial cable
100ohm
L1
L1=L2
100ohm
L2
T/L matching
(+/− 0.1mm)
> 100ohm
L3
> 100ohm
L4
> 100ohm
L5
> 100ohm
L6
L3 =L4+L5=L6
Resource Share X 4
DUT1
DUT2
DUT3
DUT4
Short
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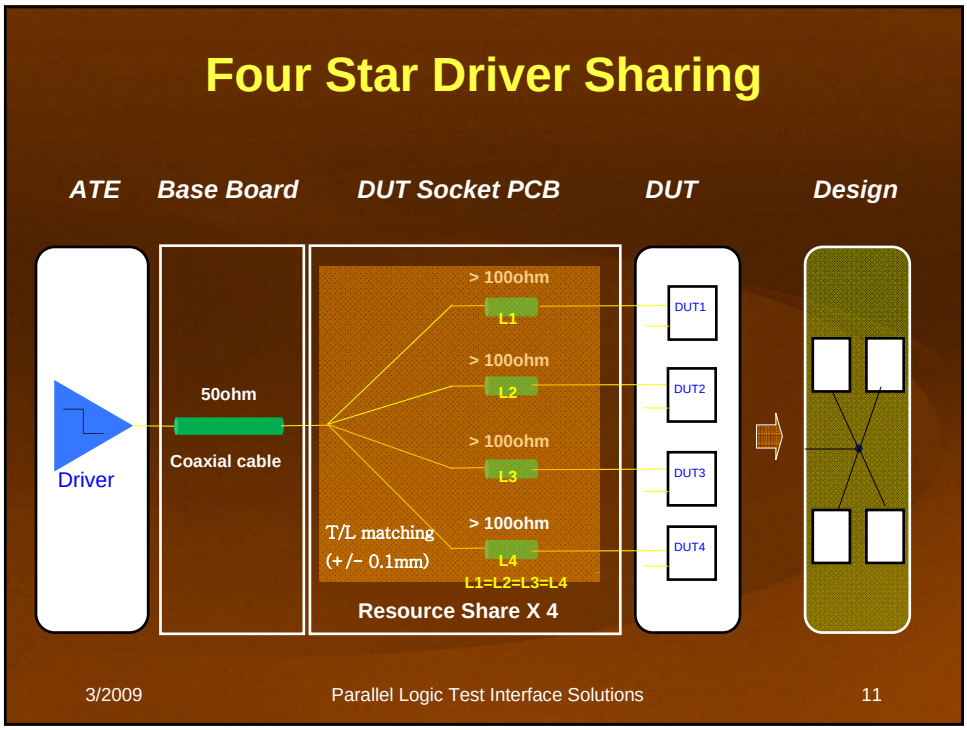
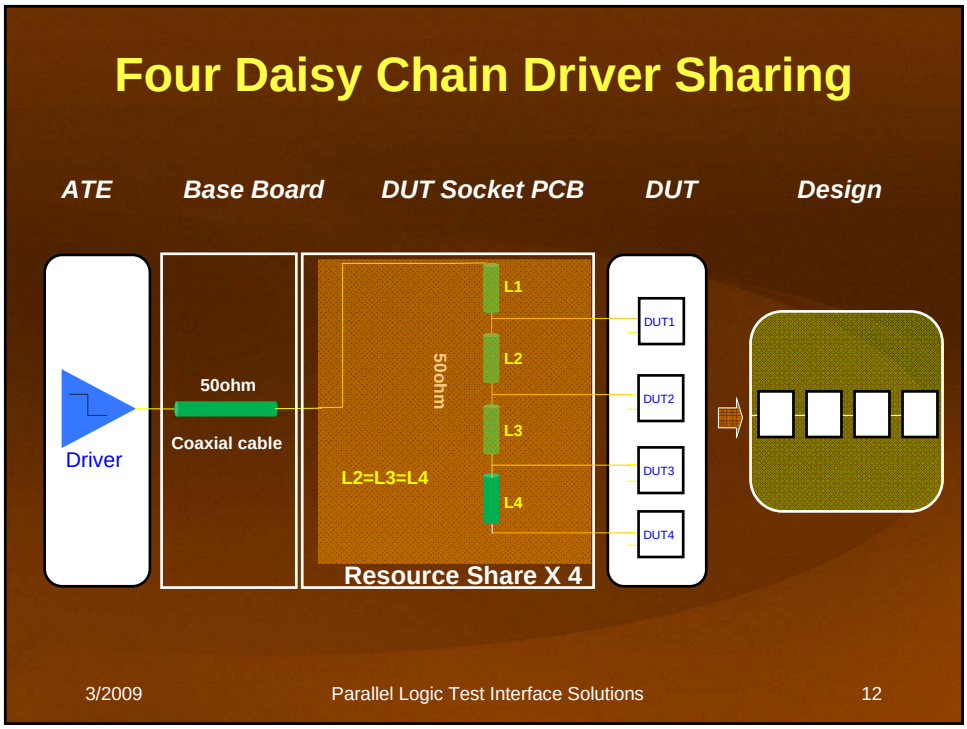
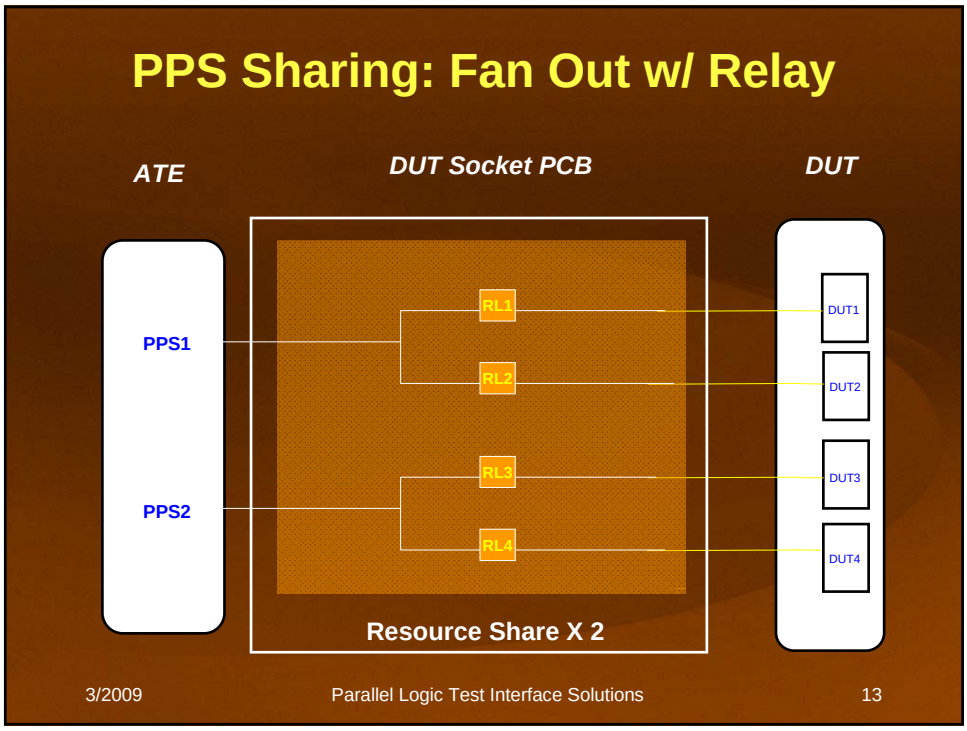
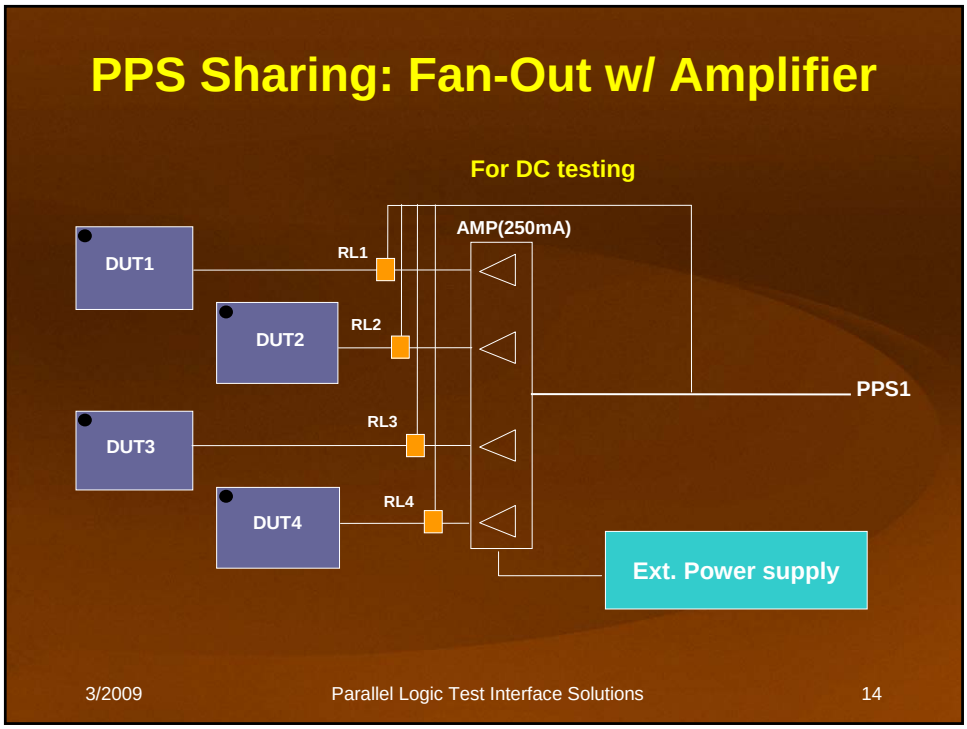
10


Four Star Driver Sharing
ATE
Base Board
DUT Socket PCB
DUT
Design
Driver
50ohm
Coaxial cable
> 100ohm
L1
> 100ohm
L2
> 100ohm
L3
> 100ohm
L4
T/L matching
(+/- 0.1mm)
L1=L2=L3=L4
Resource Share X 4
DUT1
DUT2
DUT3
DUT4
3/2009
Parallel Logic Test Interface Solutions
11

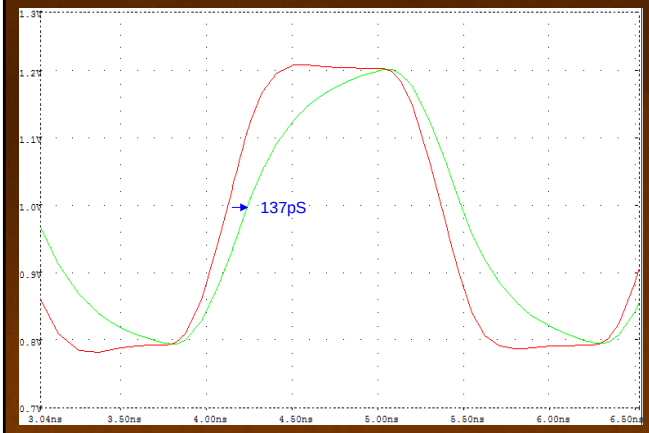

Four Daisy Chain Driver Sharing
ATE
Base Board
DUT Socket PCB
DUT
Design
Driver
50ohm
Coaxial cable
50ohm
L1
L2
L3
L4
L2=L3=L4
Resource Share X 4
DUT1
DUT2
DUT3
DUT4
3/2009
Parallel Logic Test Interface Solutions
12


PPS Sharing: Fan Out w/ Relay
ATE
DUT Socket PCB
DUT
PPS1
PPS2
RL1
RL2
RL3
RL4
DUT1
DUT2
DUT3
DUT4
Resource Share X 2
3/2009
Parallel Logic Test Interface Solutions
13


PPS Sharing: Fan-Out w/ Amplifier
For DC testing
AMP(250mA)
DUT1
DUT2
DUT3
DUT4
RL1
RL2
RL3
RL4
PPS1
Ext. Power supply
3/2009
Parallel Logic Test Interface Solutions
14

Paper #1

Signal Performance: Two Y Sharing



Freq: 400MHz

VIH/VIL: 1.2v / 0.8v

TR / TF: 400pS

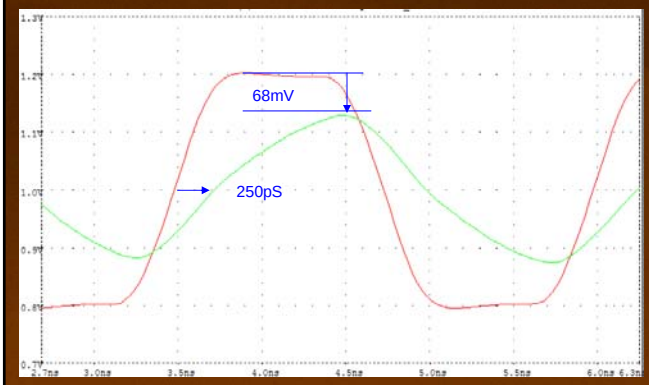
DUT Input Cap:3pF

Red: Non-Share

Green:Two-Share

3/2009 Parallel Logic Test Interface Solutions 15

Signal Performance: Four YY Sharing



Freq: 400Mhz

VIH/VIL: 1.2v / 0.8v

TR / TF : 400pS

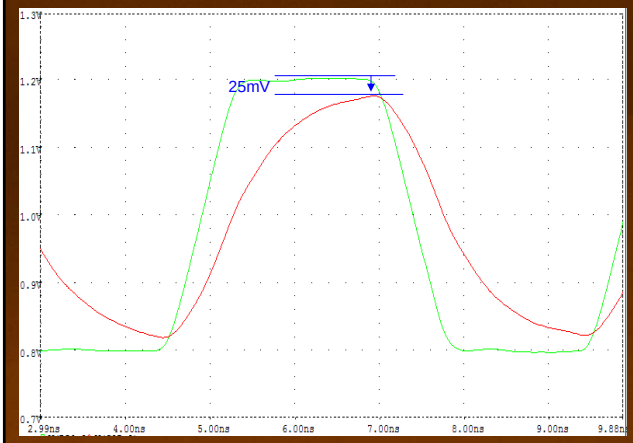
DUT Input Cap:3pF

Red: Non-Share

Green: Four-Share

3/2009 Parallel Logic Test Interface Solutions 16

Signal Performance: Four YY Sharing



Freq: 200Mhz

VIH / VIL: 1.2v/ 0.8v

TR / TF : 800pS

DUT Input Cap:3pF

Green: Non-Share

Red: Four-Share

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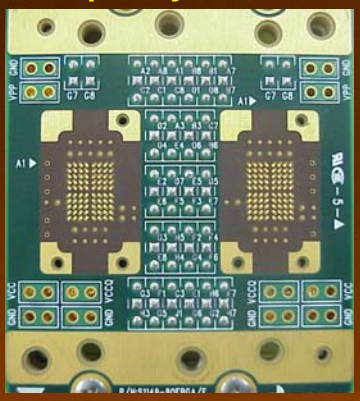
DUT Socket PCBs

Two Y Driver Share

Package: 80FBGA

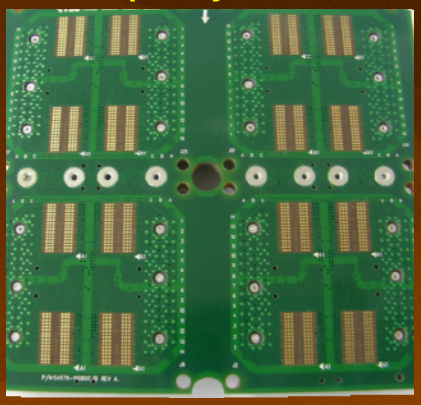
Frequency: 250MHz



Four YY Driver Share

Package: 100BOC

Frequency: 400MHz

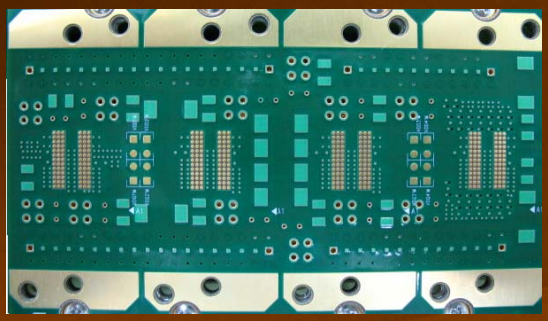


3/2009 Parallel Logic Test Interface Solutions 18

DUT Socket PCBs

Four Daisy Chain Driver Sharing

Package: 78TFBGA
Frequency: 800MHz



3/2009 Parallel Logic Test Interface Solutions 19

32DUT Logic / SOC Test

Package: 176 eTQFP
Frequency: 200MHz

Socket
(Inset Photo)

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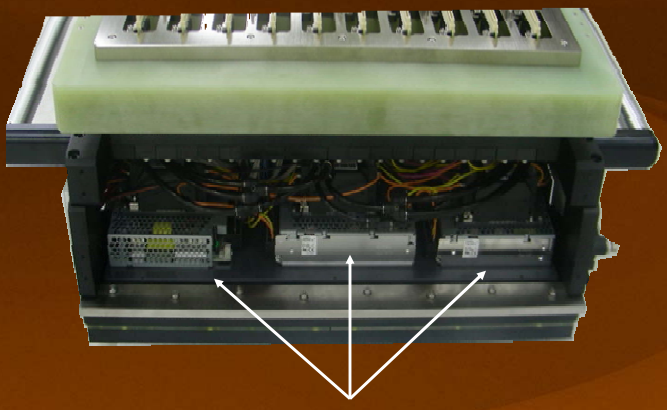
Additional DUT Power Supplies

External PPS System Integrated in Logic Test Interface



External Power Supplies

3/2009 Parallel Logic Test Interface Solutions 21

Parallel Logic / SOC Test Benefits

- Reduce Cost of Test
  - Increased parallelism
  - Reduction of load board design cost
- Maintenance Improvement
  - Individual socket boards are changeable
  - Individual channels to DUT are repairable
- Signal Quality is Improved with Coax
  - Minimize cross talk
  - Excellent impedance control (50ohm)
  - Reduction of TPD

3/2009 Parallel Logic Test Interface Solutions 22

Logic/SOC ATE Considerations

- S/W support of resource sharing modes
- Calibration support of resources sharing modes
- S/W support external power supply options
  - Force, Measure & Calibration
- Test program development tools for parallel testing
- ATE calibration support through interface to DUT

3/2009 Parallel Logic Test Interface Solutions 23

High Parallel Logic Test Is Not For Everybody….

- Short test time may negate benefits of parallel test
  - Consider handler index time
- Consider cost of handler & change kit
- DUT volume may not justify higher parallelism
- Consider change-over time for high mix environment
- Very high I/O & mixed signal still a challenge!
- Signal performance of shared I/O lines
  - Decreased DUT amplitude at comparator
  - I/O turn-around time
  - Am I strobing the DUT or what is in the interface?

3/2009 Parallel Logic Test Interface Solutions 24

Conclusions

- **Parallel Logic / SOC Test Can be Increased….**
  - ✓ Apply parallel memory interface technology
  - ✓ Utilize resource sharing techniques
  - ✓ Utilize memory handlers & change kits
  - ✓ Utilize DFT/BIST/Scan to reduce I/O requirements
  - ✓ Pursue high speed and fine pitch applications
  - ✓ Pursue additional DUT power supply solutions

3/2009 Parallel Logic Test Interface Solutions 25

CID: A New Breakthrough Solution for Contactor Hardware Tracking

Jonathan D. Mondero – TI (Philippines)
Kevin Tiernan – TI (Houston)
Mike Guenther – TI (Houston)
Eugene Batilo – ECT (Singapore)

2009 BiTS Workshop
March 8 - 11, 2009

Presentation Topics

- Background
- Objective / Purpose
- Case for Action – The Current process
- Contactor Recording – How is it done today?
- The Solution: CID – Contactor
- CID Module – Design Architecture / Details
- Tester Hardware Hookups
- Methodology – CID Process Overview
- Results / Conclusions

Background

- Contactor tracking is important for better inventory management and control – for better planning and cost reduction
- Accurate usage records are needed for proactive scheduling of maintenance
- To date, TI had used barcodes to manually track contactors and no accurate usage records exist to associate each contactors on how often it is used

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 3

Objective / Purpose

- We developed a new method of tracking contactors using an EEPROM imbedded on the contactor to provide…
  - Accurate Usage Records
  - Unit-Level Data Association
  - Real Time Monitor (RTM)

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 4

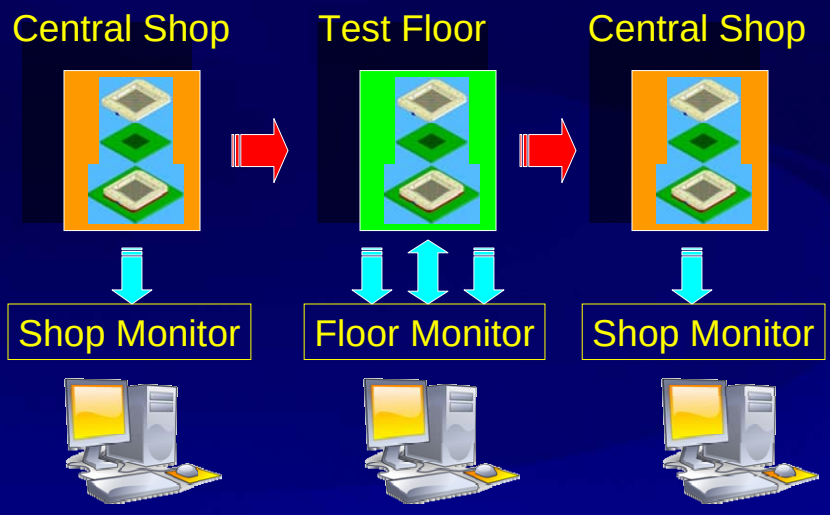
Case for Action – Current Process

Current practices uses sticker barcodes that are not permanent – They lose valuable information (history, insertion, setup issues).

The barcode peel off and fade when run under extreme conditions.

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 5

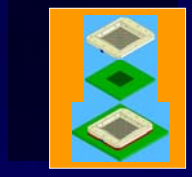
Contactor Recording How is it done today?



3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 6

Contactor Recording How is it done today?

Central Shop



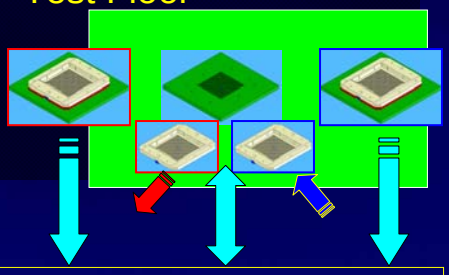
Shop Monitor

- Bring up loadboard screen and scan in loadboard ID
- Scan in contactor(s) ID associated with loadboard before checking out

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 7

Contactor Recording How is it done today?

Test Floor



Floor Monitor

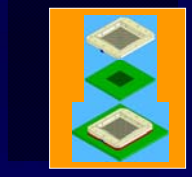
- Scan loadboard ID into SMS before running the lot
- Changing contactor(s) requires scanning out old contactor and scanning new contactor
- Re-scan loadboard before lot begins.

Very Manual Process!

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 8

Contactor Recording How is it done today?

Central Shop



Shop Monitor

- Scan loadboard after returning from the tester
- Scan out contactor(s) before returning the loadboard and contactor for storage.

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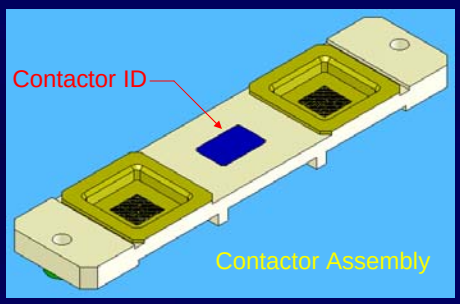
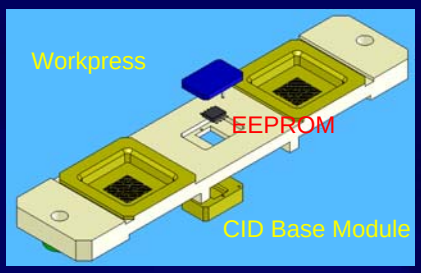
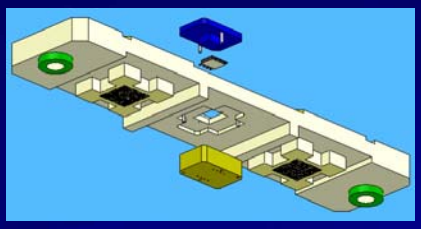
The Solution: CID – Contactor



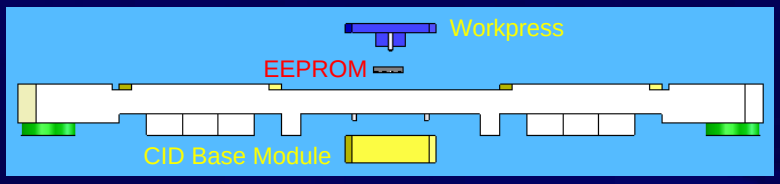


Chip Cap and Resistors will be mounted and routed to the loadboard design.

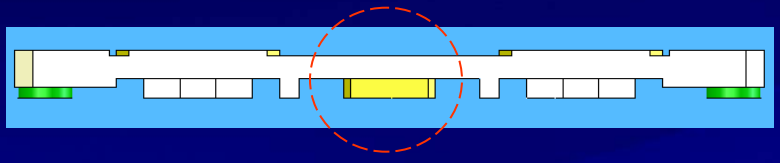


3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 10

CID Module – Design Architecture

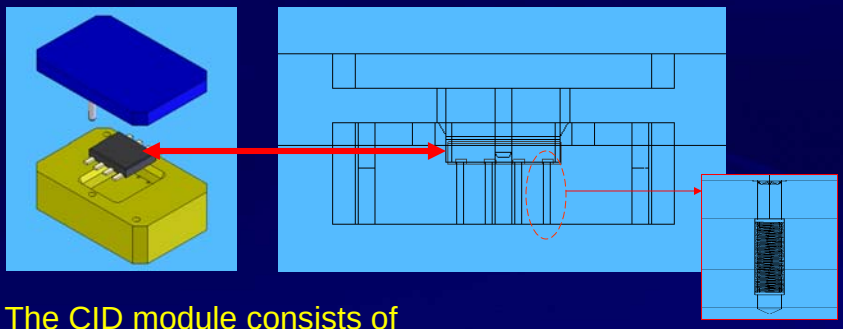


Two guide pins are used to help register alignment to the contactor body



3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 11

CID Module – Design Architecture



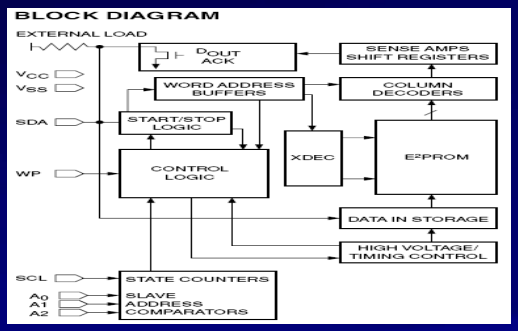
The CID module consists of two piece PEI (Polyetherimide) blocks and with a pin retainer plate that hold the 8 pogo pins that contact with DIB & IC

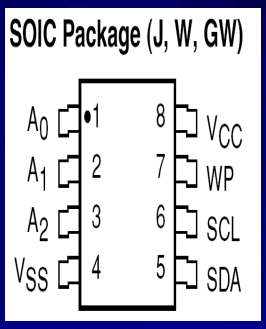
3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 12

CAT24C04WI – EEPROM Details

FEATURES

- 400 kHz I²C Bus Compatible*
- 1.8 to 5.5Volt Operation
- Low Power CMOS Technology
- Write Protect Feature
  — Entire Array Protected When WP at V_{IH}
- Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-pin DIP, SOIC, TSSOP and MSOP packages
  - "Green" package option available
- Commercial, Industrial, Automotive and Extended Temperature Ranges





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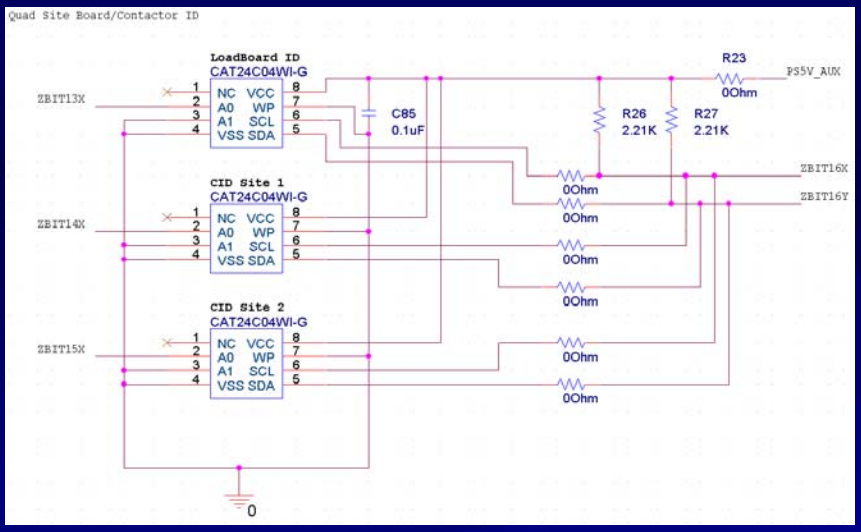
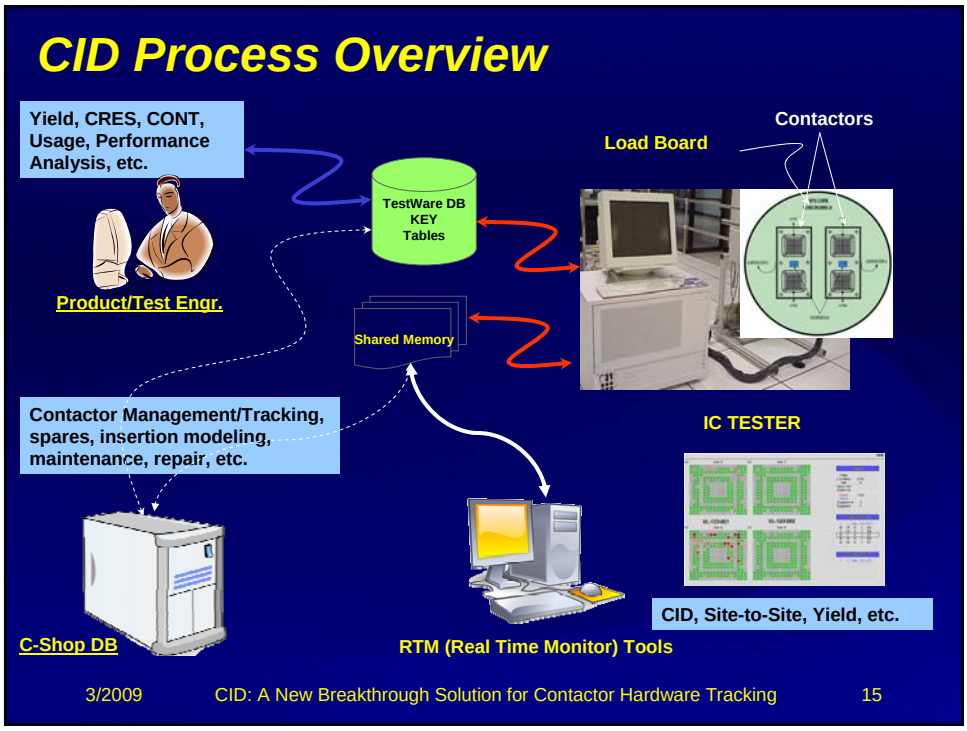
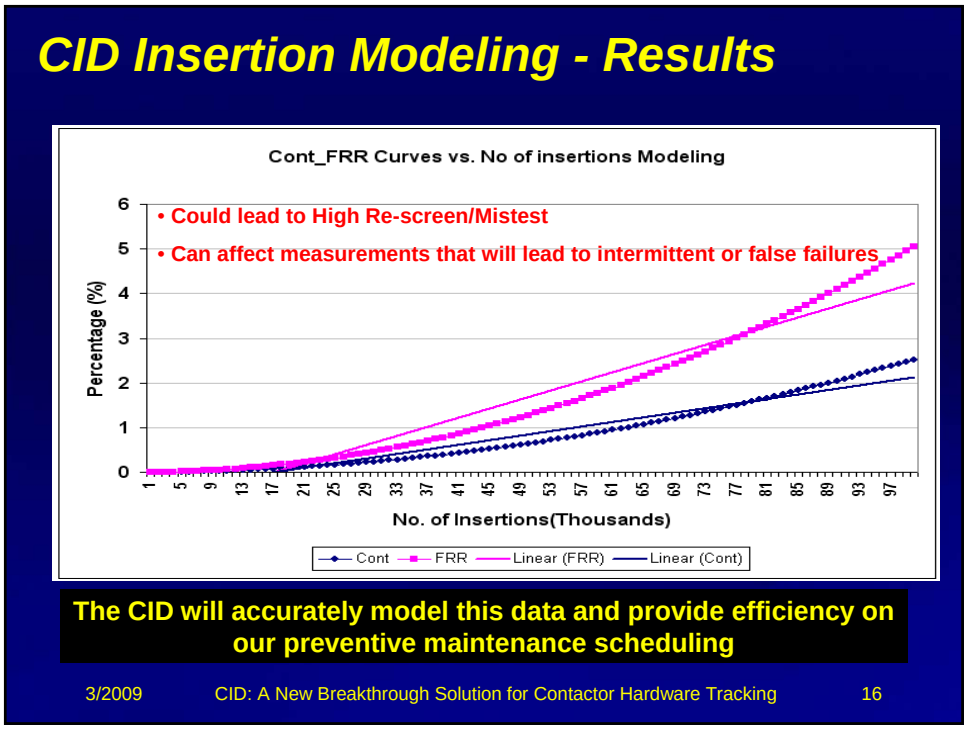
Tester Hardware Hookups



3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 14


CID Process Overview
Yield, CRES, CONT, Usage, Performance Analysis, etc.
TestWare DB KEY Tables
Load Board
Contactors
Product/Test Engr.
Shared Memory
IC TESTER
Contactor Management/Tracking, spares, insertion modeling, maintenance, repair, etc.
CID, Site-to-Site, Yield, etc.
C-Shop DB
RTM (Real Time Monitor) Tools
3/2009
CID: A New Breakthrough Solution for Contactor Hardware Tracking
15


CID Insertion Modeling - Results
Cont_FRR Curves vs. No of insertions Modeling
• Could lead to High Re-screen/Mistest
• Can affect measurements that will lead to intermittent or false failures
Percentage (%)
No. of Insertions(Thousands)
Cont
FRR
Linear (FRR)
Linear (Cont)
The CID will accurately model this data and provide efficiency on our preventive maintenance scheduling
3/2009
CID: A New Breakthrough Solution for Contactor Hardware Tracking
16

Conclusion

- The CID is an intelligent and cost effective solution to improve the way we track contactors automatically
- The CID addresses the need for accurate usage records by associating "Unit Level" data with the contactor being used
- The CID can be implemented at TI without the need for high investment or new system infrastructure
- The CID had been proven to work on DSPS devices

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 17

Business Impact

- **COST**
  - Better Management of Spares and Peripheral
  - Align Capacity planning = Reduce Capital Expenditures
- **CYCLE TIME**
  - Accurate Preventive Maintenance Scheduling = Reduce Downtime
  - More output = On Time Delivery (OTD)
- **YIELD IMPROVEMENTS**
- **EFFICIENCY**

3/2009 CID: A New Breakthrough Solution for Contactor Hardware Tracking 18

Acknowledgements

- Nick DeJesu – TI Software Development Manager
- Glenn Lorig – TI DSP Systems PE Manager
- Gary Dirige – TIPI Product Engineering Manager

Mechanical Reliability Test as Part of Final Test of a Packaged Chip

C-Y Li, T Wooden, SM Low, TM Korhonen
Che-Yu Li and Co, Ithaca, NY
Protos Electronics, Santa Clara, CA
ADE Technologies, Singapore

2009 BiTS Workshop
March 8 - 11, 2009

Background

- Final test of packaged chip typically includes electrical and burn-in test emphasizing electrical performance
- Mechanical reliability test is typically not done
- Mechanical test would identify manufacturing and design defects that can cause early mechanical failures in service
- Omitting mechanical testing can become costly if defective chips are shipped to customer

Mechanical Reliability Test

- Luu Nguyen's team at NSC have shown that power cycle test can be used and is 10x faster compared to thermal cycling test
- Integrated as a part of test socket,
- Stand-alone power cycle system, with many samples at a time

Power Cycle vs. Thermal Cycle

- Accelerated Temperature Cycling (ATC)
  - Most widely used accelerated life test
  - Sample is placed inside test chamber and chamber is cycled between extreme temperatures
  - Time consuming because of the time the chamber needs to reach test temperature
- Power cycling test
  - Heat is generated by powered electronic device
  - More representative of field conditions, because package is heated differentially
  - Typical cycle is faster than in thermal cycling

Previous Research

- 2005 ECTC paper "Powercycling Reliability, Failure Analysis and Acceleration Factors of Pb-free Solder Joints" by K. Setty, G. Subbarayan and Luu Nguyen
- Sample: 36 I/O WLCSP package with Pb-free Sn4Ag0.5Cu solder joint
- Test: Power cycle 0-100 °C and Temperature cycle -40-125 °C, followed by failure analysis including destructive SEM analysis
- Test Results:
  - Power cycle: cycle time 10 min, failed after 2368 cycles
  - Temperature cycle: cycle time 60 min, failed after 1368 cycles
  - Failure mechanism similar in both samples

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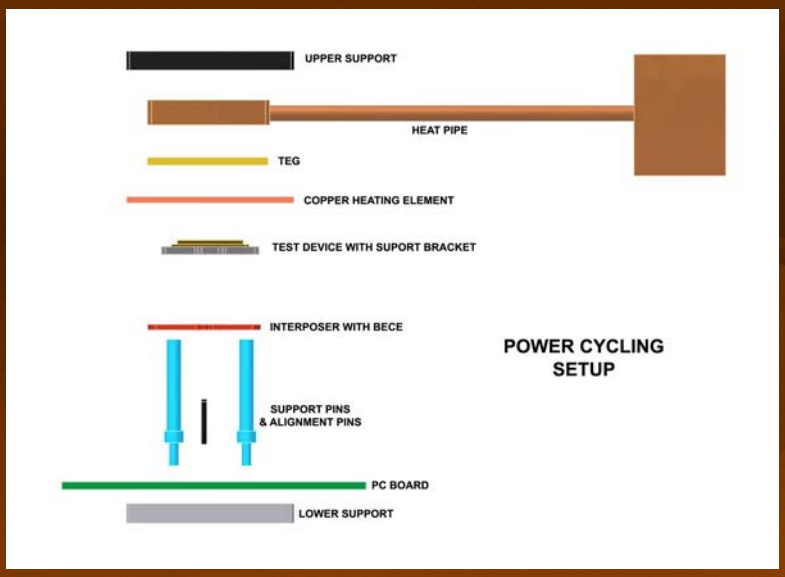
Power Cycle Test Set-Up



3/2009 Mechanical Reliability Test as Part of Final Test of a Packaged Chip 6

Power Cycle Test Details

- Heating plate was made from 90 mil thick copper plate. Grooves were cut in the copper plate in which nichrome 60 resistance wire was inserted. The heating element was driven by HB-25 motor controller with PWM frequency of 9.2khz and a load current limit of 25 amps.
- 42 watt Thermoelectric/Peltier Module was placed next to heating plate. The device was used in the heating cycle to heat the device on one side with the added advantage of cooling the heat pipe and the upper aluminum support on the other side. By reversing the power to the Peltier module we were able to shorten the heating and cooling times.
- The heat pipe was placed on top of the Peltier module. To quickly remove the heat, the other end of the heat pipe was put in an enclosure with a fan.

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Power Cycle Test Details (cont.)

- Three thermistors were used to monitor the procedure: one on the device to be tested, one on the heat pipe next to the heater, and the last on the heat pipe inside the fan enclosure. Temperatures were taken every 1000ms.
- The system was controlled and monitored by a Parallax Basic Stamp board and processor. The processor ran full power to the heat plate up to 95 degrees C and then the program adjusted current and timing to maintain 100 degrees C. After the prescribed time holding the temperature at 100 degrees C, the program turned the heat plate off, the fan on, and the reversed voltage to the Peltier module for cooling. After reaching 0 degrees C the cycle repeats.

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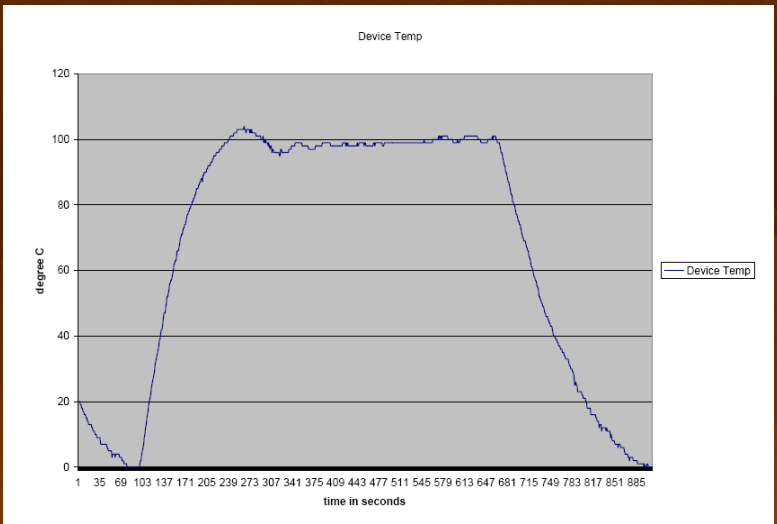
Device Temperature



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Test Socket Requirements

- Test socket with integrated power cycling unit
- Monitor changes in resistance during mechanical testing
- Low noise is essential to capture changes in resistance due to crack growth
- Most test sockets do not have good enough electrical performance

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Test Socket Requirements

- Low & stable resistance of electrical contact
  - Failure monitoring
  - High service temperature
  - High power, high current
- Other requirements
  - High frequency
  - Large array
  - Fine contact pitch

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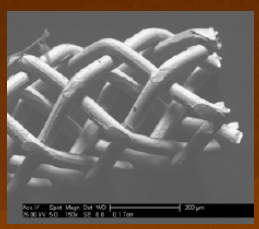
Braided Electrical Contact Element BeCe™

- Meets requirements
- Multiple helical springs operating in parallel

BeCe SEM Image of Tip as Cut



BeCe SEM Image of Tip Plated

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Attributes of BeCe™

- Low Contact Force -- Large Array
- High Compliance -- Low Inductance / High Frequency
- Low Resistance -- High Power
- Small OD -- Fine Contact Pitch
- Plated Stainless Steel Wire -- High Service Temperature
- Multiple Contact Tips -- Redundancy
- Medical Grade Braiding Wire -- Durability

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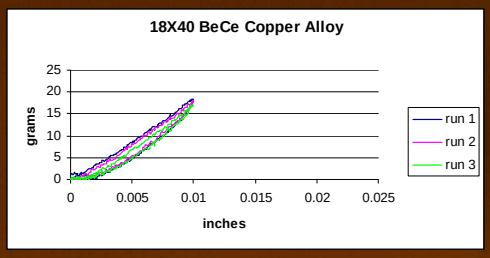
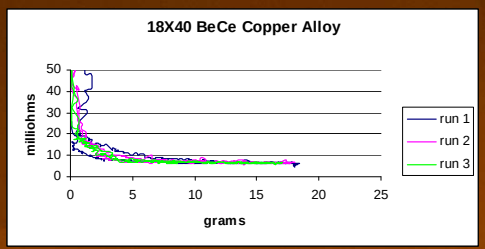
Single Pin Test Data

BeCe (Copper alloy)

- **Low Force**
  <2 g/mil
- **Low Resistance**
  <10 milliohms
- **High Compliance**
  >25% of uncompressed height





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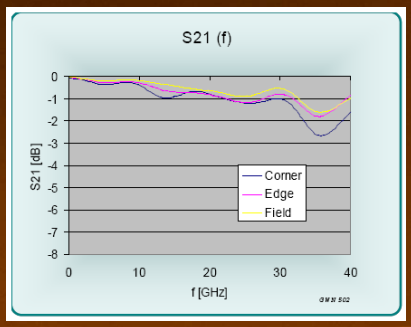
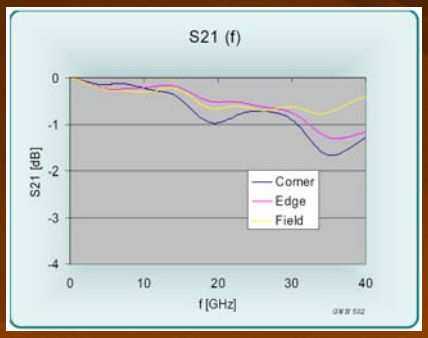
High Frequency Data

1.0 mm pitch,
5x5 array 40 mil height



0.3 mm pitch,
5x5 array 40 mil height



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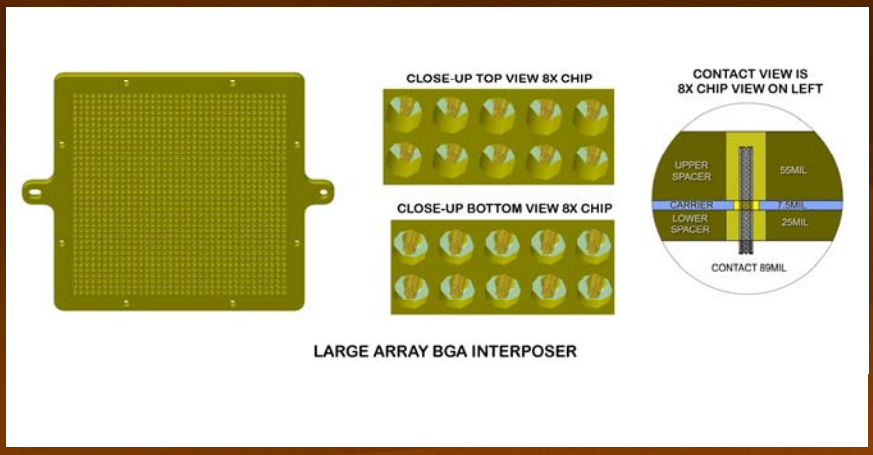
BGA Interposer



3/2009 Mechanical Reliability Test as Part of Final Test of a Packaged Chip 16

BeCe Data for BGA Interposer

- 1 mm or 0.8 mm pitch
- 1.5 on 8 copper alloy BeCe
- 80 mil BeCe height
- 14 mil OD
- Resistance 7 mΩ
- Inductance 0.6 nH
- Compliance 20%
- Array to 5000 I/O

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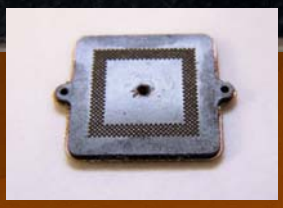
LGA Interposer

- 0.3mm pitch
- 400 I/O
- 60 mil high, 6 mil OD
- Inductance 0.6 NH
- Resistance 20 mΩ
- Contact Force <10g per I/O
- Compliance 20%



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Proposed Usage

- Integrated test socket for final test and mechanical reliability test ➔ Power cycle for 5 days ➔ ATE
- Multiple cell stand-alone system for burn-in test and mechanical reliability test ➔ Periodically to test socket and ATE

3/2009 Mechanical Reliability Test as Part of Final Test of a Packaged Chip 19

Conclusions

- Time Effective Power Cycle System Possible
- BeCe contact element meets requirements:
  - Low and stable resistance
  - High service temperature
  - High current
  - High frequency
  - Large array
  - Fine contact pitch

3/2009 Mechanical Reliability Test as Part of Final Test of a Packaged Chip 20

Substrate Bias: Application in Final Test and Burn-in of High-Power CPU's

Max Paransky
Texas Instruments

2009 BiTS Workshop
March 8 - 11, 2009

High-Power Burn-in

Conditions determined by process technology and reliability requirements:

- Chip area coverage
  - > Exercise all key structures (logic, memory, IO's)
- Time duration
- Voltage levels
  - > All transistors types powered above their normal use conditions
- Temperature
  - > Silicon Tj above use conditions

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Burn-in Oven

Burn-in ovens, boards and sockets have constraints:

- Thermal budget
  - > Finite cooling capability per DUT
- Power budget
  - > Only so many power supplies and amps per board

Problem!

These constraints limit how many units can be loaded at a time

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How to Increase Throughput?

- Reduce DUT power by lowering Vdd, Temp or both
  - > Possible with extended duration (and lots of reliability modeling)
  - > Usually economically impractical
- Apply transistor substrate bias
  - > Reduce DUT power without changes to Vdd and temperature setpoints

What's substrate bias?

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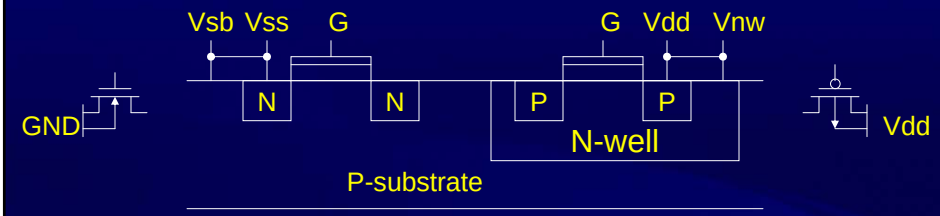
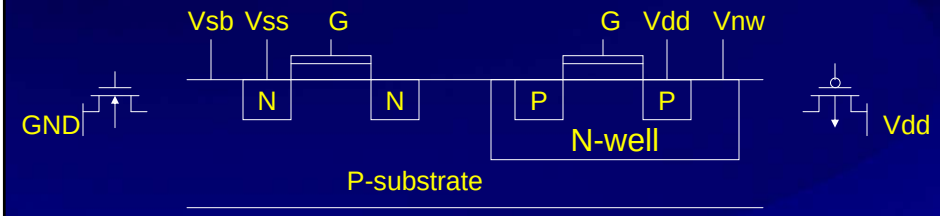
Transistor Substrate Bias



3-terminal device: no substrate bias, Vsb = Vss, Vnw = Vdd



4-terminal device: biased substrate, Vsb ≠ Vss, Vnw ≠ Vdd

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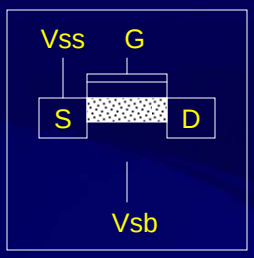
Reverse Bias Mechanism

- Increased potential across the transistor
  - > More V needed to create inversion layer in channel, so Vt increases



- Idsat α (Vgs – Vt)
  - > With fixed Vgs (Vdd) there is now less charge to carry channel current Idsat
  - > As Vt increases, Idsat decreases, and therefore total DUT power decreases

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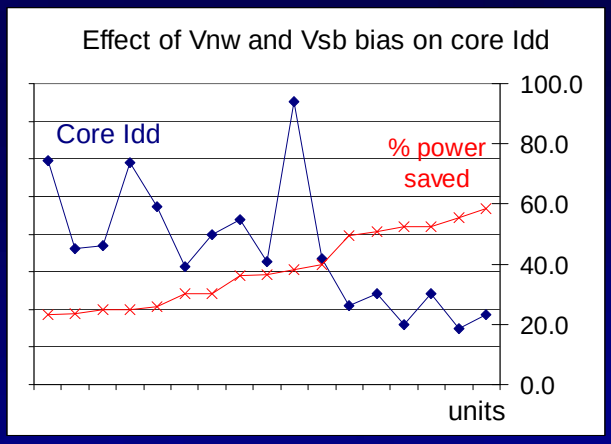
Burn-in Data

Average 38% of power saved by reverse substrate bias
> Unit-to-unit savings range is 23% - 58%

Vnw = Vdd + 0.5V
Vsb = - 0.5V



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Oven Complications

- **Vnw is positive**
  - **> But occupies oven power supplies that could otherwise be used for core Vdd**
- **Vsb is negative**
  - **> Oven doesn't have a negative power supply**
  - **> A custom board-level circuit was added for +DC/-DC conversion**
- **Adjust thermal control to avoid under-temps for low-power samples**
  - **> Tune oven heat/cool rate of response**
  - **> Tune oven ambient temperature**

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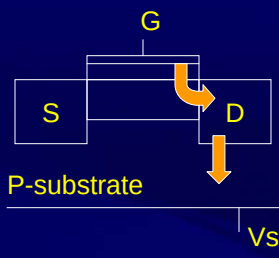
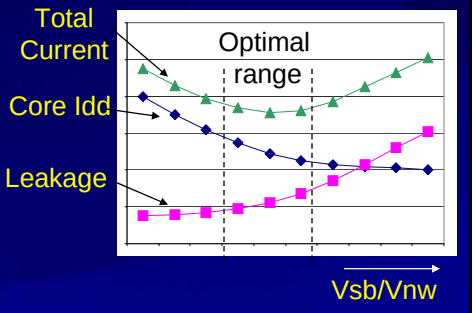
Device Limitations

Increased gate-substrate potential has negative effects:

- **Wider channel**
  - **> Gate-drain leakage increase**
- **Higher drain-substrate junction potential**
  - **> Drain-substrate leakage increase**
- **Optimal range of substrate bias**
  - **> Beyond that combined leakage overwhelms any Idd savings and total current actually increases**





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Burn-in Throughput

Power savings with substrate bias are projected to:

- **Reduce fallout due to BI power by 66%**
  - **> Good units previously beyond oven cooling capacity**
- **Increase weekly BI throughput by 75%**
  - **> Optimized DUT per board loading**

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Test and System

- ATE
  - > High speed / high power testing pushes cooling capability of handlers
- End system
  - > High speed / high power real applications push system cooling capabilities

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Mechanism Revisited

- Idsat α (Vgs – Vt)
  - > Fixed Vgs (Vdd) and adjustable Vt:
    - a) Modulate Idsat and total DUT power
    - b) Modulate switching time and overall chip performance (max frequency)

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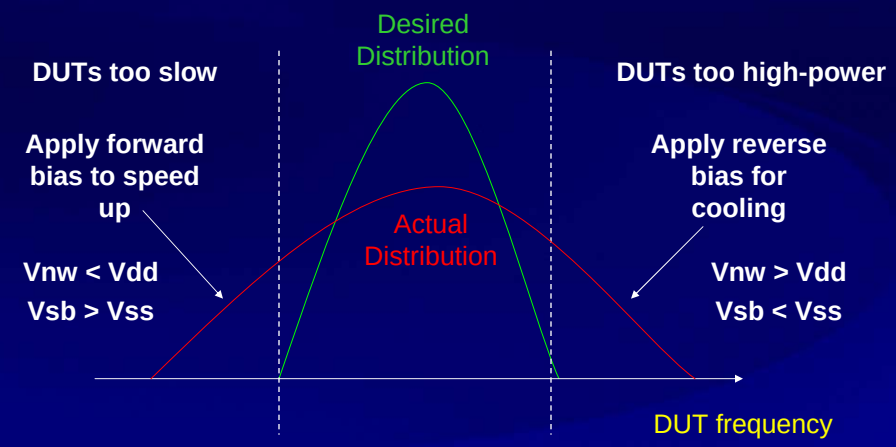
Frequency Applications



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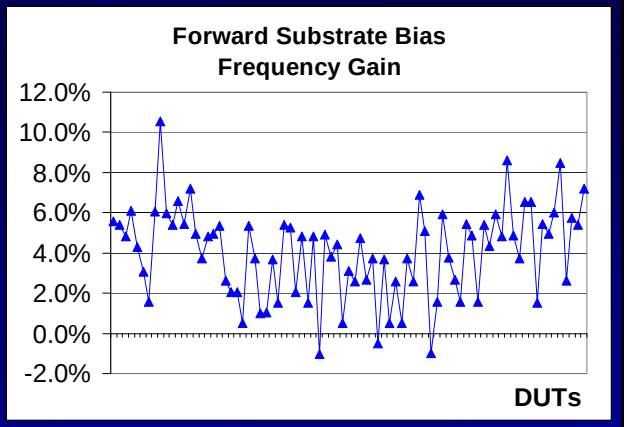
Tester Frequency Data

On average 4% of DUT frequency gained by forward substrate bias

Vnw = Vdd - 0.3V
Vsb = 0.3V



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Conclusion

Modulating substrate bias allows:

- **Increased BI yield due to power/cooling fallout**
- **Optimized BI oven/board resource use**
- **Increased max frequency on slow devices in test/system**
- **Cooling for fast/leaky devices in test/system**

Thank You!