BiTS™ Burn-in & Test Socket Workshop 2009 **Session 2**

ARCHIVE 2009

NOVEL APPROACHES TO SOCKET DESIGN

PoP Contactor - Challenges and Solutions

Jiachun (Frank) Zhou, Siang Soh, David B. Bogardus, Brian L. Hahn
—Antares Advanced Test Technologies

A Bias Clip System for the IC Alignment

Hide Furukawa—Sensata Technologies, Inc.
Hideyuki Takahashi—Sensata Technologies Japan

High Temperature, Fast Turnaround Modular Burn-in Socket

Rick A. Taylor, Stefan Lang, Ernie Frain—EP Ants GmbH

New PTB / High Power Kelvin Test Socket Concept

Gerhard Gschwendtberger—Multitest Elektronische Systeme GmbH

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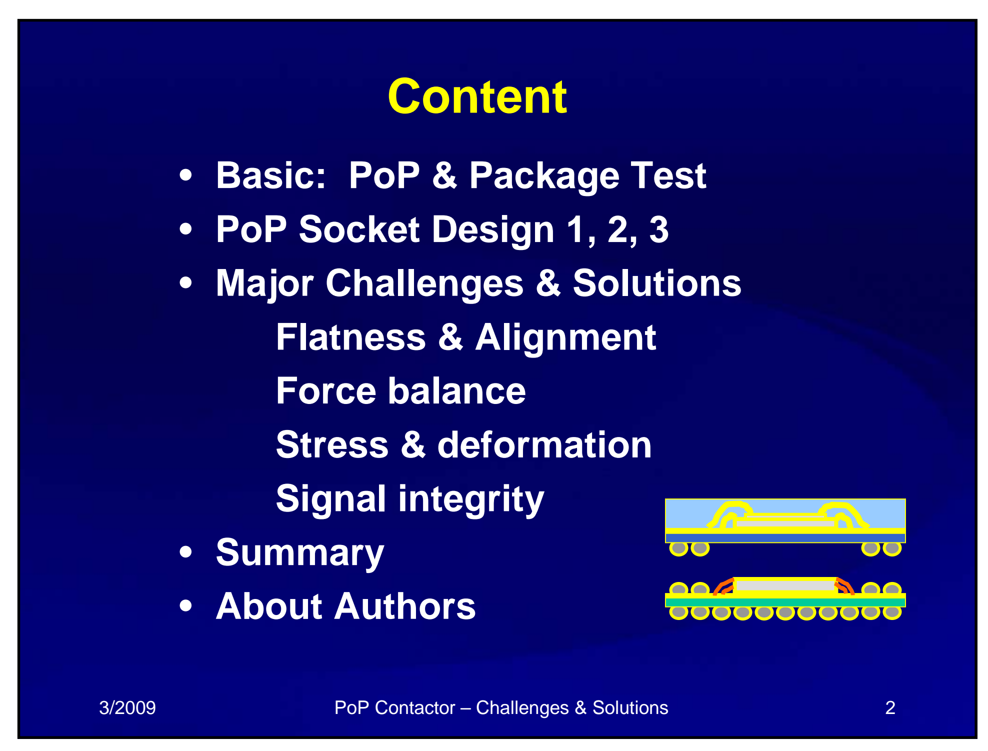
PoP Contactor –
Challenges & Solutions
Jiachun Zhou (Frank)
Siang Soh, David B. Bogardus
Brian L. Hahn (presenter)
Antares Avanced Test Technologies
BiTS
Burn-in & Test Socket Workshop
2009 BiTS Workshop
March 8 - 11, 2009
antares
Advanced Test Technologies


Content
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• PoP Socket Design 1, 2, 3
• Major Challenges & Solutions
Flatness & Alignment
Force balance
Stress & deformation
Signal integrity
• Summary
• About Authors
3/2009
PoP Contactor – Challenges & Solutions
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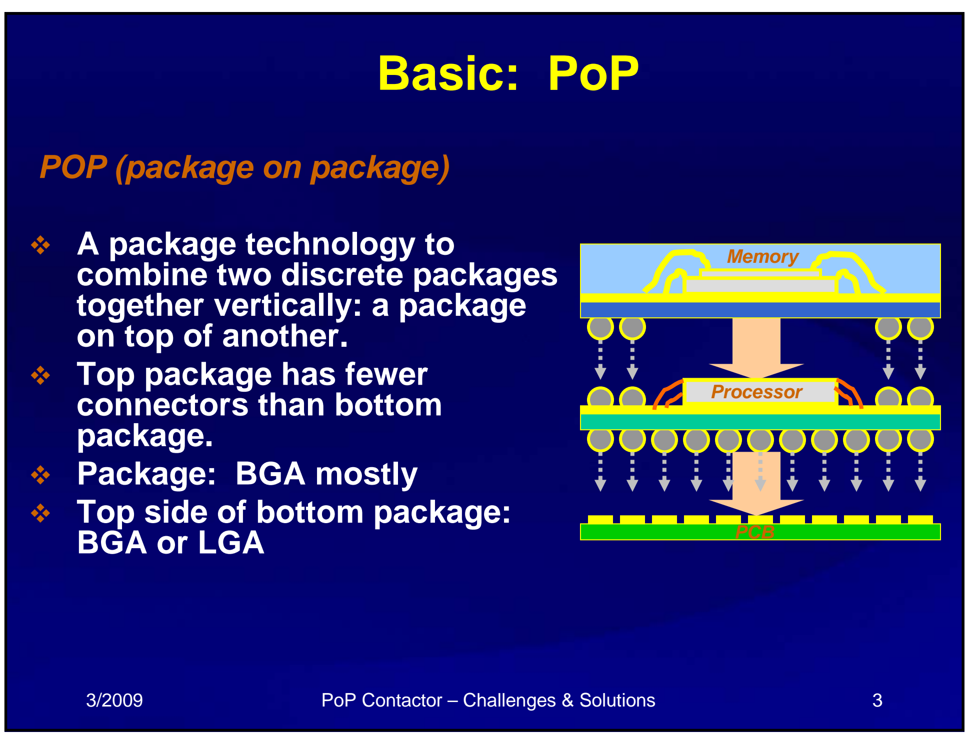

Basic: PoP
POP (package on package)
A package technology to combine two discrete packages together vertically: a package on top of another.
Top package has fewer connectors than bottom package.
Package: BGA mostly
Top side of bottom package: BGA or LGA
Memory
Processor
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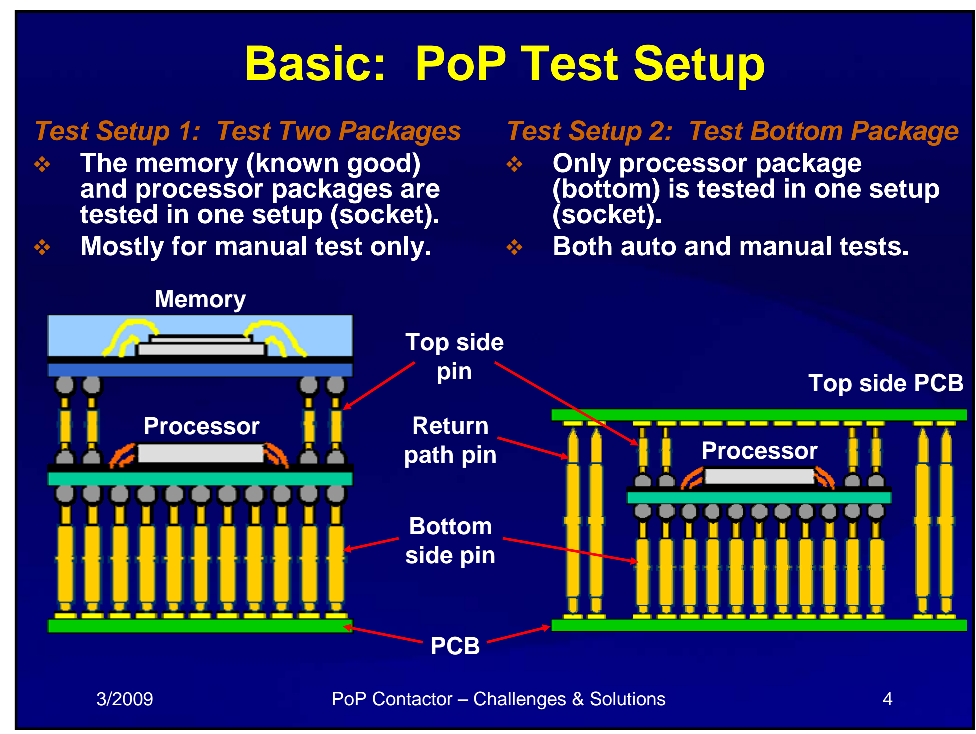

Basic: PoP Test Setup
Test Setup 1: Test Two Packages
The memory (known good) and processor packages are tested in one setup (socket).
Mostly for manual test only.
Test Setup 2: Test Bottom Package
Only processor package (bottom) is tested in one setup (socket).
Both auto and manual tests.
Memory
Processor
Top side pin
Return path pin
Bottom side pin
PCB
Top side PCB
Processor
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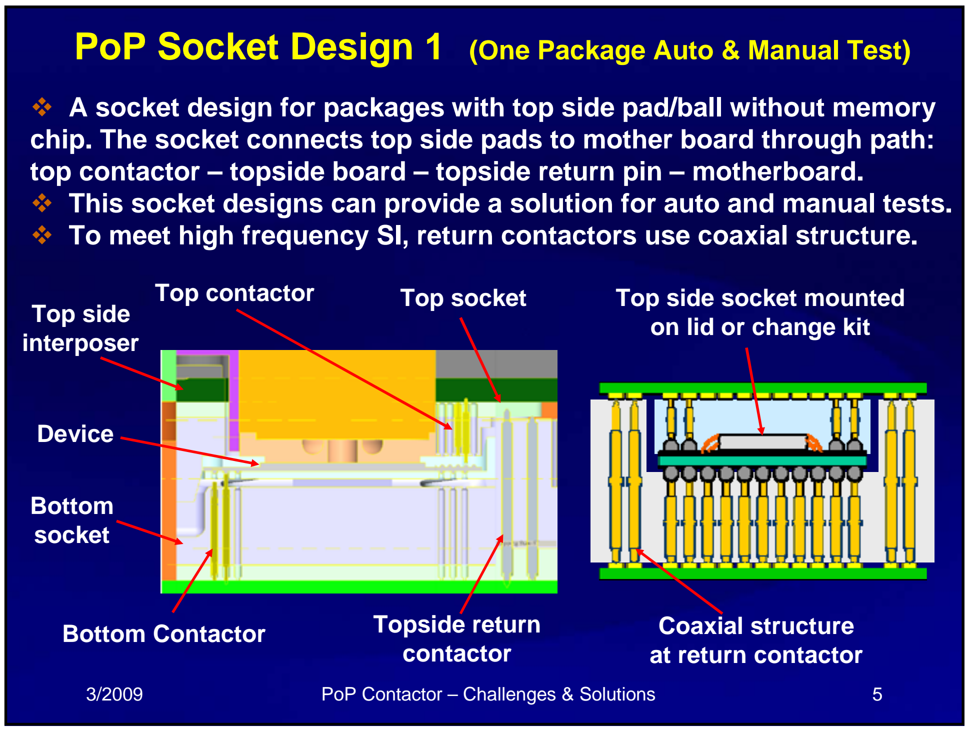
PoP Socket Design 1 (One Package Auto & Manual Test)
A socket design for packages with top side pad/ball without memory chip. The socket connects top side pads to mother board through path: top contactor – topside board – topside return pin – motherboard.
This socket designs can provide a solution for auto and manual tests.
To meet high frequency SI, return contactors use coaxial structure.
Top contactor
Top socket
Top side socket mounted on lid or change kit
Top side interposer
Device
Bottom socket
Bottom Contactor
Topside return contactor
Coaxial structure at return contactor
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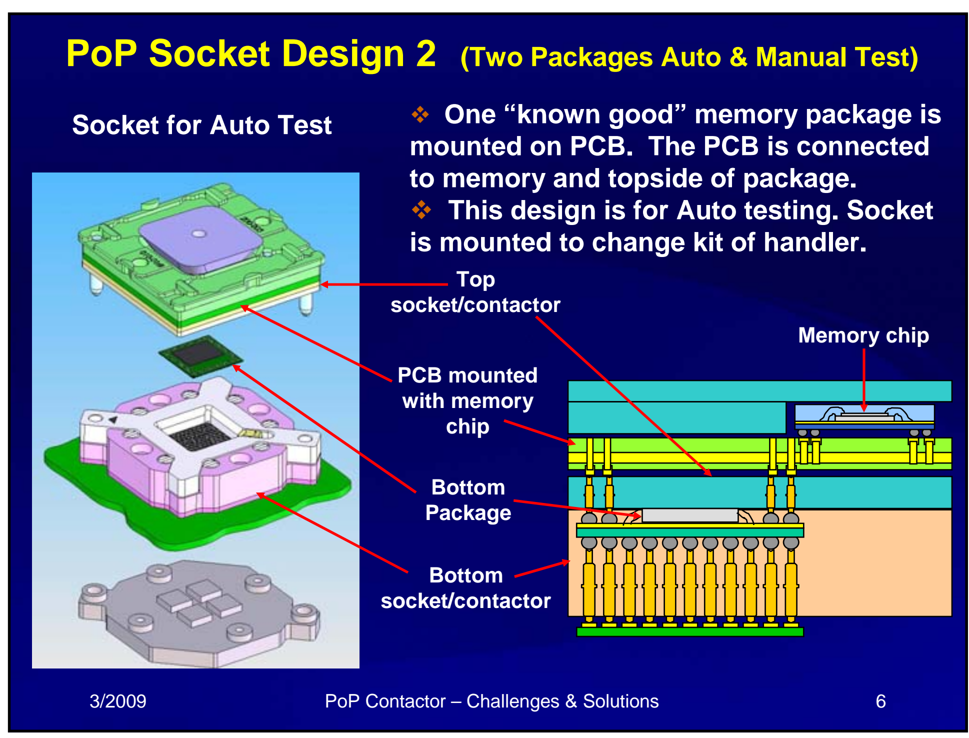
PoP Socket Design 2 (Two Packages Auto & Manual Test)
Socket for Auto Test
One "known good" memory package is mounted on PCB. The PCB is connected to memory and topside of package.
This design is for Auto testing. Socket is mounted to change kit of handler.
Top socket/contactor
Memory chip
PCB mounted with memory chip
Bottom Package
Bottom socket/contactor
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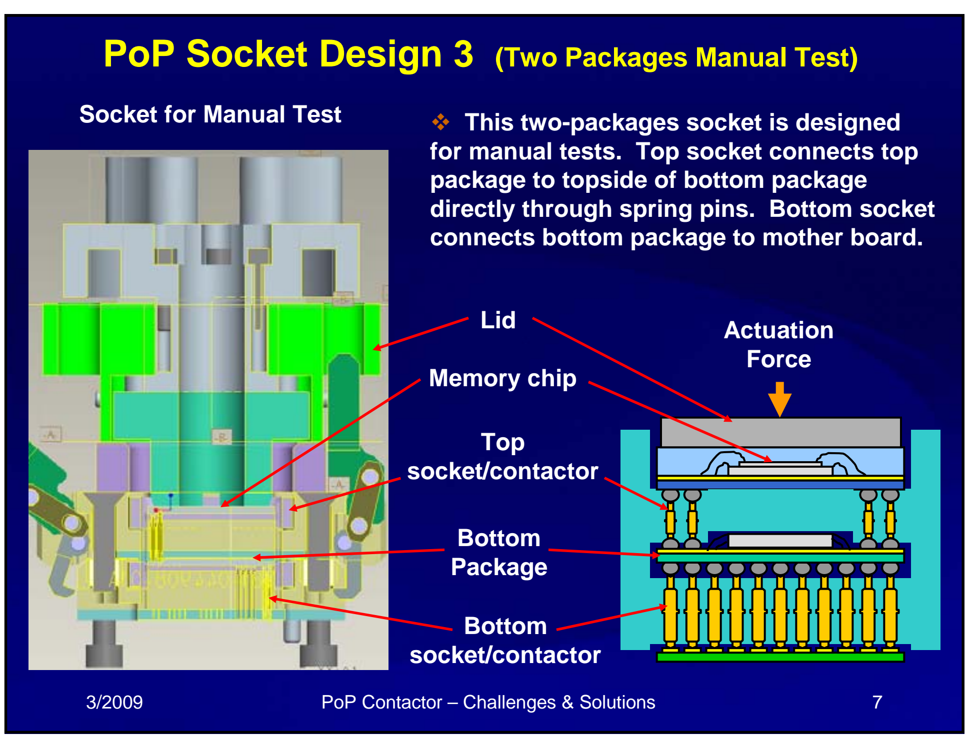
PoP Socket Design 3 (Two Packages Manual Test)
Socket for Manual Test
This two-packages socket is designed for manual tests. Top socket connects top package to topside of bottom package directly through spring pins. Bottom socket connects bottom package to mother board.
Lid
Memory chip
Top socket/contactor
Bottom Package
Bottom socket/contactor
Actuation Force
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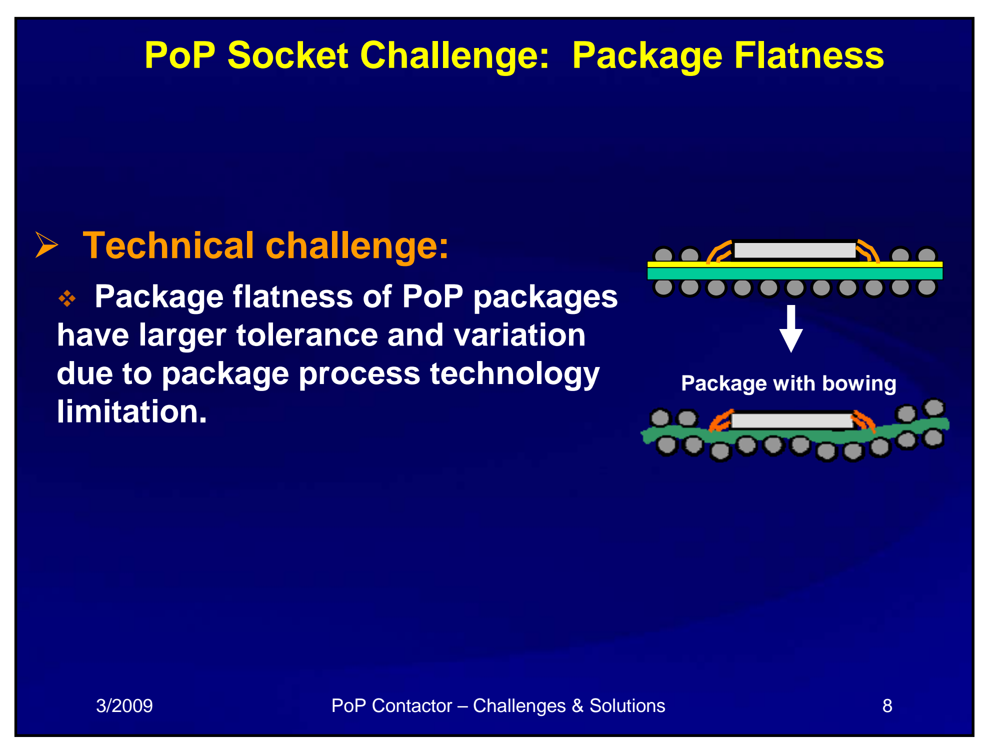
PoP Socket Challenge: Package Flatness
Technical challenge:
Package flatness of PoP packages have larger tolerance and variation due to package process technology limitation.
Package with bowing
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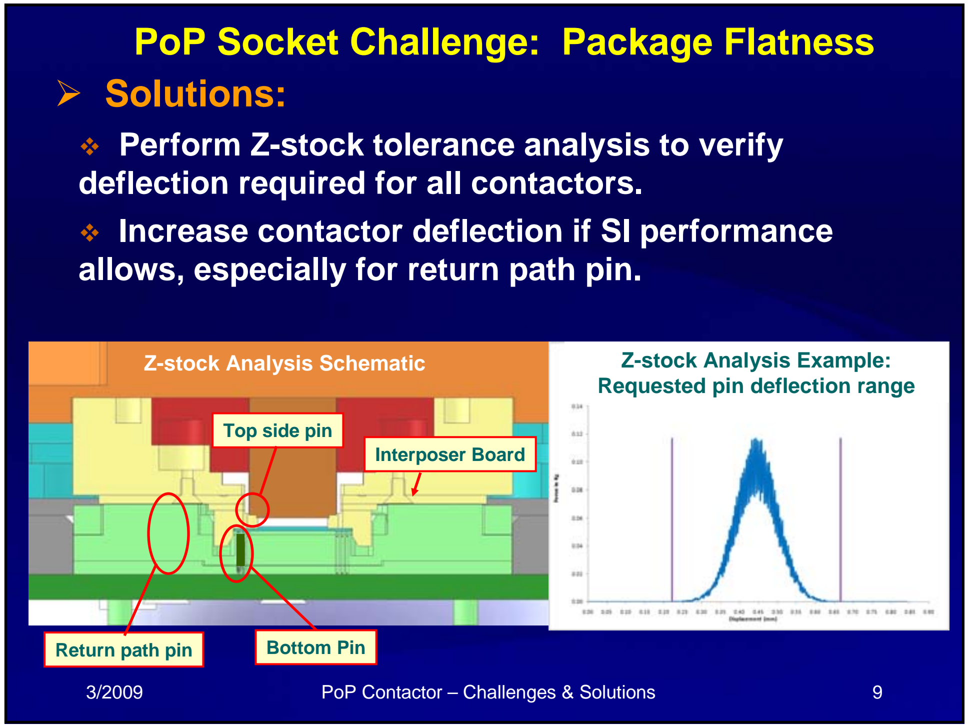
PoP Socket Challenge: Package Flatness
Solutions:
Perform Z-stock tolerance analysis to verify deflection required for all contactors.
Increase contactor deflection if SI performance allows, especially for return path pin.
Z-stock Analysis Schematic
Top side pin
Interposer Board
Return path pin
Bottom Pin
Z-stock Analysis Example:
Requested pin deflection range
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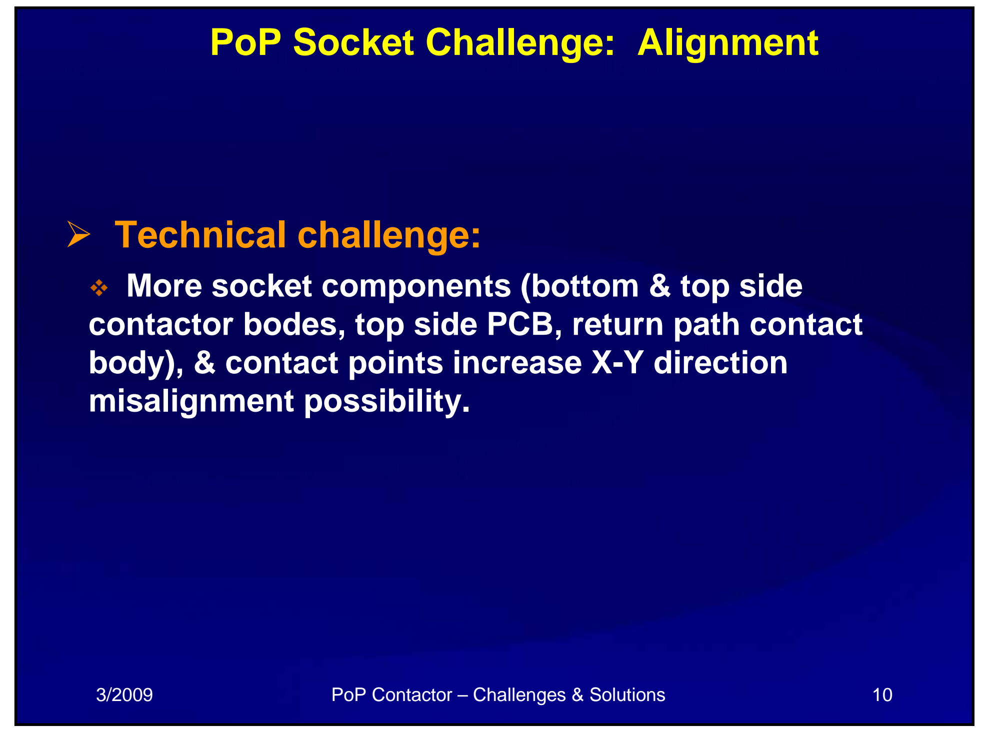
PoP Socket Challenge: Alignment
Technical challenge:
More socket components (bottom & top side contactor bodes, top side PCB, return path contact body), & contact points increase X-Y direction misalignment possibility.
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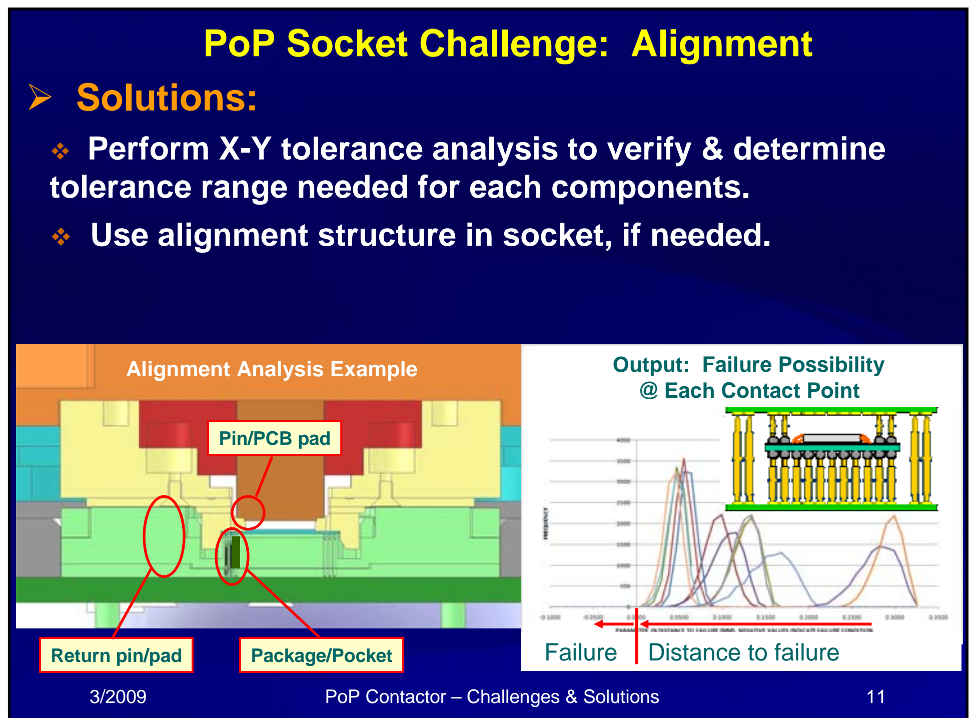
PoP Socket Challenge: Alignment
Solutions:
Perform X-Y tolerance analysis to verify & determine tolerance range needed for each components.
Use alignment structure in socket, if needed.
Alignment Analysis Example
Pin/PCB pad
Return pin/pad
Package/Pocket
Output: Failure Possibility
@ Each Contact Point
Failure
Distance to failure
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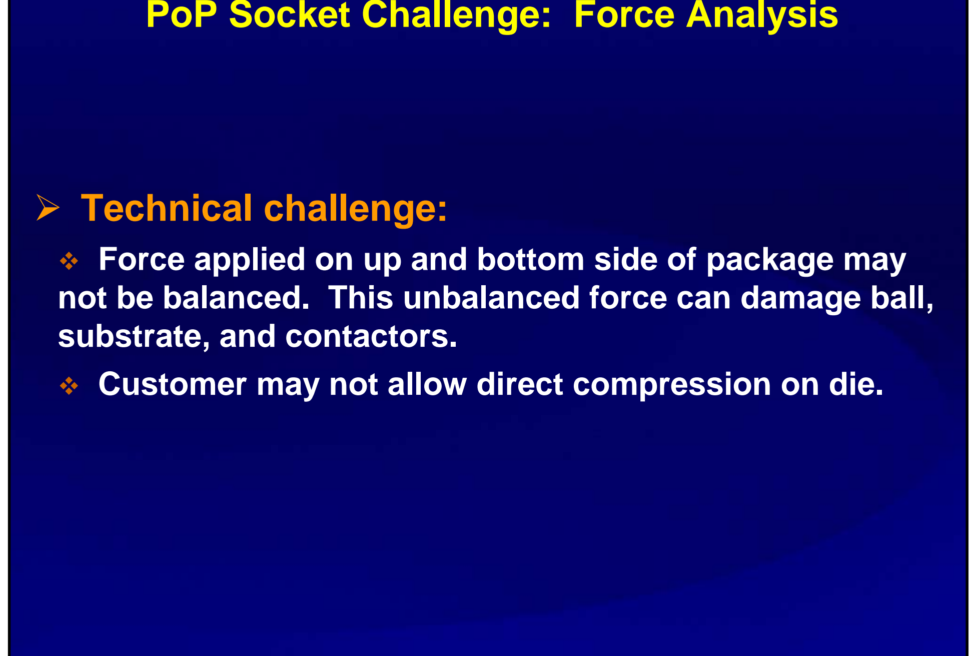
PoP Socket Challenge: Force Analysis
Technical challenge:
Force applied on up and bottom side of package may not be balanced. This unbalanced force can damage ball, substrate, and contactors.
Customer may not allow direct compression on die.
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PoP Socket Challenge: Force Analysis

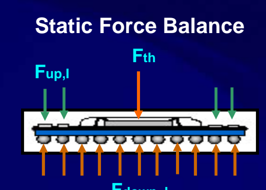
- **Solutions:**
  - Force balance analysis & FEA to determine proper pin force to avoid package deformation.
  - Force balance analysis will include static and dynamic statues.
  - Static force balance on package:

    $F_{down,J} * M = F_{up,I} * N + F_{th}$

    Where: M – qty of down side pin

    N – qty of up side pin

    F_{th} – force applied on die



  - Dynamic force balance analysis: transient force balance on package when chuck moving down with compression forces from top side & bottom side pins. This analysis provides potential deformation and stress on device substrate by all these forces.

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PoP Socket Challenge: Stress & Deformation

- **Technical challenge:**
  - Package stress, deformation or break, under non-uniform force distribution.
  - Package under lateral force if using active alignment feature.
  - Socket and top side socket deformation under preload. At small pitch, material strength may become limitation and cause bowing.

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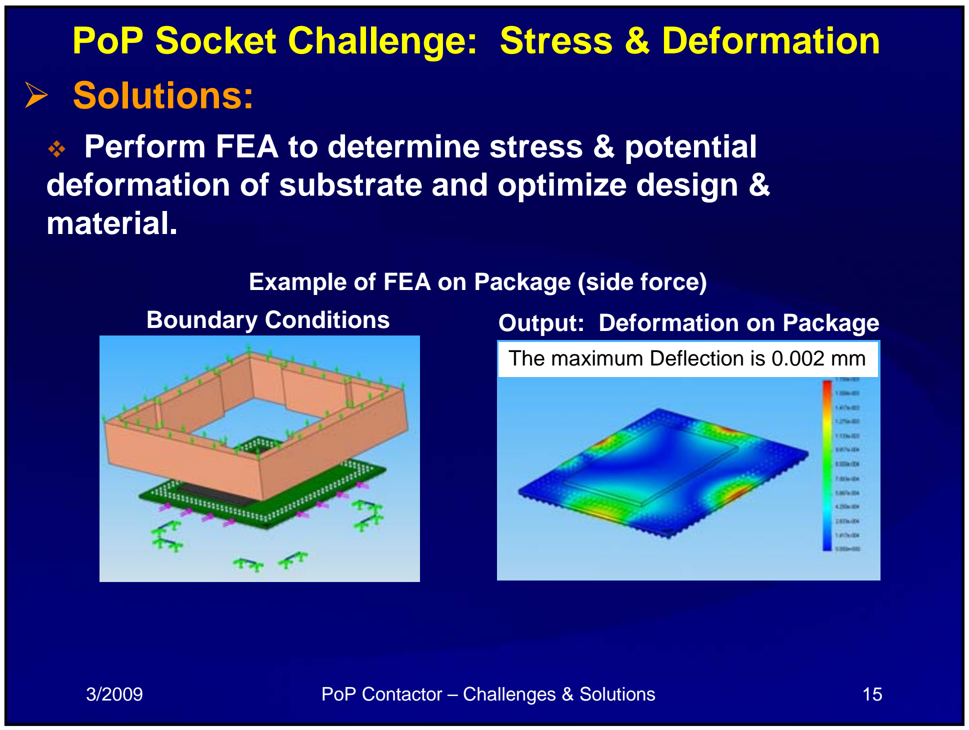
PoP Socket Challenge: Stress & Deformation
Solutions:
Perform FEA to determine stress & potential deformation of substrate and optimize design & material.
Example of FEA on Package (side force)
Boundary Conditions
Output: Deformation on Package
The maximum Deflection is 0.002 mm
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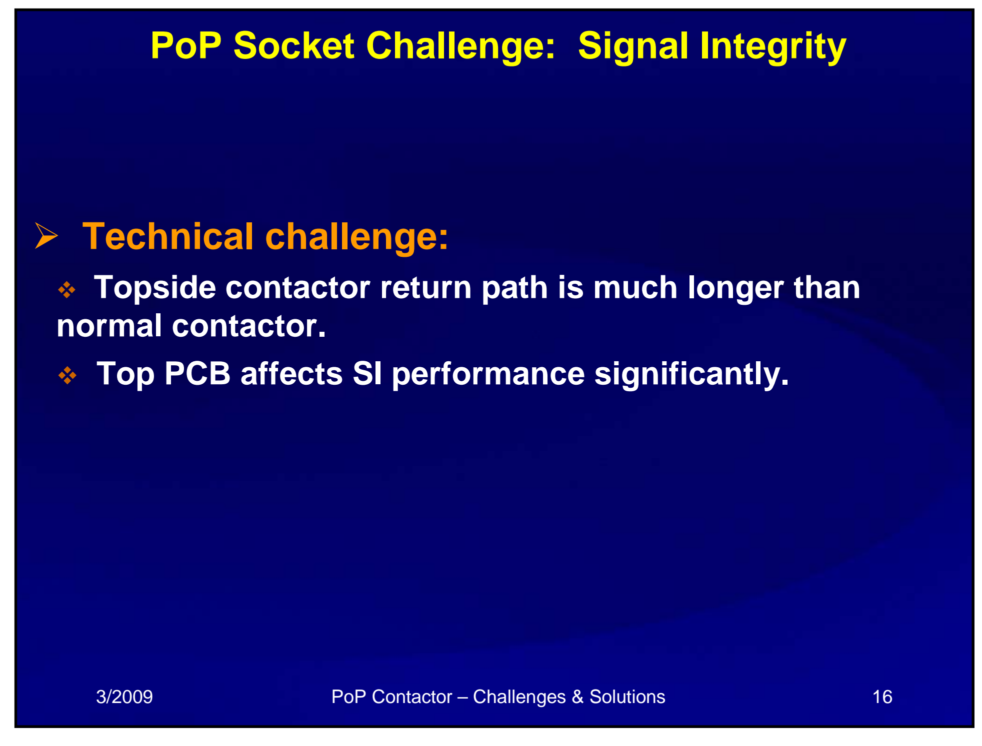
PoP Socket Challenge: Signal Integrity
Technical challenge:
Topside contactor return path is much longer than normal contactor.
Top PCB affects SI performance significantly.
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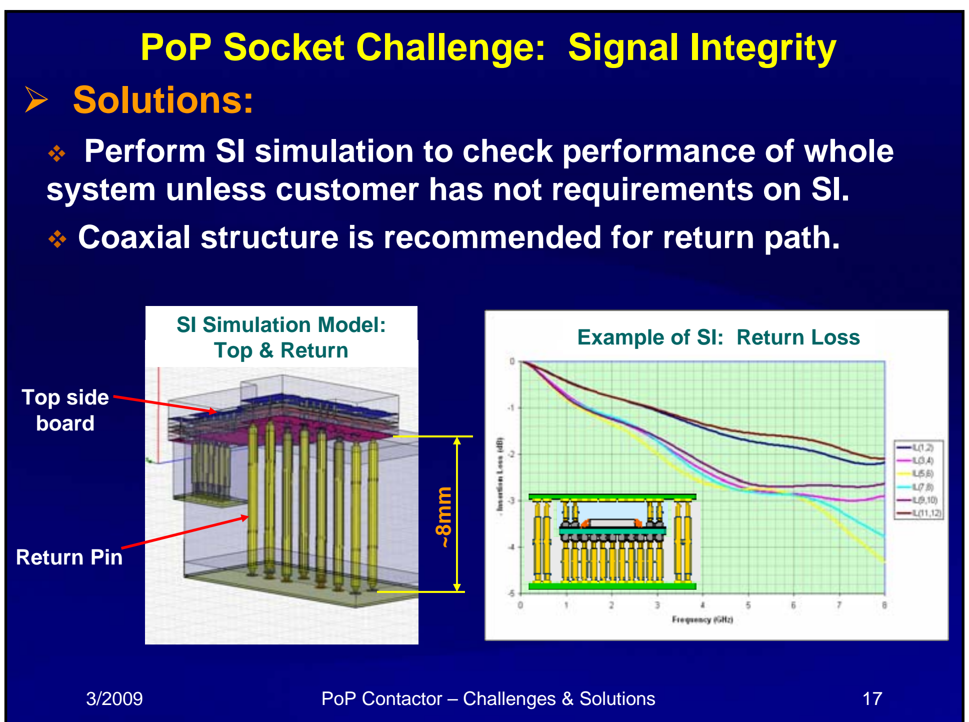

Summary

- Antares has developed various socket structures for PoP package test. These structures can meet different package test setup on auto or manual tests.

- Mechanical analysis & SI simulation should be performed to ensure success of contactor system, including:

  - Tolerance (Z stock and X-Y)
  - Force (static and dynamic)
  - FEA (package and socket)
  - SI (whole top side path to motherboard)

- Joint design in interface solution, socket/lid, change kit and board, can avoid interferences of components to ensure success of PoP contactor.

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About Authors

Jiachun Zhou (Frank), PhD
Eng Manger, Antares ATT
1030 N. Colorado St., Gilbert, AZ 85233
Ph: (480)682-6225

Siang Soh
Design Engineer, Antares ATT
48507 Milmont Dr., Fremont CA 94538
Ph: (408)834-1432

David B. Bogardus
Product/Applications Engineer, Antares ATT
1030 N. Colorado St., Gilbert, AZ 85233
Ph: (480)682-6218

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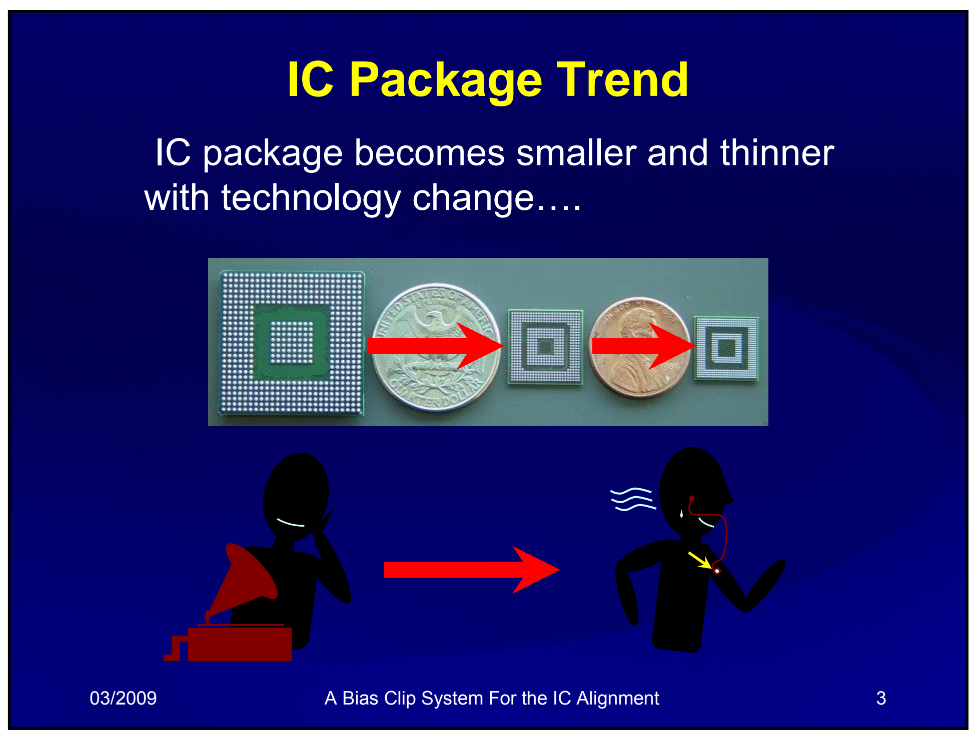
Overview

- IC package Trend
- Burn In Test Socket Trend along with IC
- Contact and IC Ball Alignment
- Tolerance Stack up
- IC Drop Test
- Bias Clip Solution

03/2009 A Bias Clip System For the IC Alignment 2

Paper #2


IC Package Trend
IC package becomes smaller and thinner with technology change….
03/2009
A Bias Clip System For the IC Alignment
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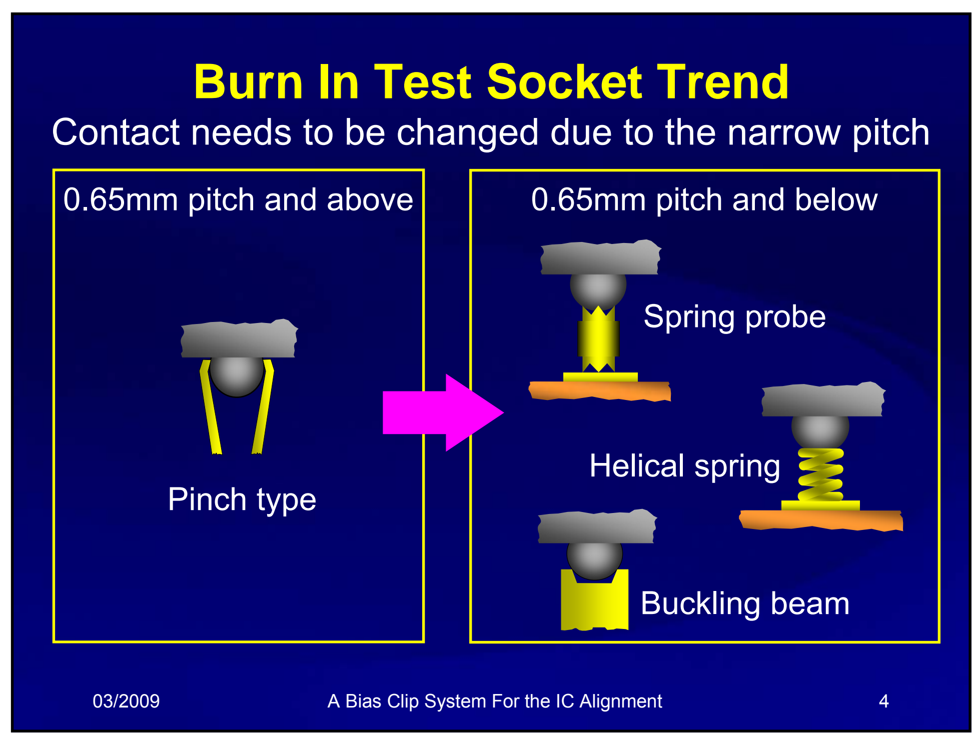
Burn In Test Socket Trend
Contact needs to be changed due to the narrow pitch
0.65mm pitch and above
Pinch type
0.65mm pitch and below
Spring probe
Helical spring
Buckling beam
03/2009
A Bias Clip System For the IC Alignment
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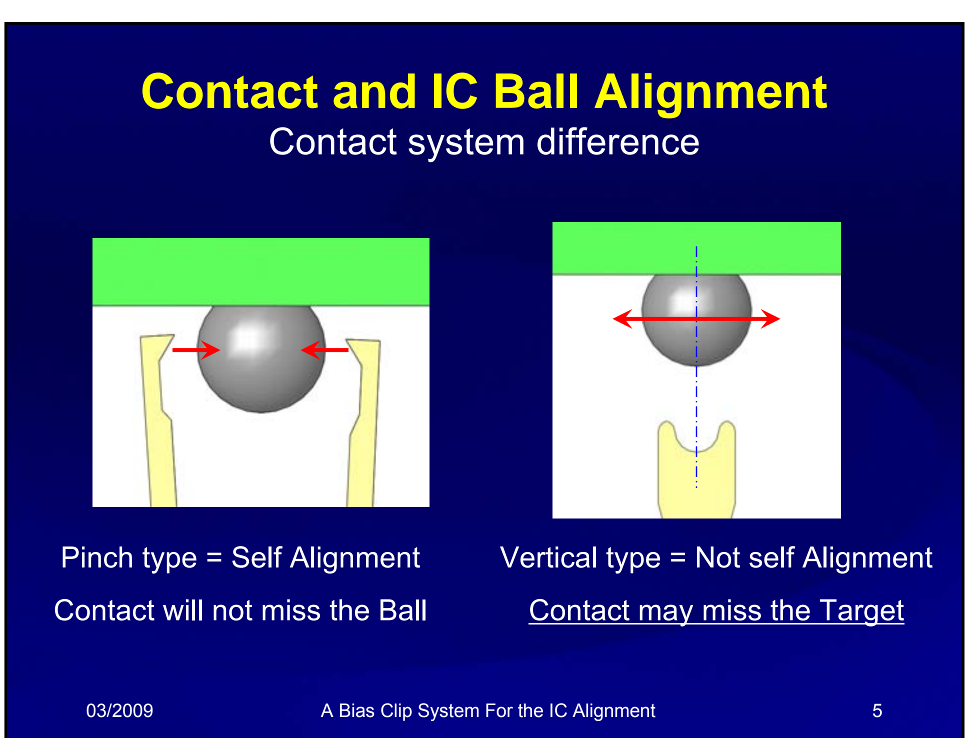
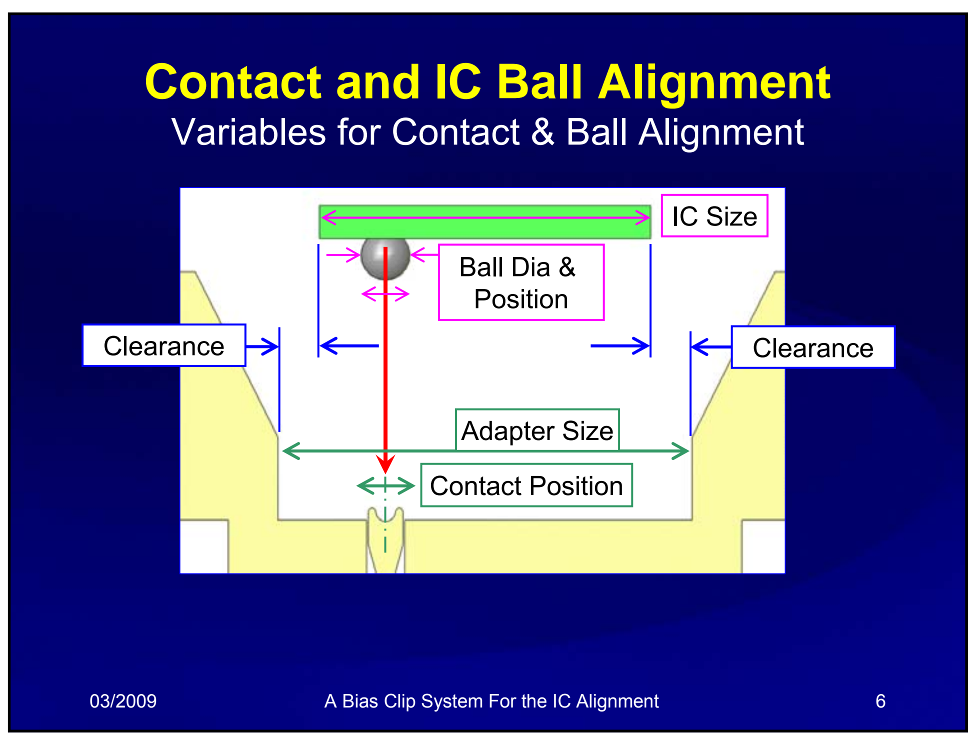
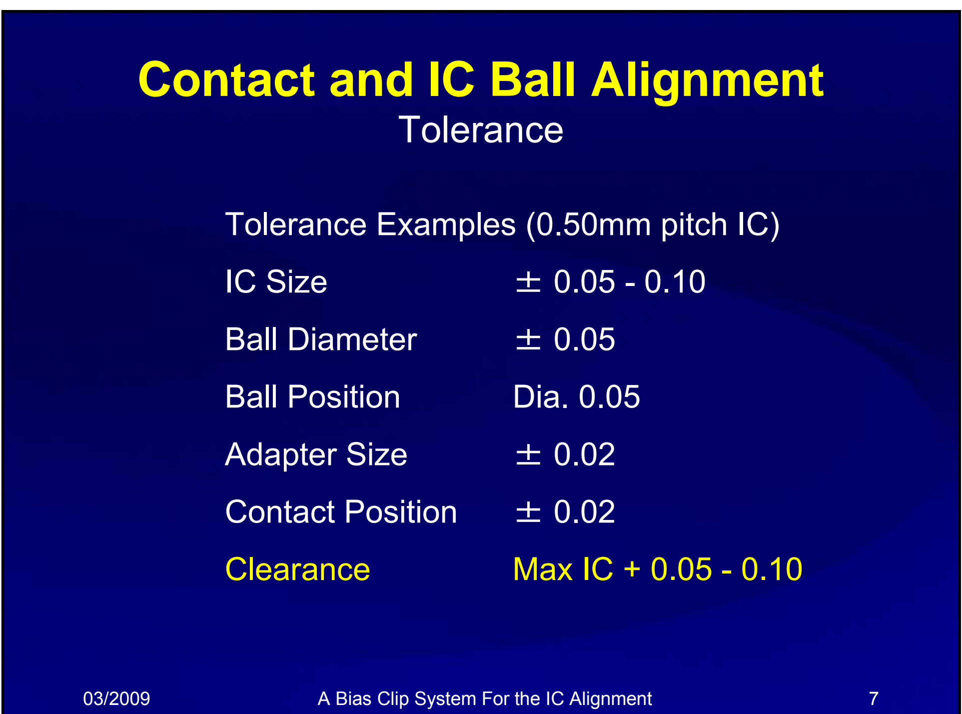
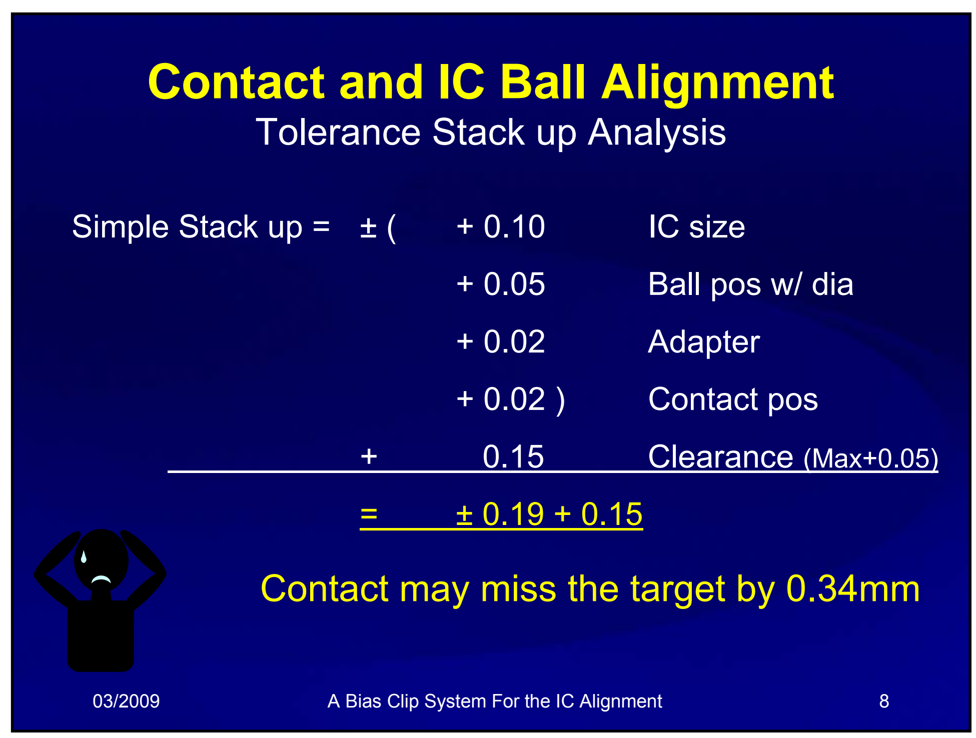
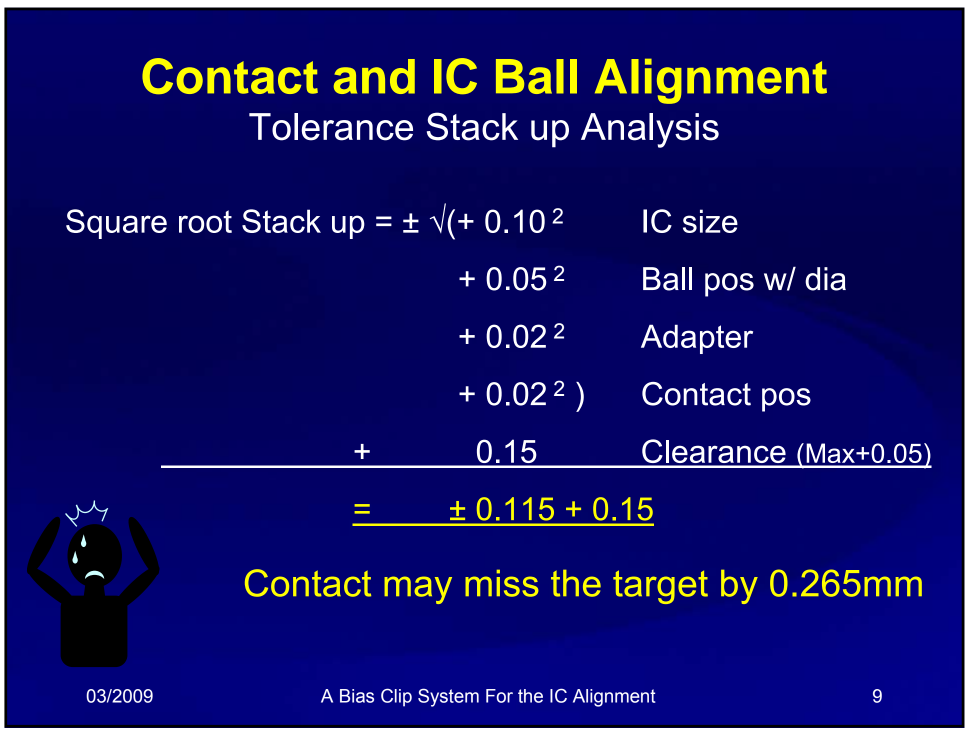

Contact and IC Ball Alignment
Contact system difference
Pinch type = Self Alignment
Contact will not miss the Ball
Vertical type = Not self Alignment
Contact may miss the Target
03/2009
A Bias Clip System For the IC Alignment
5


Contact and IC Ball Alignment
Variables for Contact & Ball Alignment
IC Size
Ball Dia &
Position
Clearance
Clearance
Adapter Size
Contact Position
03/2009
A Bias Clip System For the IC Alignment
6


Contact and IC Ball Alignment
Tolerance
Tolerance Examples (0.50mm pitch IC)
IC Size ± 0.05 - 0.10
Ball Diameter ± 0.05
Ball Position Dia. 0.05
Adapter Size ± 0.02
Contact Position ± 0.02
Clearance Max IC + 0.05 - 0.10
03/2009
A Bias Clip System For the IC Alignment
7


Contact and IC Ball Alignment
Tolerance Stack up Analysis
Simple Stack up = ± (+ 0.10 IC size
+ 0.05 Ball pos w/ dia
+ 0.02 Adapter
+ 0.02) Contact pos
+ 0.15 Clearance (Max+0.05)
= ± 0.19 + 0.15
Contact may miss the target by 0.34mm
03/2009
A Bias Clip System For the IC Alignment
8


Contact and IC Ball Alignment
Tolerance Stack up Analysis
Square root Stack up = ± √(+ 0.10 2
+ 0.05 2
+ 0.02 2
+ 0.02 2)
IC size
Ball pos w/ dia
Adapter
Contact pos
+ 0.15 Clearance (Max+0.05)
= ± 0.115 + 0.15
Contact may miss the target by 0.265mm
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A Bias Clip System For the IC Alignment
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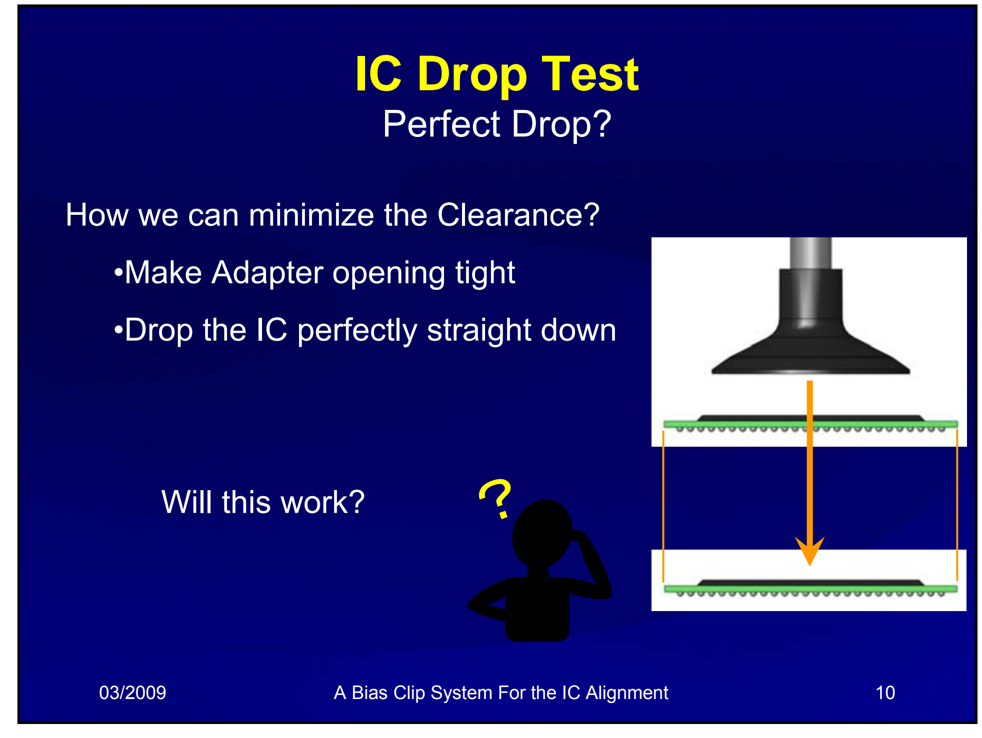
IC Drop Test
Perfect Drop?
How we can minimize the Clearance?
•Make Adapter opening tight
•Drop the IC perfectly straight down
Will this work?
?
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A Bias Clip System For the IC Alignment
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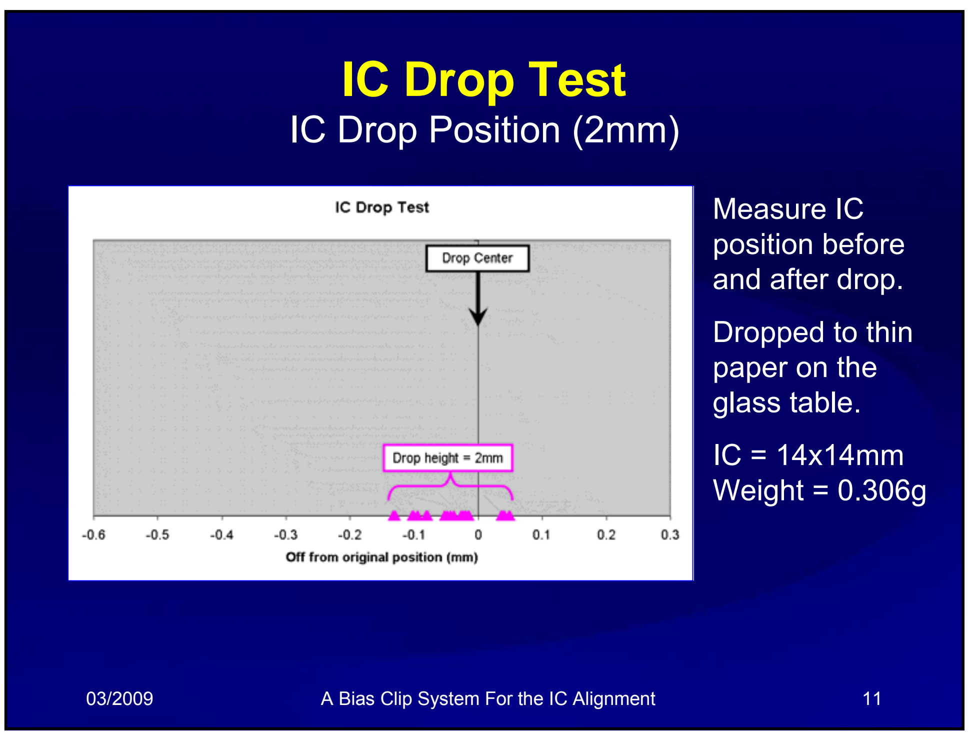
IC Drop Test
IC Drop Position (2mm)
IC Drop Test
Drop Center
Drop height = 2mm
-0.6 -0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3
Off from original position (mm)
Measure IC position before and after drop.
Dropped to thin paper on the glass table.
IC = 14x14mm
Weight = 0.306g
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A Bias Clip System For the IC Alignment
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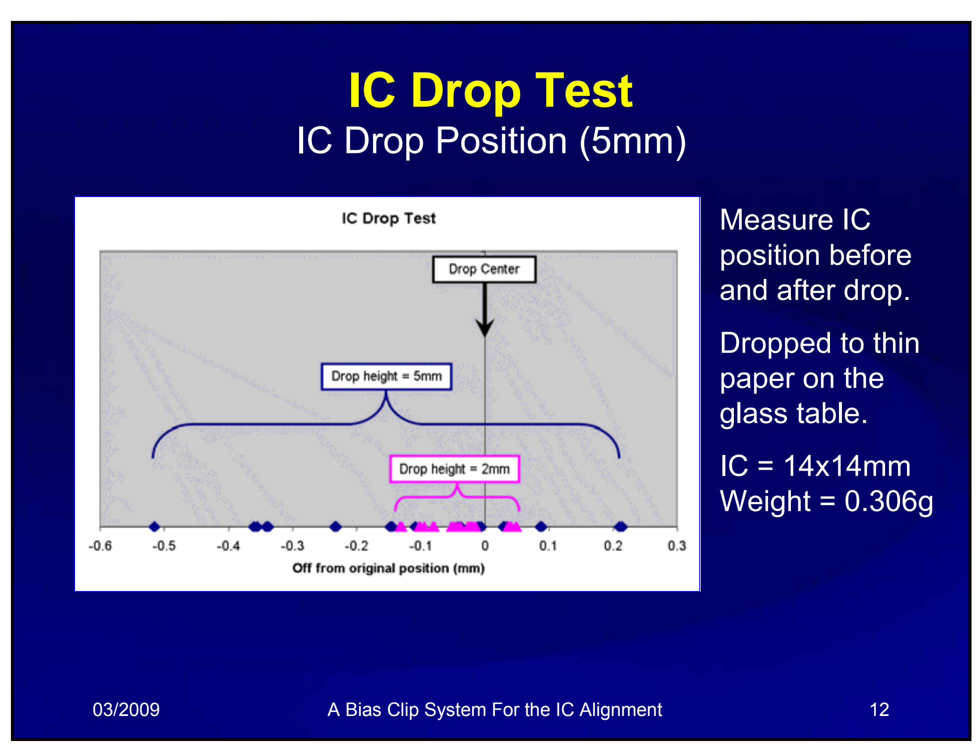
IC Drop Test
IC Drop Position (5mm)
IC Drop Test
Drop Center
Drop height = 5mm
Drop height = 2mm
-0.6 -0.5 -0.4 -0.3 -0.2 -0.1 0 0.1 0.2 0.3
Off from original position (mm)
Measure IC position before and after drop.
Dropped to thin paper on the glass table.
IC = 14x14mm
Weight = 0.306g
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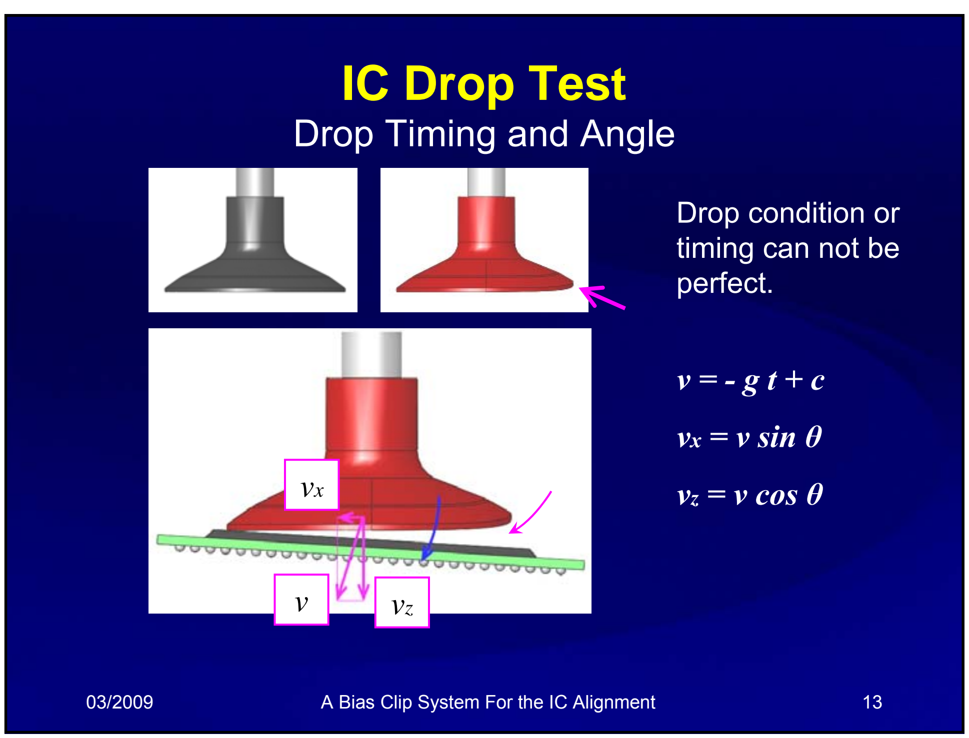
A Bias Clip System For the IC Alignment
12


IC Drop Test
Drop Timing and Angle
Drop condition or timing can not be perfect.
v = - g t + c
vx = v sin θ
vz = v cos θ
vx
v
vz
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A Bias Clip System For the IC Alignment
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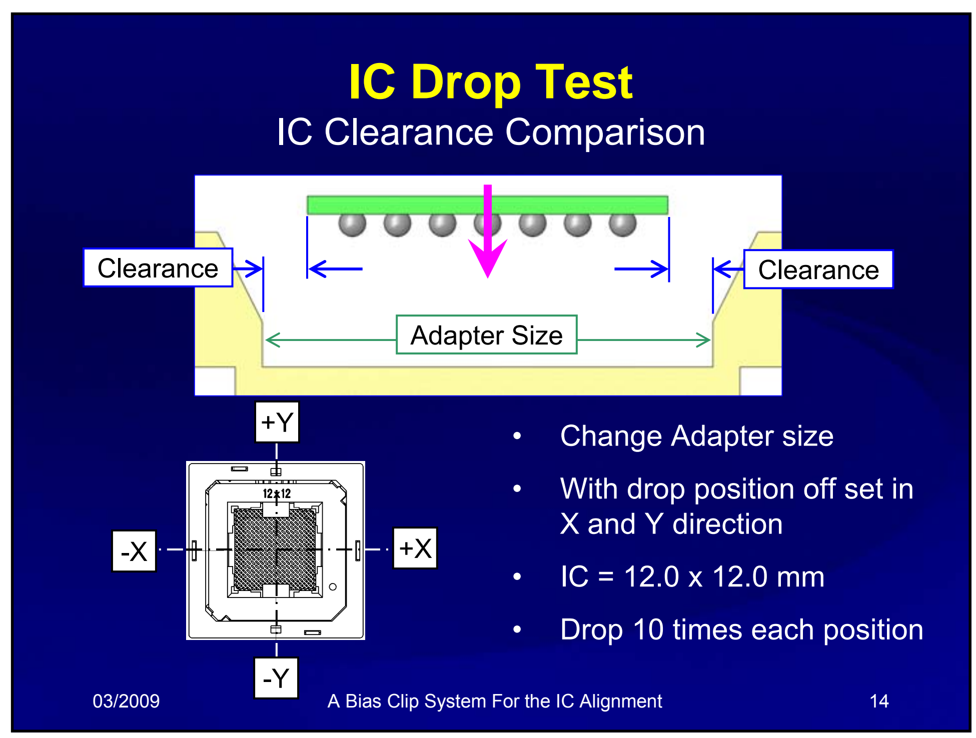
IC Drop Test
IC Clearance Comparison
Clearance
Clearance
Adapter Size
+Y
-X
+X
-Y
12x12
• Change Adapter size
• With drop position off set in X and Y direction
• IC = 12.0 x 12.0 mm
• Drop 10 times each position
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A Bias Clip System For the IC Alignment
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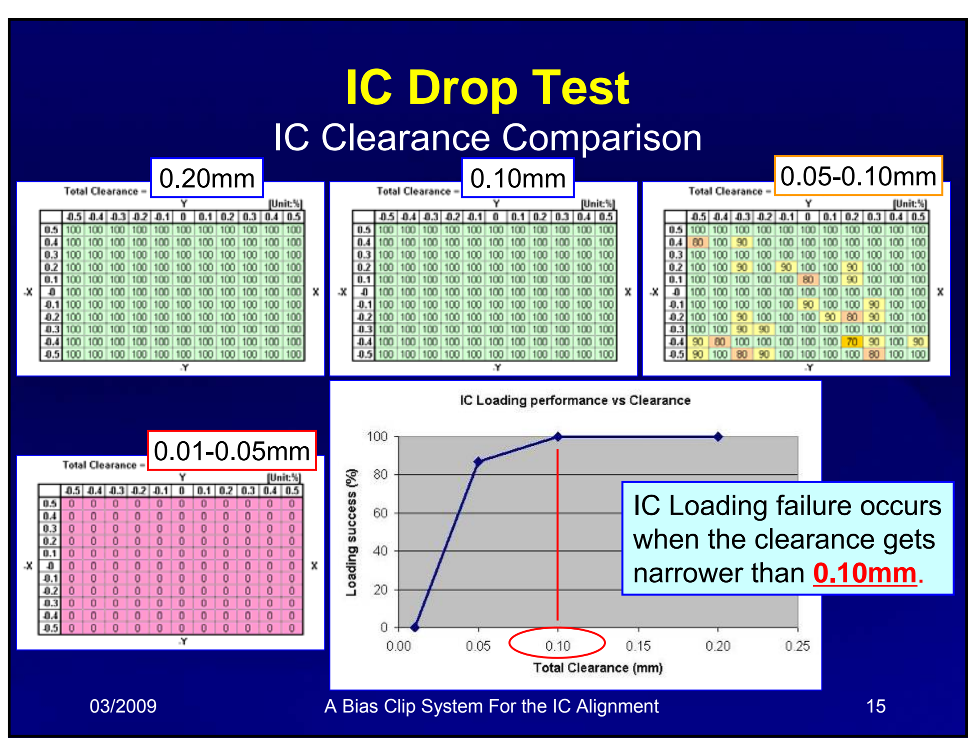
IC Drop Test
IC Clearance Comparison
0.20mm
0.10mm
0.05-0.10mm
0.01-0.05mm
IC Loading performance vs Clearance
Loading success (%)
Total Clearance (mm)
IC Loading failure occurs when the clearance gets narrower than 0.10mm.
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A Bias Clip System For the IC Alignment
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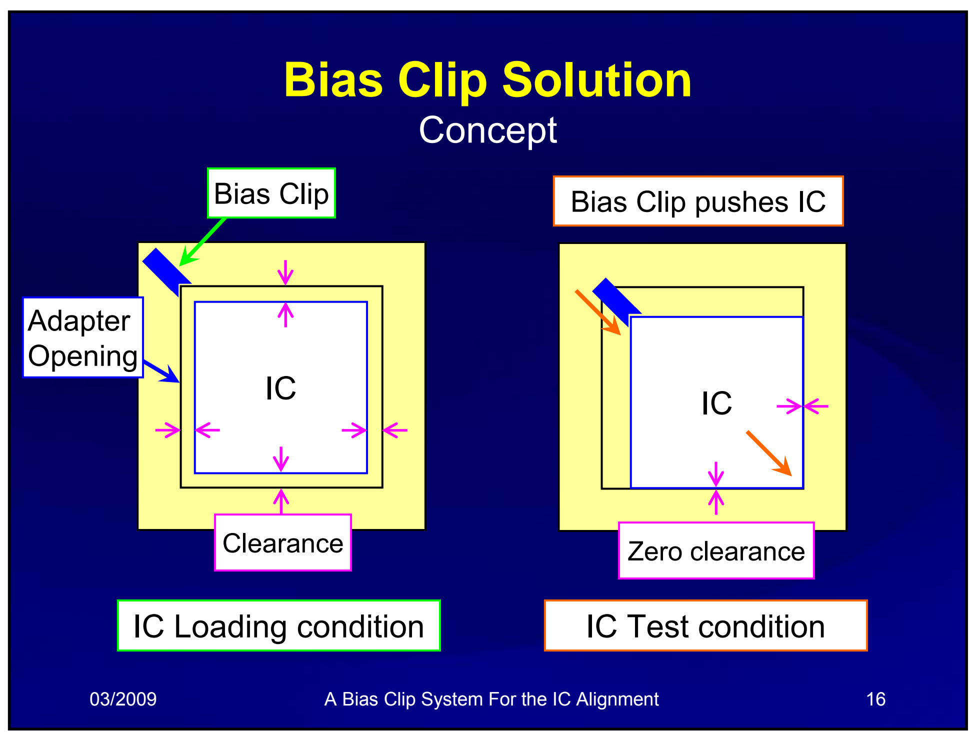
Bias Clip Solution
Concept
Bias Clip
Adapter Opening
IC
Clearance
IC Loading condition
Bias Clip pushes IC
IC
Zero clearance
IC Test condition
03/2009
A Bias Clip System For the IC Alignment
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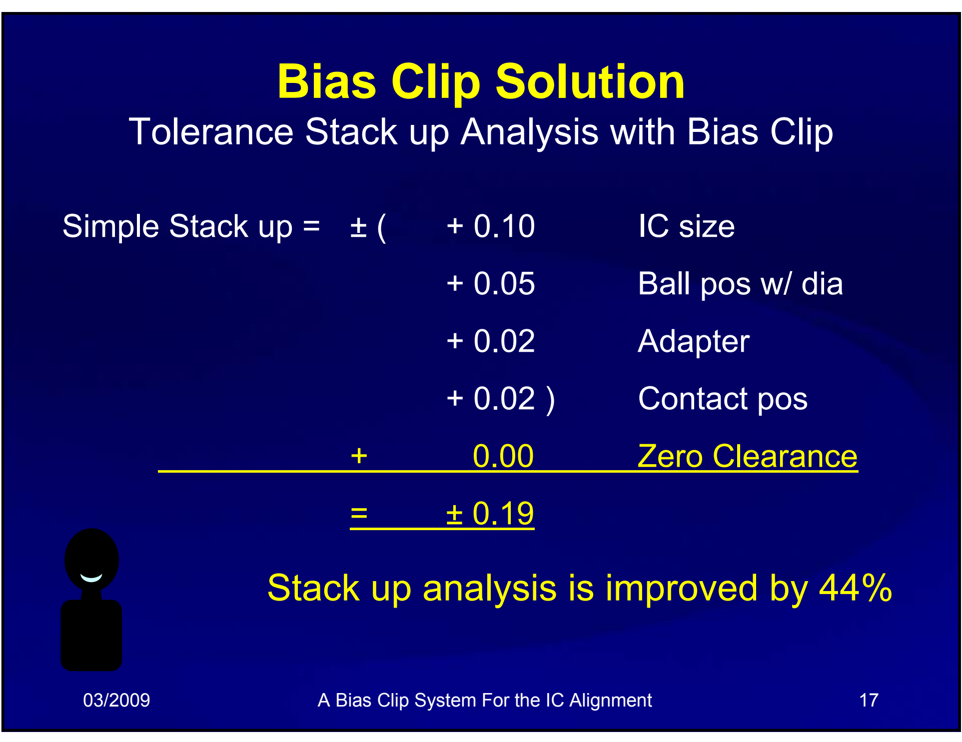
Bias Clip Solution
Tolerance Stack up Analysis with Bias Clip
Simple Stack up = ± (+ 0.10 IC size
+ 0.05 Ball pos w/ dia
+ 0.02 Adapter
+ 0.02) Contact pos
+ 0.00 Zero Clearance
= ± 0.19
Stack up analysis is improved by 44%
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A Bias Clip System For the IC Alignment
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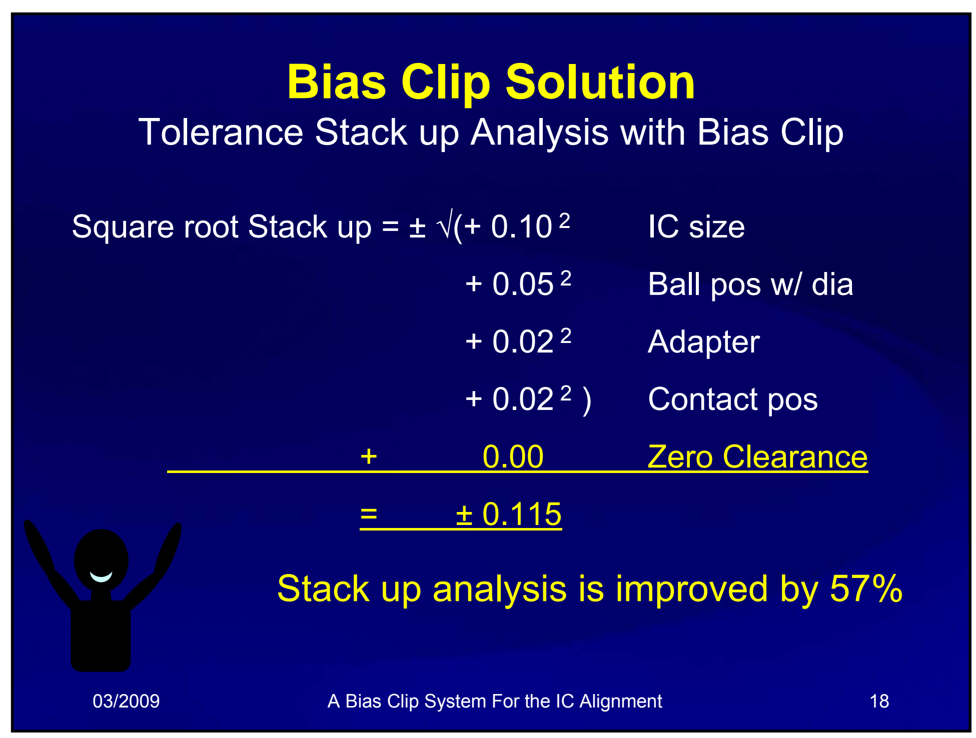
Bias Clip Solution
Tolerance Stack up Analysis with Bias Clip
Square root Stack up = ± √(+ 0.10 2 IC size
+ 0.05 2 Ball pos w/ dia
+ 0.02 2 Adapter
+ 0.02 2) Contact pos
+ 0.00 Zero Clearance
= ± 0.115
Stack up analysis is improved by 57%
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A Bias Clip System For the IC Alignment
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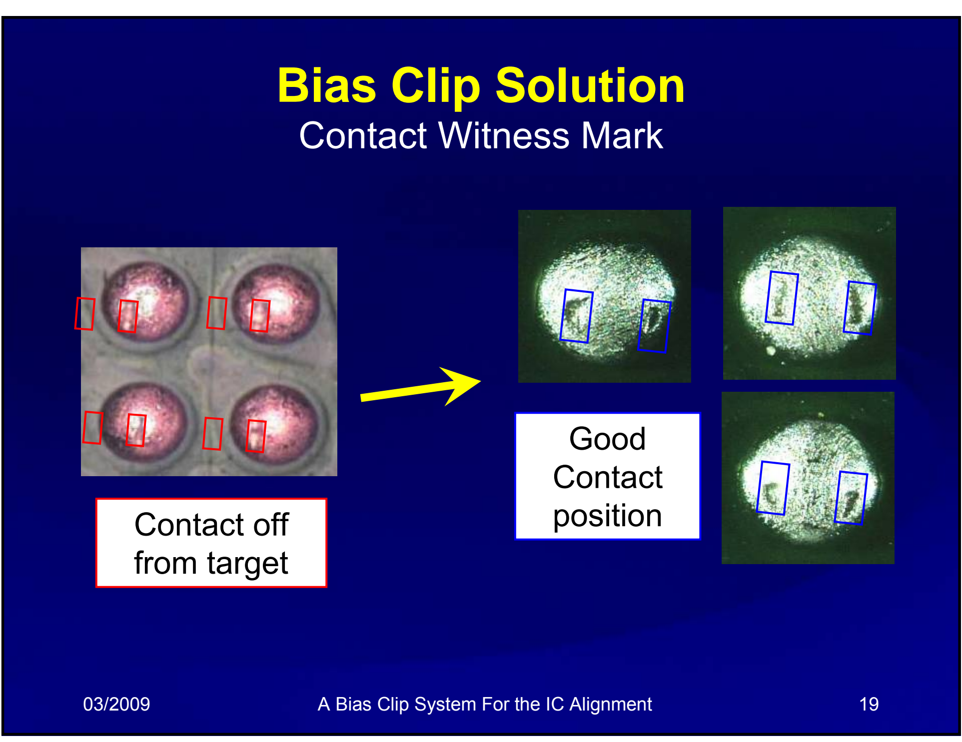
Bias Clip Solution
Contact Witness Mark
Contact off from target
Good Contact position
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A Bias Clip System For the IC Alignment
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Bias Clip Solution
Summary
• Wide Clearance for IC loading
• Available for Open Top & Clamshell
• Works with vertical type contact
• Patented
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A Bias Clip System For the IC Alignment
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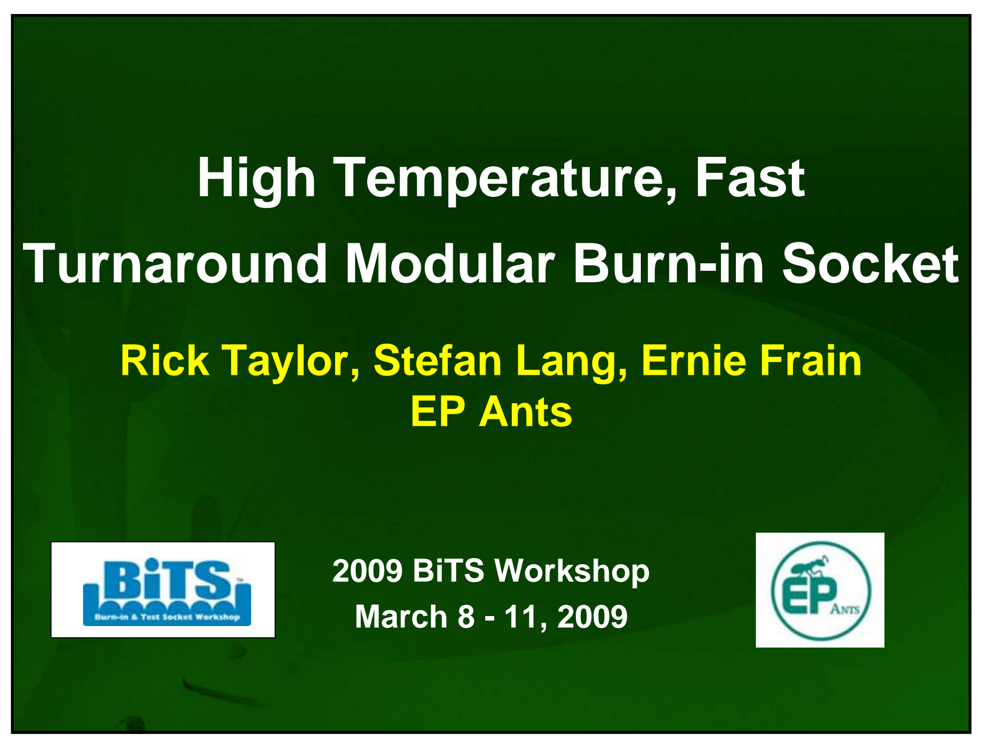
High Temperature, Fast
Turnaround Modular Burn-in Socket
Rick Taylor, Stefan Lang, Ernie Frain
EP Ants
BiTS Burn-in & Test Socket Workshop
2009 BiTS Workshop
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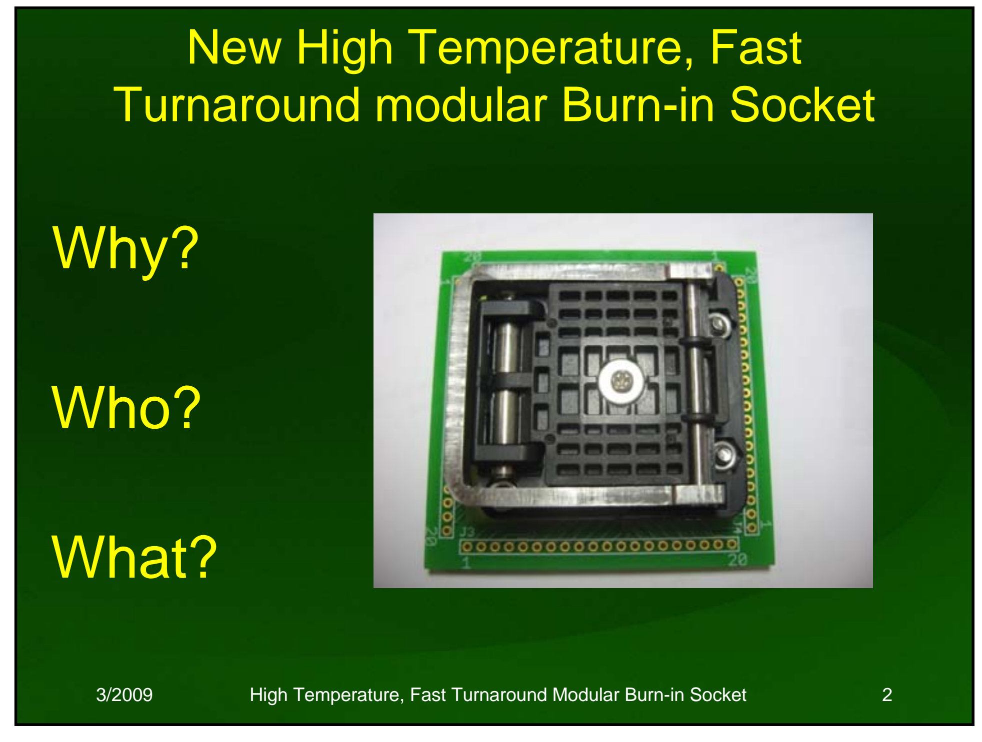
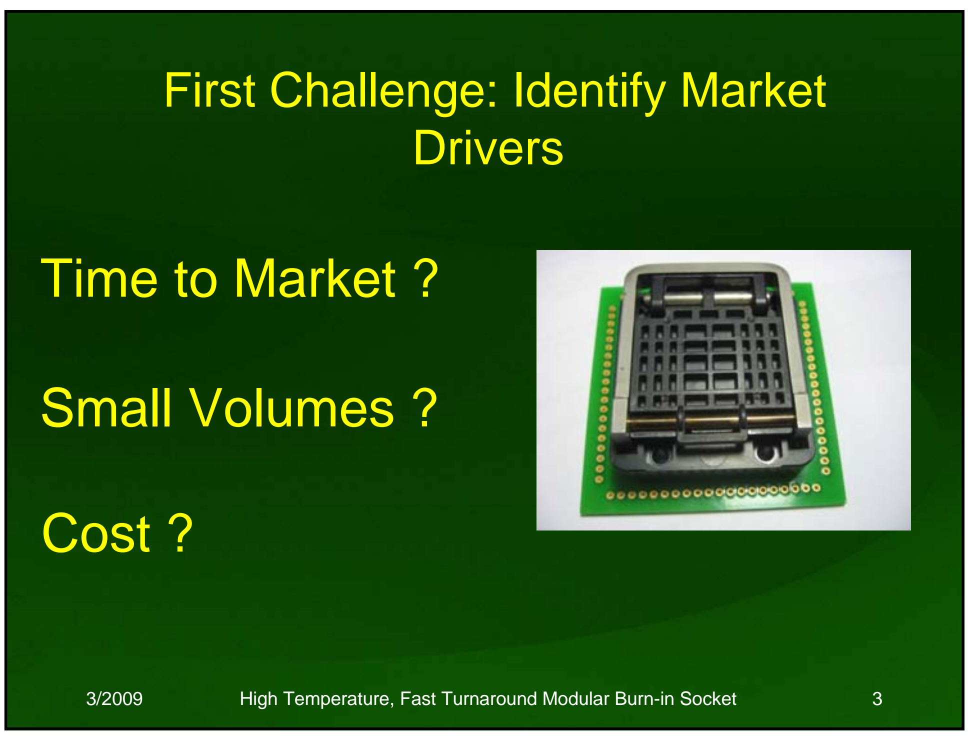
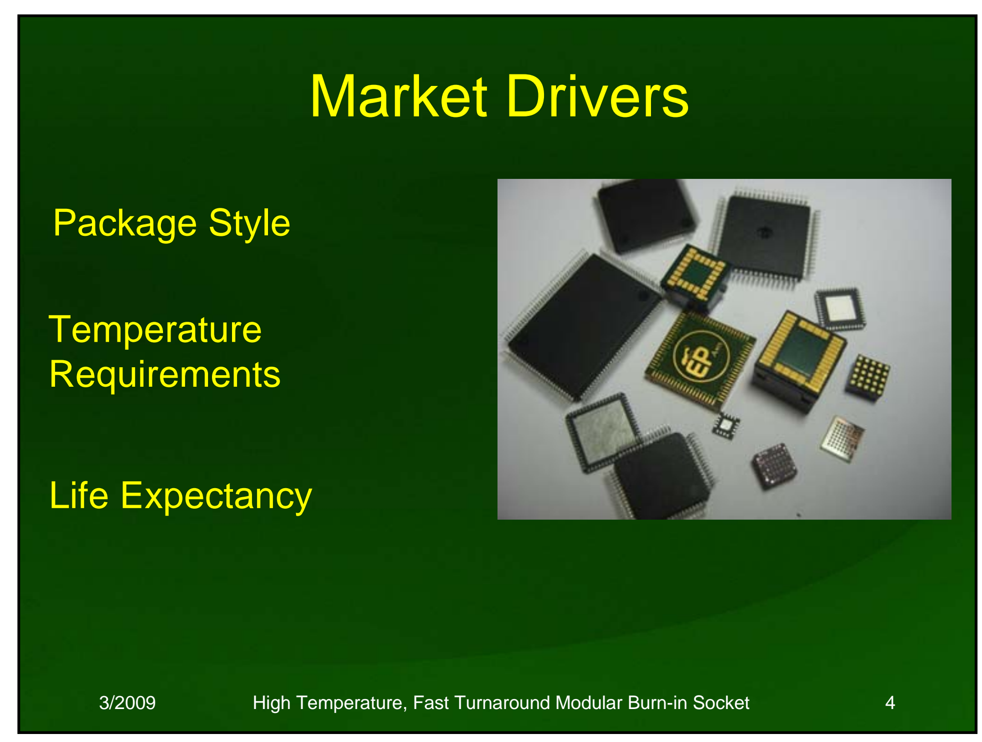
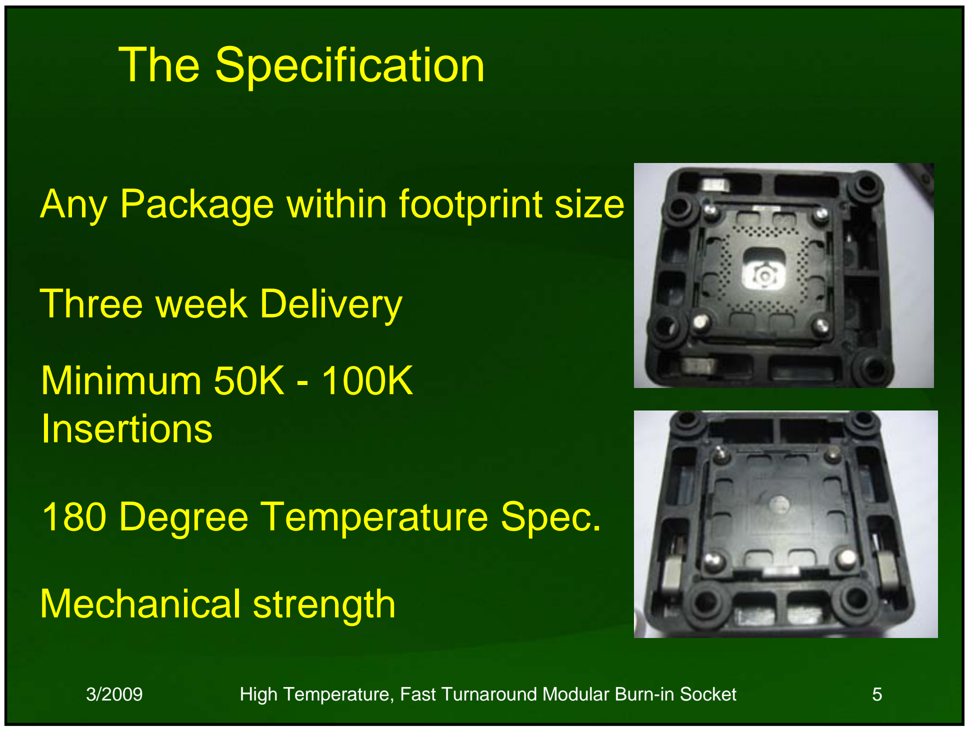
EP Ants

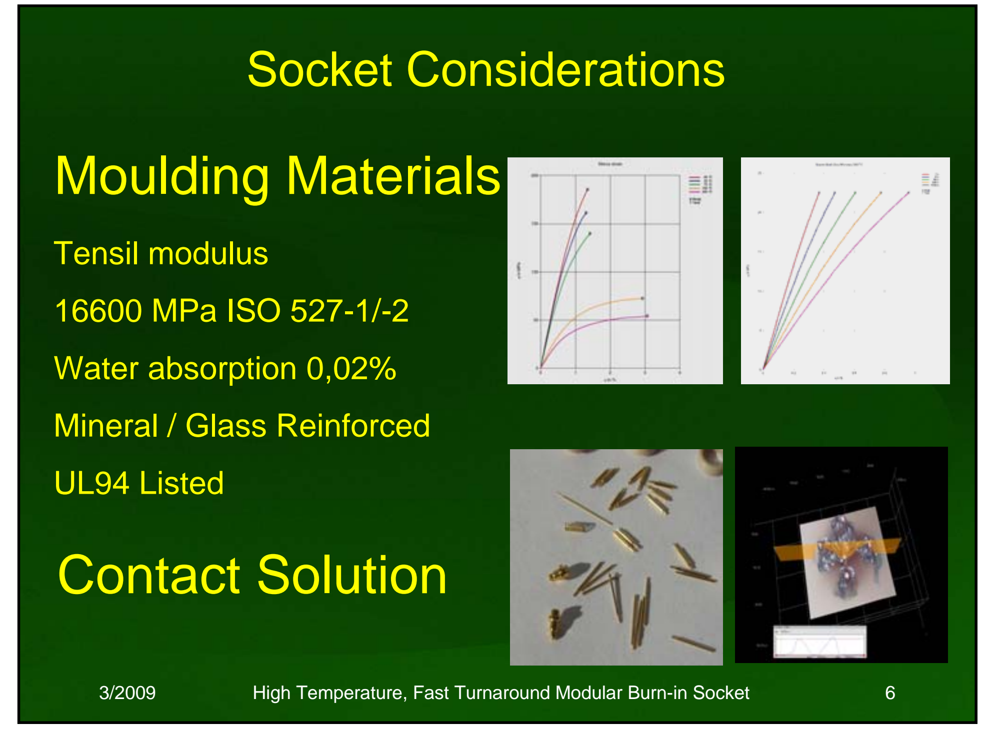

New High Temperature, Fast
Turnaround modular Burn-in Socket
Why?
Who?
What?
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
2


First Challenge: Identify Market Drivers
Time to Market ?
Small Volumes ?
Cost ?
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
3


Market Drivers
Package Style
Temperature Requirements
Life Expectancy
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
4



The Specification
Any Package within footprint size
Three week Delivery
Minimum 50K - 100K Insertions
180 Degree Temperature Spec.
Mechanical strength
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
5



Socket Considerations
Moulding Materials
Tensil modulus
16600 MPa ISO 527-1/-2
Water absorption 0,02%
Mineral / Glass Reinforced
UL94 Listed
Contact Solution
3/2009
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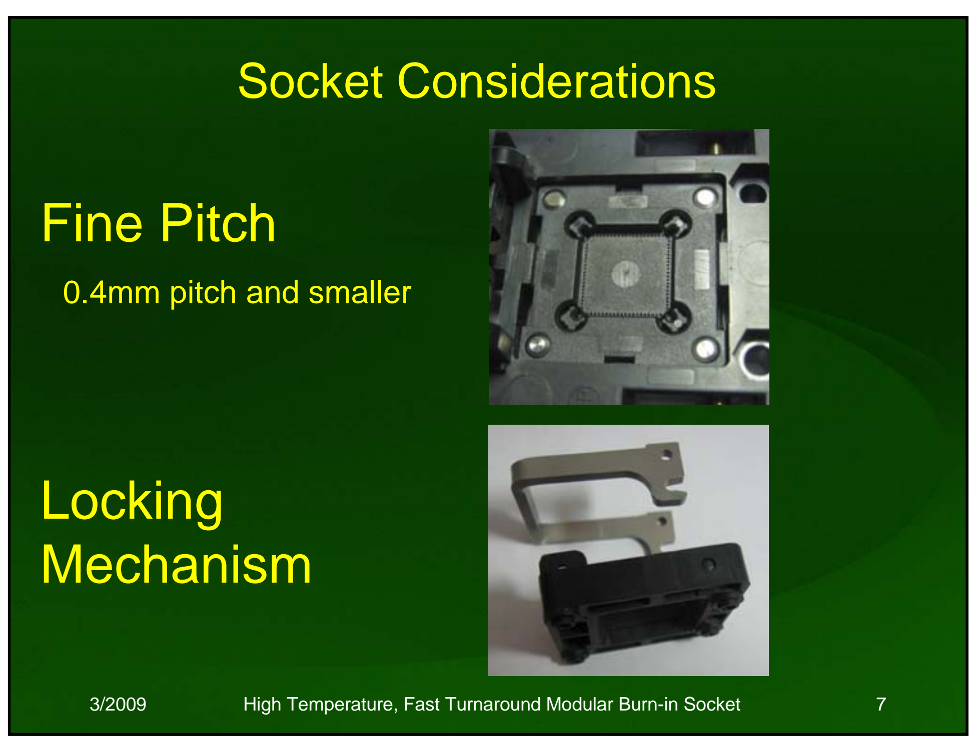
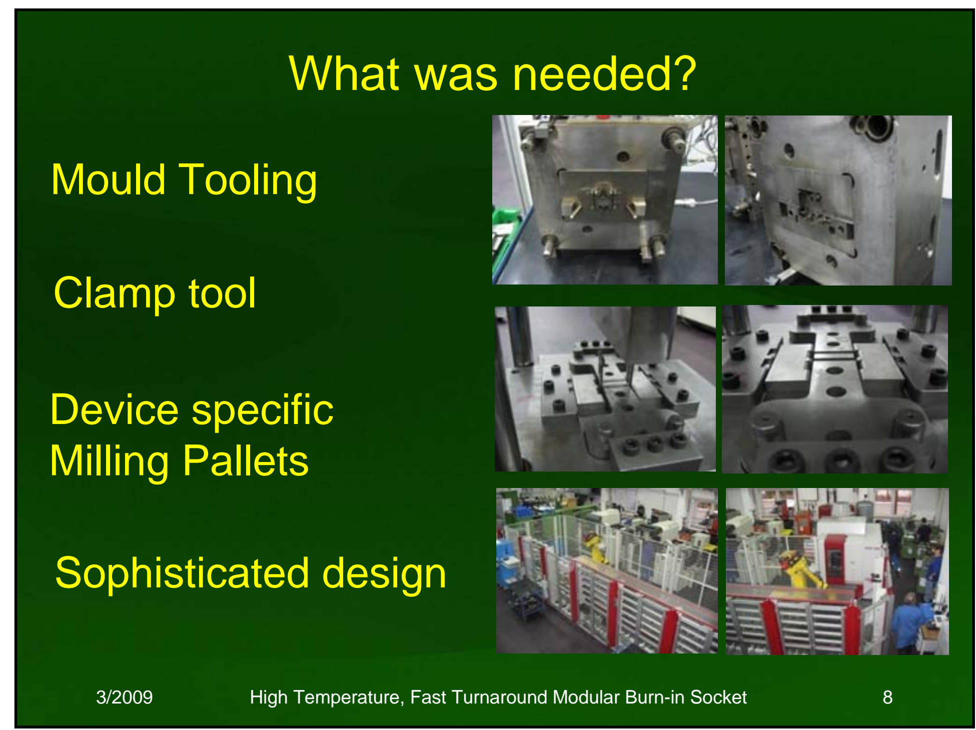
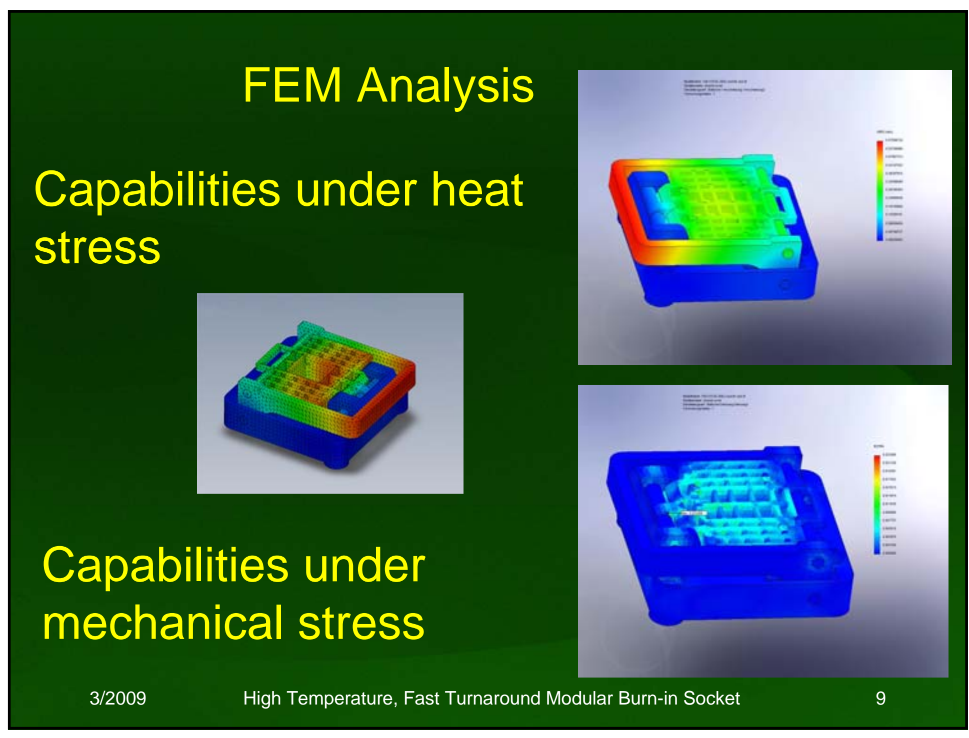
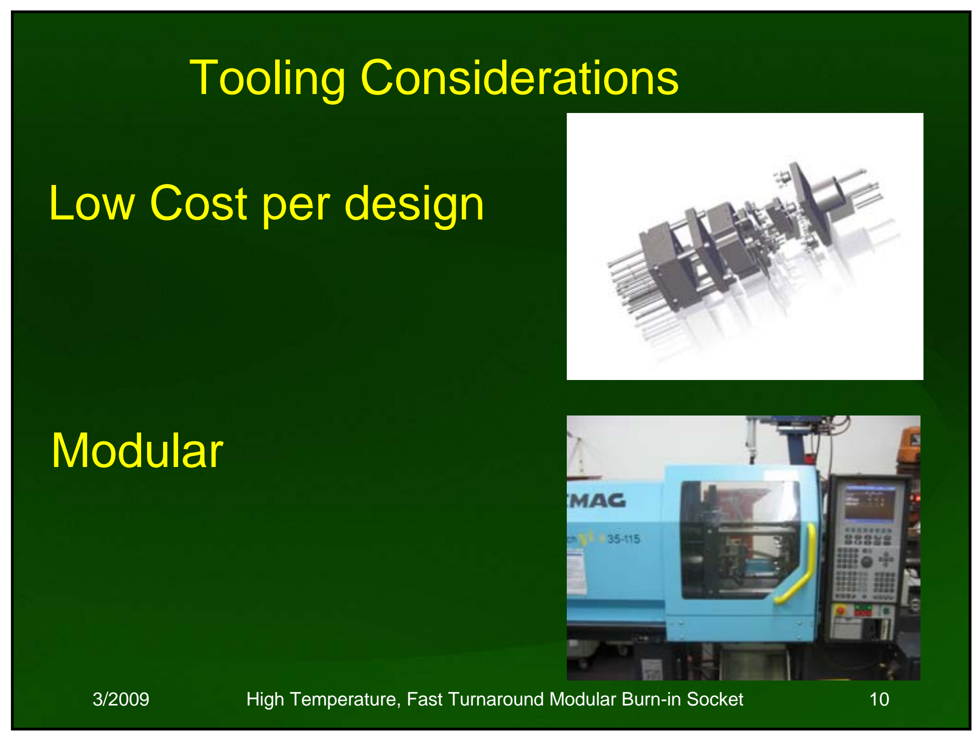
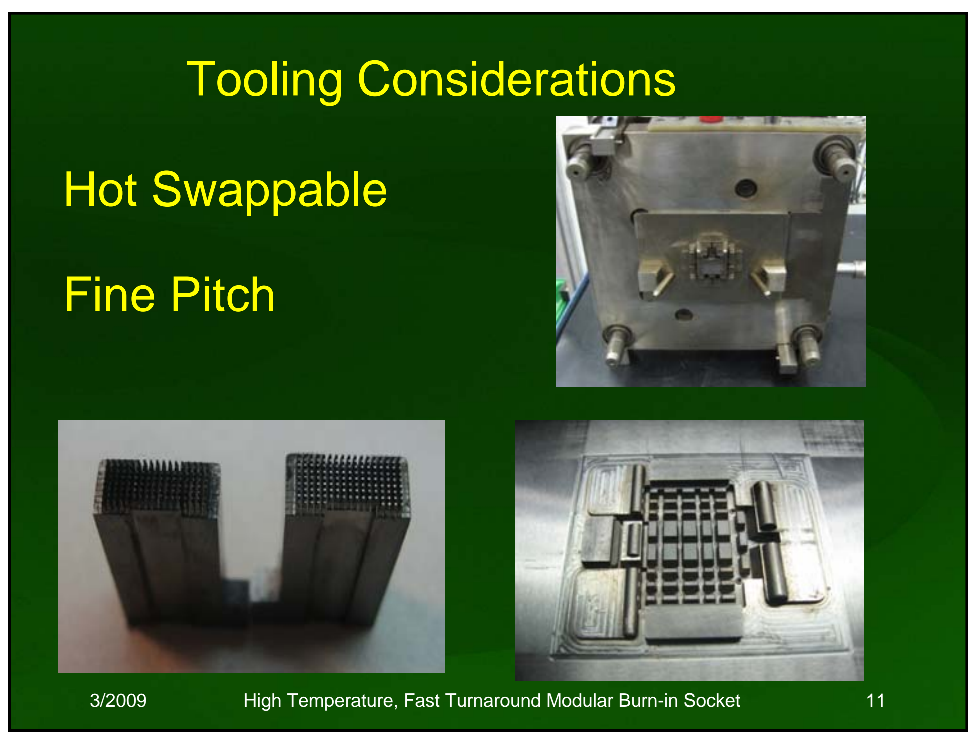
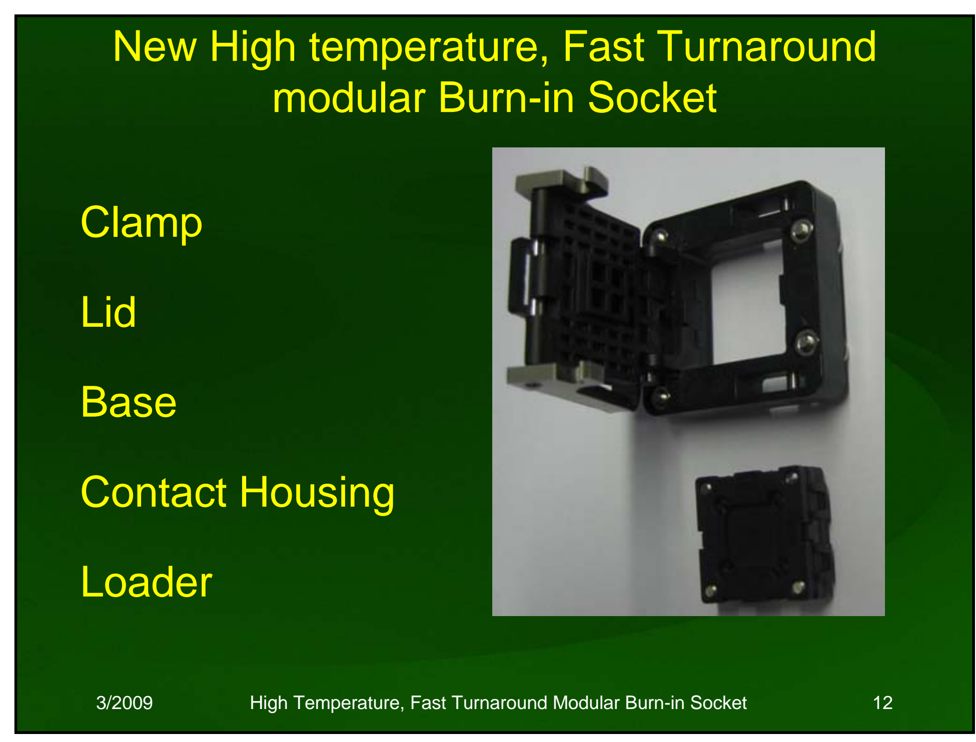

Socket Considerations
Fine Pitch
0.4mm pitch and smaller
Locking
Mechanism
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
7

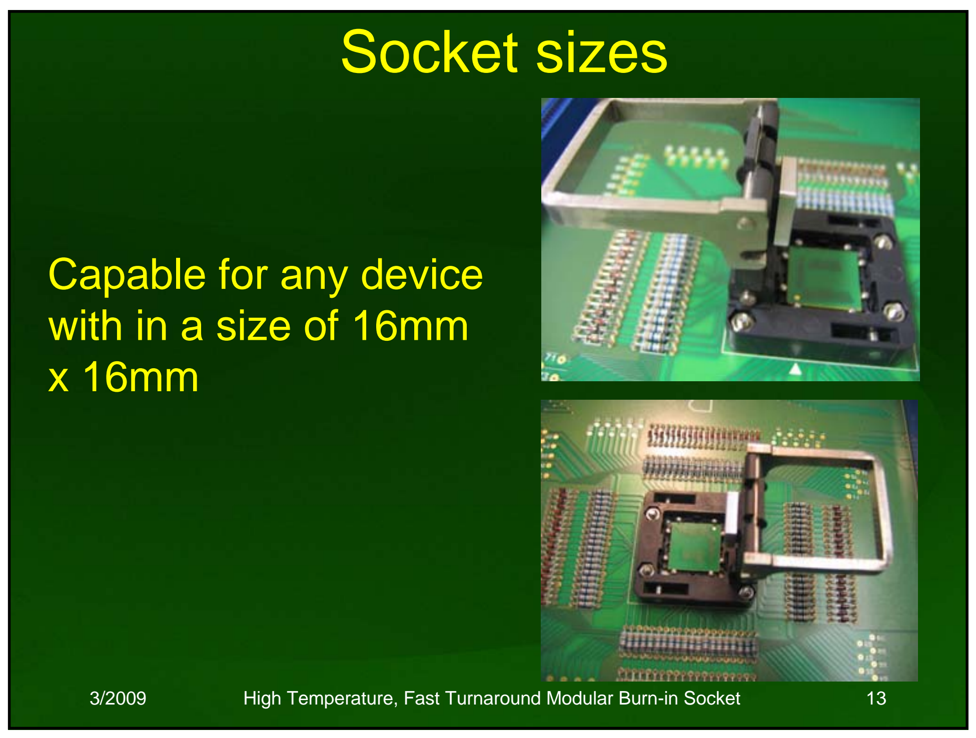

What was needed?
Mould Tooling
Clamp tool
Device specific
Milling Pallets
Sophisticated design
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
8

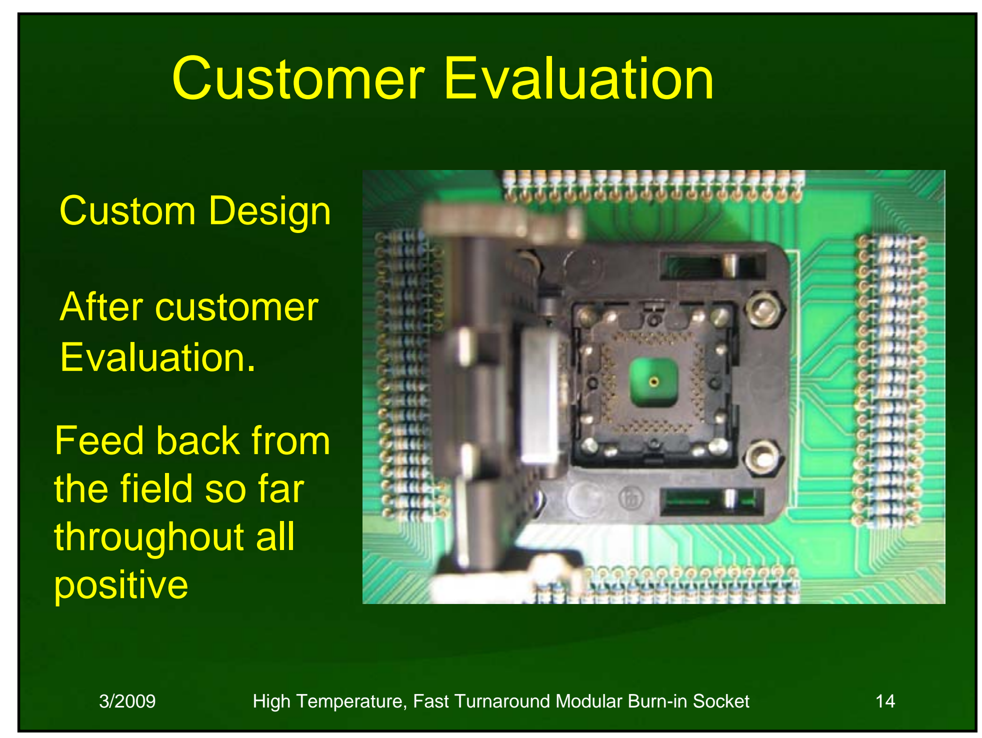

FEM Analysis
Capabilities under heat stress
Capabilities under mechanical stress
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
9

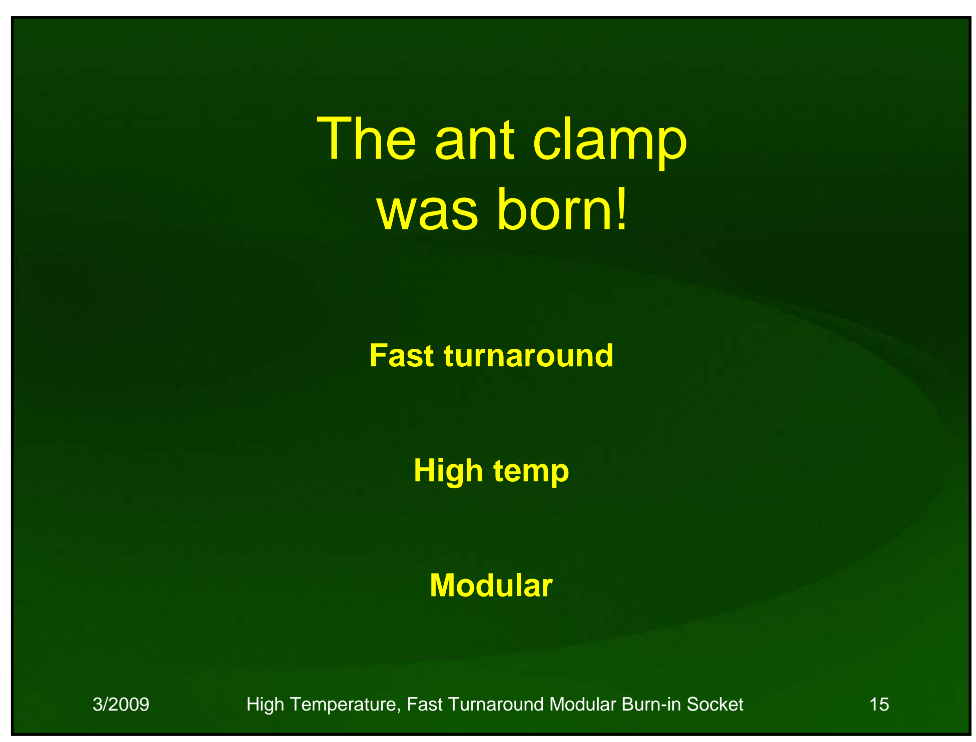

Tooling Considerations
Low Cost per design
Modular
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
10


Tooling Considerations
Hot Swappable
Fine Pitch
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
11


New High temperature, Fast Turnaround modular Burn-in Socket
Clamp
Lid
Base
Contact Housing
Loader
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
12


Socket sizes
Capable for any device with in a size of 16mm x 16mm
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
13


Customer Evaluation
Custom Design
After customer Evaluation.
Feed back from the field so far throughout all positive
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
14


The ant clamp
was born!
Fast turnaround
High temp
Modular
3/2009
High Temperature, Fast Turnaround Modular Burn-in Socket
15

New PTB / High Power Kelvin Test Socket Concept

Gerhard Gschwendtberger
Multitest elektronische Systeme GmbH

2009 BiTS Workshop
March 8 - 11, 2009

Content

- Test socket requirements
- Lead-free challenges
- Test socket influence on cost of test
- Test socket features
- Characterization methods
- Correlation to high volume production
- Implementation
- Summary

Test Socket Requirements

- Suitable for QFN, QFP, SOP, lead pitch 0.3mm
- PTB capability, short contact length
- High current capability, 50A @ pulse
- Minimum leakage current
- Suitable for all lead-free packages
- Lifespan > 1 Mio insertions
- Temperature range –55°C to 200°C

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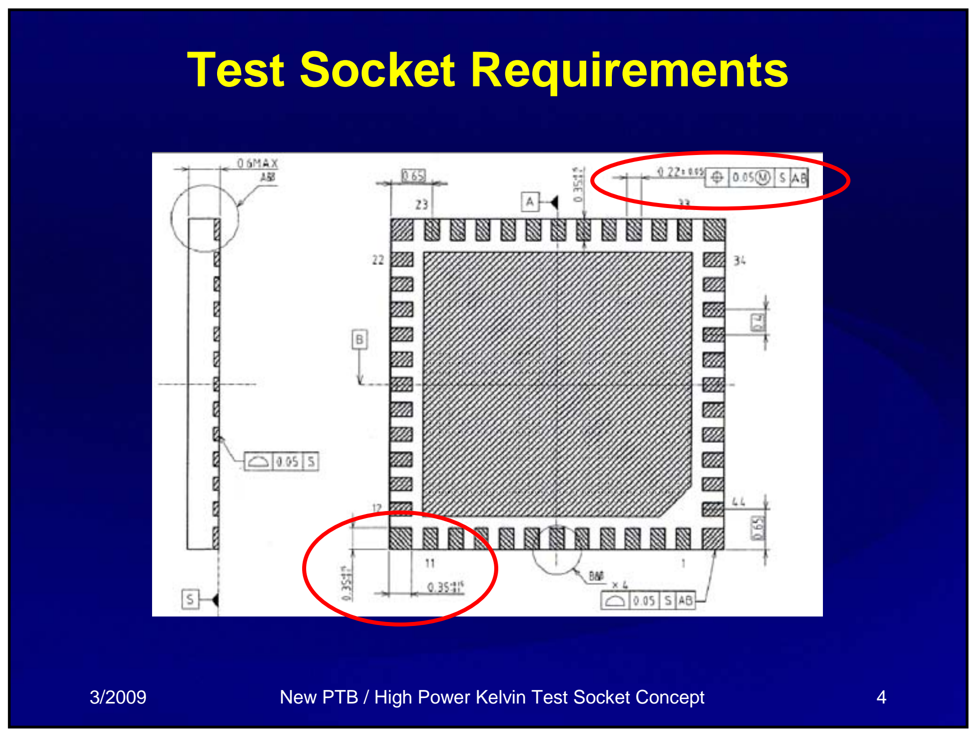
Test Socket Requirements



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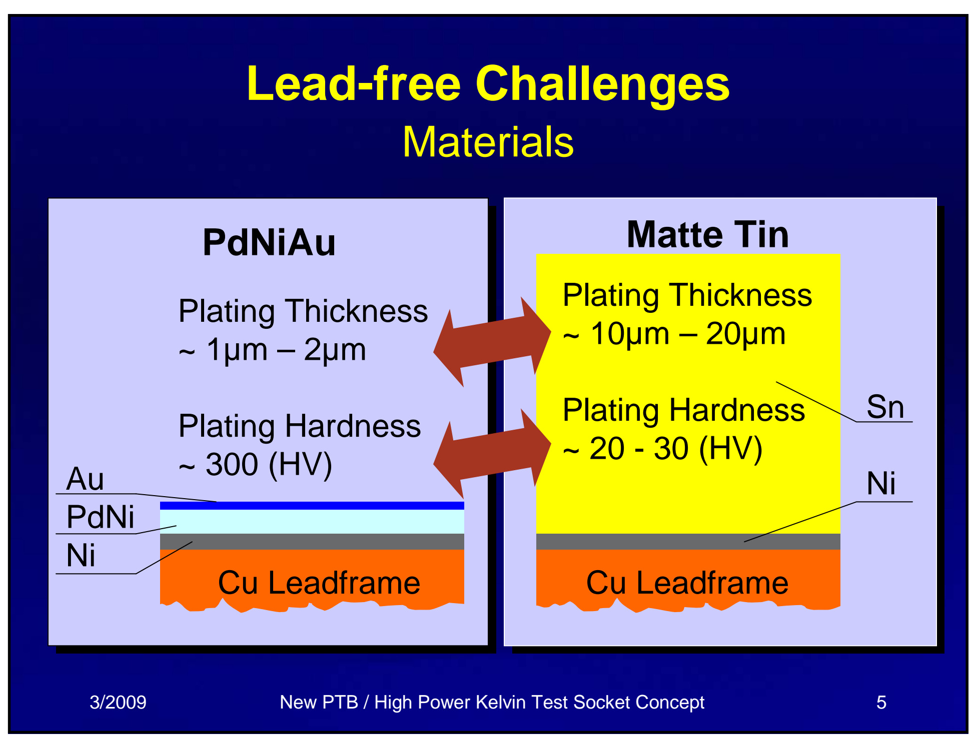
Lead-free Challenges
Materials
PdNiAu
Plating Thickness
~ 1µm – 2µm
Plating Hardness
~ 300 (HV)
Au
PdNi
Ni
Cu Leadframe
Matte Tin
Plating Thickness
~ 10µm – 20µm
Plating Hardness
~ 20 - 30 (HV)
Sn
Ni
Cu Leadframe
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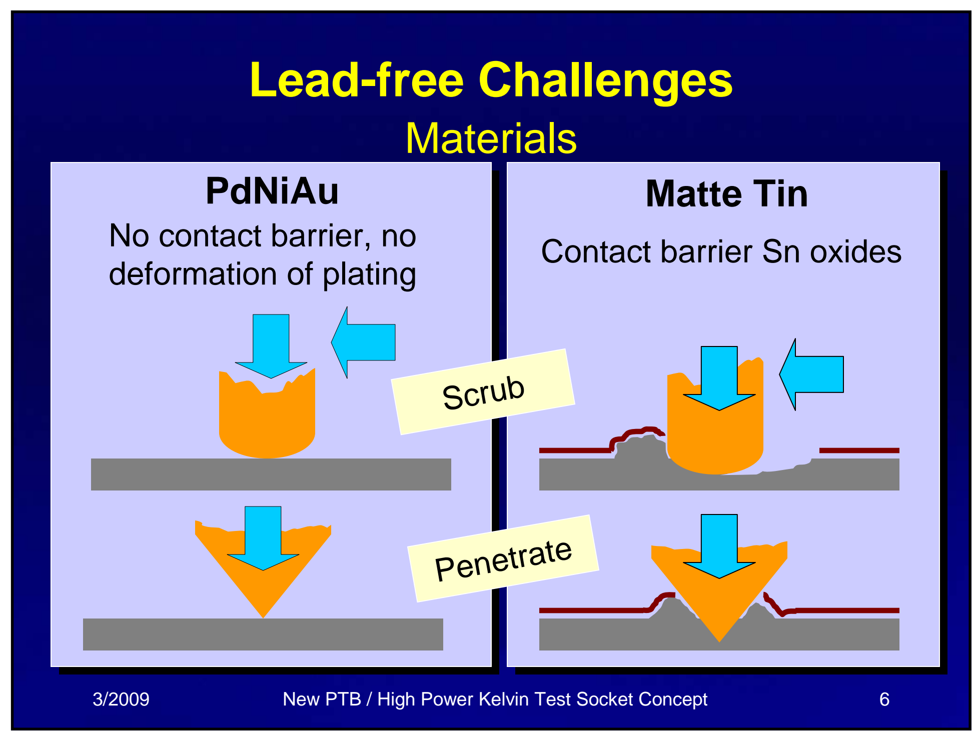
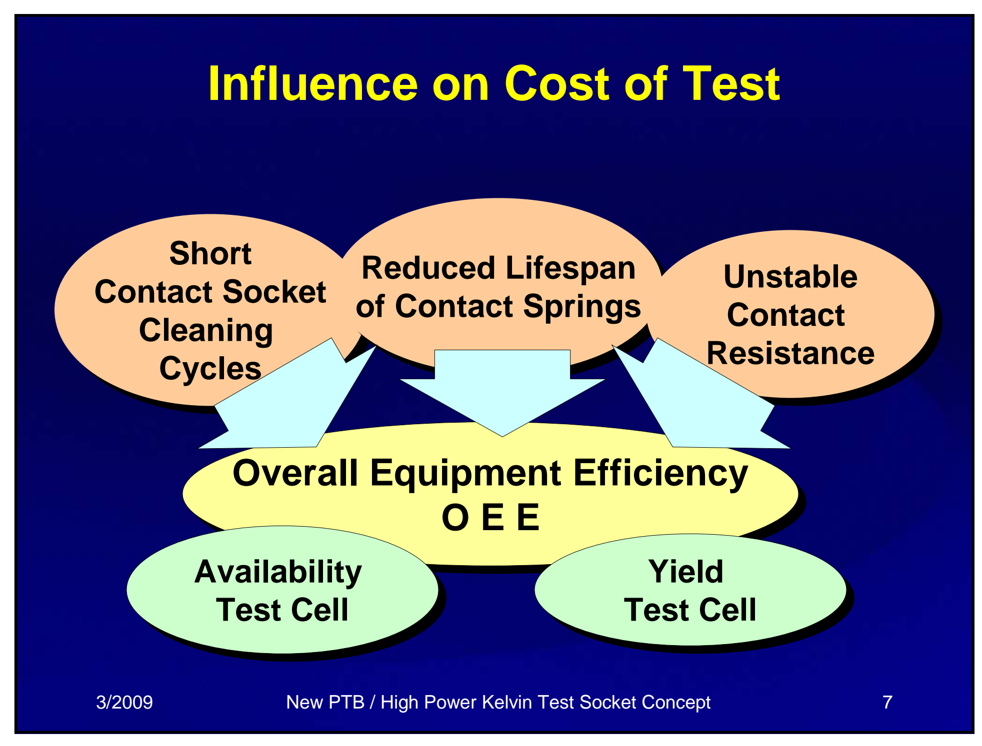

Lead-free Challenges
Materials
PdNiAu
No contact barrier, no
deformation of plating
Matte Tin
Contact barrier Sn oxides
Scrub
Penetrate
3/2009
New PTB / High Power Kelvin Test Socket Concept
6


Influence on Cost of Test
Short Contact Socket Cleaning Cycles
Reduced Lifespan of Contact Springs
Unstable Contact Resistance
Overall Equipment Efficiency
O E E
Availability Test Cell
Yield Test Cell
3/2009
New PTB / High Power Kelvin Test Socket Concept
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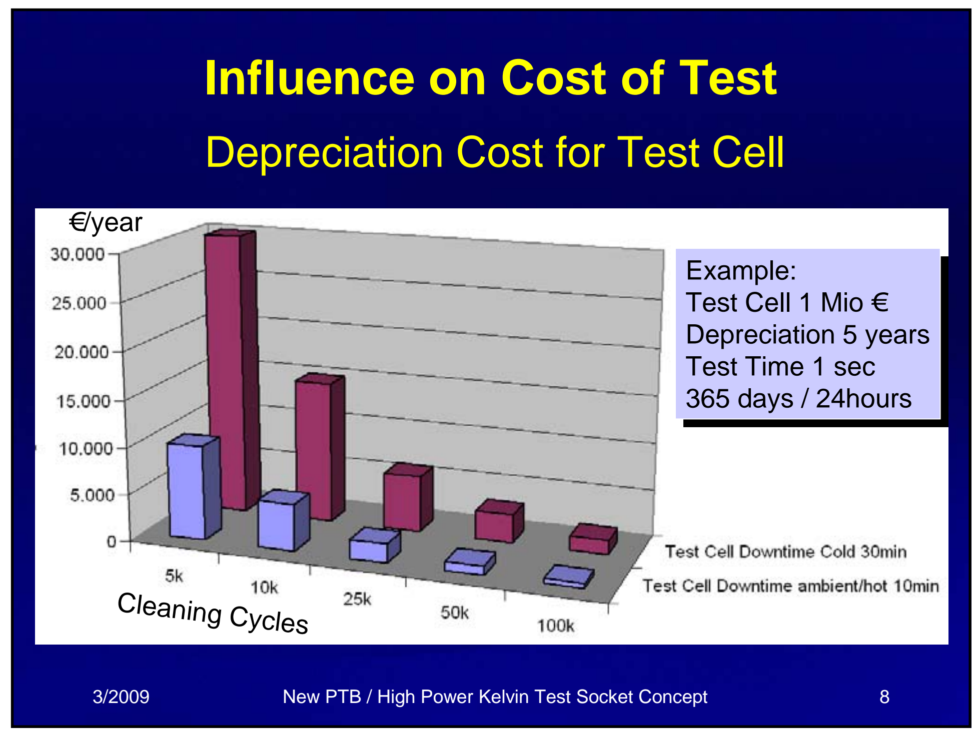
Influence on Cost of Test
Depreciation Cost for Test Cell
€/year
30.000
25.000
20.000
15.000
10.000
5.000
0
5k
10k
25k
50k
100k
Cleaning Cycles
Test Cell Downtime Cold 30min
Test Cell Downtime ambient/hot 10min
Example:
Test Cell 1 Mio €
Depreciation 5 years
Test Time 1 sec
365 days / 24hours
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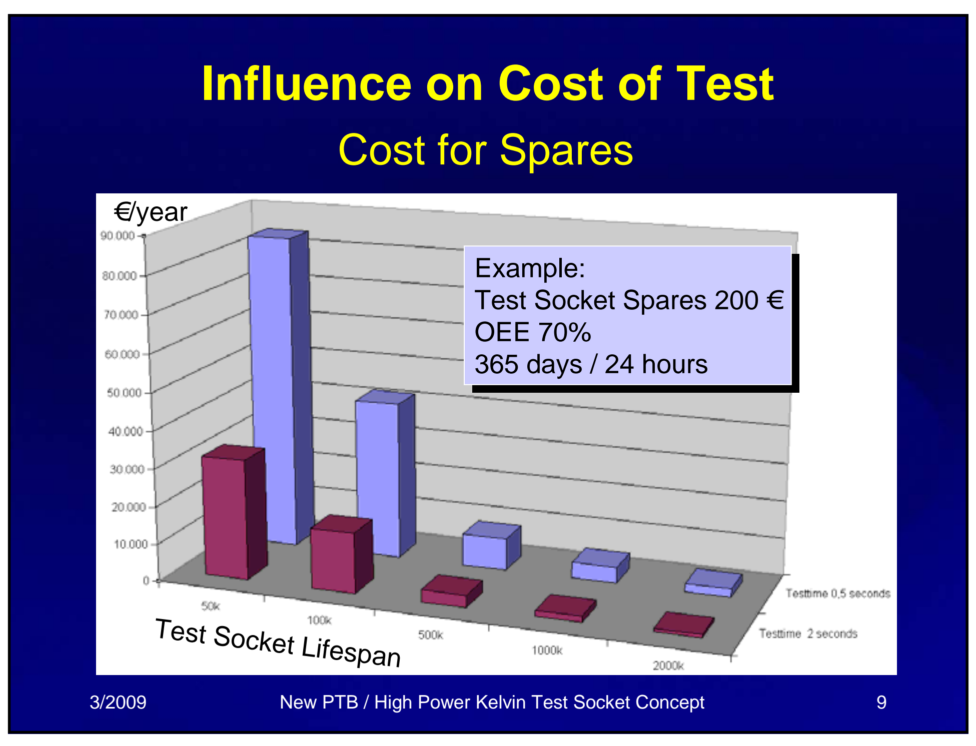
Influence on Cost of Test
Cost for Spares
€/year
Example:
Test Socket Spares 200 €
OEE 70%
365 days / 24 hours
Test Socket Lifespan
3/2009
New PTB / High Power Kelvin Test Socket Concept
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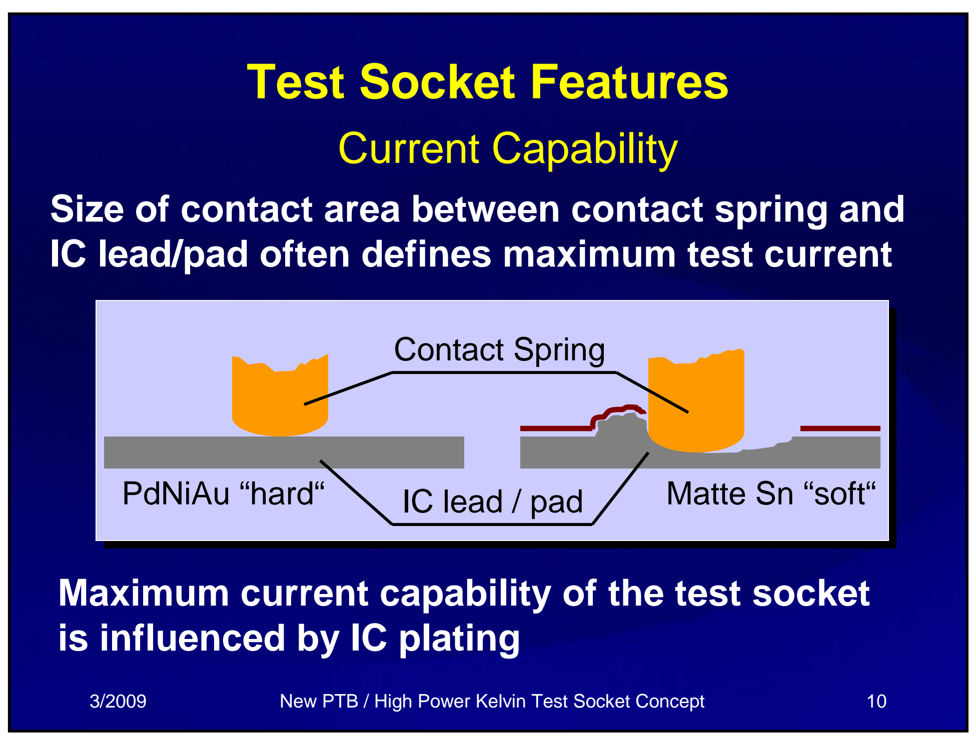
Test Socket Features
Current Capability
Size of contact area between contact spring and IC lead/pad often defines maximum test current
Contact Spring
PdNiAu "hard"
IC lead / pad
Matte Sn "soft"
Maximum current capability of the test socket is influenced by IC plating
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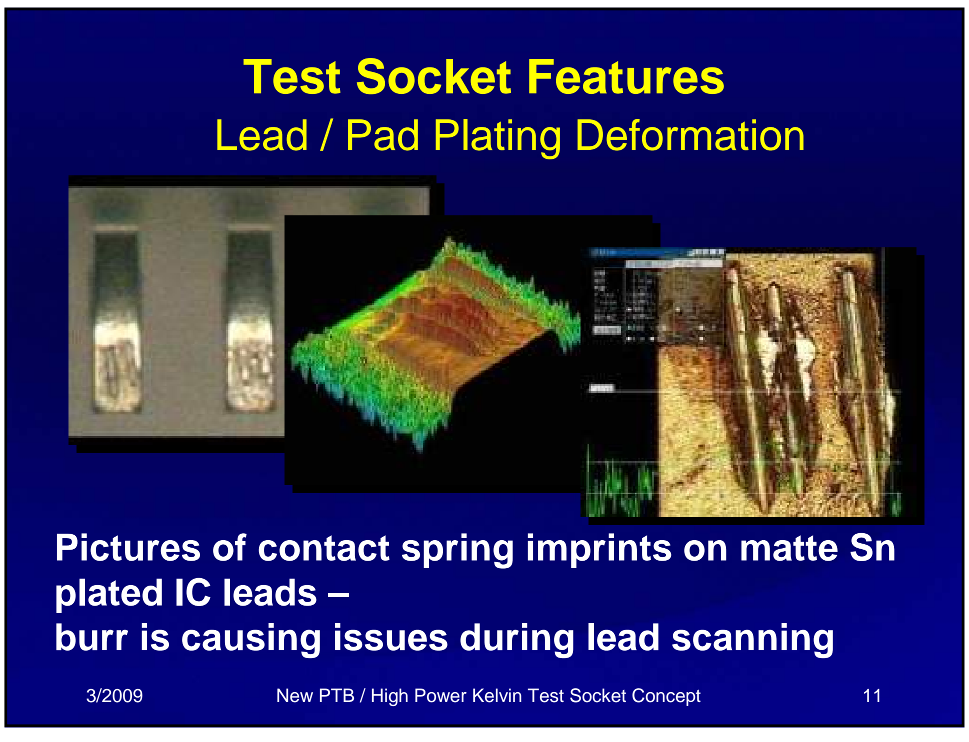
Test Socket Features
Lead / Pad Plating Deformation
Pictures of contact spring imprints on matte Sn plated IC leads –
burr is causing issues during lead scanning
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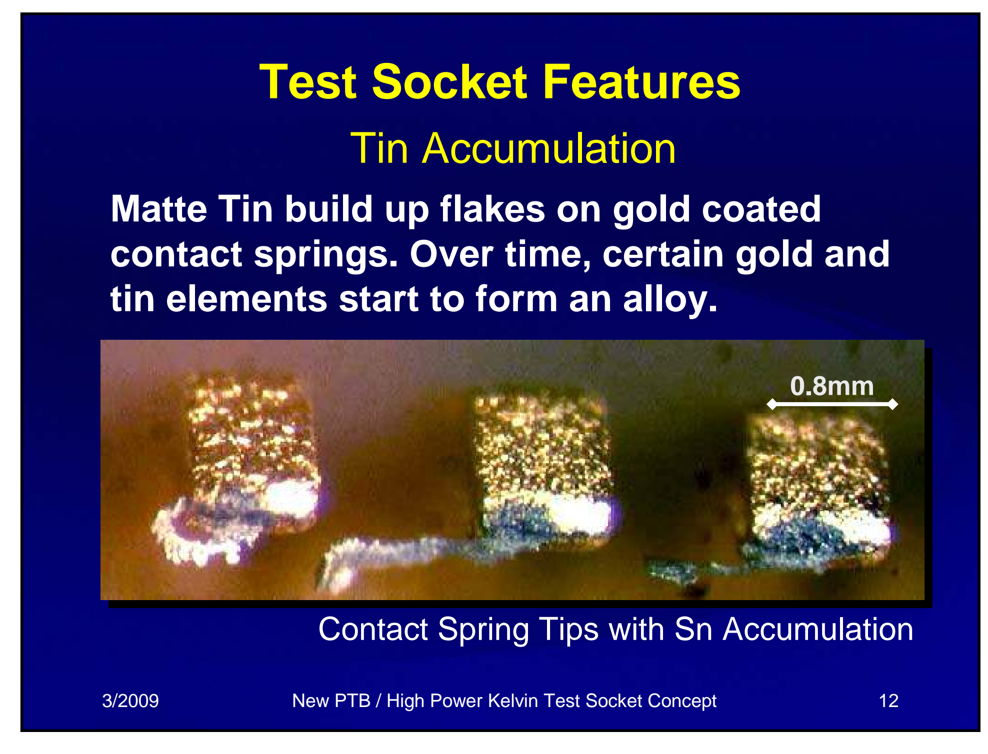
Test Socket Features
Tin Accumulation
Matte Tin build up flakes on gold coated contact springs. Over time, certain gold and tin elements start to form an alloy.
0.8mm
Contact Spring Tips with Sn Accumulation
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12

Test Socket Requirements

Lead-free Requirements

- Contact spring wear resistance against PdNiAu
- No or minimum Sn transfer and accumulation
- Remove / protrude oxide barriers of Sn
- Minimum impact onto IC lead plating
- Compatible electrical behaviour, contact resistance, current capability, signal fidelity etc.

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New Kelvin Contactor Concept

NanoKelvin®

- Cantilever based concept
- Single spring / piece
- Contact springs moulded into plastic body

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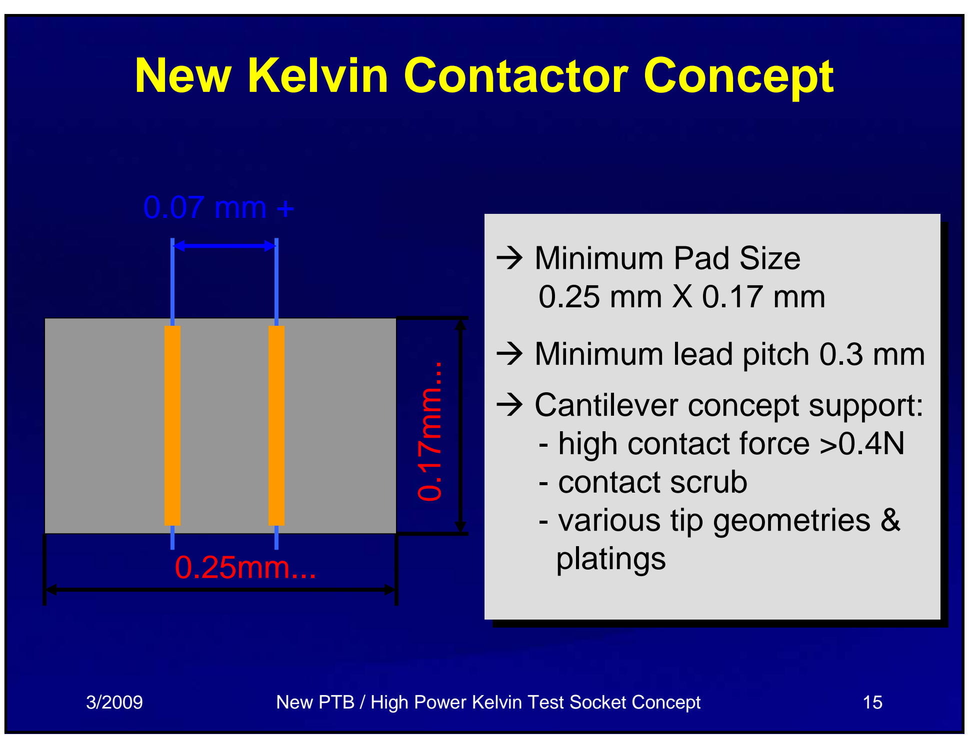
New Kelvin Contactor Concept
0.07 mm +
0.17mm...
0.25mm...
→ Minimum Pad Size
0.25 mm X 0.17 mm
→ Minimum lead pitch 0.3 mm
→ Cantilever concept support:
- high contact force >0.4N
- contact scrub
- various tip geometries & platings
3/2009
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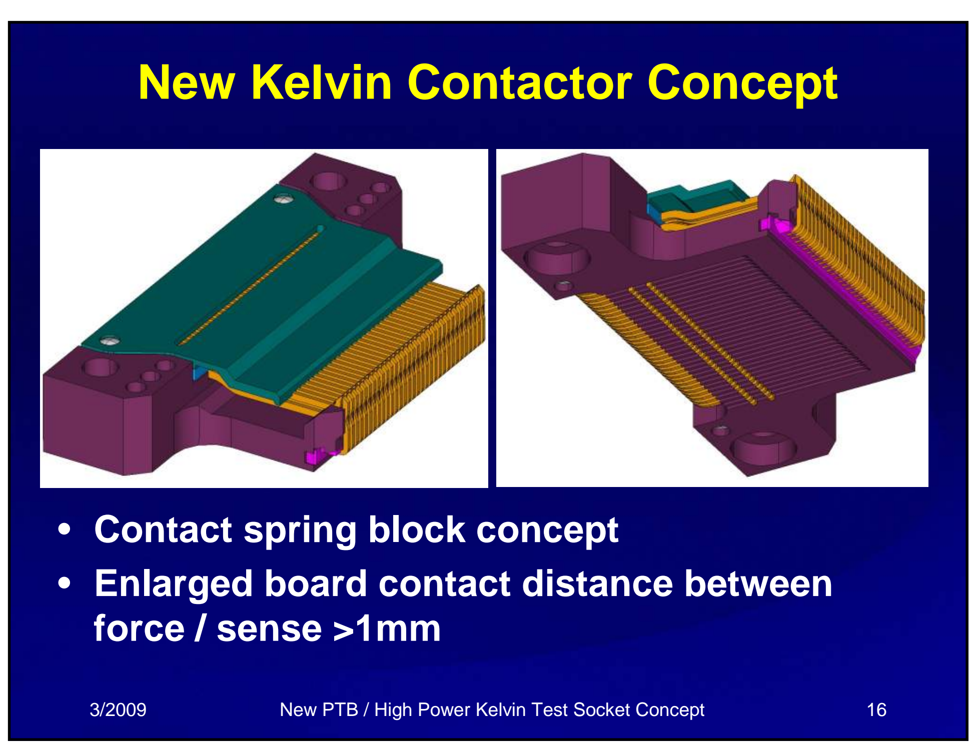
15


New Kelvin Contactor Concept
• Contact spring block concept
• Enlarged board contact distance between force / sense >1mm
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16

New Kelvin Contactor Concept
NanoKelvin®
QFP128/0.4
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New PTB / High Power Kelvin Test Socket Concept
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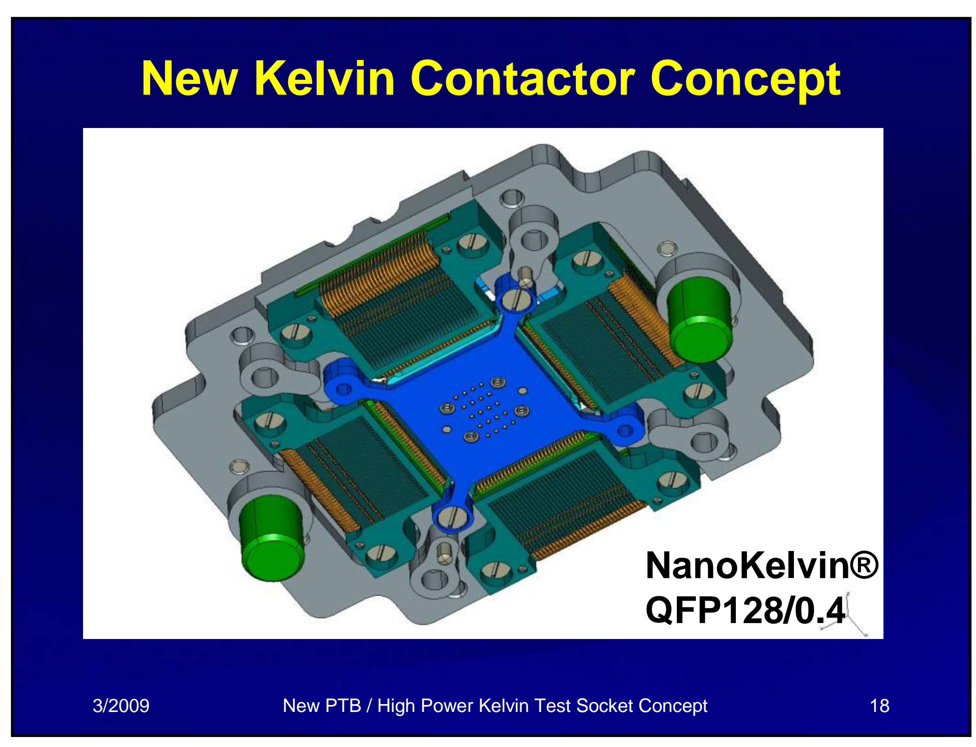
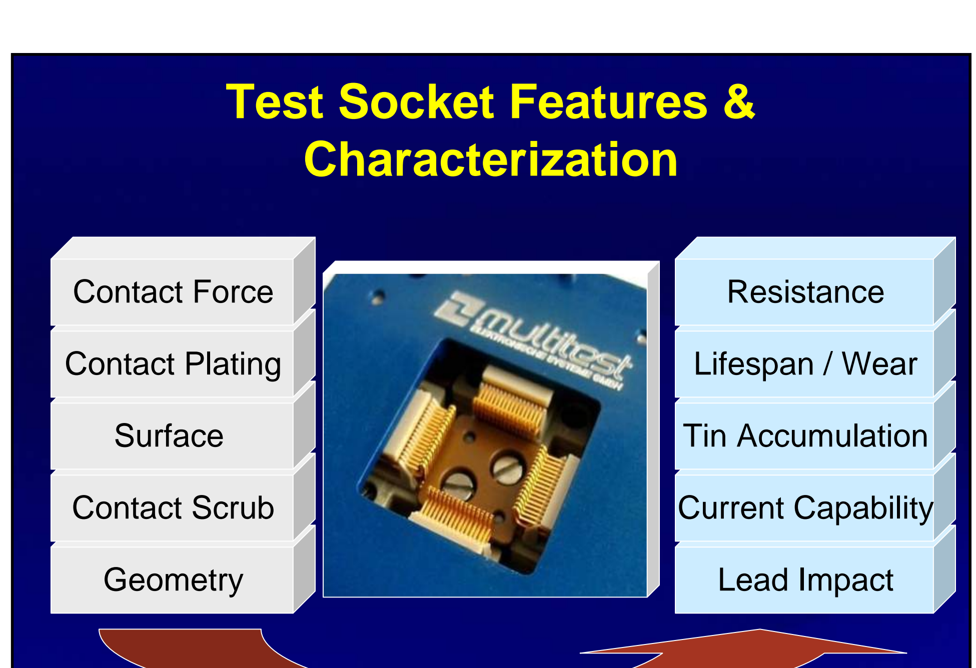

New Kelvin Contactor Concept
NanoKelvin®
QFP128/0.4
3/2009
New PTB / High Power Kelvin Test Socket Concept
18



Test Socket Features & Characterization
Contact Force
Contact Plating
Surface
Contact Scrub
Geometry
multitest
Resistance
Lifespan / Wear
Tin Accumulation
Current Capability
Lead Impact
3/2009
New PTB / High Power Kelvin Test Socket Concept
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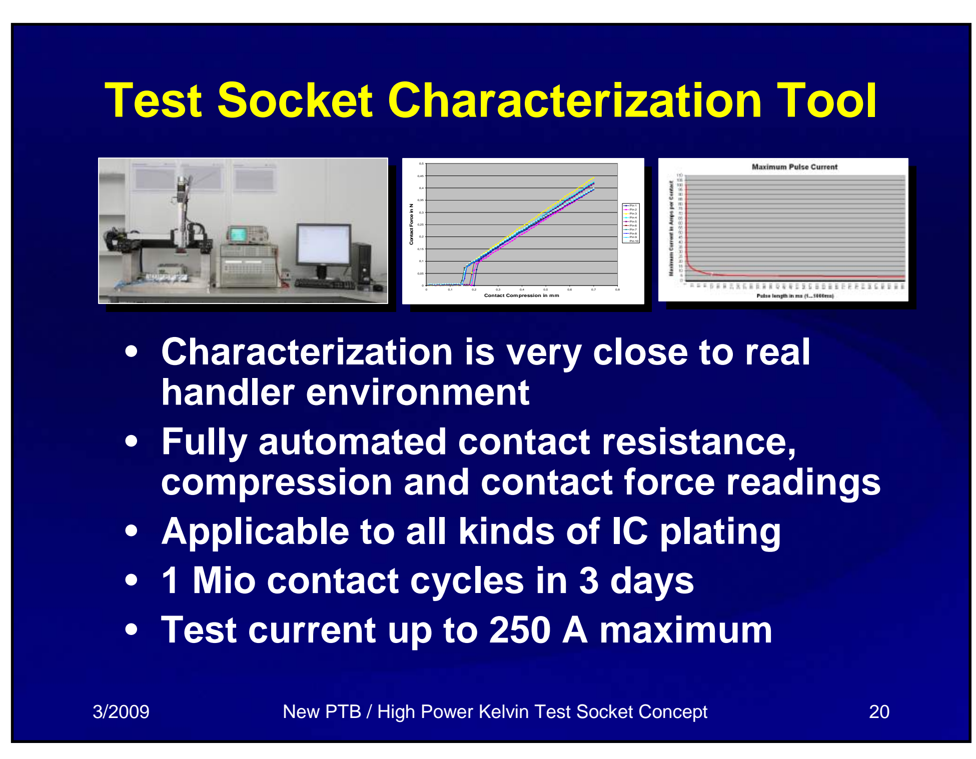

Test Socket Characterization Tool
Maximum Pulse Current
• Characterization is very close to real handler environment
• Fully automated contact resistance, compression and contact force readings
• Applicable to all kinds of IC plating
• 1 Mio contact cycles in 3 days
• Test current up to 250 A maximum
3/2009
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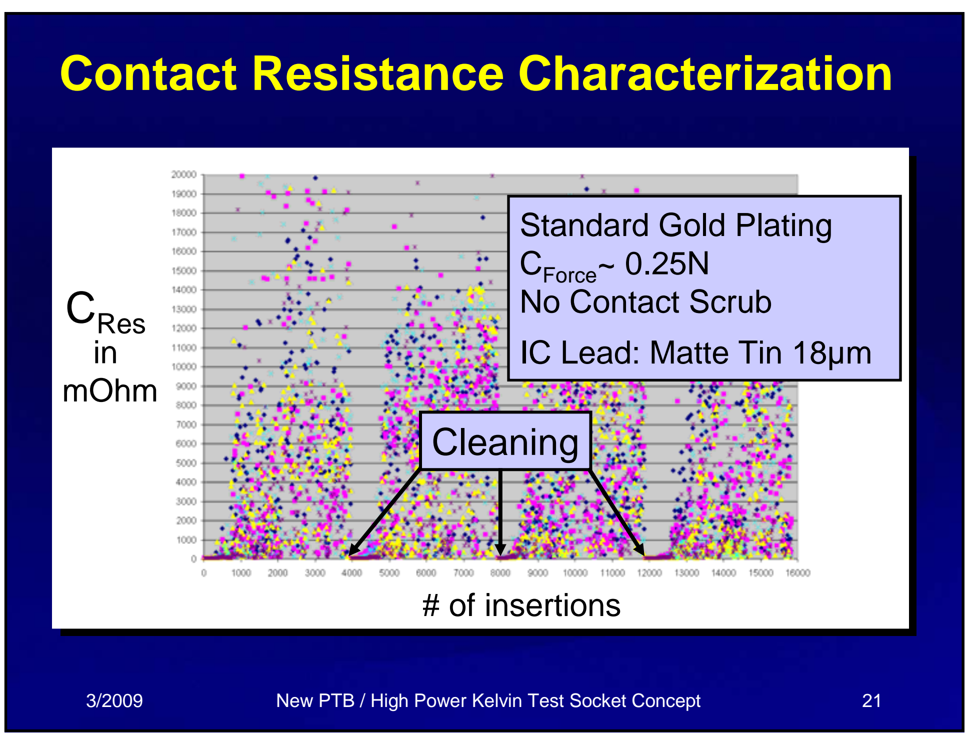
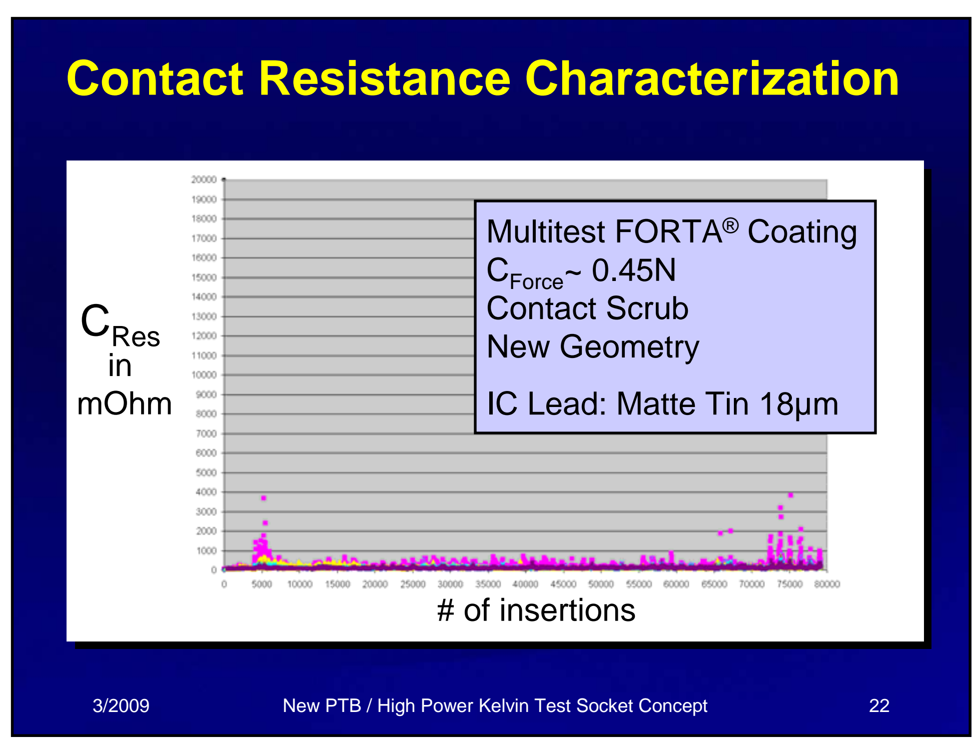
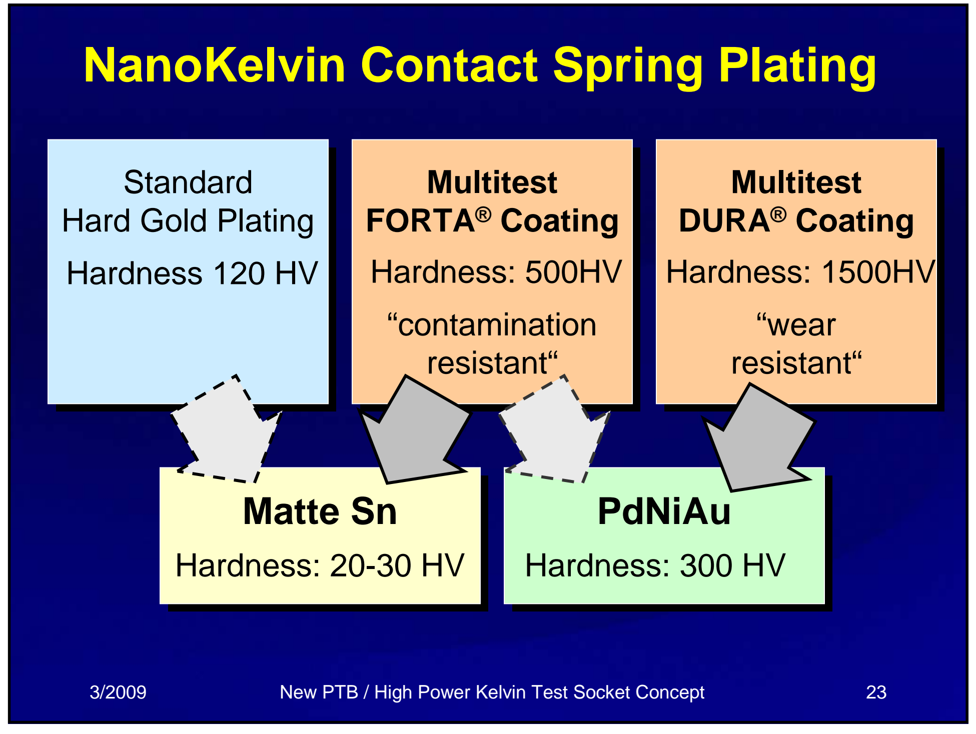
20


Contact Resistance Characterization
Standard Gold Plating
CForce~ 0.25N
No Contact Scrub
IC Lead: Matte Tin 18µm
Cleaning
CRes in mOhm
# of insertions
3/2009
New PTB / High Power Kelvin Test Socket Concept
21


Contact Resistance Characterization
Multitest FORTA® Coating
CForce~ 0.45N
Contact Scrub
New Geometry
IC Lead: Matte Tin 18µm
CRes in mOhm
# of insertions
3/2009
New PTB / High Power Kelvin Test Socket Concept
22


NanoKelvin Contact Spring Plating
Standard
Hard Gold Plating
Hardness 120 HV
Multitest
FORTA® Coating
Hardness: 500HV
“contamination resistant“
Multitest
DURA® Coating
Hardness: 1500HV
“wear resistant“
Matte Sn
Hardness: 20-30 HV
PdNiAu
Hardness: 300 HV
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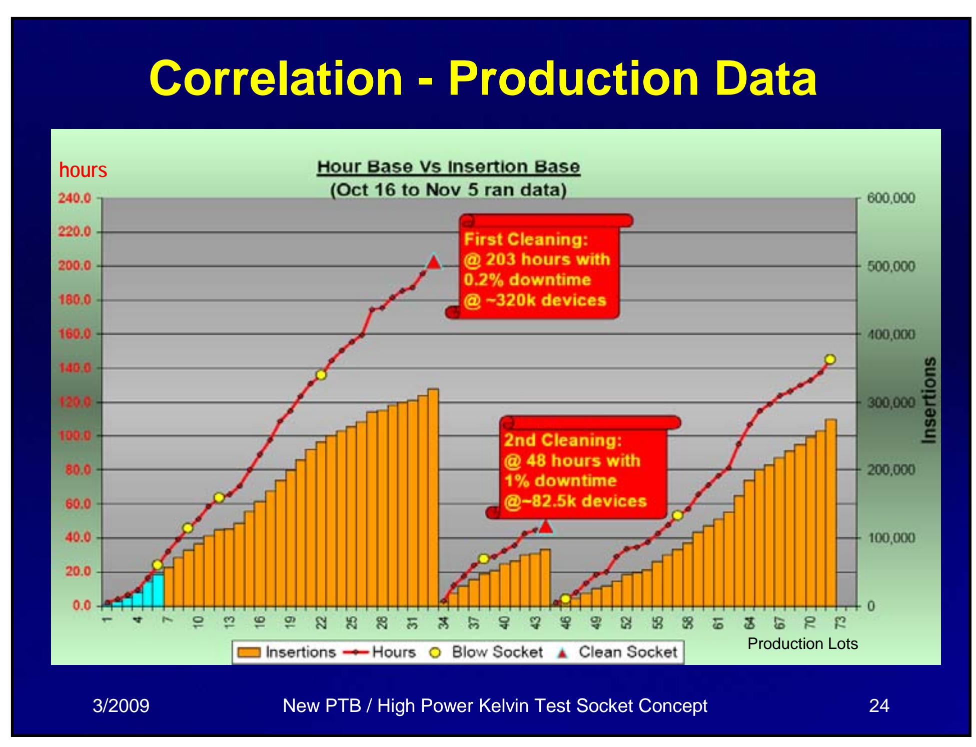
Correlation - Production Data
hours
Hour Base Vs Insertion Base
(Oct 16 to Nov 5 ran data)
First Cleaning:
@ 203 hours with
0.2% downtime
@ ~320k devices
2nd Cleaning:
@ 48 hours with
1% downtime
@~82.5k devices
Insertions
Production Lots
Insertions
Hours
Blow Socket
Clean Socket
3/2009
New PTB / High Power Kelvin Test Socket Concept
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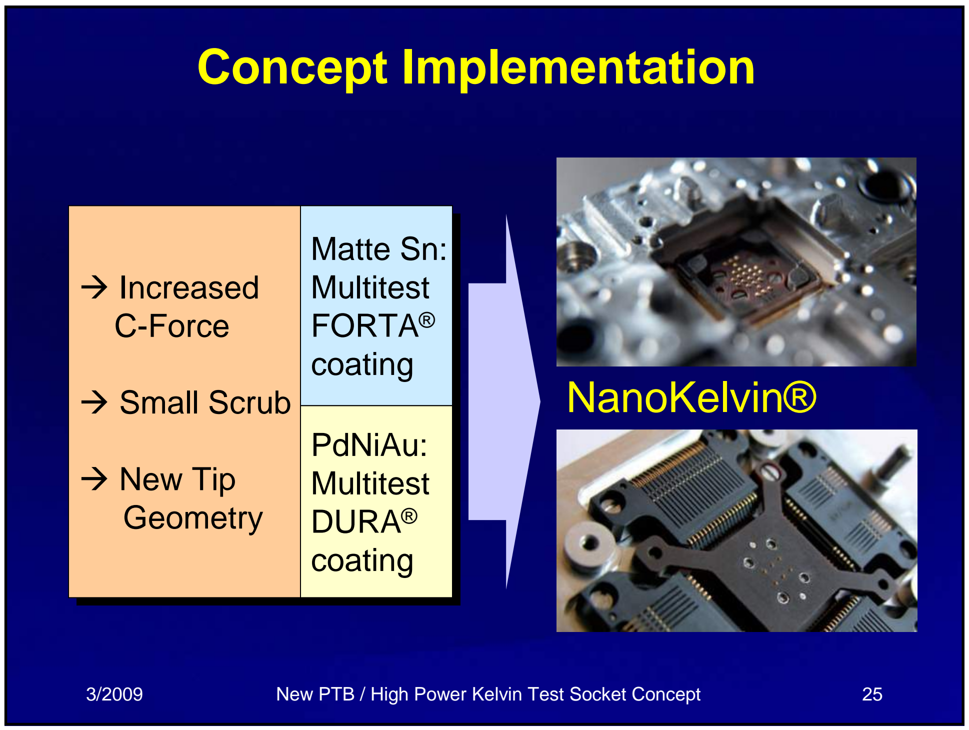

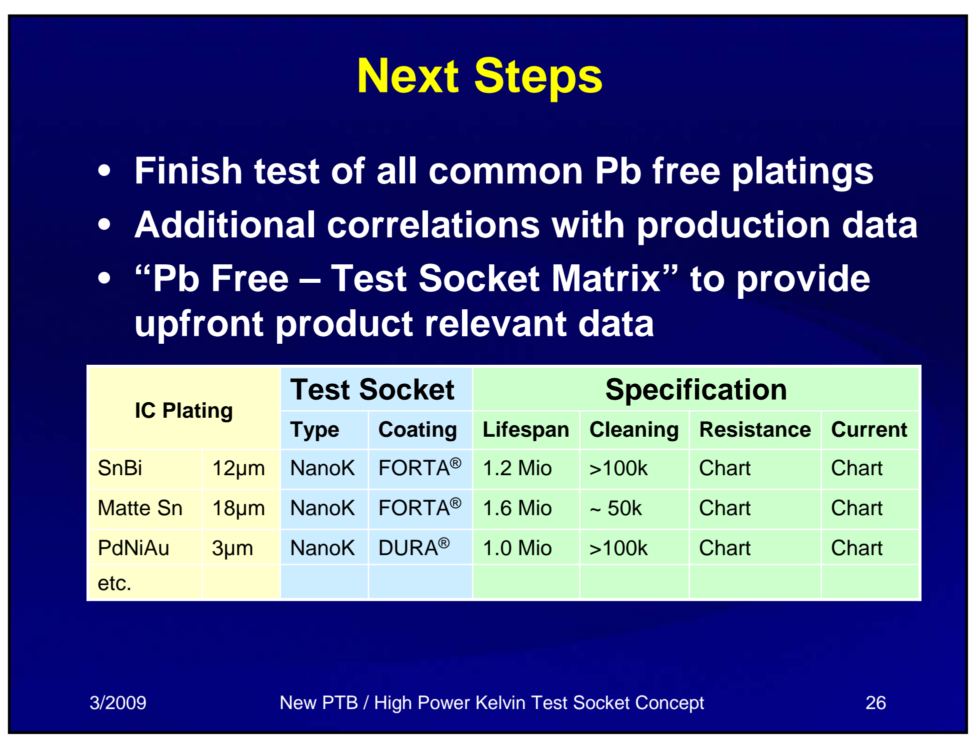

IC Plating		Test Socket		Specification			
		Type	Coating	Lifespan	Cleaning	Resistance	Current
SnBi	12µm	NanoK	FORTA®	1.2 Mio	>100k	Chart	Chart
Matte Sn	18µm	NanoK	FORTA®	1.6 Mio	~ 50k	Chart	Chart
PdNiAu	3µm	NanoK	DURA®	1.0 Mio	>100k	Chart	Chart
etc.							

Summary

- New socket characterization principles allow to lessen the gap between lab test results and socket performance in high volume production
- Matte Sn and PdNiAu plating require dedicated contact coatings to address their individual requirements
- Cleaning cycles better than 50k and socket lifespan above 1Mio insertions, reached by optimized test socket settings, significantly lower cost of test

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