BiTS 2009 — Burn-in & Test Socket Workshop

Session 1

ARCHIVE 2009

LIVING THE HIGH LIFE (HIGH CURRENT & POWER)

Pulsed Current-Carrying Capacity of Small Metallic Conductors as Applied to Device Test
Harlan Faller— Johnstech International Corporation

Power Integrity Ingenuity at Test
Abram Detofsky, Omer Vikinski, Shaul Lupo, Tim Swettlen—Intel Corporation

Moore or Less: Effects of Higher Currents on Socket Life
Kevin DeFord—Interconnect Devices, Inc.

Design Considerations in Socketing High Power Devices
Jec Sangalang—Yamaichi Electronics USA Inc.
Mike Noel—Freescale

Pulsed Current-Carrying Capacity of Small Metallic Conductors as Applied to Device Test

Harlan Faller, P.E.
Johnstech International

2009 BiTS Workshop
March 8 - 11, 2009

Agenda

- Introduction
- Fourier's Law and Heat Transfer
- Pulsed Current Techniques
  - Steady-State vs. Pulsed Current Heating
  - Temperature Behavior in Conductors due to Pulsed Current
  - Transient Analysis
- Case Study: Power MOSFET
  - DUT Type and its Electrical Parameters
  - Heat Generation in DUT due to Applied Pulse of Energy
- Conclusions
- Glossary of Terms
- Appendices

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Introduction

- Objective of this Presentation:
  - To demonstrate Pulsed Current Thermal Techniques as applied to Electrical Conductors and Device Test
- Goal:
  - To provide a set of Guidelines to Users of the Methodology presented herein
- Future Work:
  - Expand on these Guidelines

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Fourier's Law and Heat Transfer

•Fourier's Equation in one dimension

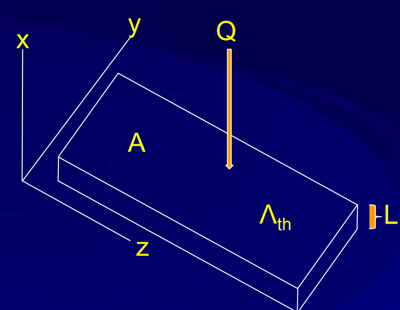
–General: $(\partial^2 T/\partial x^2) = (c*\rho/\Lambda_{th})*(\partial T/\partial t)$

•Λ_{th} = specific thermal conductance
•c = specific thermal capacitance
•ρ = density of material
•T = temperature
•x = coordinates of heat conduction

•Conductive Heat Transfer

–Specific: $Q = -k*A*(\Delta T/L)$

•Q = heat flux in Watts
•k = Λ_{th} = specific thermal conductance
•A = area through which heat is transferred
•ΔT = thermal rise across area of conductance
•L = path length of thermal flow



Schematic of Heat Flow in Conductor

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Steady-State vs. Pulsed Current Heating

- Steady-State: 100% Duty Cycle – Static
  - Consistent, internal heating of DUT and Contact Pins
  - $Q_{INT} = I^2R = m*c_p*\Delta T_{SS}$
  - $\Delta T_{SS} = I^2R/(m*c_p)$
  - Obeys exponential law: $\Delta T = \Delta T_{SS}*(1-e^{-t/\tau})$ → heating
- Pulsed Current Heating: transient – Dynamic
  - Duty cycle less than 100%
  - Single-shot pulse application
  - Multiple pulse application
  - High pulse currents for duty cycles <1%

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Temperature Behavior in Conductor during Steady-State Current Application

- Given a BeCu Contact with these parameters:
  - $R = 1.03 \times 10^{-3}\ \Omega$ — $m = 2.47 \times 10^{-7}$ Kg
  - $c_p = 418.7$ J/Kg-K
  - I = 1 through 6 Amps applied current @ 100% DC
- Table of Current vs. ΔT across Contact

DC (Amps)	Calc. ΔT (°C)	Meas. ΔT (°C)
1.0	+20.0	+20.0
2.0	+23.0	+24.0
3.0	+28.0	+29.0
4.0	+35.0	+38.0
5.0	+44.0	+47.5

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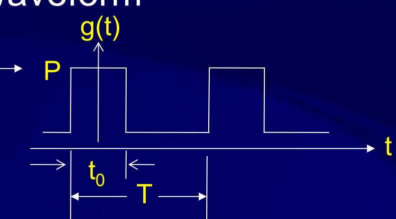
Temperature Behavior in Conductor During Pulse Current Application

- Heating of bond wires ≈ transient heating of one-dimensional slab with a step change in energy generation rate
- CCC* in wire follows same analysis as used for P-C conductors or wire-wrap interconnections

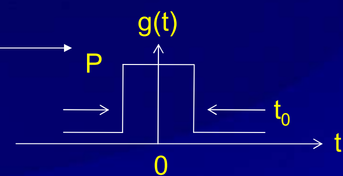
*CCC = Current-Carrying Capacity (Amps)

Temperature Behavior in Conductor During Pulse Current Application

- For a pulsed rectangular waveform
  - $P_{AV} = P * (t_0/T)$
  - $P_{RMS} = P * (t_0/T)^{1/2}$



- For a rectangular pulse
  - $g(t) = P$ for $(-t_0/2) < t < t_0/2)$
    $= 0$ otherwise



Temperature Behavior in Conductor During Pulse Current Application

- Given a BeCu Contact with these parameters:
  - $R = 1 \times 10^{-3}\ \Omega$ $m = 1 \times 10^{-7}$ Kg
  - $P = 1 \times 10^{-3}$ Watts $c_p = 400$ J/Kg-K
  - Conditions: Contact is a "free body" suspended in air
- At a current of 1 amp @ 100% duty cycle ($t_0/T = 1$)
  - $Q_{int} = I^2R = m^* C_p{}^*\Delta T$
  - $\Delta T = (1^2 * 1\times10^{-3})/(1\times10^{-7} * 400) = 25°C \uparrow$
- If duty cycle = 50% ($t_0/T = 0.5$) and peak power remains the same…
  - I = 0.707 amps
  - $\Delta T = (0.707^2 * 1\times10^{-3})/(1\times10^{-7} * 400) = 12.5°C \uparrow$
  - Thus halving the duty cycle, halved the temperature rise

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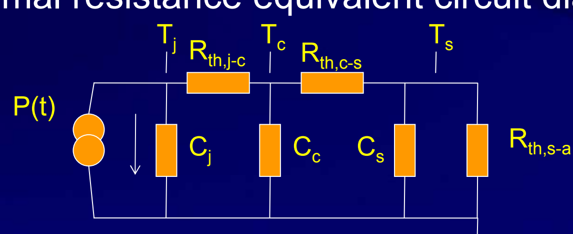
Transient Analysis

- Transient heating of DUT with 100% duty cycle current pulse
- DUT thermal resistance equivalent circuit diagram



R_{th} Schematic Model of DUT-TS

- $T_j = T_{SS}{}^*[1-\exp(-t/(R_{th,x}{}^*C_{th,x}))]$
- $R_{th,x}$ = relative thermal resistance
- $R_{th,x}{}^*\ C_{th,x}$ = time constant (τ)
- t = time (sec)
- $C_{th,x}$ = relative thermal capacitance

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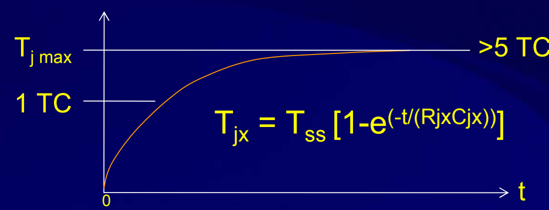
Transient Analysis

- Table & Graph of T_j vs. Time

1 TC =	**63.2% T_{SS}**
2 TC =	86.5% T_{SS}
3 TC =	95.0% T_{SS}
4 TC =	98.2% T_{SS}
5 TC =	99.3% T_{SS}



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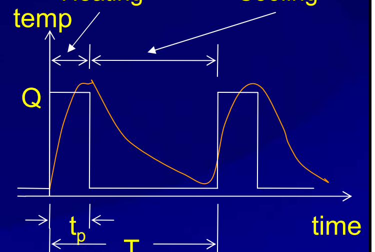
Transient Analysis Using Composite Thermal Equation

- Transient heating of DUT w/ low duty cycle current pulses
- Summation process built on alternate heating & cooling cycles
  - Composite thermal equation: $T_f = T_{amb} + \underbrace{T_{ss}(1- \exp(-t/\tau))}_{\text{Heating}} + \underbrace{T_i(\exp(-t/\tau))}_{\text{Cooling}}$
    - •T_f = final temp/cycle
    - •T_i = temp at end of previous heat cycle
    - •T_{amb} = ambient temperature
    - •T_{ss} = overall steady-state temp
    - •τ = time constant



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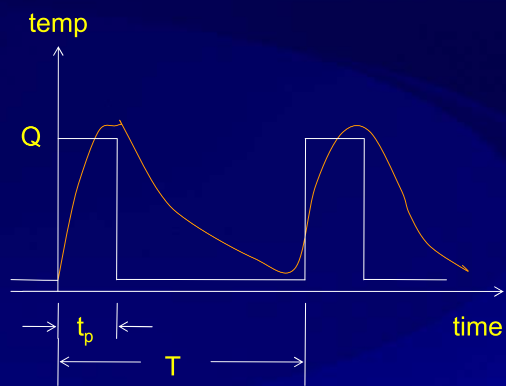
Transient Analysis
Using Composite Thermal Equation

- Graph of heating vs. time
  - –$T(t) = f(t) * R_{th} * Q$
    - $f(t)$ = thermal step function response
    - $f(t_0) = 0$
    - $f(t_\infty) = 1$
    - R_{th} = thermal resistance



Transient Analysis
using Composite Thermal Equation

- A 10 Hertz square wave (P_{AVG} = 1W) is applied to a DUT and cycled 5 times. What is the temperature of the die?

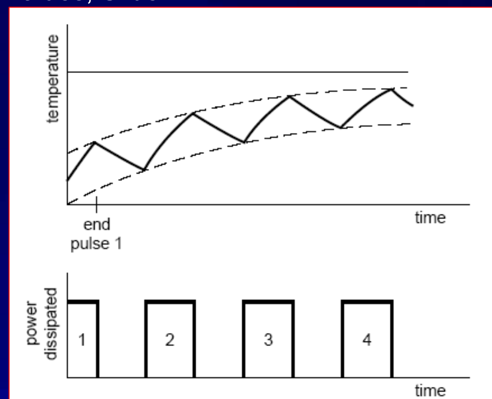
T_{amb} = +30°C R_{th} = 10°C/W T_{ss} = +60°C
C_{th} = 0.01W-sec/°C $T_{ON} = T_{OFF}$ = 0.05 sec TC = 0.10 sec

Table of Calculated Values

T_1	60*(1-exp(-0.05/0.10))	= 23.6°C	Heating	
T_2	23.6*(exp(-0.5))	= 14.3°C	Cooling	
T_3	14.3 + 60*(1-exp(-0.05/0.10))	= 37.9°C	Heating	TC1
T_4	37.9*(exp(-0.5))	= 23.0°C	Cooling	
T_5	23.0 + 60*(1-exp(-0.05/0.10))	= 46.6°C	Heating	
T_6	46.6*(exp(-0.5))	= 28.3°C	Cooling	
T_7	28.3 + 60*(1-exp(-0.05/0.10))	= 51.9°C	Heating	TC2
T_8	51.9*(exp(-0.5))	= 31.5°C	Cooling	
T_9	31.5 + 60*(1-exp(-0.05/0.10))	= 55.1°C	Heating	~TC3
T_{10}	55.1*(exp(-0.5))	= 33.4°C	Cooling	

Transient Analysis

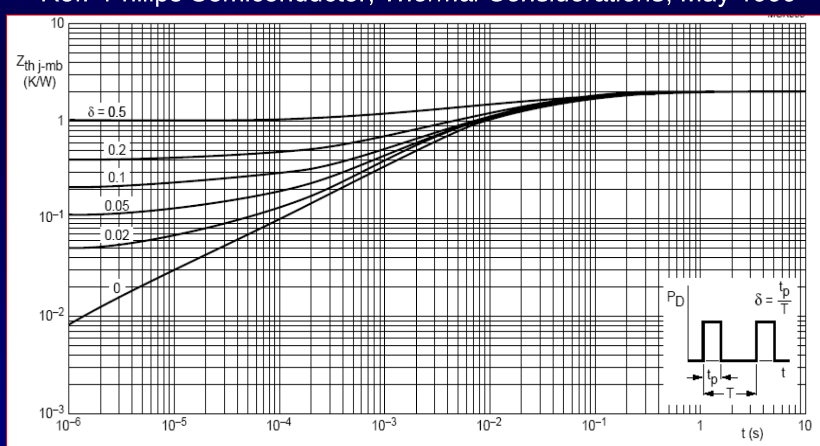
- Chart showing series of power pulses
  - Ref 1: Philips Semiconductor, *Thermal Considerations*, May 1999
  - Ref 2: Table of Calculated Values, Slide 14
- A train of power pulses increases T_{AVG} because the DUT doesn't have time to cool between pulses
  - Cf. Chart at right



Transient Analysis

Graph of thermal impedance vs. pulse time/duty factor

Ref: Philips Semiconductor, *Thermal Considerations*, May 1999



Transient Analysis

Things to consider when using Graph on previous slide

- If pulse time is very short:
  - Power dissipated doesn't have a limiting action
  - Pulse current and maximum voltage form the only limits
- A train of power pulses increases T_{AVG} :
  - DUT doesn't have time to cool between pulses
- Short pulses at low frequencies:
  - Lower the final temperature that the DUT junction reaches
- Peak junction temp usually occurs at end of applied pulse:
  - Its calculation will involve transient thermal impedance
- Avg. junction temp is calculated (if applicable) by using avg. power dissipation and the DC thermal resistance

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Calculations using Data & Graph

- Calculate junction temp of DUT
  - Use a single-shot pulse
    - Peak current and voltage = 50 amps @ 20VDC for 100 microseconds
    - Pulse repeated after 20 seconds (Duty Cycle, $\delta \sim 0$)
    - $P_p = I^*E = 50*20 = 1000$ Watts
    - $T_{mb} = +30°C$
  - Use transient analysis for short duration pulse
    - $Z_{th,j\text{-}mb} = 1.8\times10^{-2}$ K/W (from graph on slide 16)
    - $\Delta T_{j\text{-}mb} = P^*Z_{thj\text{-}mb} = 1\times10^{3} \times 1.8\times10^{-2} = 18°C$
    - $T_{j\text{-}peak} = T_{mb} + \Delta T_{j\text{-}mb} = 30 + 18 = +48°C$

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Calculations using Data & Graph

- Calculate junction temp of DUT, cont'd...
  - Salient facts gleaned from this high power application
    - Junction temp of device is not exceeded if pulse is…
      - Of short duration
      - Single-shot or low duty cycle

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Case Study: Power MOSFET

Analytical procedure to determine junction temp of die subjected to a particular pulse width and peak power

- DUT type and its electrical parameters
- Test socket and contact pin data
- Contact pin, insert & IF parameter values
- Interface geometry for DUT-TS-LB
- Interface evaluation & thermal rise
- Heat generation in DUT & mounting base
  - Application of high power pulse to DUT
  - Temperature of mounting base
  - Temperature of junction of die

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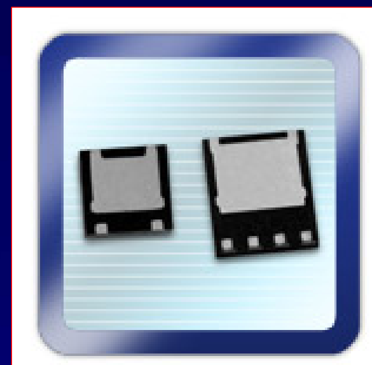
DUT Type and Electrical Parameters

- Package size: 3.3 x 3.3 mm, 0.65mm pitch, 8 pads
- Electrical parameters
  - V_{IN} =20V, max.
  - I_{IN} = 40 A, max.
  - Specific heat ~ 200J/Kg-K
  - Mass ~ $1x10^{-4}$ Kg
  - Electrical resistivity (R_e) ~ $1x10^{-2}$ Ω
- Other
  - $R_{th, j-c}$ = 2.4°C/W
  - $C_{th, j-c}$ = 0.1W-sec/°C
  - $J_{T,max}$ = +175°C
  - P_{DISS} (<10sec) = 3.8W



Power QFN MOSFET
Courtesy: PSi Technologies

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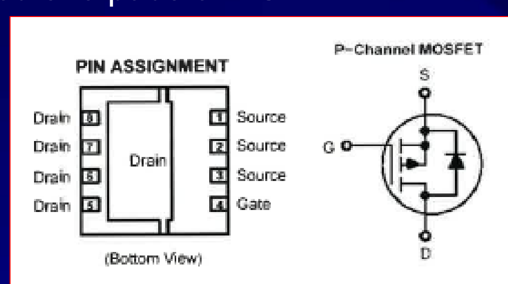
Test Socket and Contact Pin Data

- Contact Pins: AuNi-plated BeCu – 8 req'd.
- Ground/Thermal Insert: Copper
- Surface of DUT leads: Matte Tin or NiPdAu-plated
- Force of DUT against Contacts at I.F. ~65 grams/pin
- Typical Contactor pin-outs to pads of DUT
  - Source: 3 pins
  - Gate: 1 pin
  - Drain: 4 pins



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Contact Pin, Insert & IF Data

Calculated Contact Pin/Insert/IF values

Parameter	Calc. Value
R_E (Contact Pin)	7.0×10^{-4} Ω/pin
R_E (IF)	1.3×10^{-3} Ω/IF
R_E (Contact Pin + IFs)	3.3×10^{-3} Ω
R_E (Copper Insert)	2.6×10^{-6} Ω
R_E (Copper Insert + IFs)	3.9×10^{-5} Ω
R_{TH} (Contact Pin)	142°C/W
R_{TH} (Contact Pin + IFs)	150°C/W
R_E (Copper Insert)	0.5°C/W
R_E (Copper Insert + IFs)	1.0°C/W

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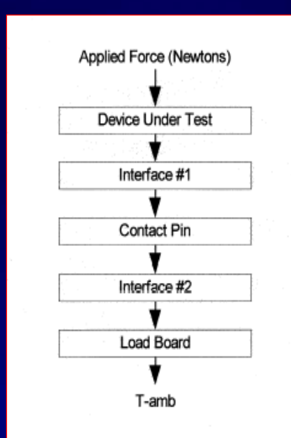
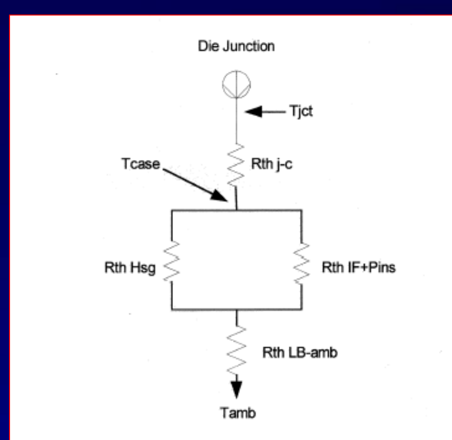
DUT $R_{th,x}$ Geometry for DUT-TS-LB

Block and schematic diagrams of DUT $R_{th,x}$ geometry





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Interface Evaluation & Thermal Rise

- Evaluation of IFs @ V_{IN} = 20V and 40A
  - $V_{IF,\ Sn\text{-}BeCu}$ = 40A*7.6x10^{-4}Ω/3 pins = 10mV/pin
  - $V_{IF,\ Au\text{-}BeCu}$ = 40A*1.3x10^{-3}Ω/3 pins = 13.4mV/pin
  - Softening voltage is 70mV for tin and 80mV for gold
- Calculate S-S temp rise across contact pins
  - $\Delta T_{SS} = I^2R/(m^*c_p) = 40^2 * (1.1\text{x}10^{-3}/3)/(3^*2.6\text{x}10^{-6}*418.7) = 171°C$
  - R_{th} = 150/3 = 50.0°C/W
  - $C_{th} = m^*c_p$ = 3*262x10^{-6}*418.7 = 3.3x10^{-3} W-sec/°C
  - τ = R_{th} * C_{th} = 50.0* 3.3x10^{-3} = 165 milliseconds
  - ΔT_{pin} = 171*(1-exp(-0.100/165)) = 0.1°C

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Heat Generation in DUT & Mounting Base

- Apply a single-shot pulse of 800W peak for 100 microseconds
  - Duty cycle (δ) ~ 0
  - Apply graph from slide 16 – go to curve of (δ) ~ 0
  - $Z_{th,\ j\text{-}mb}$ = 0.1°C/W
  - $\Delta T_{j\text{-}mb} = P_{PEAK} * Z_{th,\ j\text{-}mb}$ = 800 * 0.1 = 80°C
- Determine temp of mounting base from thermal equation
  - Mass of metal = 2.0x10^{-5}Kg
  - R_E = 8.6x10^{-4}Ω
  - τ = 165x10^{-3} secs
  - T_{mb} = +25 + 171*(1-exp(-1x10^{-6}/165x10^{-3})) = 25°C
- Calculate the temp of the die junction
  - $T_{j,die} = T_{mb} + \Delta T_{j\text{-}mb}$ = +25 + 80 = 105°C < 175°C

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Conclusions

- Generally, reducing the duty cycle of a current pulse applied to a conductor reduces its internal temperature rise
- Transient analysis can be done in several ways…
  - By using the equations presented herein
  - By using a thermal Z vs. pulsed DC graph
- Application of a high peak power pulse of short duration to a power MOSFET is possible w/o damage to the device, providing:
  - Applied pulse is single-shot and of short duration (Duty cycle ~ 0)
  - Repetition time of pulse is very long (several seconds)
  - Breakdown voltage of the device is not violated
- Examples and most data in this presentation are calculated

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Glossary Of Terms

Terms and Units used in Heat Transfer

– Heat flux	J/m^2-s
– Heat transfer rate	$dQ = qA(W/m^2)$
– Mass density, ρ	Kg/m^3
– Specific heat, c_p	J/Kg-K
– Thermal conductivity, k	W/m-K
– Thermal energy	Q(Joules)
– Thermal resistance, R_{TH}	°C/W
– Thermal capacitance, C_{TH}	W-sec/°C
– Thermal time constant, γ or τ	seconds

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Appendix A: Thermal Characteristics of Materials

Material	Conductivity	Specific Heat
Silver	429.0 W/m-K	325 J/Kg-K
Copper	401.0	384
Gold	319.0	129
Aluminum	237.0	903
Tungsten	173.0	125
Nickel	90.4	444
Beryllium-Copper	90.0	420
Iron	80.4	450
Platinum	71.6	133
Tin	66.8	227
Lead	35.3	128

Source: Ruben, S., *Handbook Of The Elements* (Open Court: La Salle, IL 1996)

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Appendix B: Softening/Melting Voltages

Material	Softening Volts (V)	Melting Volts (V)
Aluminum	0.10	0.30
Iron	0.19	0.19
Nickel	0.16	0.16
Copper	0.12	0.43
Zinc	0.10	0.17
Silver	0.09	0.37
Cadmium	0.15	---
Tin	0.07	0.13
Gold	0.08	0.43
Palladium	0.57	0.57
Lead	0.12	0.19
60Cu,40Zn	0.20	---

Source: Timron Scientific Inc., *Electrical Contacts And Electroplates In Separable Connectors*

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Appendix C: Critical Factors of Thermal Paths

- Pressure at the interface
- Hardness of the contact surfaces
- Size of the contact surface asperities
- Geometry of contacting surfaces
- Average gap thickness of void spaces
- Thermal conductivity of fluid in void spaces
- Thermal conductivity of contact materials

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Power Integrity Ingenuity at Test

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2009 BiTS Workshop
March 8 - 11, 2009

Agenda

- Tester Power Delivery Basics
- Time versus Frequency Domain Analysis
- HVM Test and the Challenges of Package scaling
- The Capacitor-in-Socket (CiS) Concept
- CiS Performance Data
- CiS Challenges and Next Steps
- Conclusions

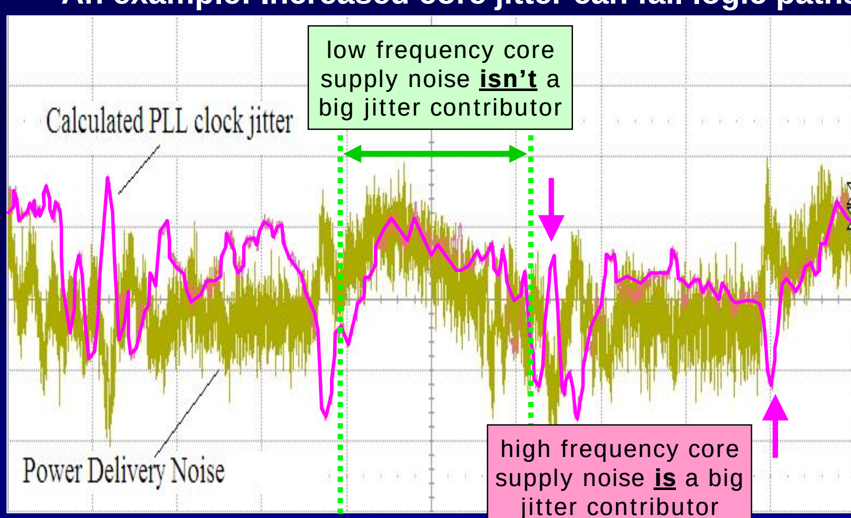
3/2009 Power Integrity Ingenuity at Test 2

Tester Power Delivery Basics

- **The purpose of a power delivery network is distribute power and return current to each CPU device under test while:**
  - **Keeping rail collapse/ripple under a specified value**
  - **from DC to the full bandwidth of the switching CPU's switching elements**

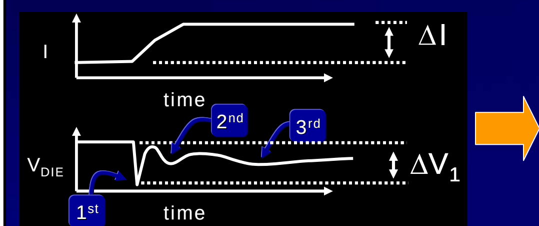
Why is a good PDN Important?

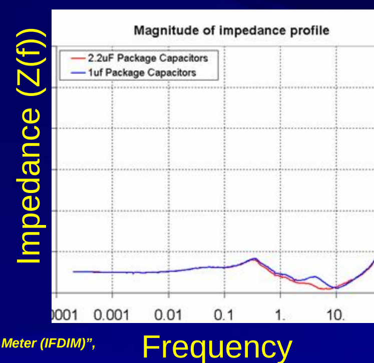
- **An example: Increased core jitter can fail logic paths**



Analysis Methods

- We've migrated our design methods from time domain to frequency domain



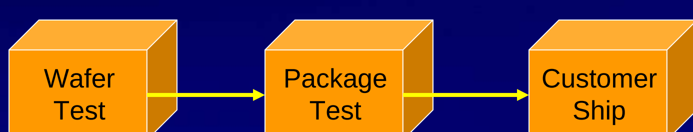


Source: Alex Waizman, "Integrated Power Supply Frequency Domain Impedance Meter (IFDIM)", Electrical Performance of Electronic Packaging, 2004. IEEE 13th Topical Meeting

3/2009 Power Integrity Ingenuity at Test 5

What is Manufacturing Test?

- The purpose of manufacturing Test is to:
  - Screen for defects (primarily the job of the Wafer Test module)
  - Classify the DUT (primarily the job of the Package Test modules)
  - Configure the DUT (done at various wafer and package Test steps)



HVM Test = defect screen + classification + configuration

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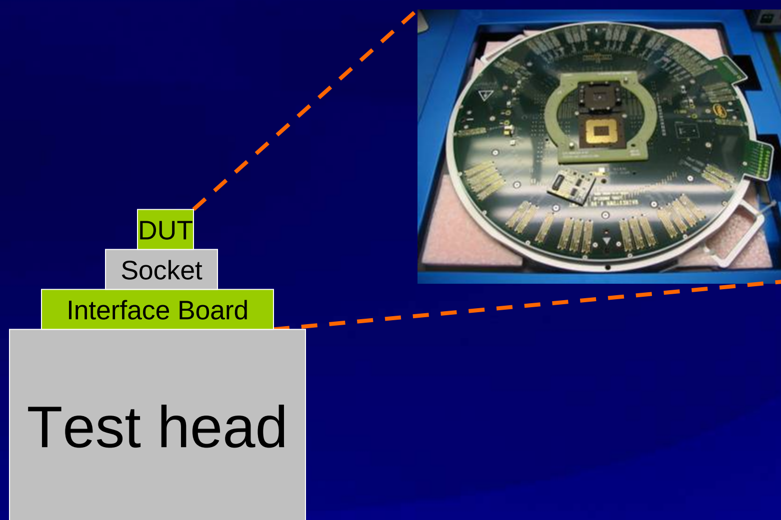
Package (Class) Test in Pictures



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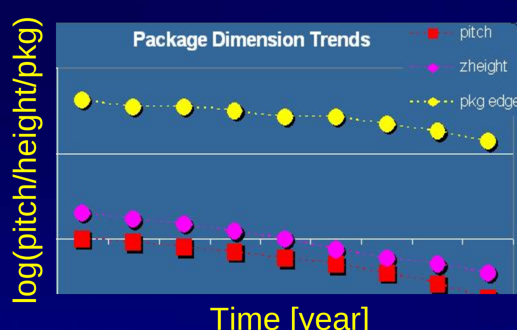
The Problem

- **Aggressive package scaling continues on modern microprocessors**



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The Problem (cont.)

- Package designers trade-off package area reductions and on-package components like capacitors
- Capacitor removal places more Power Integrity burden on the customer motherboard and the DIB

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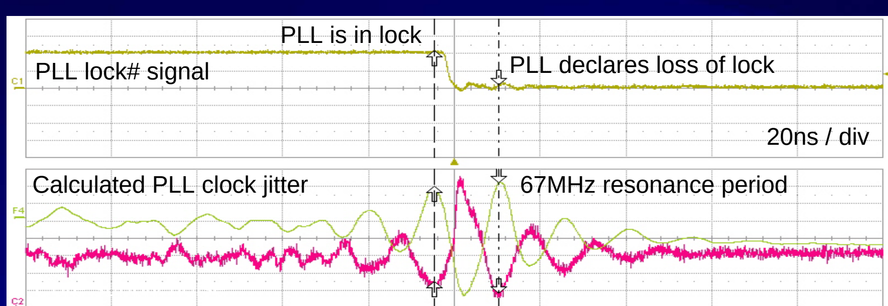
The Problem in the Time Domain

- For small form factor CPUs, Vcc power integrity droop was causing the PLL to lose lock in the TIU



data by S. Smoler and A. Shema

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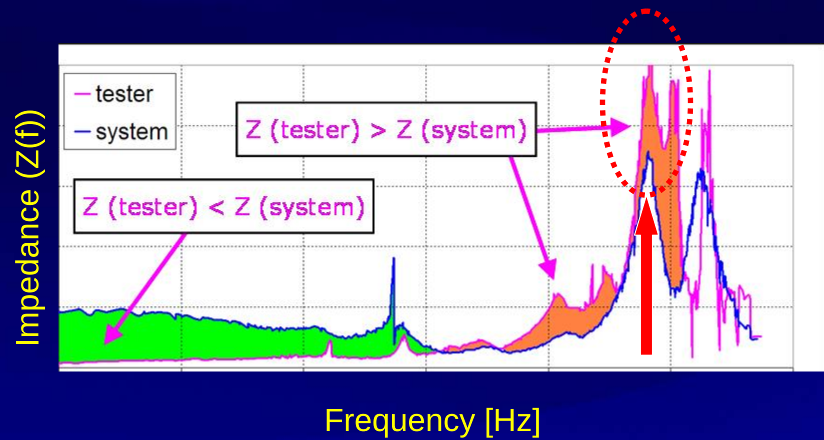
The Problem in the Frequency Domain

- Big differences seen at ~70MHz resonance



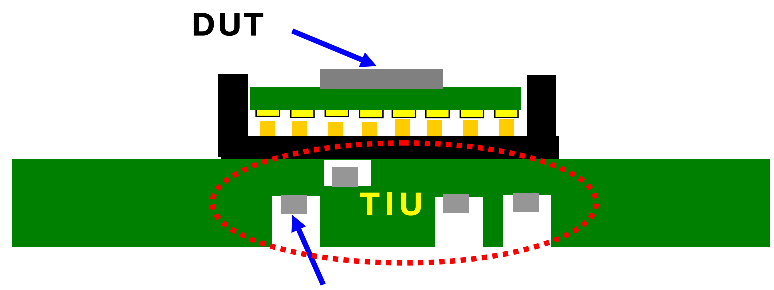
Comparing the CRB and TIU

- The TIU has decoupling capacitors much farther away from the DUT than the Customer Reference Board (CRB)

Paper #2

Alternate solutions: Recess Cavity PCB Design

- Create cavities in the PCB to bring the capacitors closer to the DUT
  - shortens the inductive loop



Caps located in recessed cavities

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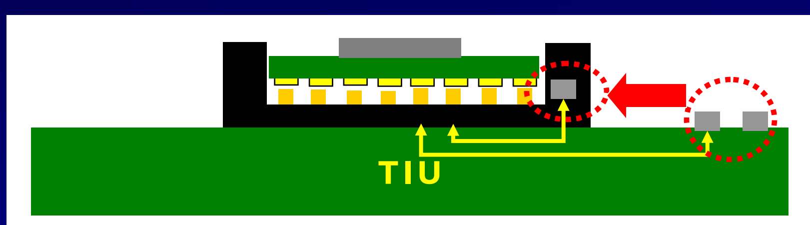
Alternate solutions: Embedded Capacitors

- Move capacitors into the socket perimeter
- Helps by shortening the inductive loop between DUT and caps



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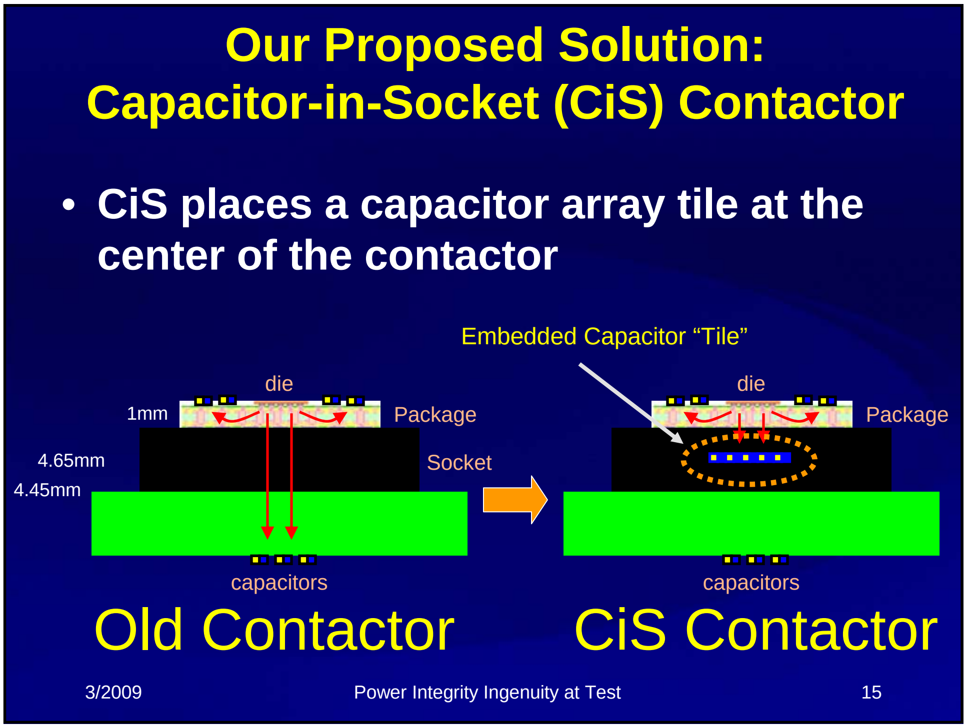
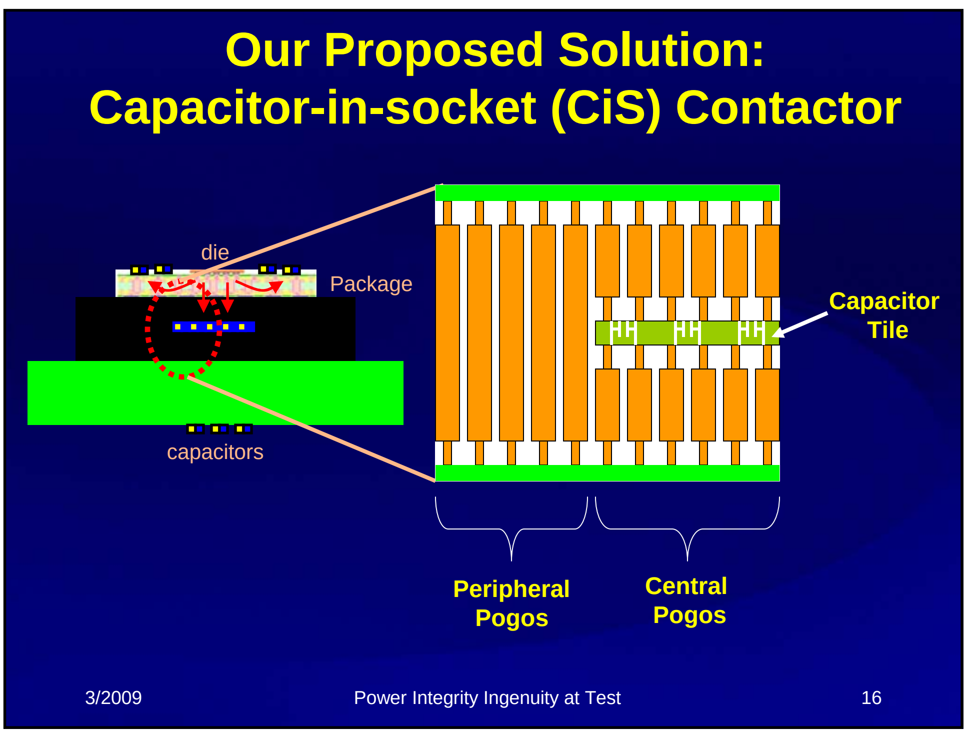
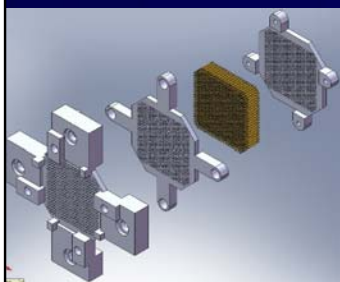

Our Proposed Solution:
Capacitor-in-Socket (CiS) Contactor
• CiS places a capacitor array tile at the center of the contactor
Embedded Capacitor "Tile"
die
1mm
Package
4.65mm
4.45mm
Socket
capacitors
die
Package
capacitors
Old Contactor
CiS Contactor
3/2009
Power Integrity Ingenuity at Test
15

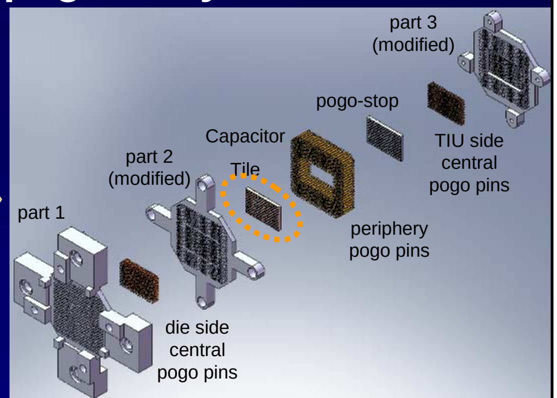

Our Proposed Solution:
Capacitor-in-socket (CiS) Contactor
die
Package
capacitors
Capacitor
Tile
Peripheral
Pogos
Central
Pogos
3/2009
Power Integrity Ingenuity at Test
16

The Capacitor-in-Socket (CiS) Solution

- CiS partitions the contactor into TIU and die-side central pogo arrays



Today



CiS

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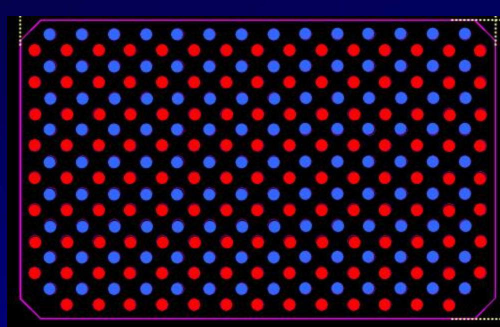
The Capacitor Tile

- The Tile can be ceramic or PCB-based…
- ~60uF total for Vcc core



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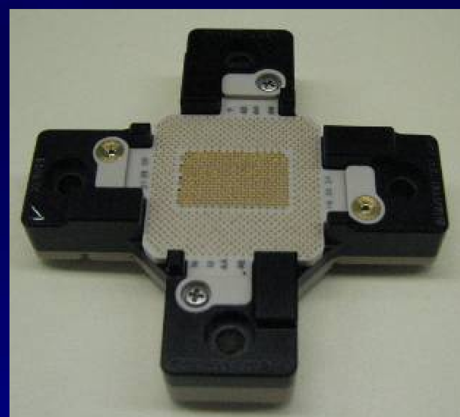
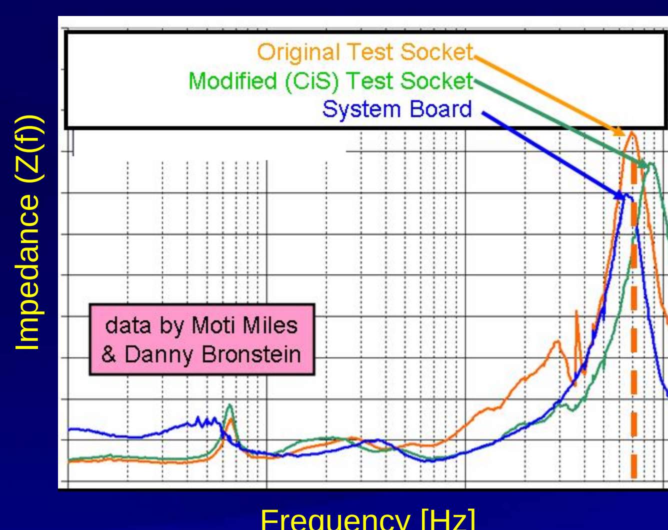
CiS in Photos

- CiS CPU Socket



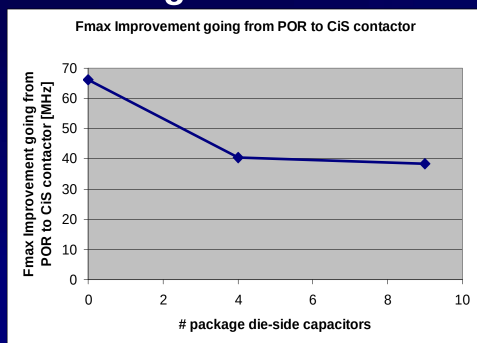
Frequency-domain Performance of CiS

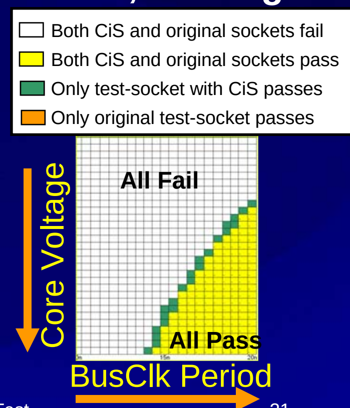
- CiS contactor attenuates and shifts the 70MHz resonance peak



CiS Performance: Fmax

- CPU performance improvements seen in terms of core Fmax
- The fewer the package capacitors, the larger the gains





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CiS Challenges

- CiS CPU Socket needs to complete HVM qualification next
  - Thermal cycling, Co-planarity checks, Contact resistance life cycling >100K cycles
- CiS Hardware Concerns
  - Contactor is very complex
    - 3 pin flavors; need to find ways to simplify
  - Factory maintenance a concern
  - How well does the Capacitor Tile scale with shrinking BGA pitches?
- How can the supply base help us address these concerns? How could we do this better?

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Conclusions

- There is constant pressure for reducing CPU package size which forces power integrity design trade-offs
  - More burden is placed on Test hardware
- Concepts like CiS significantly improve the Test Hardware PDN
  - Moving caps close to the DUT reduces the total loop inductance
- We need to collaborate with the supply base in addressing these growing Power Integrity challenges

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Acknowledgements

- Scott Mokler
- Moti Miles
- Danny Bronstein
- Michael Hill

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  - (503)613-8056

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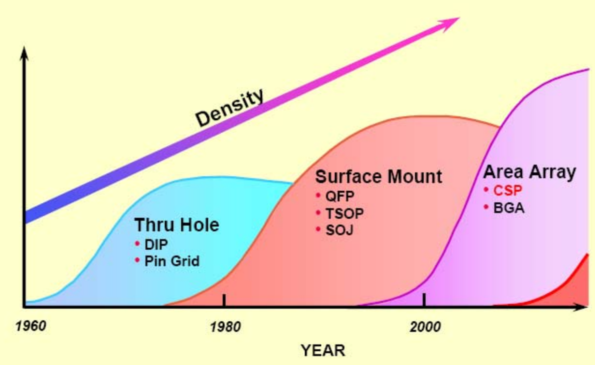
Moore or Less:

Effects of Higher Currents on Socket Life

Authored and Presented by:
Kevin DeFord
Interconnect Devices Inc.

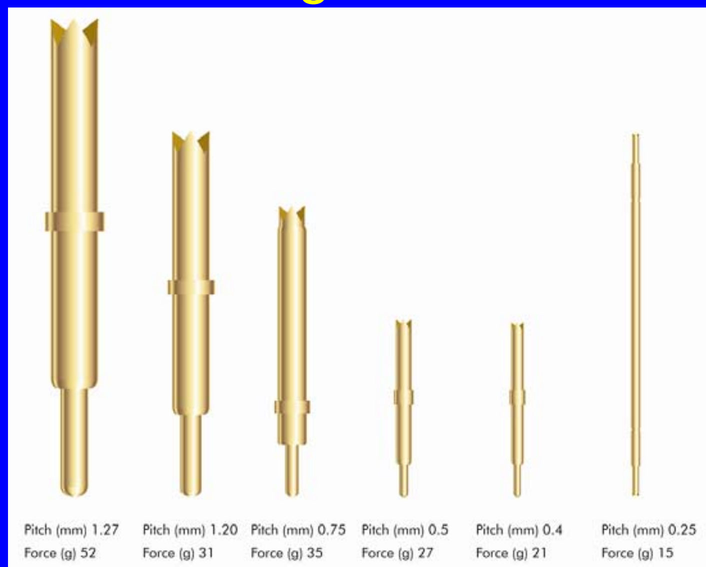
2009 BiTS Workshop
March 8 - 11, 2009

Package Family vs. Density[1]



1. Illustration provided by T. Di Stefano, Centipede Systems

Scaling of Probes



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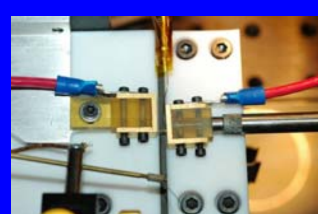
Conventional High Current Characterization Method



- Gold to gold contact
- Test at room temperature
- Increment current until limit is reached

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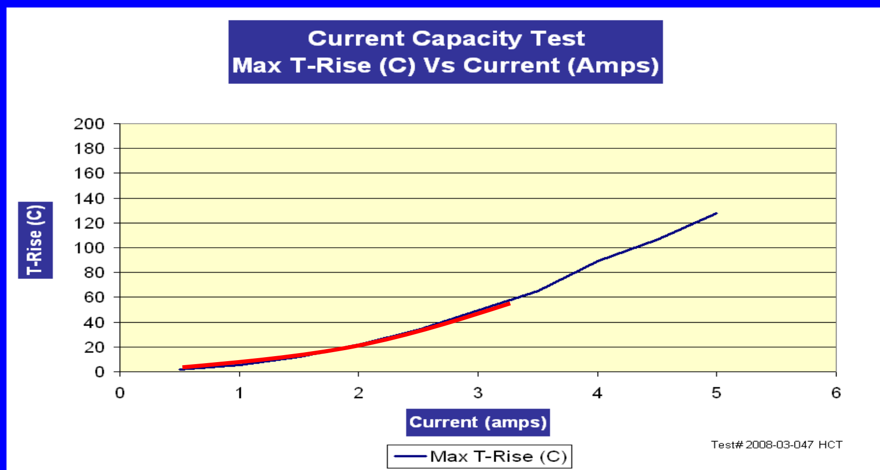
High Current Test (Free Air)



Spring Material:	Music Wire	Stainless Steel	BeCu
Max Op Temp:	85°C	180°C	120°C

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- Pros
  - Reliable method (IEC 512-3)
  - Repeatable
  - Free from artifacts
  - Low/predictable cost
- Cons
  - Doesn’t simulate contact degradation
  - Meaningful maintenance cycles

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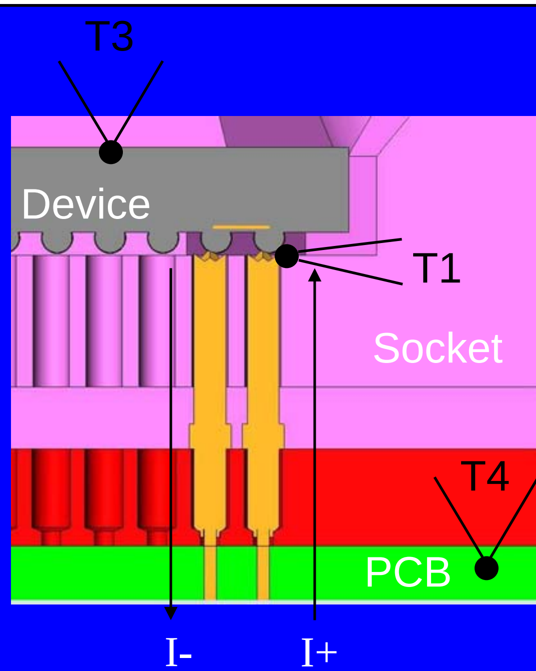
- Daisy chain devices SAC-105
- Force Current thru pairs
- Contact Interface is observed



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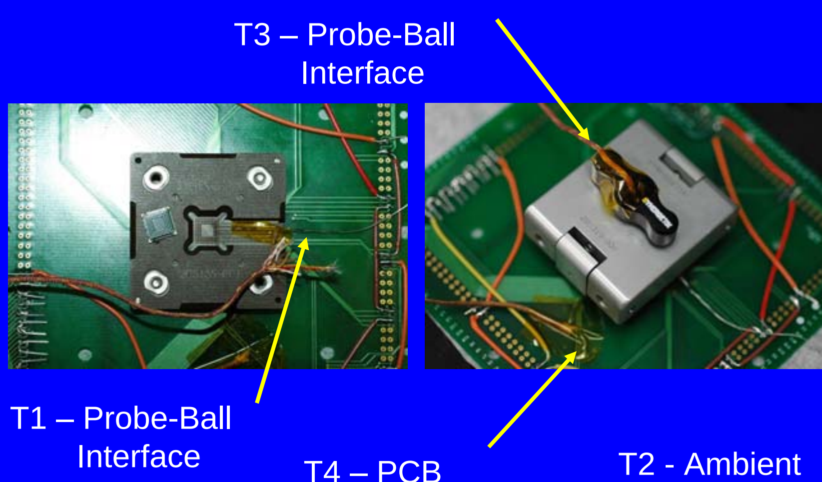
Socket Current Test Set up



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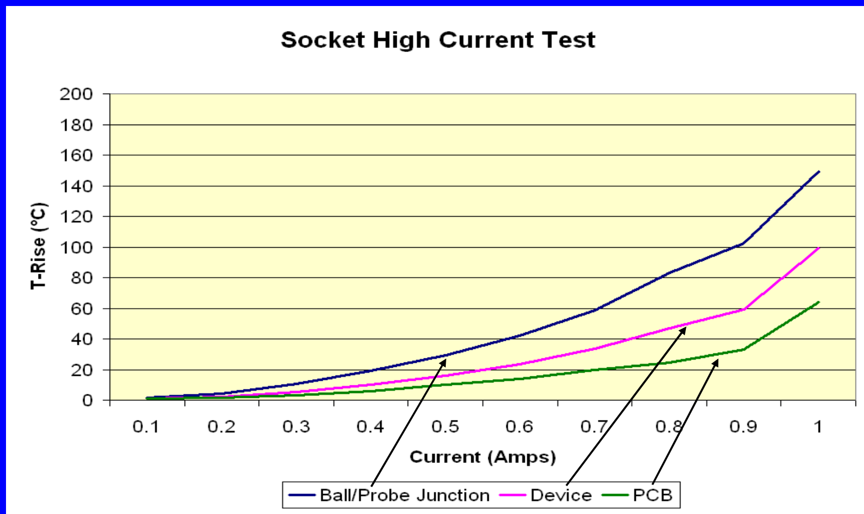
Temperature Rise vs. Current



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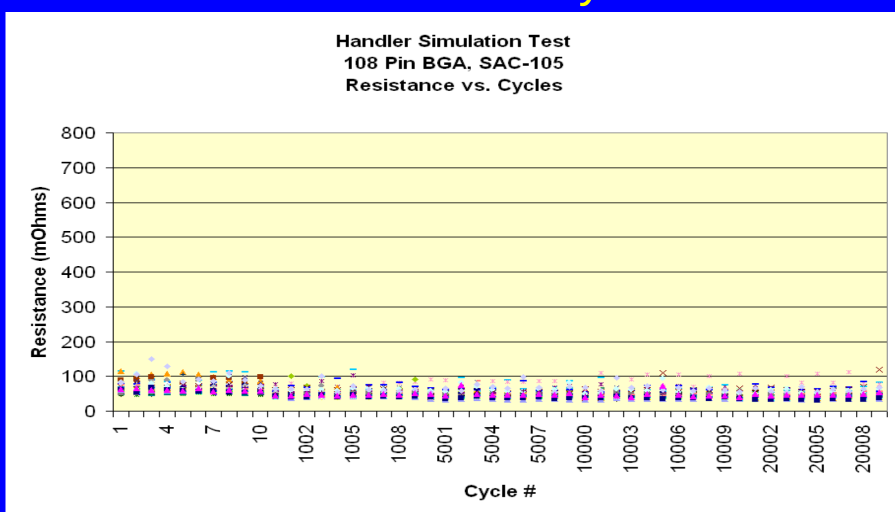
Handler Simulation Test (25mA) Resistance vs. Cycles



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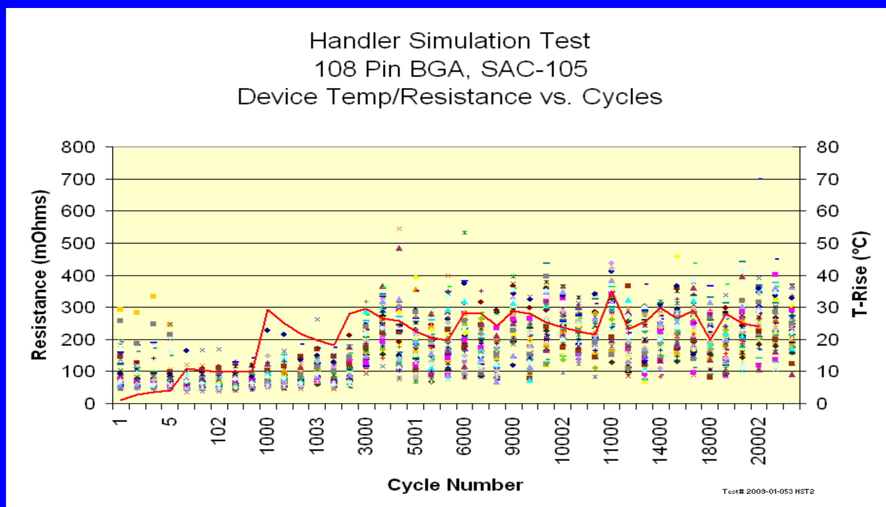
Handler Simulation Test (300mA)
Device Temp/Resistance vs. Cycles



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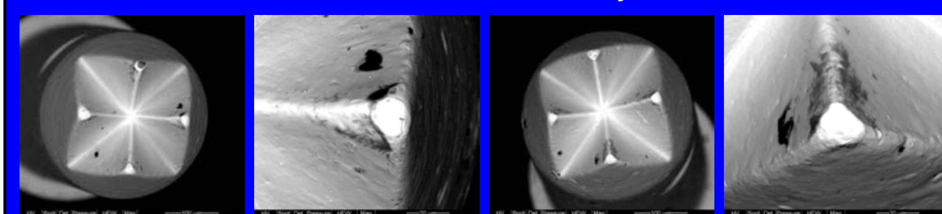
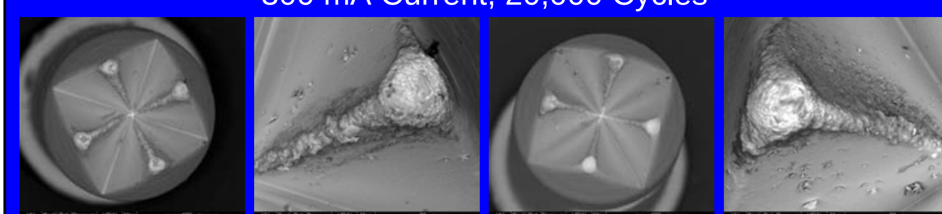
SEM photos of SAC Accumulation

25 mA Current, 20,000 Cycles



300 mA Current, 20,000 Cycles



Photos of 0,5 mm BGA probe tips after 20,000 contacts against SAC-105

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Electro-migration

Definition – enhanced movement of atoms in the direction of electron flow[2]

- A driving force is necessary
- Dependant on the Direction of Electron
- Voiding will be induced at the Cathode site
- Metal build up will occur at the Anode site

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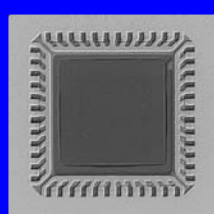
Electro-migration Experiment



- 48 Pin QFN Daisy Chain device (Sn)
- 120° Tip Used
- 500 mA Current
- Current in Series thru pairs
- 20K Cycle on HST

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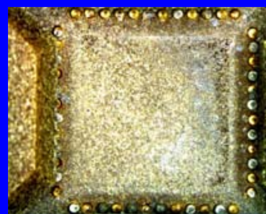
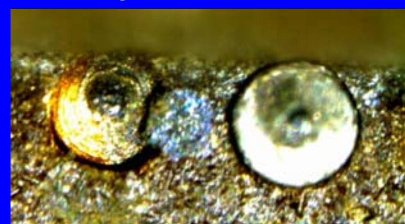
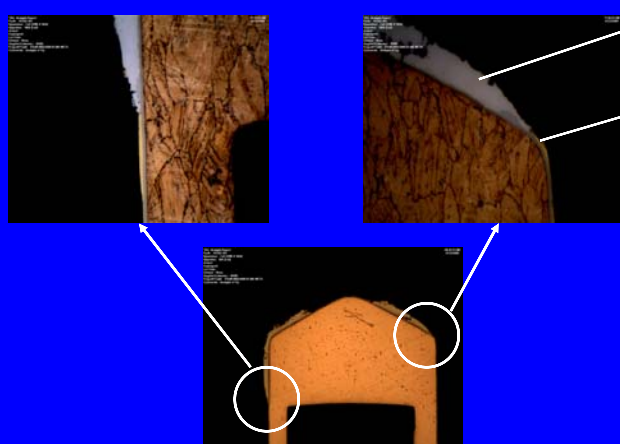


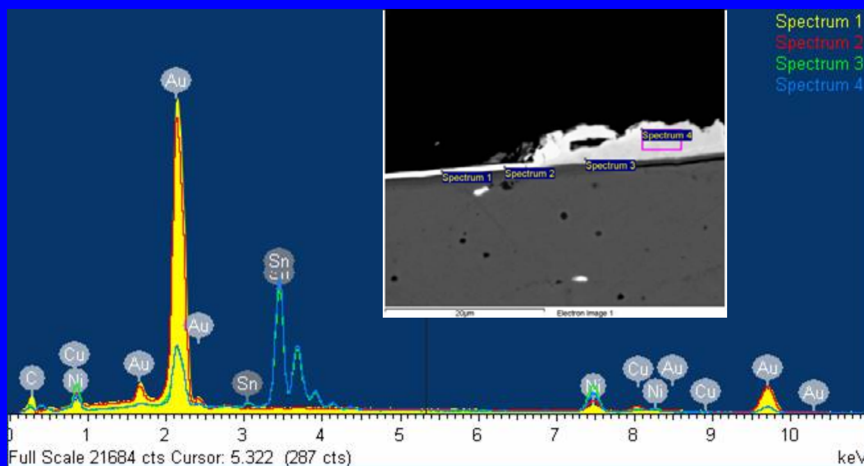


15,000 Current Cycles, 500 mA, 5 second dwell

Cross Section Analysis (Cathode)



Spectrum Analysis (Cathode)



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Summary

- Delta between IEC test method and socket
- Delta between device ball and cap
- Low/consistent R at low current
- Higher/Variable R at higher current
- Accelerates SAC transfer to tips
- Electro-migration occurs at the Anode site

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References

- **<u>Illustration,</u> T.Di Stefano, Centipede Systems**
- **<u>Electro-migration in solder interconnects</u>,** Riet Labie**,** www.europeanleadfee.net,
- ITRS 2008 Update, Semi Road map

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Design Considerations in Socketing High Power Devices

Jec Sangalang
Yamaichi Electronics

Mike Noel
Freescale Semiconductor

2009 BiTS Workshop
March 8 - 11, 2009

Overview

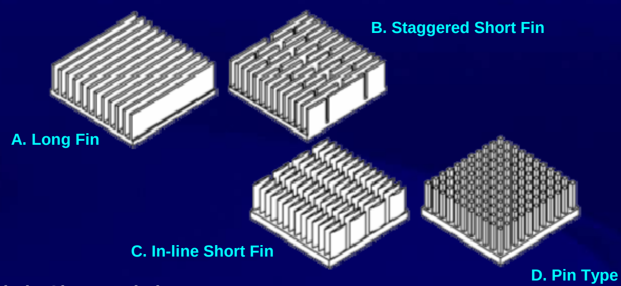
High power devices have special socket considerations

- Heat sink designs are critical
- Thermal interface resistance must be controlled
- High contact counts and heat sink force must be controlled
- Package design variations must be accounted for
- Costs must be controlled

Heat Sink Design

Fin Type

Heat sink fin type should be determined according to specific application



General Fin Characteristics

Type	Best Applicable Airflow Direction	Resulting Airflow	Manufacturing Method
A. Long Fin	Parallel	Laminar	Extrusion
B. Staggered Short Fin	Parallel	Laminar	Forging or Casting
C. In-line Short Fin	Top	Omnidirectional	
D. Pin type	Top	Omnidirectional	

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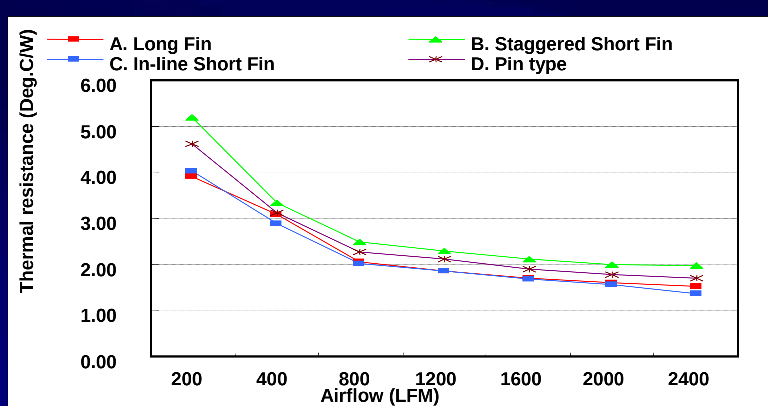
Heat Sink Design

Correlation between fin type and thermal resistance

(Assuming the same size, thickness and pitch)



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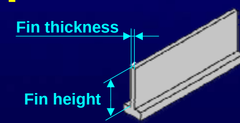
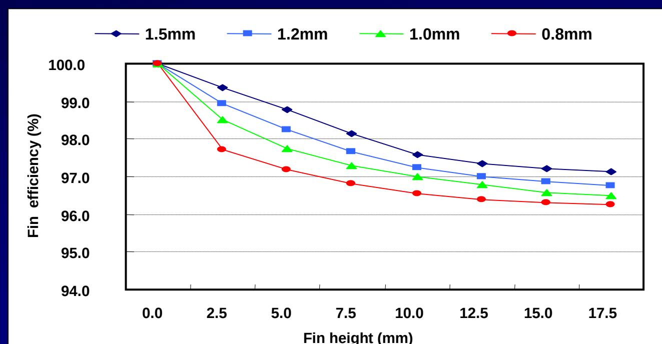
Heat Sink Design

Fin thickness



- Fin thickness affects fin efficiency by 1-2%
- Reduced fin thickness, increased fin density
- Increased fin density, increased thermal dissipation area

Correlation between Fin thickness and Thermal resistance



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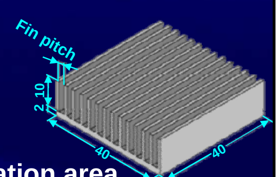
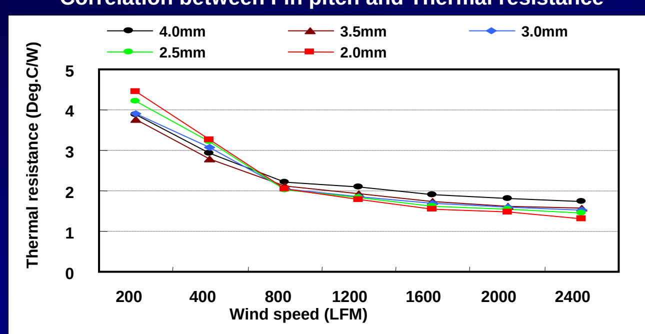
Heat Sink Design

Fin pitch



- Fin pitch has less effect under higher airflow velocity (800 - 2000LFM)
- Reduced fin pitch, increased fin density
- Increased fin density, increased thermal dissipation area

Correlation between Fin pitch and Thermal resistance



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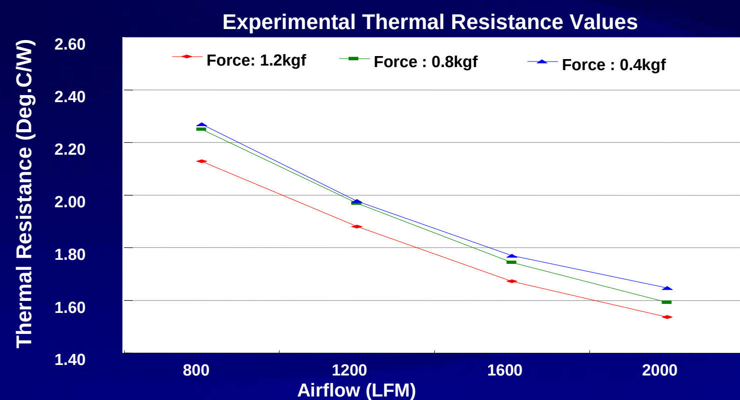
Thermal Interface

Pressure / Force Settings

- Thermal resistance improvement above 1kgf heat sink force.
- Consider the heat sink pressure for various thermal interfaces
  - Consider lidded and bare die package variations
  - Consider the force the package can take



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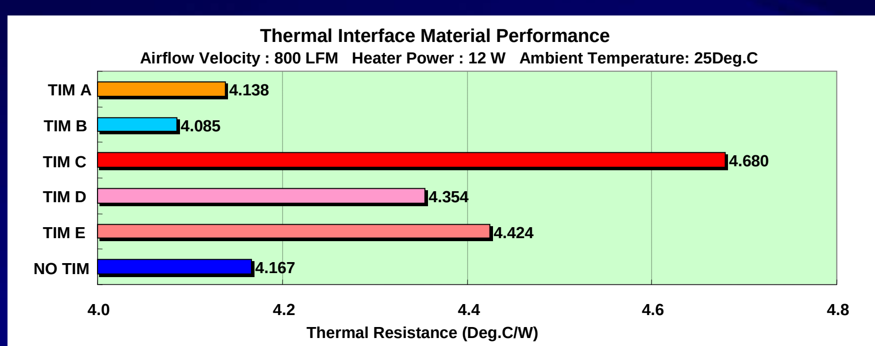
Thermal Interface

With or Without Thermal Interface Material?

- TIM is used improve interface between two conforming surfaces

- TIM introduces other socketing issues
  - increased thermal resistance, residue on device, maintenance



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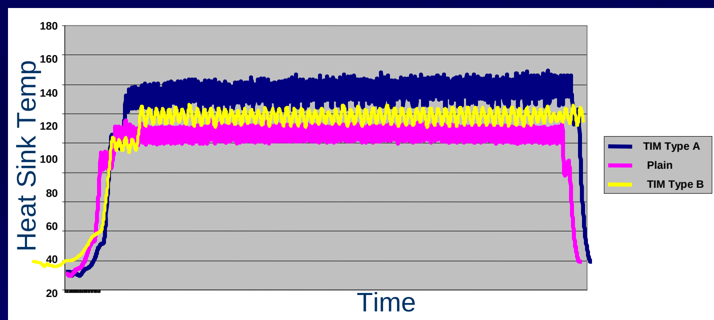
Thermal Interface

TIM Test Results



- TIM Material can have a significant impact on the overall thermal profile of the system
- Devices controlled to diode on device, measured heat sink varies based on TIM

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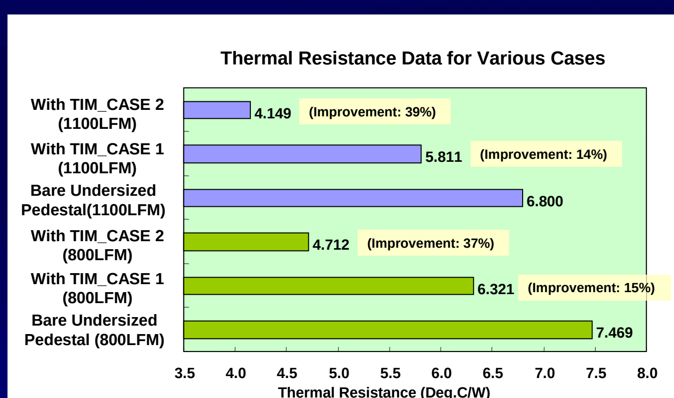
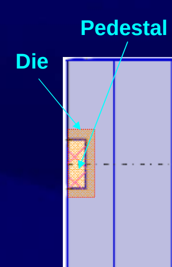
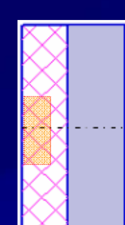
Thermal Interface

With or Without Thermal Interface Material?





CASE 1: Undersized Pedestal



CASE 2: Oversized Pedestal

Oversized heat sink pedestal with TIM shows the most improvement in thermal performance, but . . .

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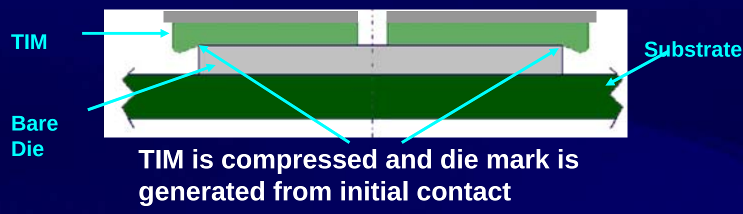
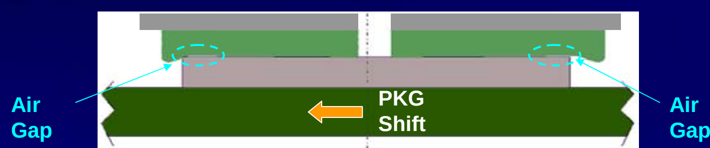
Thermal Interface

TIM on Oversized Heat Sink Pedestal



TIM is compressed and die mark is generated from initial contact



When PKG shifts, TIM is compressed outside the original die mark which causes air gap between die and HS resulting to reduced interface area.

More marks are generated as PKG's shift in different directions.

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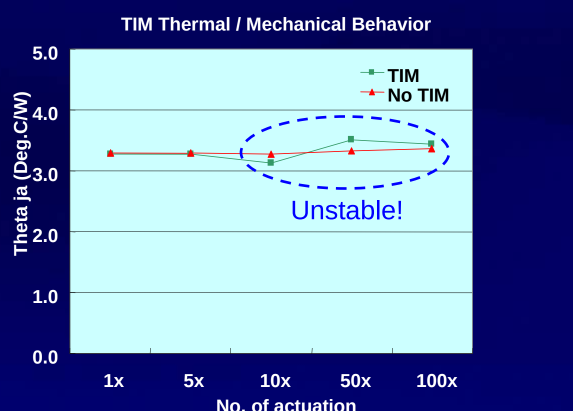
Thermal Interface

TIM on Oversized Heat Sink Pedestal



TIM Initial Condition

TIM after 100x actuations

- Thermal performance becomes unstable after several actuations
  - inconsistent thermal contact with die
- Bare sink interface with good surface finish is more stable

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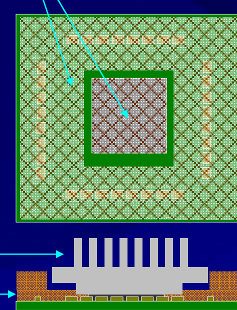
Package

Packages Play a Big Role in Socket Design

Ideally we want:

- **Maximum coverage**
  - Force delivery
  - Thermal performance
  - Package variations
- **Minimum risk**
  - Maintain package integrity



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Package

Bare Die Package

– Potential for good thermal performance, with trade offs

- **Force**
  - **Increase**
    - » Increased risk of die damage, Silicon is brittle
  - **Reduce**
    - » Reduced thermal performance
- **Coverage**
  - Increase
    - » Higher possibility of die cracking / damage
    - » Better thermal performance
  - Reduce
    - » Reduced risk of die damage
    - » Reduced thermal performance

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Package

Bare Die Package (cont)

- Thermal interface
  - **TIM**
    - Generally requires high force
    - Can introduce other interface issues
    - Need to be undersized, limited coverage
  - **Bare HS Pedestal**
    - Must have good surface finish
    - Oversized preferred for maximum die coverage
- Overall package force
  - **Force Delivery**
    - Balance force on die and substrate
    - True vertical actuation required
- Contacting
  - Contacting requirements must be met

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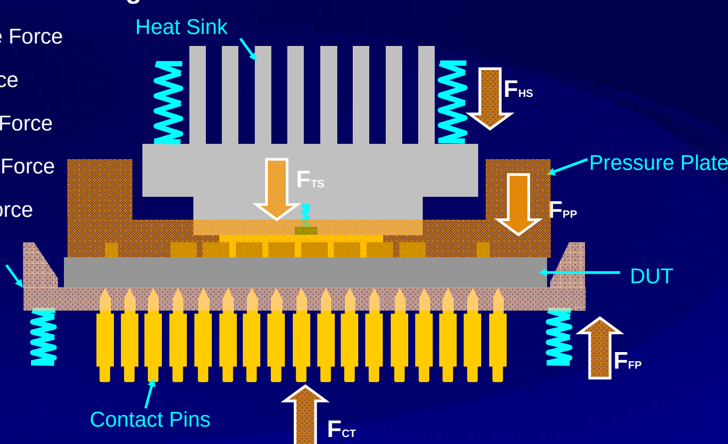
Overall Package Actuation Force

Force on die and substrate must be balanced to prevent package warping and potential die damage.

SFy = 0
$F_{PP} + F_{HS} + F_{TS} - F_{FP} - F_{CT} = 0$

F_{PP} = Pressure plate Force
F_{HS} = Heat Sink Force
F_{TS} = Temp Sensor Force
F_{FP} = Floating Plate Force
F_{CT} = Contact pin Force



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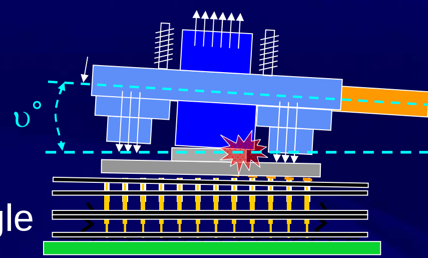
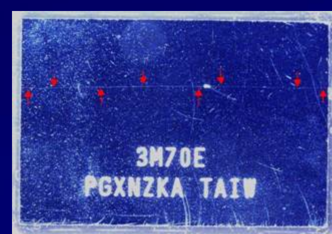
Risk of Die Damage

- Traditional lidded sockets are hinged
- The heat sink initially contacts the die at an angle
- Uneven actuation force can cause package cracking or bump failures





Damaged die

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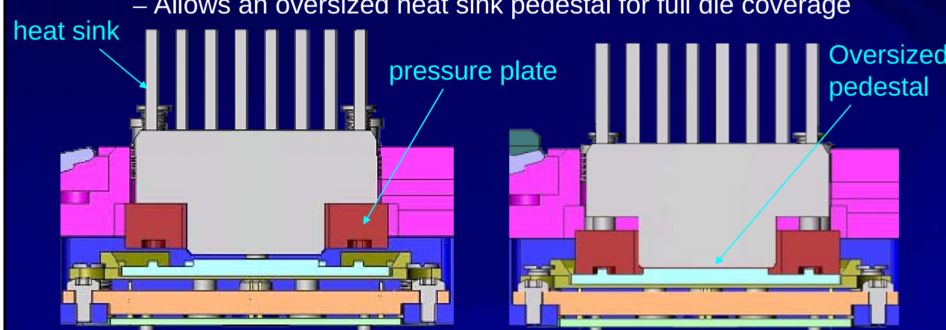
Concept to Address Risk of Die Damage

- **Separate independent force on substrate and die**
  - Heat sink for thermal interface with die
  - Pressure plate for substrate
- **Vertical actuation motion for heat sink and pressure plate**
  - Heat sink interface prevents damage on die while maintaining good thermal contact
  - Allows an oversized heat sink pedestal for full die coverage



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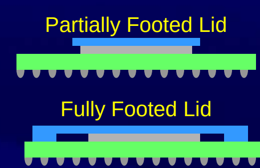
Package Considerations

Lidded Package (full / partial)



– Force Delivery
  - Less sensitive to die cracking
  - Separate or integrated heat sink / pressure plate for full lids
  - Force must be balanced with substrate for partial lids
  - Sufficient force to achieve good thermal contact
  - Package thickness variation can increase

– Thermal
  - Thermal performance generally drops
  - Heat spreader can achieve some thermal performance, but packaging costs go up
  - With plastic lid thermal performance suffers

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Contact Pin Technology

Through Hole

- Tweezer / Pinch Style
  - \+ Plane of actuation is lateral, vertical load on DUT is only for thermal interface
  - \+ Usually stamped, low per pin cost
  - – Pin count limitation, cannot sustain very high pin counts
  - – Current carrying capability is limited
  - – Individual pins are not field replaceable
  - – Socket replacement is difficult and unreliable

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Contact Pin Technology

Through Hole

- Buckling Beam
  - – Plane of actuation is vertical, load on DUT is for contacting pins and thermal interface
  - \+ Usually stamped or etched, low per pin cost
  - \+ Can sustain very high pin counts
  - – Current carrying capability is limited
  - – Individual pins are not field replaceable
  - – Socket replacement is difficult and unreliable

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Contact Pin Technology

Compression Mount

- Buckling Beam
  - – Plane of actuation is vertical, load on DUT is for contacting pins and thermal interface
  - \+ Usually stamped or etched, low per pin cost
  - \+ Can sustain very high pin counts
  - – Current carrying capability is limited
  - – Individual pins are not field replaceable
  - \+ Allows easy socket replacement

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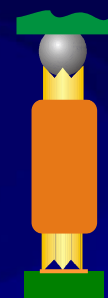
Contact Pin Technology

Compression Mount

- Spring Probe
  – Plane of actuation is vertical, load on DUT is for contacting pins and thermal interface
  – Multiple components, higher per pin cost
  + Can sustain very high pin counts
  + Current carrying capability is better
  + Individual pins are field replaceable
  + Allows easy socket replacement



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Cost Considerations

Wish list for BI Hardware Cost of Ownership

- Maximize socket re-use
- Maximize component re-use
- Ensure easy field maintenance
- Minimize initial investments
- Ensure long life of sockets

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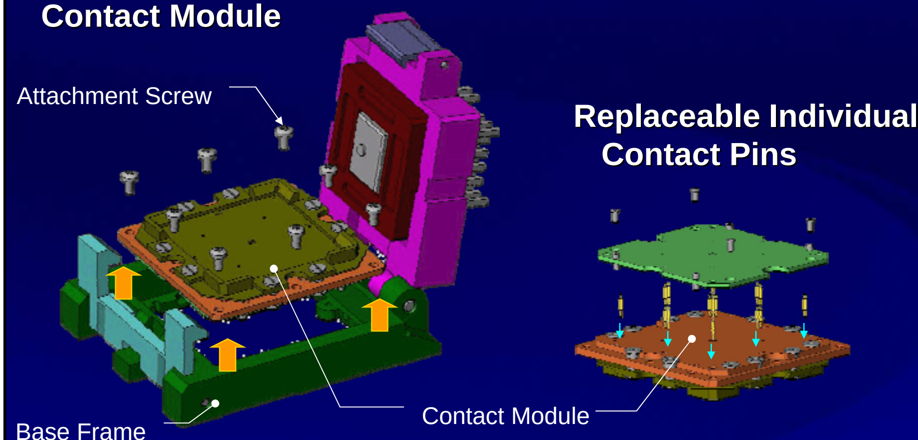
Cost Considerations

Concepts to address BI Hardware user's wish list

- ☑ Socket Re-use
  - Modular design, minimizes custom components
- ☑ Component re-use
  - Large portion of components are generic across various socket configurations
- ☑ Field Maintenance
  - Contact module is reconfigurable, individual pins are replaceable, heat sink assy, sensors and so-on
- ☑ Initial costs
  - Maximize sub assy design to achieve maximum benefit from volume of shared components, maximize use of molded components.
- ☑ Long Life
  - Utilize robust components and design

Modular Approach in Design

Replaceable / Reconfigurable Contact Module



Contact Module can be easily replaced in the field by unscrewing fasteners. Individual contact pins, Temp Sensor and Heater are also field replaceable.

Summary

Design Considerations in Socketing High Power Devices:

- Heat Sink design should be determined according to specific application
- TIM's are not stable with high actuation count applications, bare pedestal with good surface finish is more stable
- Vertical actuation motion is most suitable for bare die allowing oversized HS pedestal for maximum die coverage

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Summary

Design considerations in Socketing High Power Devices (cont)

–Separate force delivery on die and substrate is required to balance forces on the device

–Compression mount spring probe is most applicable in terms of electrical and high pin count requirements

–Manageable BI Hardware Cost of Ownership is achievable with a flexible, modular approach to socket design

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Acknowledgment

Bryan Heenan, Freescale Semiconductor

Katsumi Suzuki, Yamaichi Electronics Co., Ltd.

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