BiTS Burn-in & Test Socket Workshop 2009 Keynote Address

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IC PACKAGING: GLOBAL TRENDS, TECHNOLOGIES AND NEXT GENERATION 3D SOLUTIONS

by

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ABSTRACT

IC packaging solutions have been evolving in many ways that were forecast, and in some ways not predicted by any analysts. This presentation will look at the recent trends of IC packages in terms of package type, pitch, and integration for multi-chip and 3D solutions. In preparing for the next decade of innovations, this brief synopsis will provide a forecast for current advanced packages, and a look into future developments in 3D and package integration that may have an impact on overall test strategies and challenges going forward.

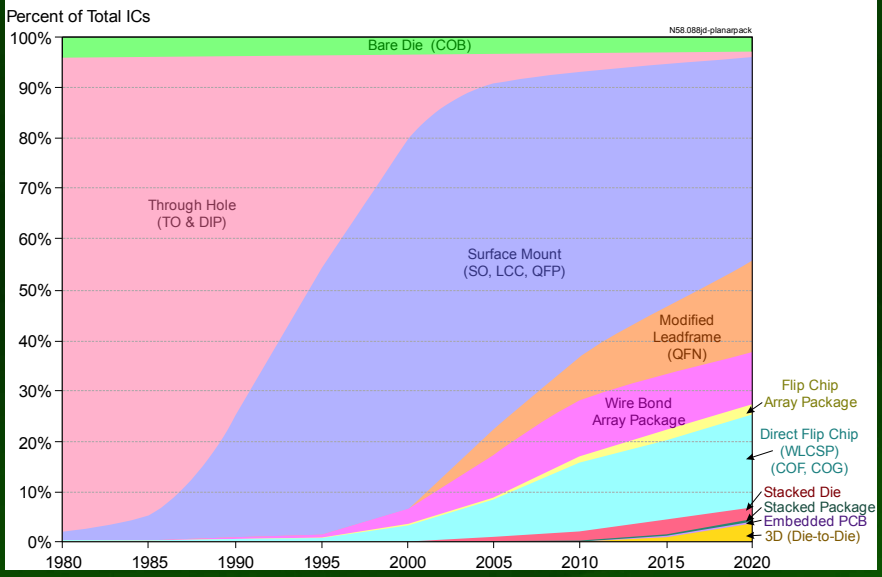
IC PACKAGING:
Global Trends, Technologies and Next Generation 3D Solutions

Brandon Prior
Prismark Partners

BiTS Workshop
March 2009

IC PACKAGE TRENDS:
Where Have We Been and Where Are We Going?

PACKAGING INTERCONNECT TRENDS



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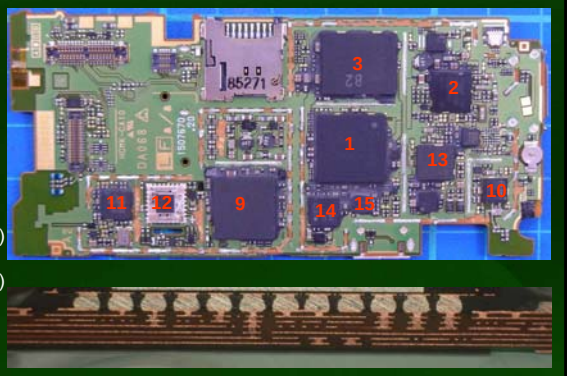
SHARP 923SH: BOARD AND MAIN COMPONENTS

108.4/387bp

- 10.5 x 4.5cm Main Board
  - Eight-layer ALIVH, 650µm thick
  - 60µm L/S, 110µm stacked vias
  - PCB price: ~ $6.50
- Major Components On One Side
  1. EMP DB3150 digital baseband: 12 x 12mm, 344 balls at 0.5mm pitch (4 rows)
  2. EMP AB3000 analog baseband: 7 x7 x0.9mm, 143 balls at 0.5mm pitch (full array)
  3. Spansion memory: 11 x 13mm, 137 balls at 0.8mm pitch (full array)
  4.-8. 2 Transceivers, 2 PA and switch on board backside
  9. Toshiba mobile turbo application process: 11 x 11 x 1.2mm, 358 balls at 0.5mm pitch (3 die, F2F and wire bond)
  10. ST Bluetooth: 4.7 x 4.7mm, 48 balls at 0.65mm pitch (full array)
  11. Broadcom GPS: 5 x 5mm, 81 balls at 0.5mm pitch (full array)
  12. Sharp one-seg TV module



Photos source: Prismark/Binghamton University

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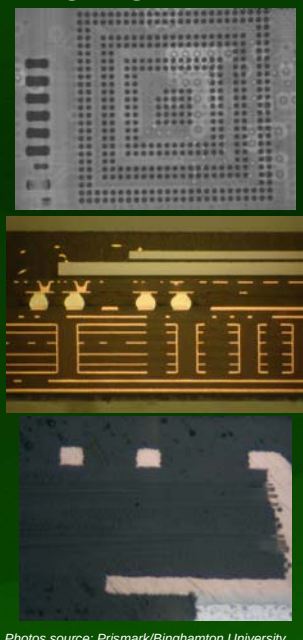
FINE PITCH CSP: Finally at Sub-0.5mm!

QUALCOMM MSM6260 NSP PACKAGE

38.6/193mvc

- Qualcomm Baseband Processor
  - HSDPA and EDGE phones
  - Multimedia/applications processing
  - Two stacked die: digital and analog
  - 11 x 11 x 0.85mm CSP, 432 balls
  - Nanoscale package (NSP): 0.4mm pitch
- 11 x 11mm Two-Layer PCB Carrier
  - 90µm glass-reinforced dielectric
  - 115µm diameter laser vias
  - 22µm copper layers
  - Min. line width 20µm
  - Min. space 45µm
  - 38µm soldermask top
  - 48µm soldermask bottom
  - Total thickness: 193µm
- Total Package Thickness: 860µm
  - Mold cap over carrier: 533µm
  - Mold cap over top die: 213µm
  - Mold cap over wire: 150µm
  - Collapsed ball height: 135µm

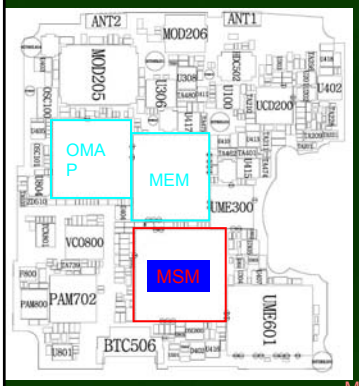


Photos source: Prismark/Binghamton University

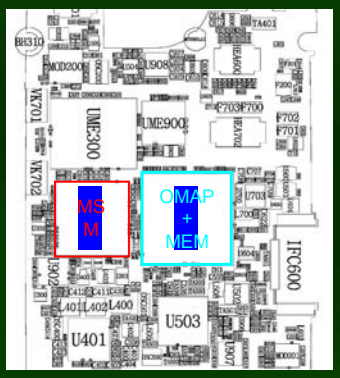
CSP, NSP, PoP

18/6.193mvc

SAMSUNG i600



SAMSUNG i550



MSM BASEBAND PROCESSOR

409-Ball CSP, 0.5mm Pitch
14mm x 14mm = 196mm²

→ 38% Smaller →

432-Ball NSP, 0.4mm Pitch
11mm x 11mm = 121mm²

OMAP APPLICATIONS PROCESSOR PLUS MEMORY

289-Ball CSP, 0.5mm Pitch
12mm x 12mm = 144mm²

164-Ball CSP, 0.6mm Pitch
13mm x 10mm = 130mm²

→ 28% Smaller →

447-Ball PoP, 0.5mm Pitch
14mm x 14mm = 196mm²

Source: Qualcomm

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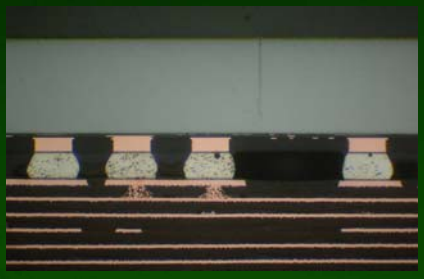
PANASONIC HEDGE TRANSCEIVER IN WLCSP

18.085bp

- Found in Panasonic P905i Mobile Phone
- 5.9 x 5.9mm Die as WLCSP
  - 500µm thick
  - 185 balls at 0.4mm pitch
  - 80µm copper post height
- 2 Metal Layer Redistribution
  - 6 – 8µm dielectric thickness
  - 5.5µm metal thickness
  - 30µm line width



Photos source: Prismark/Binghamton University

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58.1/085skc

RECENT WL-CSP APPLICATION EXAMPLES

Mobile Phone	Total Wafer CSP	WL-CSP Applications	Comments
Nokia N90	8	ESD/EMI, analog/power	6 – 25 I/O, largest die 3 x 4mm
Panasonic P901i TV	7	ESD/EMI, analog/power, other?	Up to 5mm die with 119 I/O at 0.4mm pitch
LG SB120	1	Power	5.5mm, 72 I/O at 0.5mm pitch
Apple iPhone	4	ESD/EMI, Bluetooth, WLAN	Up to 4.7mm die with 69 I/O at 0.4mm pitch
Panasonic P905i	6	Transceiver, Bluetooth, power, TV tuner (two chips),GPS	5 die use copper post tech, up to 185 I/O at 0.4mm pitch
Nokia 6220 Classic	7	ESD/EMI, power, other?	Up to 5mm die
Nokia N95	8	EMI/ESD, analog, Bluetooth, FM Radio	Up to 4mm die with 47 I/O at 0.5mm pitch

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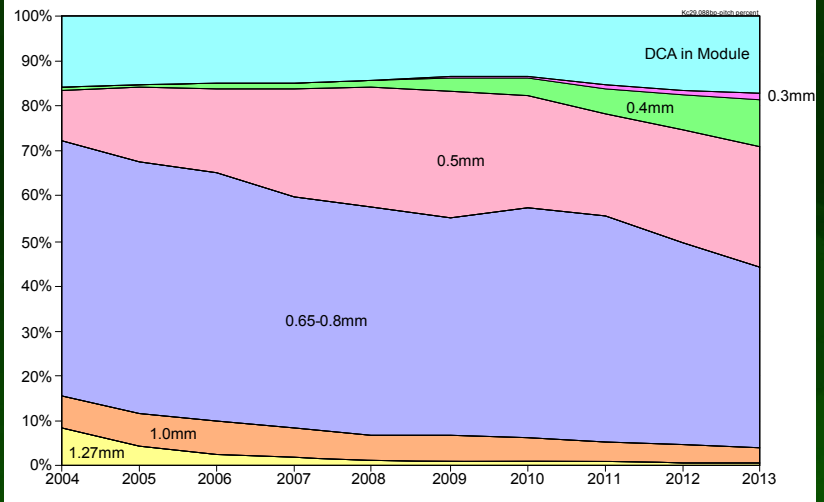
ARRAY PACKAGE PITCH TRENDS (BGA, CSP, PGA, LGA, WL-CSP)
(Excludes Small Die DCA, Display Drivers, and RF Modules)



Note: Sub 0.5mm was 2% of overall volume in 2008. By 2013 this will increase to 12% or 5.7Bn units

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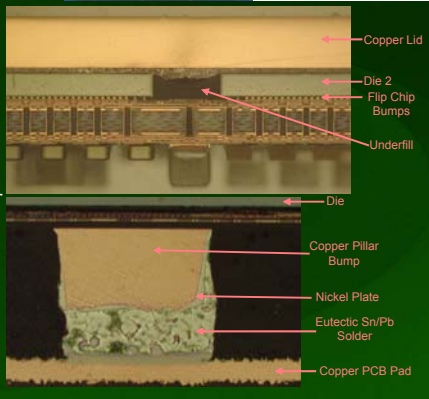
HIGH LEADCOUNT BGA: Revival of MCM?

INTEL CORE™ 2 QUAD MPU

77.12/210bp

- First-generation "Quad Core" uses two die in one package
  - 65nm low-k, 10.9mm x 13mm x 0.79mm die (x2)
  - ~ 13,700 copper/solder bumps in staggered combination (180µm pitch/220µm pitch) to yield 145µm minimum pitch
  - 86µm diameter Cu Pillar with ENIG, Die standoff is 70µm
  - Capillary underfill (Shin-Etsu)
- One-piece stamped nickel plated copper lid 34mm x 34mm
  - 1.6mm over die, 2.4mm total thickness
  - 170µm thick indium TIM
- 5+ 4+ 5 microvia substrate 37.5 x 37.5 x 1.4mm
  - 775 LGA substrate
  - Minimum L/S 20µm – 25µm (measured), 60µm via diameter (measured)
  - 25µm dielectric thickness, copper thickness 12µm -15µm
  - Core layers: 100µm -110µm LS, 200µm via diameter

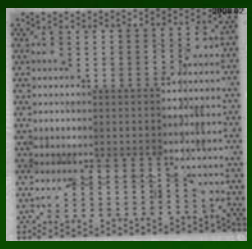


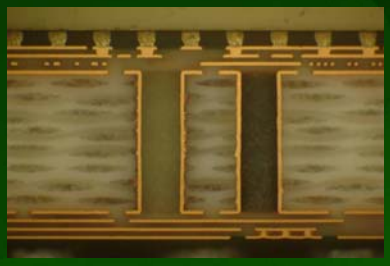
Photos Source: Prismark/Binghamton U

48.210bp

INTEL P35 NORTHBRIDGE (DP35DP Motherboard)

- 1226 FCBGA Package
  - 34mm x 34mm
  - "Balls anywhere" with 0.8mm minimum pitch
- 10.4mm x 10.4mm x 0.79mm Die
  - Approximately 3,000 bumps at 184µm pitch
  - High lead bumps with eutectic solder on pad
- 3 + 2 + 3 Substrate
  - 800µm core, 280µm PTH
  - Build-up layers have 75µm vias and ~ 25µm L/S
- Twenty-one die side capacitors (0603): 0.2-2µF each
- Heatsink and phase change pad used for thermal design power of 16W





Photos source: Prismark/Binghamton University

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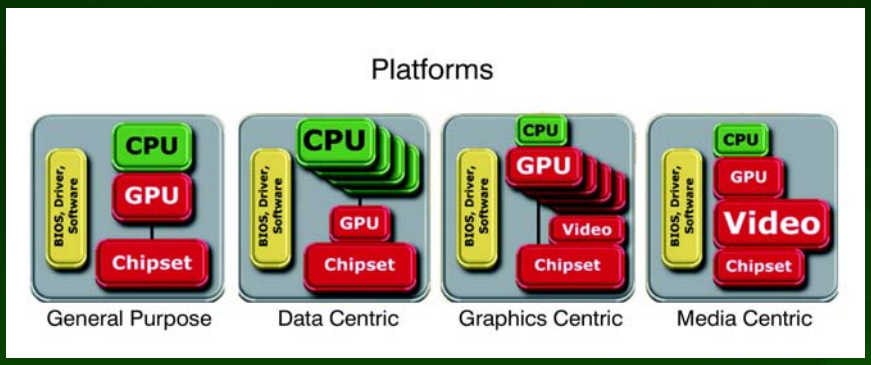
17.12/210bp

AMD/ATI FUSION ROADMAP CONCEPT



Source: AMD/ATI

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68./088bp

CISCO FLIP CHIP AND MEMORY PACKAGE (FC AMP)

- 52.5mm X 52.5mm maximum package size
- Minimum of four controlled impedance signal layers and four power rails
- Large ASIC die is flip chip mounted
- Four SRAM or DRAM die in rigid based CSPs up to 13mm x 18mm
- Die and packages are underfilled
- AlSiC and copper lids evaluated

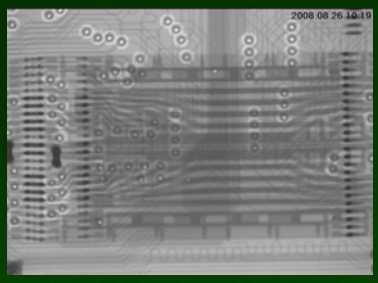
Source: Cisco

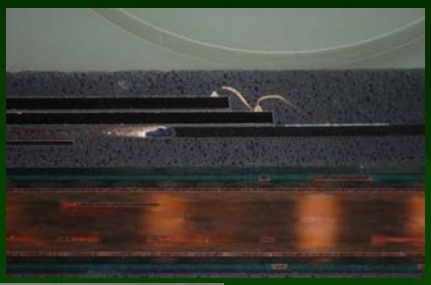
STACKED PACKAGES: Works Great for Memory but…

STACKED TSOP PACKAGES IN ASUS SSD (2)

98.1/161bp

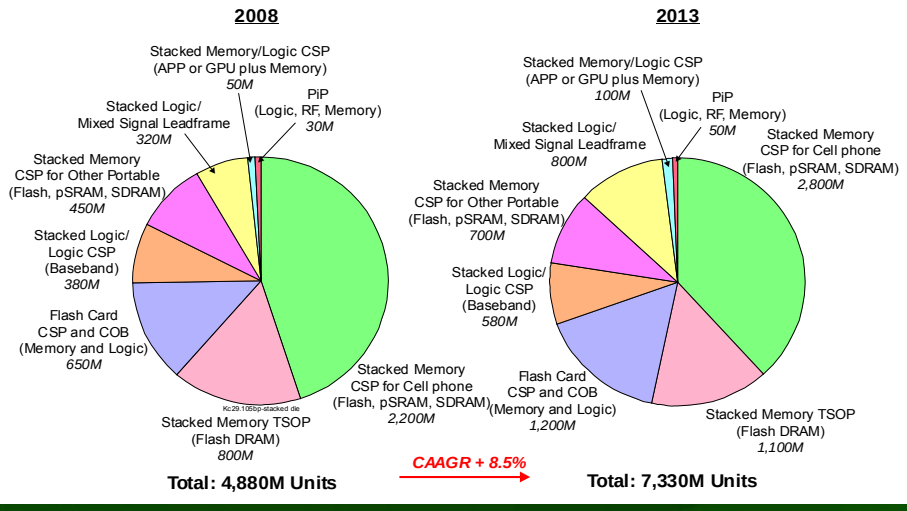
- Samsung 16Gbit MLC NAND in TSOP 48 – 2 Die Stack
  - TSOP measures 12mm x 18mm x 1mm
  - Some leads not electrically connected to board (35 connected)
  - Each 8Gbit NAND die measures 11mm x 9mm and are 125µm thick
  - Die stacked on top of one another and offset for staircase wire bonding
  - Both die use preapplied die attach material 20µm thick





Photos source: Prismark/Binghamton University

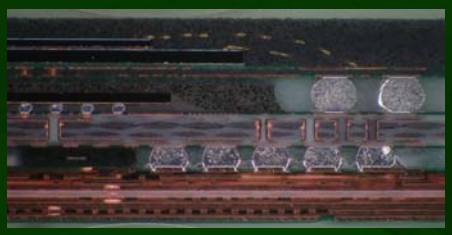
STACKED DIE-IN-PACKAGE

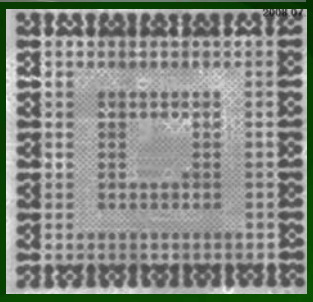


NEC BASEBAND/APPLICATIONS + SAMSUNG MEMORY PoP

108.1/105bp

- Bottom package: single die baseband/ application processor – NEC Medity M2
  - 529 balls at 0.5mm pitch (five rows)
  - ~ 1100 bumps (SnAg) at 225µm pitch 70µm standoff height
  - 8.5 x 8.5mm die is 100µm thick
  - Die is underfilled and overmolded
  - 1+ 2+ 1 substrate with 25µm L/S and 75µm vias; 360µm thick
- Top package: Samsung two-die memory stack (SDRAM, One NAND)
  - 152 balls at 0.65mm pitch
  - Top die 70µm thick, bottom die 130µm
  - Preapplied die attach 15 – 20µm thick
  - Two-layer substrate is 130µm
- Total mounted height of PoP 1.55mm, and is underfilled





Photos source: Prismark/Binghamton University

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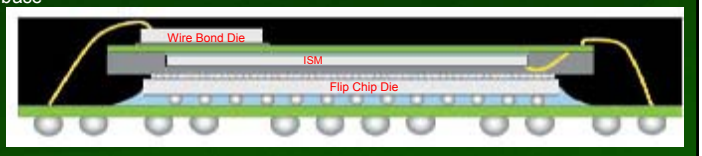
QUALCOMM MSM7200 fcPiP PACKAGE

48.6/193mvc

- 15 x 15 x 1.4mm fcPiP Package
  - 543 balls, 0.5mm pitch
  - Includes three die
    - Digital baseband
    - Analog baseband
    - Memory
  - Underfilled
  - Packaged by STATS ChipPAC
- fcPiP Package Concept
  - FC package base
    - Digital baseband
  - Internal stacked module
    - Memory in LGA package
    - Placed upside down in flip chip die
  - Bare die
    - Analog baseband placed on ISM
  - Wire bonding of ISM and bare die
    - To FC package base
    - Overmold



Source: STATSChipPAC

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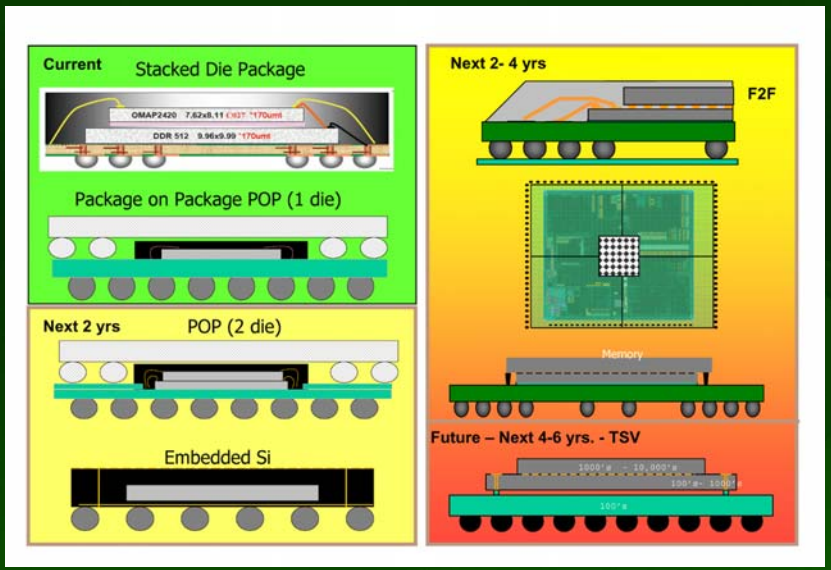
NEXT GENERATION 3D: Which Will Prevail?

87.1/105BP

TI WIRELESS PACKAGE ROADMAP

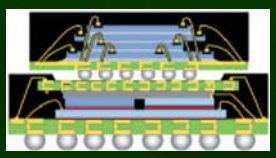


Source: TI

48.1/105bp

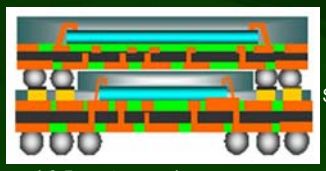
SECOND-GENERATION PoP SOLUTIONS

- STATS ChipPAC Fan in PoP (Fi-PoP)
  - Substrate mounted within bottom package
  - Allows for smaller x-y dimensions



Source: STATSChipPAC

- ASE Mold Array PoP (MAP PoP)
  - Allows for 0.5mm pitch top package
  - Mold standardization (faster time to market)
  - Less warpage, higher yield



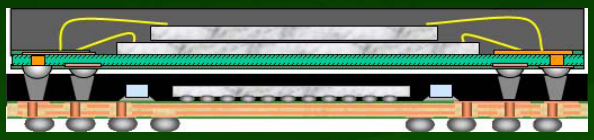
Source: ASE

- As package I/O increase, need for 0.4mm bottom and 0.5mm top package emerge
  - Baseband/application processing seeing pincounts of 600 and higher in 2008; within two years may see I/O approach 1,000
  - To keep 12mm – 14mm body size, 0.4mm must be used
- JEDEC task group setting 0.4mm top package standards to handle 200 – 250 I/O for DDR2 memory

29.1/105bp

AMKOR PoP WITH THROUGH MOLD VIAS (TMV)

- Uses standard FBGA package with wire bond, flip chip, or stacked die
  - After molding, blind via created through mold compound to expose bond pads on package substrate
  - Vias filled with conductive material to help attach top solder balls
- Two key advantages
  - Eliminates warpage problems as entire package is molded
  - Enables reduced pitch on top package
- Test vehicle uses 14 x 14mm size
  - 620 balls at 0.4mm pitch bottom package
  - 200 balls in two rows at 0.5mm pitch top package
- Working with two key players in mobile phone baseband



Source: Amkor

108.1/085bp

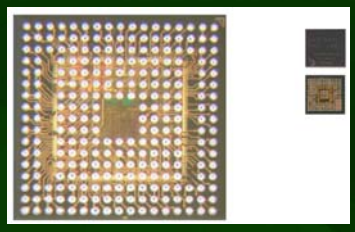
FAN-OUT WAFER-CSP TECHNOLOGY

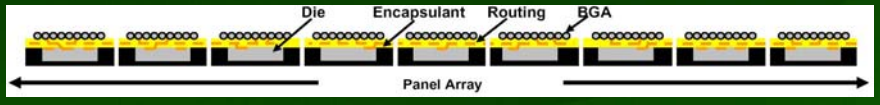
- Basic process involves dicing wafer and creating reconfigured wafer or panel with room for fan-out RDL layers
- Significant interest and development at many IDMs and subcontract package assemblers
  - Freescale, NXP, ST, Infineon, others
  - ASE, STATS ChipPAC, Amkor, etc.
- Offers small and thin "package" solution but has limitations
  - Is smaller than wire bond CSP, but larger than wafer CSP
  - Likely to be more expensive than either technology initially
- A potential bridge between FC-CSP, flip chip DCA, WLCSP, and 3D TSV
- Most likely application is a pad limited device (small die, high I/O) that would have other devices attached as face-to-face bonding

108.1/085bp

FREESCALE REDISTRIBUTED CHIP PACKAGE (RCP)

- Freescale Fan-Out Wafer Level CSP Solution
- Ultra Low-k Compatible
  - Pb-free
  - Ultra-thin package approach (< 0.5mm)
  - No package substrate
  - No wire bond/bumps
  - Multichip solutions can still be done as backend process (PoP, etc.)
- Volume Production Planned in 2009
  - Low volume production in Tempe
  - First production in Q1 2009 using SMARTMOS die for consumer application
  - Wireless handset devices to start production in 2H 2009
    - Looking for Manufacturing Partners





Source: Freescale

108.1/105bp

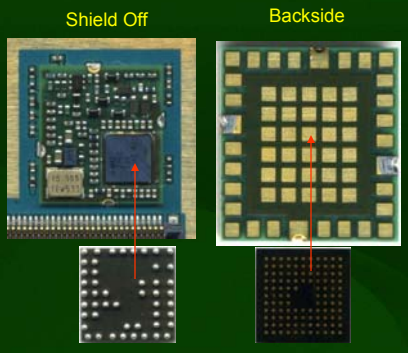
FAN-OUT WAFER LEVEL CSP – SUMMARY

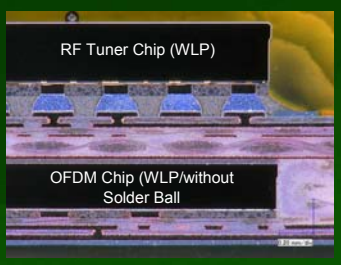
Process:	Leading processes are based on reconfigured wafer that use fab-like redistribution process (photolithography/plating). 200 and 300mm wafer sizes.
Costs:	RDL solutions for a 300mm wafer (at ~ $250) are cost effective when die I/O density is high. However, a reconfigured wafer may have half as many die, doubling cost.
Production Status:	Approaching volume production at Freescale and Infineon/ASE. Q1 2009 − low volumes, Q4 2009 − high volumes.
Business Logistics:	"Assembly" yield is drawback that has plagued this concept since the 1980s or earlier. If process does not achieve better than 99.5% yield, then must be reworkable, or a very low value die. Die sourcing from multiple companies can also be an issue.
Other Limitations:	A solution to support multiple die of various configurations is where this technology fits. Also, offers extension of WLCSP for pad limited die.

MURATA ISDB-T One-Seg MOBILE TV TUNER MODULE

37.9/333bp

- Mobile TV Tuner for Japanese Phones
  - Second-generation: 9.6 x 8.7 x 1.5mm
  - First generation: 13.2 x 10.8 x 1.4mm
  - 40% smaller due to Casio EWLP PCB embedded die
- 9.6 x 8.7 x 0.8mm PCB
  - Six layers total
  - Four microvia layers, 40µm vias
  - Embedded WLP between L4 – 5
  - Casio EWLP technology
  - Fabricated by NEC Toppan
- Fujitsu OFDM Demodulator
  - 6.4 x 6.4 x 0.3mm EWLP
  - Embedded in PCB
  - 113 Cu pillars, 0.5mm pitch
  - 50µm encapsulant, 250µm Si thickness
- MAXIM ISDB-T One Seq Tuner
  - 3.2 x 3.2 x 0.5mm WLP Mounted on PCB, underfilled
  - 48 pillars/balls, 0.4mm pitch
- Design and SMT Assembly by Murata
  - 76 components, mostly 0201 passives
  - 60 LGA pads, 1mm pitch
  - Metal EMI shield
  - Up to 0.5M units/month, now discontinued due to die shrink





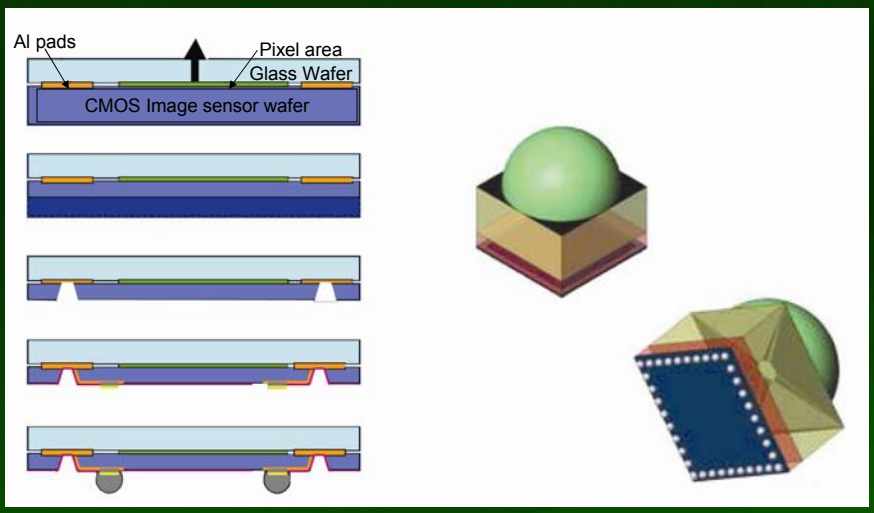
78.294bp

3D WAFER INTERCONNECT APPLICATIONS

- Memory Die (Flash and DRAM)
  - Justification: miniaturization, increased speed, lower power consumption
  - Low interconnect density and parallel interconnect structure
  - Low power (thermal management)
  - Parallel interconnect structure
  - Same size die (wafer level bonding possible)
- High Speed Processors and Memory
  - Justification: electrical performance improvements with shorter interconnect path, separation of logic and memory
  - Challenges
    - Thousands of vias
    - Large die alignment
    - Power dissipation
    - KGD
    - 3D design tools
- Image Sensor, RF and MEMS
  - Combine specialty die with logic/controller
  - Shorter interconnect path
  - Wafer capping

78.5/294tp

STMICROELECTRONICS
WAFER-LEVEL CAMERA WITH TSV – FIRST GENERATION



Source: ST

88.5/294bes

3D/TSV ENABLING TECHNOLOGIES
A Complex Implementation Challenge

- Through-Silicon Via Fabrication
- Wafer Thinning
- Fine Pitch Wiring and Interconnection (W2W, D2W, F2F)
- Fine Pitch Test for KGD
- Power Delivery, Distribution, and Thermal Management
- Competitive Alternatives: Well-Entrenched Incumbent Technologies
  - Fine pitch wire bond
  - Stacked die
  - Flip chip
  - WLP
  - PoP/PiP

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THANK YOU!

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