# 2009 Poster Session 1

# ARCHIVE 2009

## Contact Challenges with Leadless Devices

Justin Toops, Kiley Beard, John Diller—Interconnect Devices, Inc.

## Interconnect Technology: Is There Really a Sweet Spot?

Paul Schubring—Plastronics
Praba Prabakaran—Antares Advanced Test Technologies

## A Fast Optimization Approach Which Integrates Mechanical & Electrical Performance into High Speed Socket Design

Dr. Yen-Chih Chang—Hon Hai Precision Ind. Co. Ltd.
Andrew Gattuso—Foxconn Electronics, Inc.

## High Performance Electrical Contact For 0.3-0.4 mm Contact Pitch

SM Low—ADE Technologies
Che-Yu Li, Tia Kohornen—Che-Yu Li & Co.
Adam Hopper—Protos Electronics

BiTS 2009

# Contact Challenges with Leadless Devices

Justin Toops, Kiley Beard, Jon Diller – IDI

**Spring Probes**

**VS.**

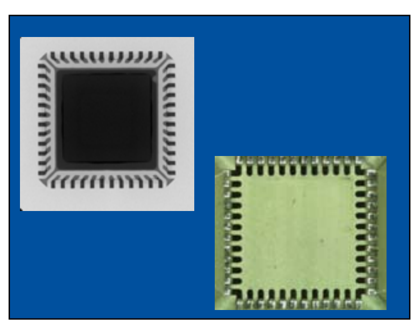
**Wiping Contacts**

- Reduced 4 pt crown
- OAL 3.30mm
- 27 gram force

- 120° Spear
- OAL 3.30mm
- 32 gram force

- Concave
- OAL 3.30mm
- 32 gram force

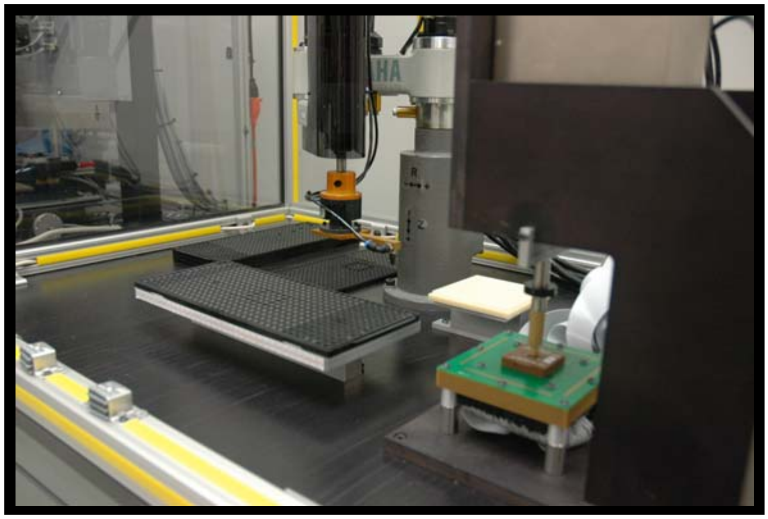
- Dyno™
- Height 3.14mm
- 90 gram force



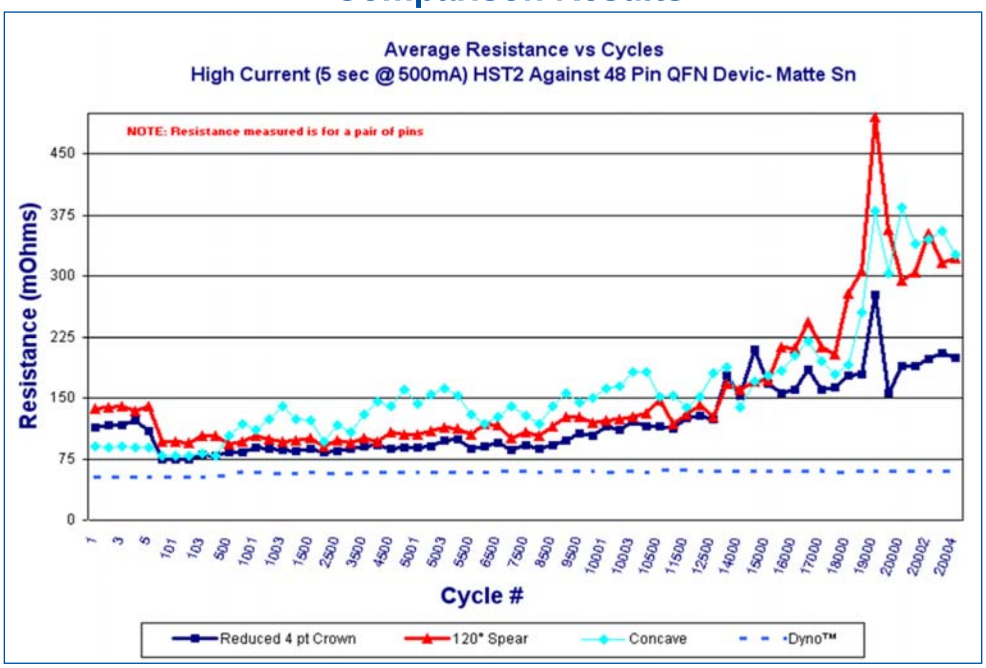
3/2009 Contact Challenges with Leadless Devices 1

**Poster #1**

## Handler Simulation Testing Setup



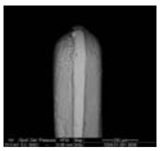
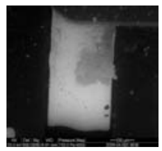
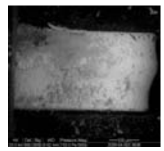
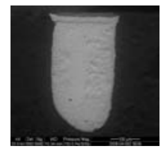
## Comparison Results




3/2009 Contact Challenges with Leadless Devices 2

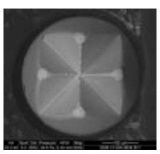
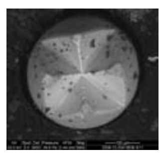
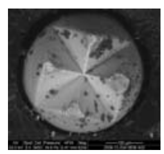
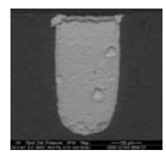
## Wiping Contacts

**Before** | **After** | **Witness Mark**

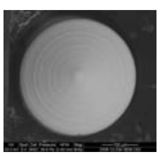
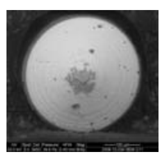
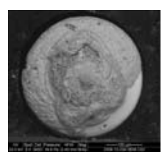
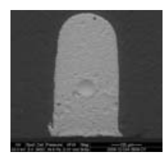





**DYNO™**

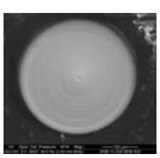
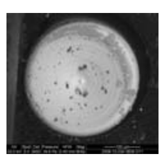
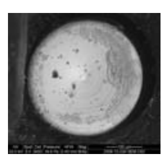
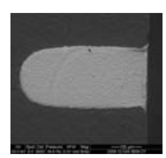
## Spring Probes

Reduced 4pt Crown

120° Spear

Concave

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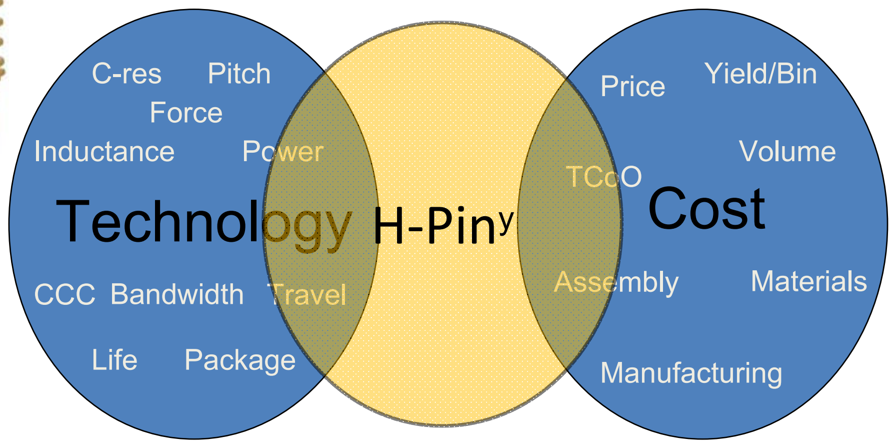
# Interconnect Technology:
## Is there really a sweet spot?

Paul Schubring, Plastronics
Praba Prabakaran, Antares Advanced Test Technologies




## 1. Introduction

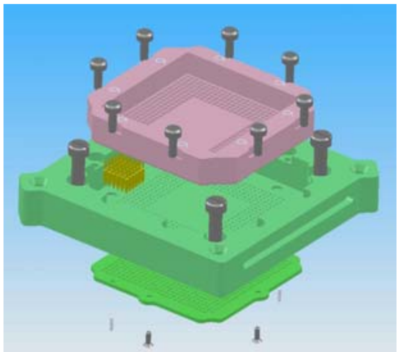
Semiconductor *product diversification* continues at record pace.

Performance capabilities of interconnect technologies too often lead to *mutually exclusive product solutions* –

***COST** or **CAPABILITY***

The result: Broad array of products in the factory that *increase product cost and resource requirements* – **people and money**.

Plastronics introduced the H-Pin at BiTS2008 as a single interconnect solution to address a broad range of products for Burn-In, Test, and System Level Test and enable lower cost of ownership and shorter development lead times.



## 2. Overview

The H-Pin is a stamped contact with spring probe performance providing a robust contact solution for Burn-in, Test, and programming applications.

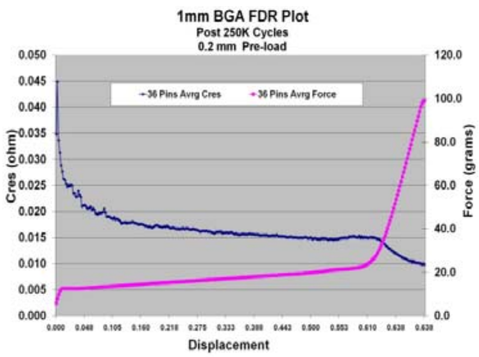
## 3. Validation Overview

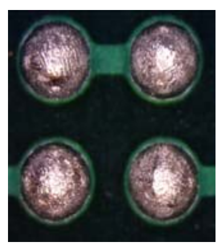
H-Pins tested:

- LGA: 0.5mm and 1.0mm
- BGA: 0.5mm and 1.0mm
- 500 and 700 pin sockets
- Au Device simulator

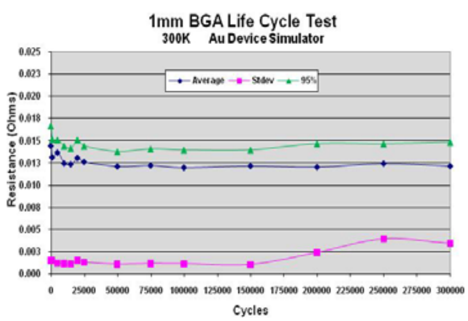
Testing Performed:

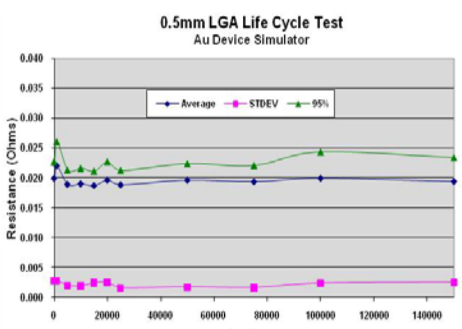
- FDR
- Life Cycle / C-res
- CCC
- Signal Integrity
- Extended Bake Test

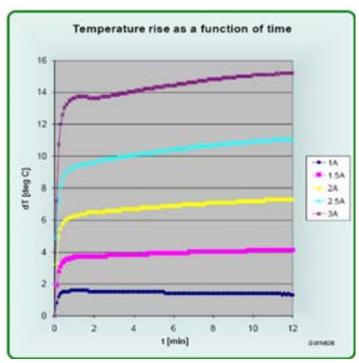


Witness marks: 150C / 1000 hrs



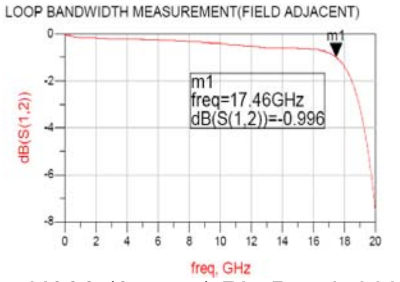



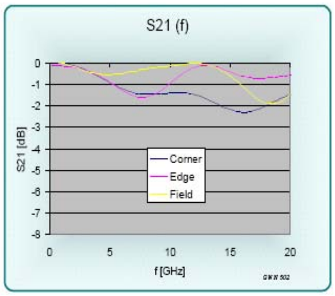

H077 (1mm) T-rise

3/2009 Interconnect Technology: Is there really a sweet spot? 2

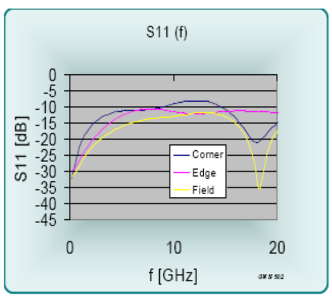
**Poster #2**




H038 (0.5mm) Pin Bandwidth




H038 Pin Insertion Loss




H038 Pin Return Loss

## 4. Test Summary

C-res down to 13 mΩ with 3mΩ standard deviation

150-300K life cycles

-50°C to 180°C Temperature Rating

High Bandwidth

< 1nH inductance

High Current Carrying Capacity

## 5. Conclusion

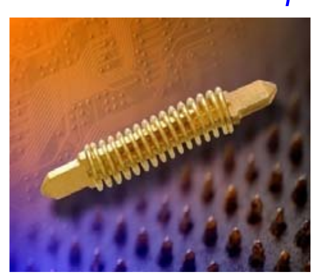
With performance comparable to the best attributes of competitive interconnect solutions, H-Pin delivers mechanical and electrical performance for a broad spectrum of semiconductor products at an *unmatched price point*.

H-Pin's highly scalable manufacturing capacity makes *delivery and lead time issues* a thing of the past.

*Relative* Performance of Test and Burn-in Technologies

| | | Standard Burn-in Socket | Probe Pin Test Socket | Membrane Test Socket | *H-Pin* |
|---|---|---|---|---|---|
| Electrical | Current Carrying Capacity in Amps (higher the better) | 0.5 | 2+ | 2+ | 2+ |
| Electrical | Resistance in mOhms (lower the better) | 50 | 100 | 10 | <35 |
| Electrical | Inductance in nH (lower the better) | 6 | 2 | 0.4 | 0.9 |
| Mechanical | Contact Life in thousands of cycles | 10 | 250+ | 25 | 250+ |
| Mechanical | Contact Travel in mm | 0.20 | .50+ | 0.10 | .50+ |
| Production Costs | Assembly of Socket Automation or Manual | A | M | M | A |
| Production Costs | Cost at 1mm Contact cost per pin | A | C | D | E |
| Production Costs | Cost at .5mm pitch Contact cost per pin | A | C | D | E |

With robust performance at high volume price and fast delivery, the H-Pin hits the *sweet spot.*



Patent No: US 7,025,602

Relative Cost: A<E<D<C

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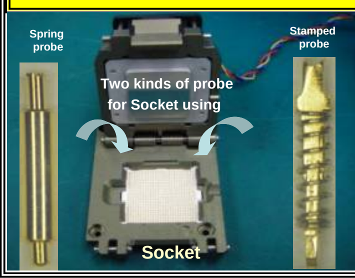
# A Fast Optimization Approach which Integrates Mechanical and Electrical Performance into High Speed Socket Design

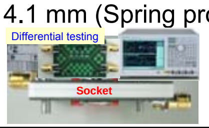
Dr. Yen-Chih Chang and Andrew Gattuso

## Present Capability



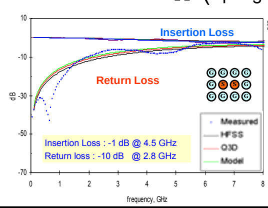

### Mechanical

Full Stroke：0.8 mm
Working Stroke：0.7 mm
Spring Force：33 g ± 20%
Seating height :
2.7 mm (Stamped probe)
4.1 mm (Spring probe)

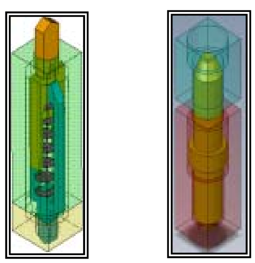



### Electrical (single pin)

Lself ：1.9 nH (Calculation)
RBulk：2.3 mΩ (Spring Probe)
d probe)




## Target：High Speed Test



### Mechanical：

Full Stroke：0.5 mm
Working Stroke：0.4 mm
Spring Force：30 g ± 20%
Seating height : 2.0 mm

### Electrical：(single pin)

Lself ：0.9 nH (Calculation)
RBulk：1.8 mΩ (Spring)
4.5 mΩ (Stamped)

## Fast Socket Design Approach

| Design Target | Feasible Layout | Design Model | SI Evaluating |
|---|---|---|---|
| Key Spec.<br>Pitch=0.5 mm<br>Self inductance < 1nH<br>Port impedance<br>SI parameter | Pin's configuration | Design rule：<br>Mechanical<br>Electrical<br>- Housing Design<br>- Impedance criteria<br>- Tolerance analysis<br>- manufacturability | - Loop L,C<br>- Effective L,C for test pattern<br>- SI performance by using SPICE |

3/2009 A Fast Optimization Approach which Integrates Mechanical and Electrical Performance into High Speed Socket Design 1

Poster #3

## Feasible Layout

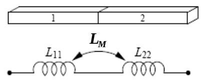
# Socket design for 0.5 pitch

**Determine Pin's configuration**

**Key : *Pin's self-inductance < 1 nH***

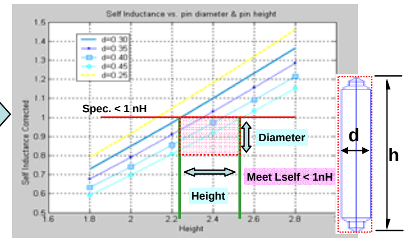
- Cannot be explicitly measured,
- Strictly mathematical concepts.

$L_{self} = L_{11} + L_{22} + L_M$



$L_{kk} = 2 \cdot h \cdot \left( \ln\left(\frac{4 \cdot h}{d}\right) - 0.75 \right)$

$L_M = 0.1 \cdot \left( h_1 \cdot \ln\left(\frac{h_1 + h_2}{h_1}\right) + h_2 \cdot \ln\left(\frac{h_1 + h_2}{h_2}\right) \right)$




Pin's height, diameter range

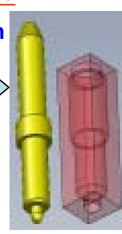
**Theoretical calculation normally have 5% deviation with Q3D simulation!**

## Design Model

**Mechanical Considerations**

Current Skills limit
Spring (Normal force vs. LLCR )
Tolerance analysis
Assembling
Reliability

**Design Rule**



**Control impedance for Socket**

**Design Rule**

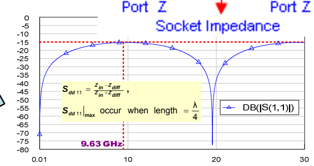
Choose housing material
Capacitance vs.effective $\varepsilon$
Housing design

**Criteria for Min. Reflections**


**Impedance design Target**

Matching with port impedance for minimum Reflections

| Port Impedance | Differential Impedance, Ω | |
|---|---|---|
| | Lower Bound | Upper Bound |
| 100 | 90.45 | 110.55 |
| 85 | 76.89 | 93.97 |




**Target for Control Impedance**

## SI Analysis

- Checking whether Socket's SI performance can meet the spec.
- Looking for ways to improve SI performance

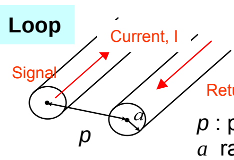
**Step 1: Calculate the inductance and capacitance of a loop**

For Spring Probe: Through the two-wire transmission line formula

**Inductance :** $L = \frac{\mu_0}{\pi} \ln\left(\frac{p}{a}\right)$

**Capacitance :** $C = \frac{\pi \varepsilon_r \varepsilon_0}{\cosh^{-1}\left(\frac{p}{2a}\right)}$

**Loop**




$p$ : pitch
$a$ radius

**Modify the L,C through a semi-empirical formula for correctness.**



Poster #3

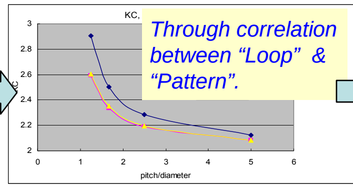
## SI Analysis

**Step 2: Obtain the effective inductance and capacitance of patterns**

Loop | Transfer Function | Test Pattern

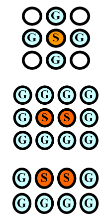
$L_{Loop}$

$C_{Loop}$

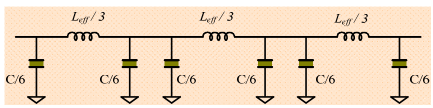



$L_{eff} = K_L \times L_{Loop}$

$C_{eff} = K_C \times C_{Loop}$



**Step 3: SI performance by SPICE**

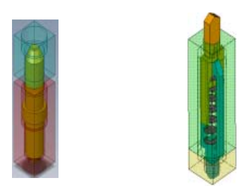



1. Normally,10 % larger compared with measurement & simulation.
2. Model result as an "Upper Bound".

## Final Design

***0.5 mm pitch Test socket***

Spring Probe | Stamped Probe



S Parameters ：

Housing material：PEEK, $\varepsilon_r$=2.85

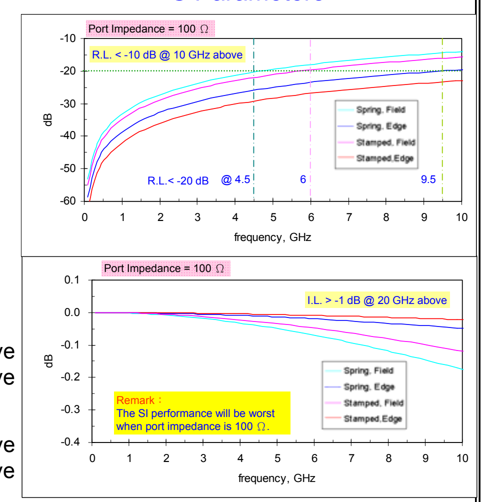
For Spring Probe：

Return Loss < -10 dB @ 10 GHz above
Insertion Loss > -1 dB @ 20 GHz above

For Stamping probe：

Return Loss < -10 dB @ 20 GHz above
Insertion Loss > -1 dB @ 20 GHz above

S Parameters




## Conclusion

Based on analytical formulas, LC model, and correlated with measurement data, this approach has proven to help the designer quickly catch SI characteristics when designing high speed sockets.

Che-Yu Li and Co.
ADE Technologies
Protos Electronics

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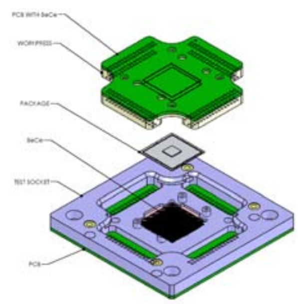
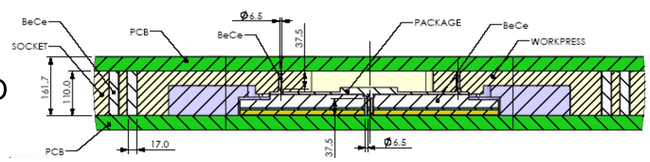
# High Performance Electrical Contact for 0.3-0.4 mm Contact Pitch

Che-Yu Li*, SM Low**, A Hopper***, TM Korhonen*
* Che-Yu Li and Co., LLC, Ithaca, NY
** ADE Technologies, Singapore
*** Protos Electronics, Santa Clara, CA

## POP Socket

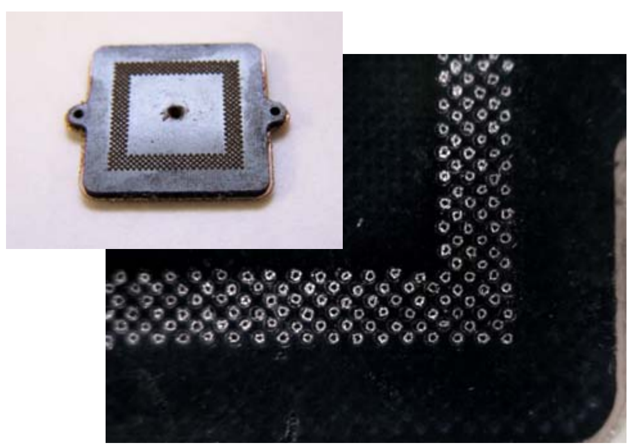
- Upper and lower BeCe (BGA)
- Return BeCe (LGA)
- 0.4 mm pitch (BGA)
- Over 600 I/O
- 50 mil high, 6.5 mil OD
- Inductance 0.5 NH
- Resistance 25 mΩ
- Contact force < 10g/ IO
- Compliance 20%






## 0.3 mm Interposer

- 0.3 mm pitch
- 400 I/O
- 60 mil high, 6 mil OD
- Inductance 0.6 NH
- Resistance 20 mΩ
- Contact force <10g/ IO
- Compliance 20%



3/2009 High Performance Electrical Contact for 0.3-0.4 mm Contact Pitch 1

## Issues in High Pitch

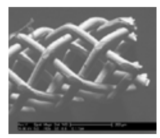
- Current technologies are difficult to scale below .4 mil pitch
- Smaller size of springs and probe tips results in decrease in mechanical strength
- Many test socket materials are not able to withstand the high contact forces required by high pin counts
- High power is required – difficult to further decrease cross-sectional area of contact
- Signal integrity at high frequencies needs to be improved
- New approaches needed to continue scaling to tighter pitches

## Braided Electrical Contact Element

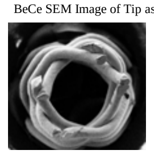
- BeCe ™
- 8 helical springs operating in parallel


All Dimensions in mils

Coreless BeCe
0.7x2.5x15



BeCe SEM Image of Tip as Cut

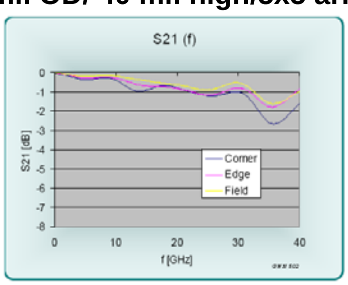


## Attributes

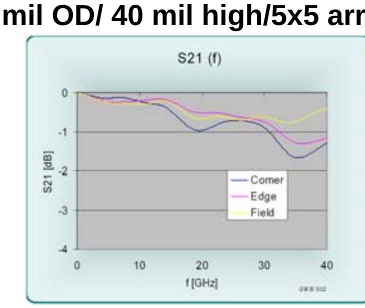
- Low Contact Force ➔ Large Array
- High Compliance ➔ Low Inductance or High Frequency
- Low Resistance ➔ High Power
- Small OD ➔ Fine Contact Pitch
- Plated Stainless Steel Wire ➔ High Service Temperature
- Multiple Contact Tips ➔ Redundancy
- Medical Grade Braiding Wire ➔ Durability

## High Frequency Data

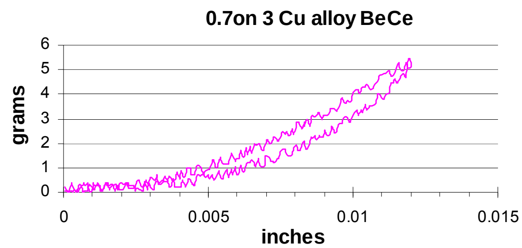
**14 mil OD/ 40 mil high/5x5 array**



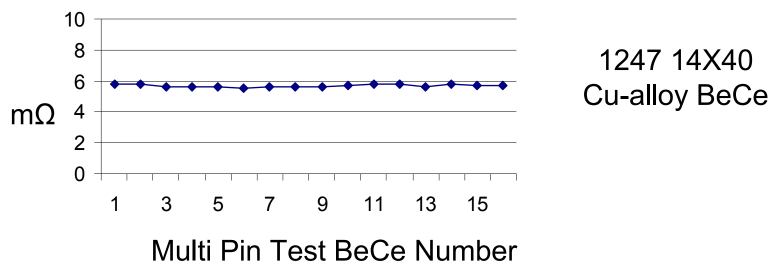

**6 mil OD/ 40 mil high/5x5 array**



## Single Pin Test Data for 6 mil OD BeCe

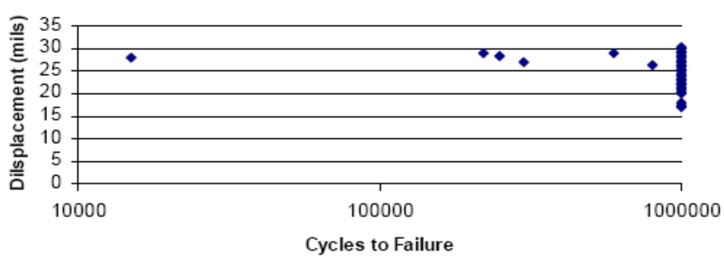



## Area Array Multiple Pin Test Data




## Durability of BeCe Array

- > 1 million cycles near elastic limit
- Displacement loading
- 98 mil 36 pin array, unplated stainless steel






Poster #4