BiTS Burn-in & Test Socket Workshop 2008 Tutorial

ARCHIVE 2008

"Basic Chip Reliability Concepts (Product RE "101")"

Ann Swift
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This talk focuses on the basic concepts of CMOS semiconductor screening and failure rate projections. Basic reliability engineering concepts are discussed (the "bathtub" curve, the difference between wearout and defect mechanisms, acceleration factors, etc.). Failure rate models to relate accelerated testing/stressing to product lifetimes are illustrated. Various manufacturing screens (such as Burn-in and Voltage Screen) are shown along with their impact on product failure rates. What the future might hold for reliability screening is also discussed.

Who should have attended this tutorial?

What is that accelerated testing/stressing that companies do using the sockets developed by BiTS member companies? Have you ever wondered what these product reliability engineers you talk to do? If so, this tutorial will help you understand the world of reliability engineering and accelerated testing/stressing. This talk will focus on basic concepts of CMOS semiconductor screening and failure rate projections. Various manufacturing screens (such as Burn-in and Voltage Screen) will be discussed along with their impact on product failure rates. The talk will begin with the basic concepts of reliability engineering. The differences between wearout and defect mechanisms in semiconductor devices will be discussed. Reliability testing methods including stress acceleration and screening will be illustrated and examples of how to relate accelerated data to "real life" will be discussed. This tutorial is a must for anyone interested in starting to understand the field of chip reliability.

Basic Chip Reliability Concepts (Product RE "101")

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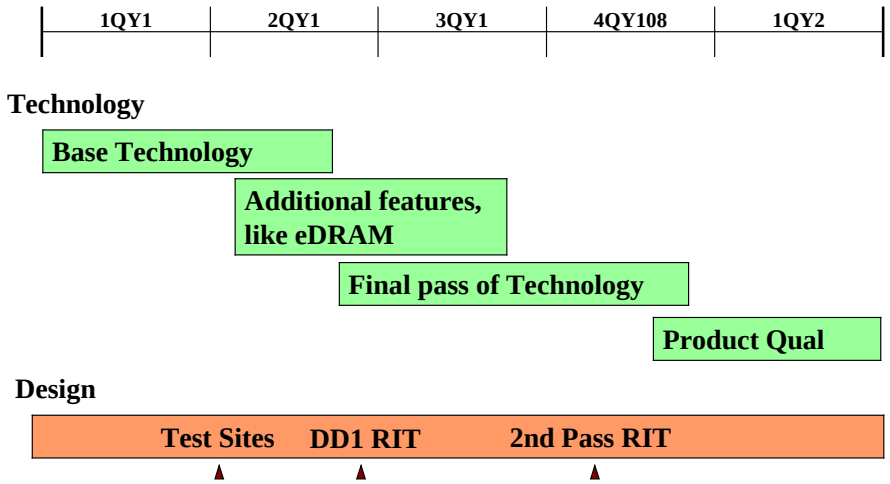
WHY AM I HERE????

- To try and help you answer two essential questions…
  - Why do they ask me to provide economic, reliable, high temperature / high power contacting solutions?
  - What do Reliability Engineering people do with the information they collect from the stresses they run?

HOPEFULLY YOU WILL NOT BE AS "SNOWED" AS MY TRUCK IN VERMONT

- **Time to market ➔ directly impacted by time to qualify a product**

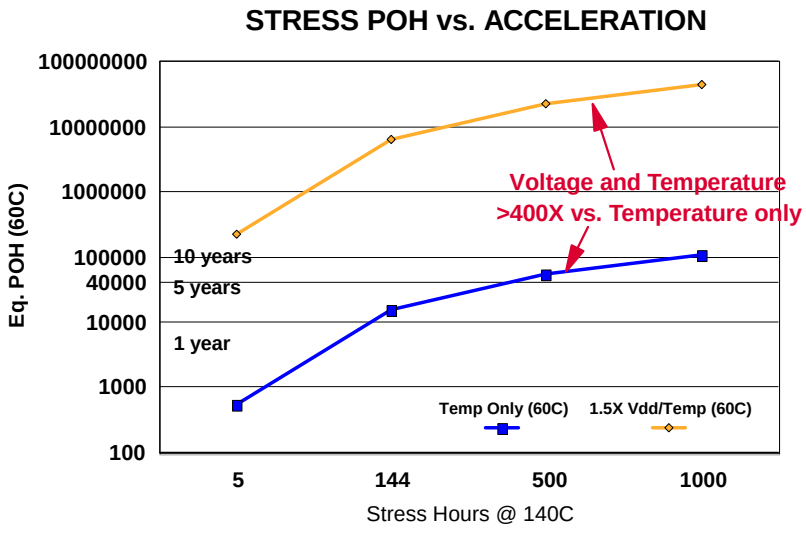
QUALIFICATION FLOW



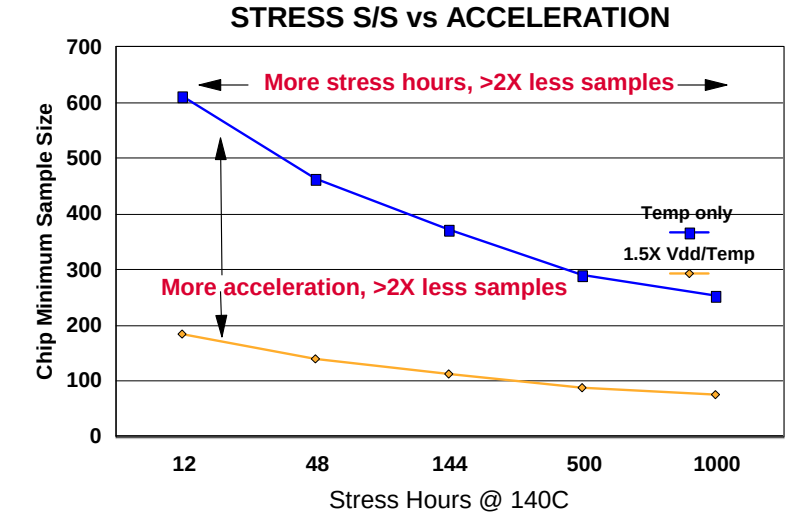
ACCELERATION IMPORTANT

- Less acceleration ➔ more time on stress to get to a required equivalent Power on Hours (POH) point
- Less acceleration ➔ more samples needed to get enough fails/statistics to develop a model and project failure rates

VOLTAGE / TEMPERATURE ACCELERATION IMPORTANCE



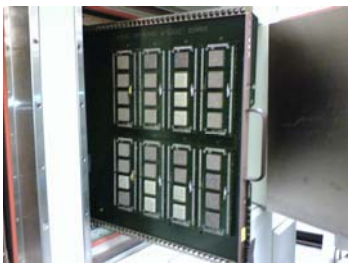
VOLTAGE / TEMPERATURE ACCELERATION IMPORTANCE

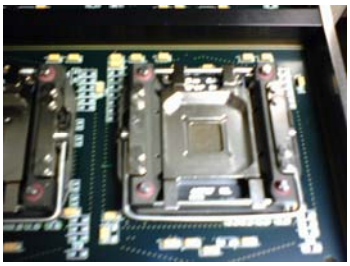


STRESS CAPACITY IMPORTANT

- More acceleration➔ more power➔
  - Less parts per Burn-in Board (BIB)
  - More BIBs and stress tools needed to stress required sample size
    - Or longer qual cycle times due to having to make several runs through capacity available
  - More cost due to more sockets / tools required
  - More risk due to more complicated socket/thermal and BIB/stress oven designs
- BI tooling is the "bricks and mortar" of qualification stresses

STRESS CAPACITY IMPORTANT





STRESS CAPACITY IMPORTANT

- **Illustration - Program schedule gives you 2 months to stress (and do test readouts on) 1000 parts for 1000 hours**

Ovens **$1M**	**2 (16 BIB slots/oven)** **$2M**	**4 (16 BIB slots/oven)** **$4M**
BIBs **$5-7K**	**32 (16 x 2 ovens)** **$160K-$224K**	**64 (16 x 4 ovens)** **$320K-$448K**
Sockets **$300-$400*** **(*high power can be $500-$800!!)**	**1024 (32 x 32 per BIB)** **$307.2K-$409.6K**	**1024 (64 x 16 per BIB)** **$307.2K-$409.6K**
Total	**$2.47M-$2.63M**	**$4.63M-$4.86M**

Approx. 2X More

And if you did not want to spend that, ~2X more time to run stresses serially

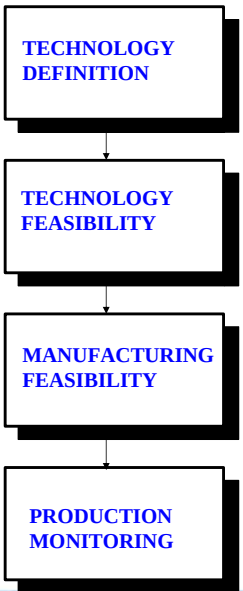
OUTLINE

- **Reliability Stressing/Model**
  - Qualification Cycle
  - Reliability "Categories"
    - "Technology" RE mechanisms
    - "Defect" / "Product" RE mechanisms
  - Building a Reliability Model
    - Product Stress Profiles/Measurements
    - Effects of Screens
  - Reliability Modeling
    - FITs, Chi-Squared, etc.
- **Manufacturing Screens**
- **Reliability Monitoring**

RELIABILITY STRESSING/MODEL

- Qualification Cycle
- Reliability "Categories“
  - “Technology” RE mechanisms
  - “Defect” / “Product” RE mechanisms
- Building a Reliability Model
  - Product Stress Profiles/Measurements
  - Effects of Screens
- Reliability Modeling
  - FITs, Chi-Squared, etc.

TYPICAL QUALIFICATION CYCLE RELIABILITY MILESTONES



TYPICAL QUALIFICATION CYCLE RELIABILITY MILESTONES

TECHNOLOGY DEFINITION

- FIRST ENGINEERING HARDWARE
- DETERMINE
  - CRITICAL DESIGN POINTS
  - RELIABILITY TEST VEHICLES DESIGNED
  - DESIGN MODELS
  - TEST/BURN-IN EQUIPMENT NEEDED

TYPICAL QUALIFICATION CYCLE RELIABILITY MILESTONES

TECHNOLOGY FEASIBILITY

- FORMAL TEST STRUCTURE EVALUATIONS
  - RULES FOR WEAROUT AVOIDANCE
  - CRITICAL PARAMETERS / GROUND RULE GENERATION

TYPICAL QUALIFICATION CYCLE RELIABILITY MILESTONES

MANUFACTURING FEASIBILITY

- PRODUCT HARDWARE DELIVERED
- EVALUATE
  - CHIP/ PACKAGE DESIGN ROBUSTNESS
  - PRODUCT RELIABILITY MODELS / MEASURED LEVELS
  - BURN-IN / SCREENS STRATEGY VERIFICATION
  - FABRICATOR PROCESS INTEGRITY, REPEATABILITY
  - PRODUCT MONITORS ESTABLISHED

TYPICAL QUALIFICATION CYCLE RELIABILITY MILESTONES

PRODUCTION MONITORING

- QUANITY OF PRODUCTION LEVEL HARDWARE
  - ROUTINE STRESSES/TESTS VS. TARGETS
  - MAVERICK CONTROLS
  - LINE/FIELD RETURNS PROGRAM

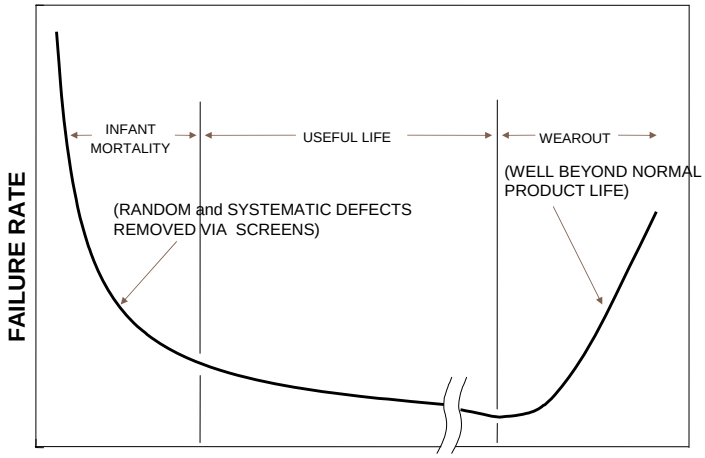
RELIABILITY STRESSING/MODEL

- Qualification Cycle
- Reliability "Categories“
  - “Technology” RE mechanisms
  - “Defect” / “Product” RE mechanisms
- Building a Reliability Model
  - Product Stress Profiles/Measurements
  - Effects of Screens
- Reliability Modeling
  - FITs, Chi-Squared, etc.

RELIABILITY CATAGORIES / MANAGEMENT STRATEGY

- WEAROUT MECHANISMS
- SYSTEMATIC DEFECTS
- RANDOM DEFECTS

"BATHTUB" CURVE



RELIABILITY "CATEGORIES"

- **Wearout**
  - Low, nearly zero failure rate until onset, then increasing failure rate until 100% failure reached (ex. electromigration)
  - Caused by technology "weak points"
  - Strategy –
    - Eliminate from design
      - Technology/design changes
      - Chip design ground rules
      - Application specifications

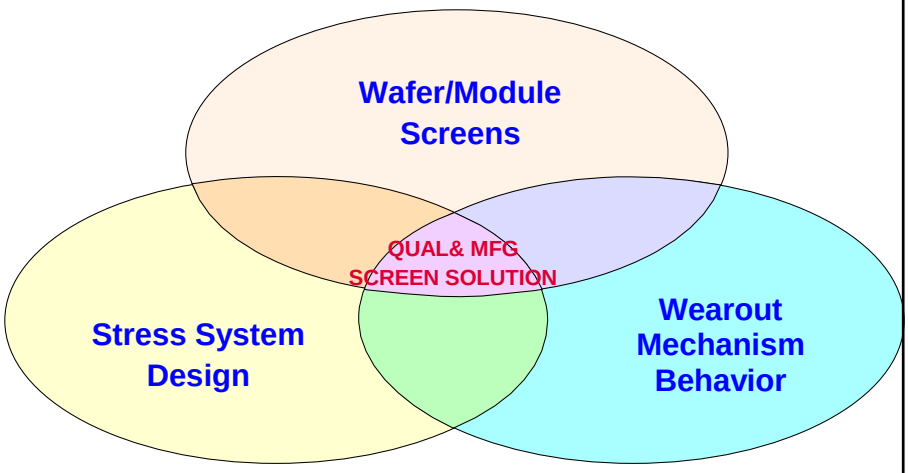
RELIABILITY "CATEGORIES"

- **Systematic Defects**
  - Process marginality beyond acceptable norm
  - Strategy –
    - Control technology and process
      - Technology design
      - Layout ground rules
      - Process monitors

RELIABILITY "CATEGORIES"

- **Random Defects**
  - Decreasing failure rate
  - Caused by process deficiencies
  - Strategy –
    - Continual defect reduction
      - Technology/tooling improvements
    - Screen out residuals
      - Wafer/chip screens
      - High efficiency burn-in
      - "Outlier" control

WHY DO I NEED TO KNOW ABOUT WEAROUT MECHANISMS?



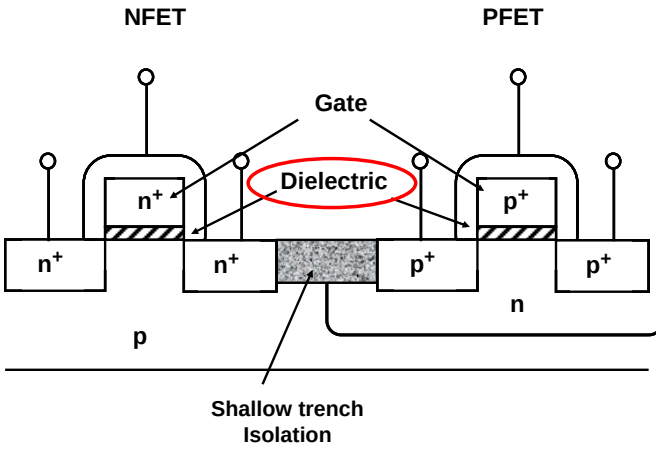
WEAROUT MECHANISMS

- **FRONT END OF LINE (FEOL)**
  - Gate Oxide Wearout
  - NBTI (Negative Bias Temperature Instability)
  - Hot Carriers
- **BACK END OF LINE (BEOL)**
  - Electromigration
  - Stress Induced Voiding
  - ILD TDDB (Interlevel Dielectric Time Dependent Dielectric Breakdown)

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Complementary MOS Technology



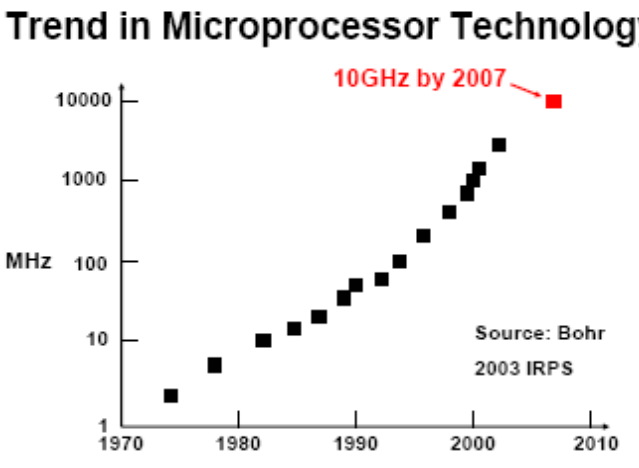
FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout – **Why Do we Care?**

- The gate dielectric is the most fragile element of a transistor
  - Extremely thin layer of material biased during normal operation.
- Aggressive scaling of the gate oxide thickness (tox) in CMOS transistors ➔ quality and reliability of ultra-thin dielectrics is of greater importance
- Gate current has grown exponentially as tox has been reduced
  - Causes increased power consumption ➔ affects device and circuit functionality (and screenability).
  - Decrease NFET drive current seen on very thin oxides ➔ performance limiter
  - Leakage current imposes a practical limit on oxide thickness
- Causes the oxide to be more susceptible to both "extrinsic" (defect) and "intrinsic" (wearout) "problems"

FEOL WEAROUT MECHANISMS

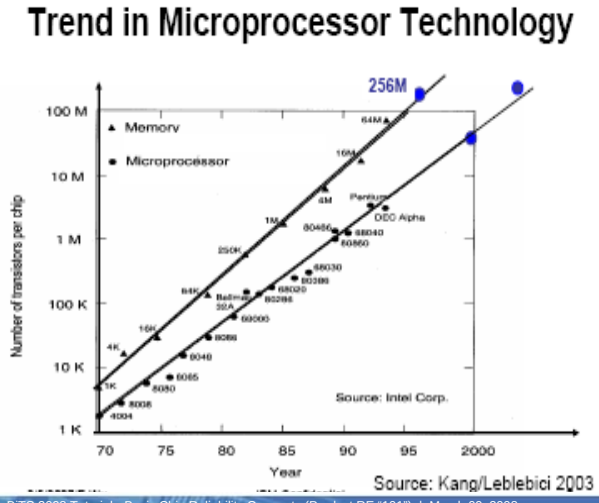
- Gate Oxide Wearout



t Wu, IBM

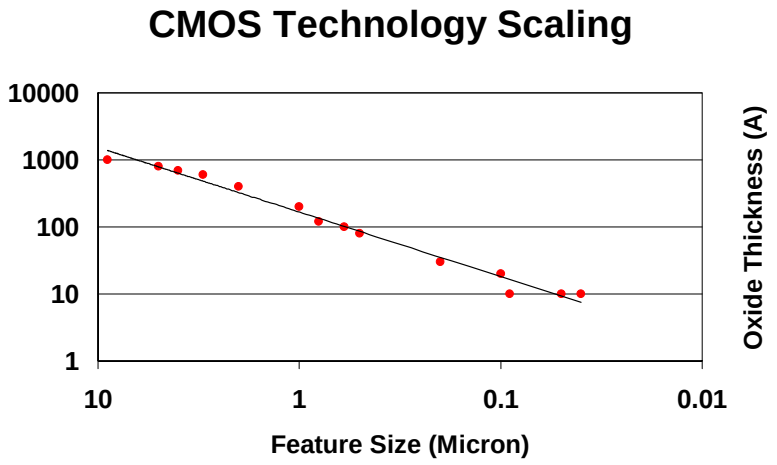
FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout



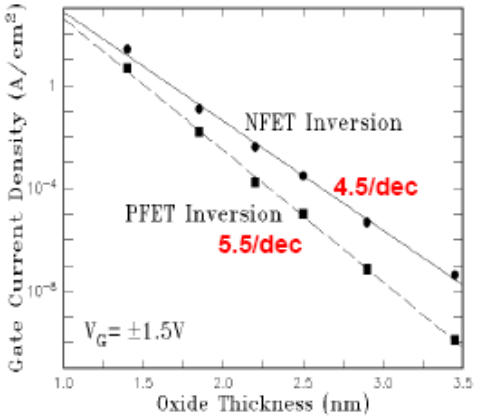
FEOL WEAROUT MECHANISMS

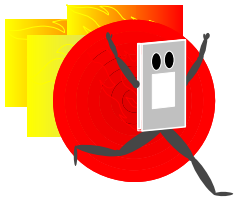
- Gate Oxide Wearout



FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout
  - Oxide scaling ➔ increase in direct tunneling ➔ more power





15 order of magnitude increase

Courtesy of Ernest Wu, IBM

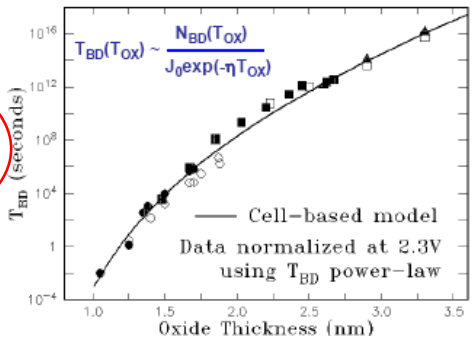
FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

Time to Breakdown and Oxide Scaling

- $T_{BD63\%}$ reduction by 20 orders from 3.5nm to ~1.0nm
- Weibull slope ➡ 5 extra orders of lifetime reduction

A lifetime reduction of 25 orders for T_{OX} scaling from 3.5 nm to ~1 nm @ const. V_G



Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

- Dielectric / Oxide Uses –
  - Active elements
    - Gate dielectric ➔ CMOS
    - Charge storage capacitor ➔ DRAM
    - Inter polyimide dielectric ➔ NVRAM
  - Passive elements
    - Capacitors ➔ analog and RF applications
    - Insulating capacitors: BEOL
    - Isolations

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

- Dielectric Materials used in Microelectronics
  - Conventional dielectric materials
    - Silicon dioxide (SiO2)
    - Nitrided oxides or Oxynitrides
      - SiO2-based dielectric (SiON)
    - Silicon nitride (Si3N4)
  - Multi-layers (SiO2/Si3N4/SiO2 or SiO2/Si3N4)
  - High-K dielectric
    - to replace SiO2-based dielectrics
  - Low-K dielectric
    - BEOL dielectric

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

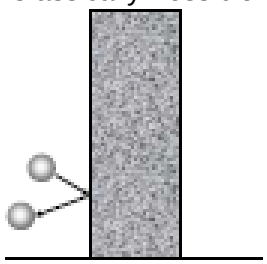
- Why SiO2 ?
  - Amorphous insulator
  - Has similar TCE (thermal coefficient of expansion) as silicon
    - Easy to grow
    - Forms a tight bond
    - Bond free from impurities
  - Easy to integrate in fabrication process
  - Stable, insensitive to subsequent high temp. process steps
  - Interface states can be electrically neutralized (H2-anneal)
  - Very large energy gap
    - High resistivity, (low leakage current, really?)
    - Not true anymore for ultra-thin oxides

Courtesy of Ernest Wu, IBM

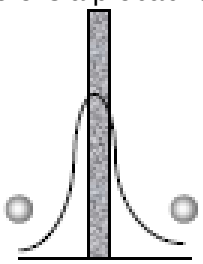
FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**
  - Quantum Mechanical Tunneling
    - If insulators can not conduct, what causes the leakage current through insulators?

Classically Possible



Quantum mechanically there is a probability it can



Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

Breakdown (BD) Mechanisms and Models

- Field-driven model
  - Thermo-chemical model (E-Model) $T_{BD} \propto \exp(\gamma E_{OX}) = \exp\left(\gamma \frac{V_{OX}}{T_{OX}}\right)$
    - Reaction is fundamental but not dominant in oxide BD

- Carrier energy-driven BD models - involving species release
  - Hole induced breakdown models – at higher voltages, leads to hole trapping and hole-related defect generation.
    - Impact ionization (thick oxides)
    - Anode hole injection (thin oxides) $T_{BD} \propto \exp\left(\frac{G}{E_{OX}}\right)$
  - Hydrogen release model (so called "trap-creation" process)
    - Lowest-energy process so far identified ➔ dominates at present MOSFET operating voltages. Follows a power-law relationship $T_{BD} \propto V^{-n}$

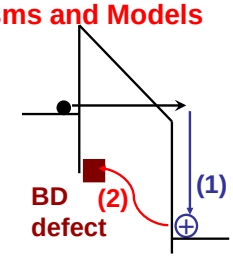
FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Breakdown (BD) Mechanisms and Models

Two-step BD process:

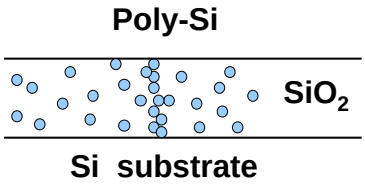
1. **Species release process (hole or hydrogen)**
2. **Reaction process with precusors to create defects**



➔

A critical defect density (N_{BD}) reached

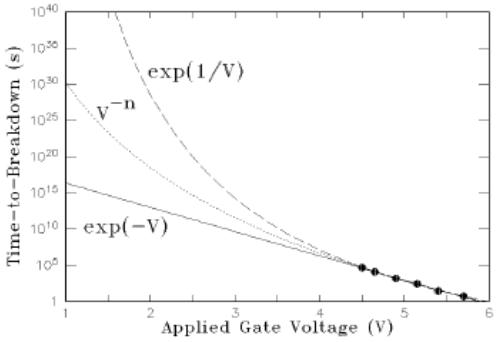
a local conducting path forms and oxide BD occurs



FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Comparison of Time to Breakdown (T_{DB}) Models

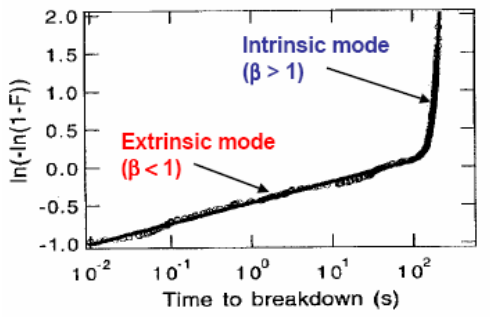


All models can fit the data within shorter time-window, but the projected results differ by many orders of magnitude in lifetimes

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**
  - Intrinsic vs. Extrinsic Breakdown
    - Oxide BD distribution in general is bimodal
    - The focus in recent years is on intrinsic breakdown
    - This does not mean extrinsic (defect based) failure does not exist



Degraeve *et al.* TED, 45, 472,1998

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

- Examples of "extrinsic" manufacturing and yield problems
  - Pinholes
  - Film uniformity
- Examples of "intrinsic" problems
  - gate current leakage increases
  - and ultimately dielectric breakdown

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

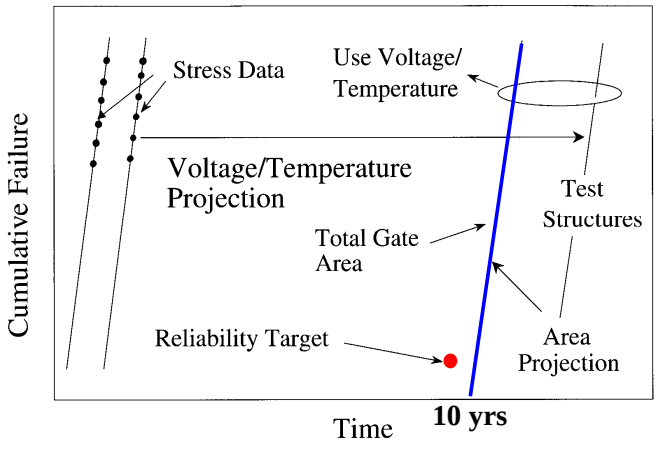
- **Gate Oxide Wearout**

- Estimating reliability requires extrapolation from higher condition measurements to normal operating conditions
  - Measurements are a function of voltage and oxide thickness
  - There appears to be a critical defect density for breakdown
    - Assuming it leads to the correct statistical behavior describing breakdown distributions – Percolation model
  - In some cases an oxide breakdown may not lead to immediate circuit failure (Hard, Soft, Progressive Breakdowns)
- To reduce error, long term (>1 year) stress experiments have been used to measure the wearout and breakdown of ultrathin oxides
- As a rule of thumb, a factor of 10 change in any reliability criterion (e.g., lifetime, failure rate, device area) results in ~0.1 nm change in the minimum *t*ox for a given supply voltage.

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

Dielectric Reliability Projection Procedure



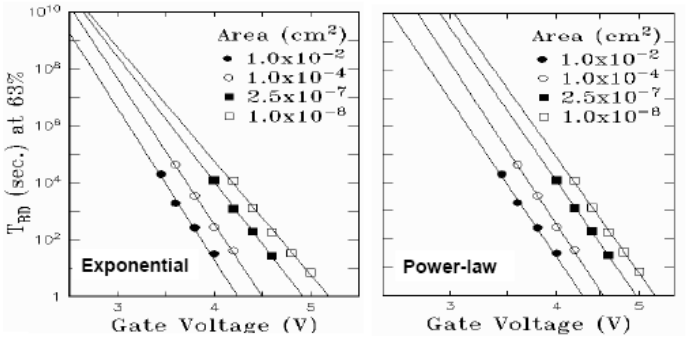
Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

  Voltage and Area Dependence of Oxide Breakdown

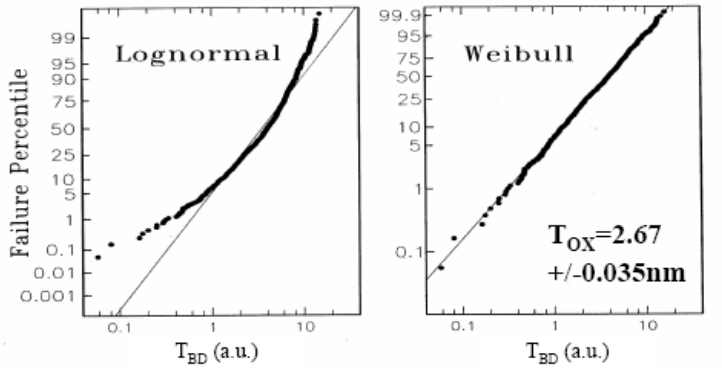
  - A power-law voltage dependence preserves Poisson area scaling
  - Consistent with voltage independence of Weibull slopes



Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout
  - Large sample size (~1000) required to show the differences
  - Weibull function provides excellent fit while lognormal function fails at low and high percentiles



- Data screened from ~ 4000 samples

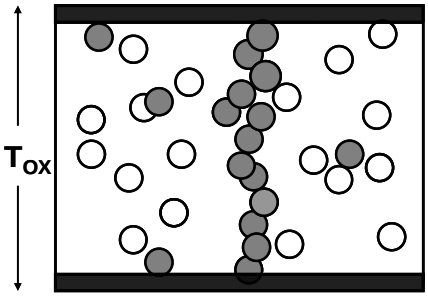
Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

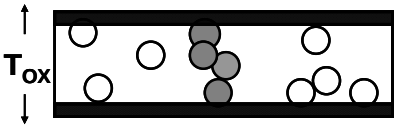
- Gate Oxide Wearout

• Thick oxides

Percolation Path



• Thin oxides



• Critical defect density is reached when the percolation path (leakage path) is formed → oxide breakdown

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

- Breakdown modes
  - Hard Breakdown (HBD)
    - probably a result of thermal damage when sufficient energy is deposited during the breakdown transient.
    - Influenced by the impedance of the circuitry driving the gate in a particular application.
  - Soft Breakdown (SBD)
    - Occurs in a localized spot, and therefore the current after breakdown is independent of device area
  - Progressive breakdown (PBD)

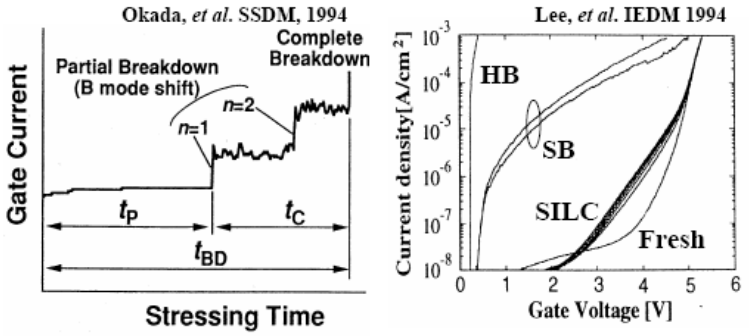
- Present research is aimed at better understanding the
  - Nature of the conduction though a breakdown spot
  - Effect of the oxide BD on device and circuit performance
    - Lab vehicle vs. SBD vs. HBD vs. PBD vs. circuit "failure"

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Soft and Hard Breakdown Observations



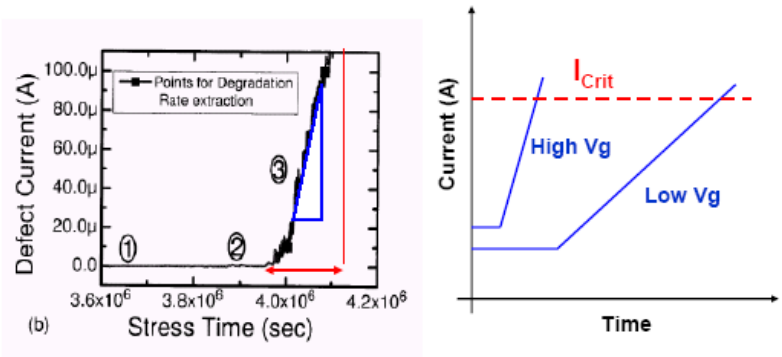
- Soft breakdown precedes hard breakdown
- SB current magnitude much lower than that of HB
- Different post breakdown I-V characteristics (IV shape)

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Newer Finding – Progressive Breakdown



Linder/Stathis *et al.* EDL, 23, 661, 2002

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

- Lab set-ups need to mimic device operation ➔ The use of the "correct" circuit in the lab is important
  - In a circuit, small transistor in series has a high impedance ➔ much lower current capability and capacitive loading
  - In the lab , need mimic by limiting the drive current to low values (corresponding to very small p-FET drivers)

FEOL WEAROUT MECHANISMS

- **Gate Oxide Wearout**

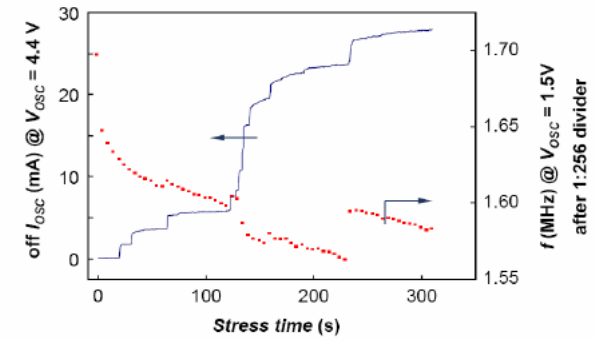
- Limiting drive current will halt the breakdown event such that the transistors may still be operational after breakdown
  - Even a hard breakdown may not completely destroy circuit
  - Experiments have shown that a ring oscillator continued to function even after multiple transistors suffered oxide breakdown ➔ probably a poor test vehicle for oxide reliability.
  - If devices survive an initial breakdown event, the subsequent stress on the damaged oxide can lead to erratic behavior and progressive degradation of the device characteristics .
  - Simple circuit analysis shows that shorting one transistor in an inverter with a resistance often seen during breakdown experiments produces a circuit which still functions as an inverter, albeit one with poorer performance and higher power consumption.

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Breakdown Effects on Circuits-Ring Oscillator

- Ring oscillator remains functional after several HBD events using T_{OX}=2.4nm and wide NFETs/PFETs



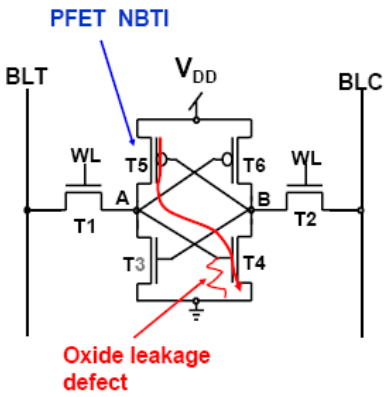
Kaczer, *et al.* TED, v49, p500, 2002

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

Breakdown Effects on Circuits - SRAM



- Gate oxide leakage degrades the pull-down N-FET
- P-FET degrades due to NBTI
- P-FET fights to keep high node at V_{DD}
- This mechanism degrades stability of the cell
- Causing Vmin to be out specification

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

- Gate Oxide Wearout

CONCLUSIONS

- Dielectric breakdown is a real phenomenon
  - More serious issues for ultra-thin dielectrics
  - Margin becomes smaller with scaling
- The study of dielectric behavior is very rich
- Requires a cross-disciplinary field
  - Materials Science
  - Electrical Engineering
  - Physics
  - Chemistry
  - Statistics
  - Mathematics

Courtesy of Ernest Wu, IBM

FEOL WEAROUT MECHANISMS

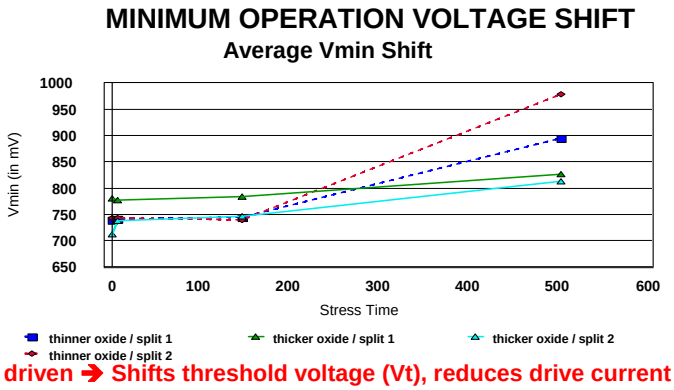
- Gate Oxide Wearout

CONCLUSIONS (con't)

- Process / Design practices can help mitigate impact
- "Extrinsic" oxide problems can be improved
  - by controlling the physical properties of the Si/SiO2 interface
    - a reduction in the strain at the Si/SiO2 interface
    - the cleanliness of the oxide
- More aggressively reduce the power-supply voltage
  - Requires tight control of threshold voltage
  - Loss of performance due to the lower supply voltage
- Power-management schemes used for low-power applications can improve reliability if sections of a chip are turned off when not in use
  - standby power, not just active power➔ oxide degradation
- If failure mechanism is not too severe, can be fixed by using error correction and

FEOL WEAROUT MECHANISMS

- **NBTI (Negative Bias Temperature Instability)** - **WHY DO WE CARE?**



- **Voltage driven → Shifts threshold voltage (Vt), reduces drive current (Idsat)**
- **Becoming more of a concern as products/technologies move towards higher drive current at lower operating voltage**
  - **At use voltages of 1.2V and below→20-50mV shifts are serious**
  - **Increases Vmin of device and slows operation frequency**

FEOL WEAROUT MECHANISMS

- **NBTI (Negative Bias Temperature Instability)**

- Also known as "slow trapping", 1st encountered by B. Deal et. Al., 1967

- Results from an accumulation of positively charged interface (donor like) states and trapped charge near the gate oxide - silicon interface region
  - Effect is more severe for PMOS FETs than NMOS FETs due to the presence of holes in the PMOS inversion layer that are known to interact with the oxide states

- Believed to be an electrochemical reaction involving electric field, holes, silicon-hydrogen bonds and temperature (Blat, et. Al., 1991)
  - During NBTI degradation, the hydrogen-silicon bonds at the Si/SiO2 interface are broken, and the reaction is limited by the diffusion of hydrogen.

FEOL WEAROUT MECHANISMS

- **NBTI (Negative Bias Temperature Instability)**

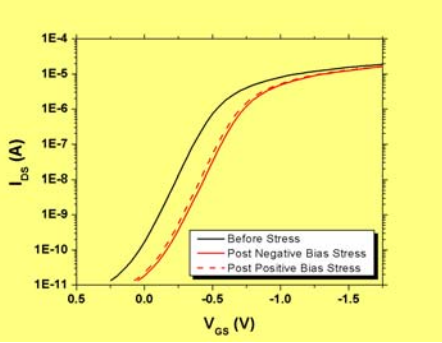
- Mechanism not ionic (ex. Sodium or Potassium) in nature
- Weak channel length dependence
- The thinner the gate oxide, the greater the shift in Vt.
- Recovers with unbiased anneal (bake)
- NBTI effect increased with
  - Nitrogen in gate oxide
  - Boron penetration
  - BEOL "charging" (plasma)
- NBTI effect decreased with
  - Barrier nitride (acts as a barrier to hydrogen rich Inter-level dielectric films)
  - Adding fluorine to oxide

FEOL WEAROUT MECHANISMS

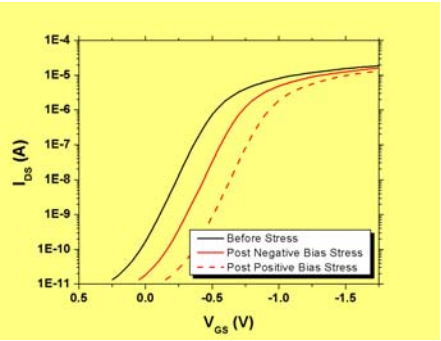
- **NBTI (Negative Bias Temperature Instability)**

NBTI vs. Mobile Ion Response

NBTI



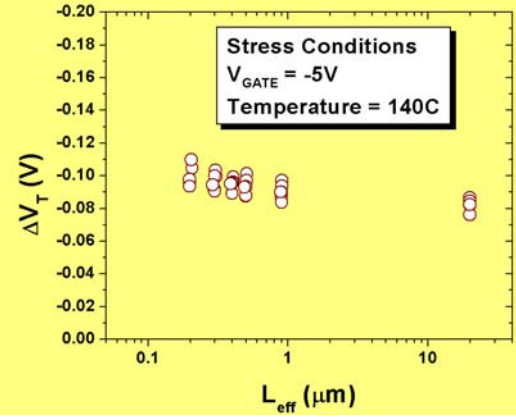
Mobile Ion



FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

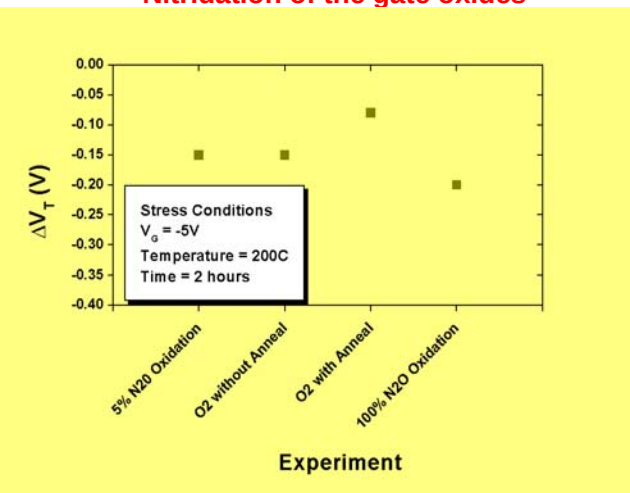
Weak channel length dependence



FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

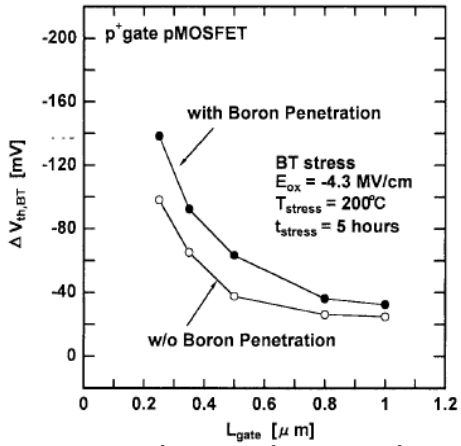
Nitridation of the gate oxides



FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

Boron penetration

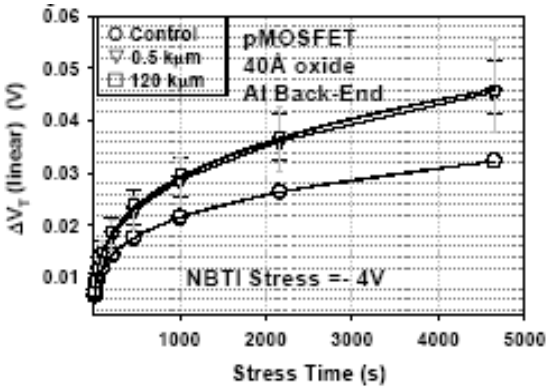


T. Yamamoto, et. al, Trans. Electron Devices, May 1999

FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

Plasma damage effects

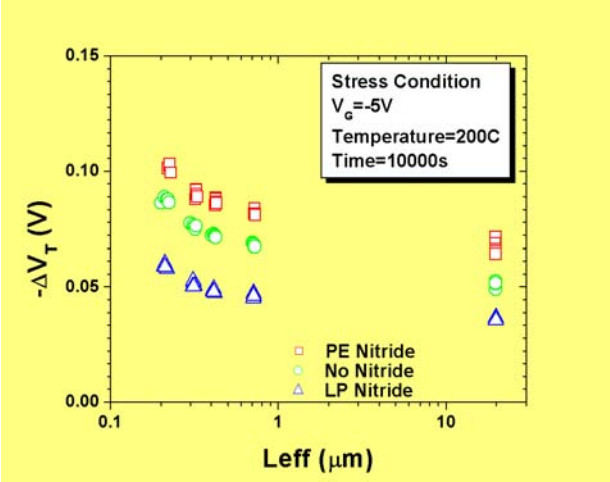


A. Krishnan, et. al, International Electron Device Meeting, 2001

FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

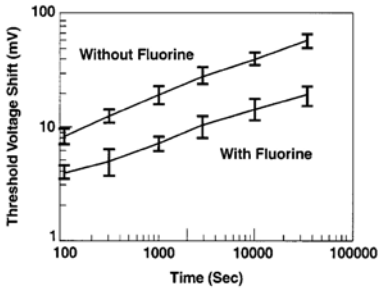
Barrier nitride (passivation)



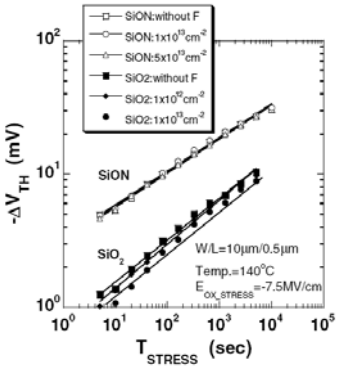
FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

Fluorine effects



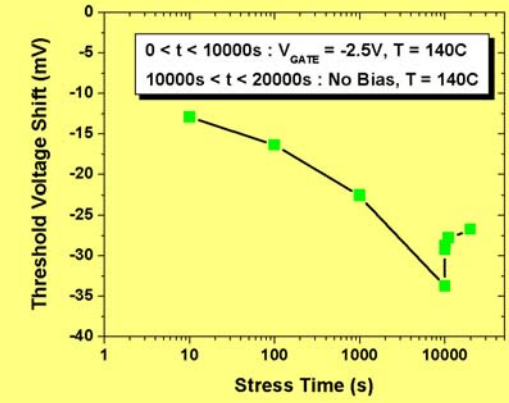
Adding fluorine to oxide reduces NBTI , T. Hook, et. al, Trans. Electron Devices, July 2001



However, the benefit of adding fluorine to nitrided oxides is diminished , Y. Mitani, IEDM, December 2002

FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)
- **Two relaxation mechanisms observed w/PMOS devices**
  - **Thermal relaxation (no bias applied)**
  - **Voltage and temperature induced relaxation**



FEOL WEAROUT MECHANISMS

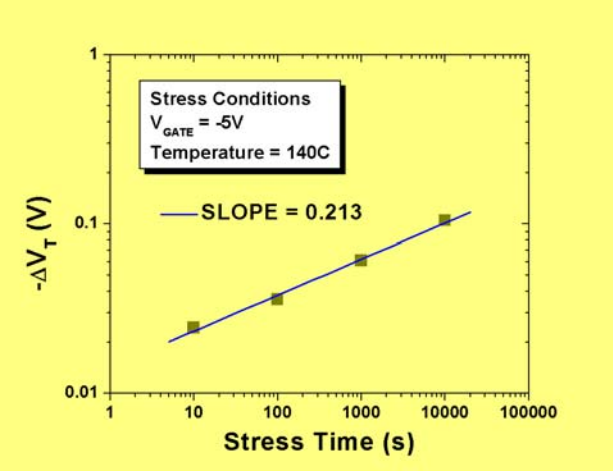
- NBTI (Negative Bias Temperature Instability)

- Modeling NBTI
  - Parametric degradation (i.e. V_t, $I_{DSAT)}$ exhibits power law dependence with time ➔ proportional to approx. $t^{0.25}$
  - Traditional DC stressing ➔ rapid degradation of transistor parameters
  - However, with AC stress (as it is during normal, frequency-dependent circuit operation), the degradation is at least partially recovered and lifetime is restored
    - The interface traps generated during the on state of the transistors are partially annealed during their off state.
  - For this reason, reliability engineers have come to realize that DC stress testing, where the transistor is always on, grossly underestimates device lifetime

FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

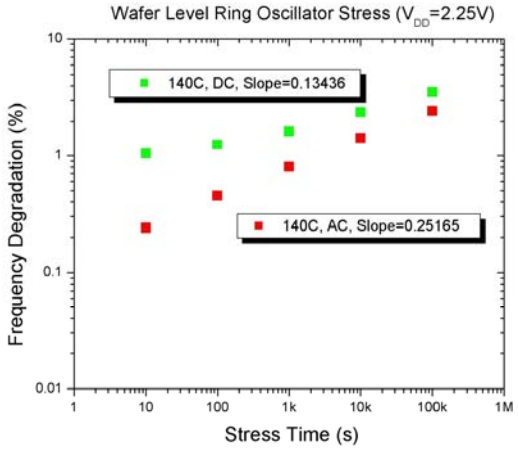
Parametric shift (i.e. V_T, I_{DSAT}) proportional to approximately $t^{0.25}$



FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

"AC" stress degradation less than "DC"



FEOL WEAROUT MECHANISMS

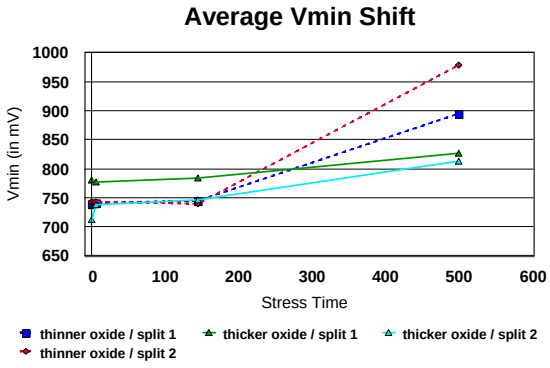
- NBTI (Negative Bias Temperature Instability)

- Why do we suspect NBTI when we see shifts in product Vmin (lowest voltage at which a product functions) or frequency shifts when we run accelerated stresses?

FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

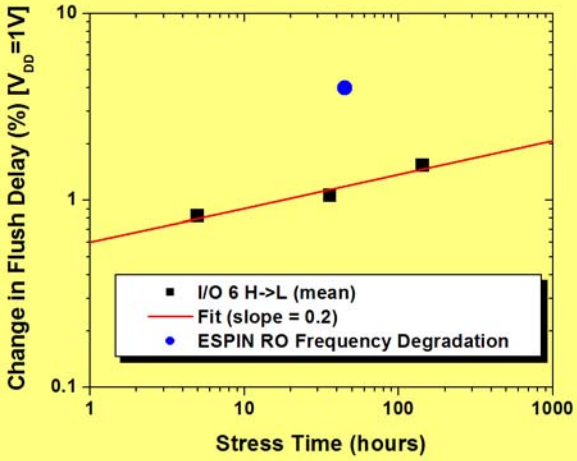
MINIMUM OPERATION VOLTAGE SHIFT



FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

DELAY AND FREQUENCY SHIFT



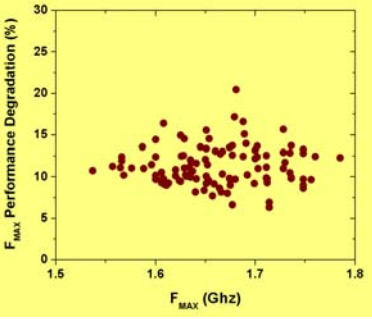
FEOL WEAROUT MECHANISMS

- NBTI (Negative Bias Temperature Instability)

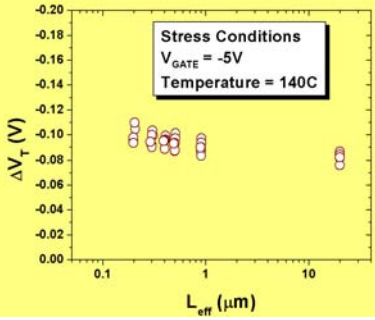
Why do we suspect NBTI?

1) Weak channel length (speed) dependence

Product



PMOS

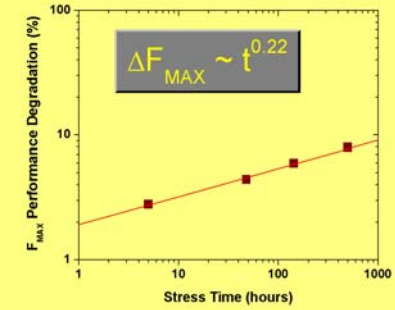


FEOL WEAROUT MECHANISMS

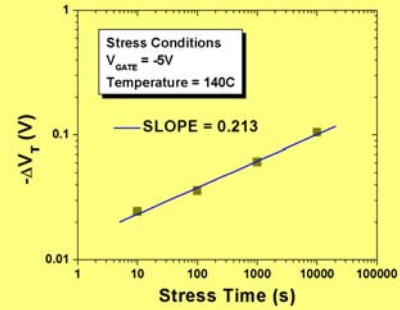
- NBTI (Negative Bias Temperature Instability)

2) Power-law time dependence approximately 0.2 - 0.25

Product



PMOS

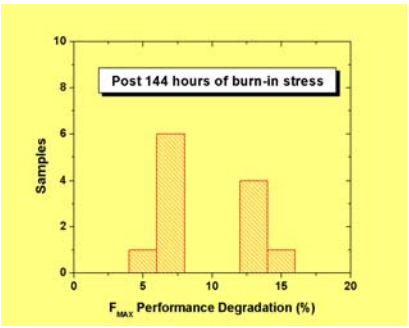


FEOL WEAROUT MECHANISMS

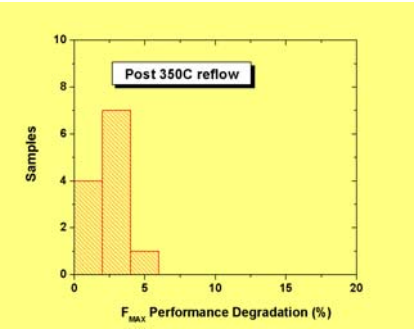
- NBTI (Negative Bias Temperature Instability)

3) Recovery with un-biased anneal

Product (post HTOL stress)



Product (post anneal)



FEOL WEAROUT MECHANISMS

- **NBTI (Negative Bias Temperature Instability**
- Circuit design options are limited to control NBTI
- Must understand the behavior of NBTI with your process and control with product operation window and guardbands
- Must control power supply tolerances (use and stress)

FEOL WEAROUT MECHANISMS

- **Hot Carriers – Why Do We Care?**
- Is accelerated by high voltage / high temperature conditions like BI or a qualification stress
- Duration at elevated conditions is important as the degradation goes by roughly the square root time
- I/O and power supply voltage control is important
- Non-conducting or "off-state" "hot e" is important during Burn-in or qualification stressing
- "Hot e" normally occurs during switching, so the less than functional speed stress oven conditions reduce degradation

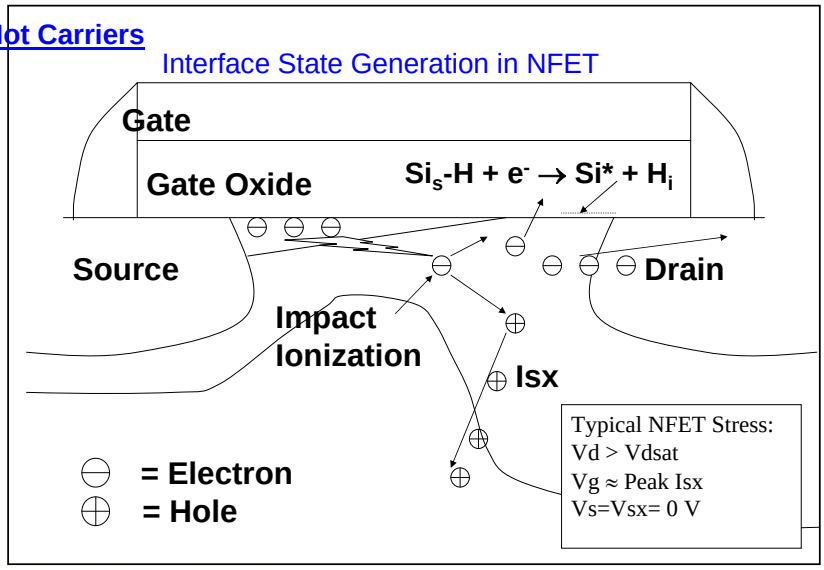
FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- Are Holes and/or Electrons that gain enough energy to cause a change in MOSFET electrical characteristics
  - Can alter circuit timing or function
- Channel length dependent
- Physical Mechanism
  - Large electric field near drain
  - Channel carriers accelerate to high energies
  - Causes interface-state generation, electron trapping/detrapping, and Hole trapping/detrapping
  - probably caused by the Electron breaking a Silicon-Hydrogen bond at the Si-SiO_2 Interface
    - If the Silicon and Hydrogen recombine, no interface trap is created
    - If the Hydrogen diffuses away, an interface trap is created

FEOL WEAROUT MECHANISMS

- **Hot Carriers**



FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- End of Life circuit effects
  - Increased propagation delay in rising edge of clock
  - Decreased propagation delay in falling edge of clock
  - For string of inverter like circuits
    - Net increase in delay➔Decrease in Max circuit/chip operating frequency (Fmax)
  - For register to register Logic circuits
    - Simulation of all circuits impractical
    - Path with longest delay (minimum clock margin) is the "Critical Path"
    - Assumes critical path a time=0 remains critical path at end of life
    - Try and simulate all basic logic blocks for shifts
    - Provide adequate timing margin and perform performance screens

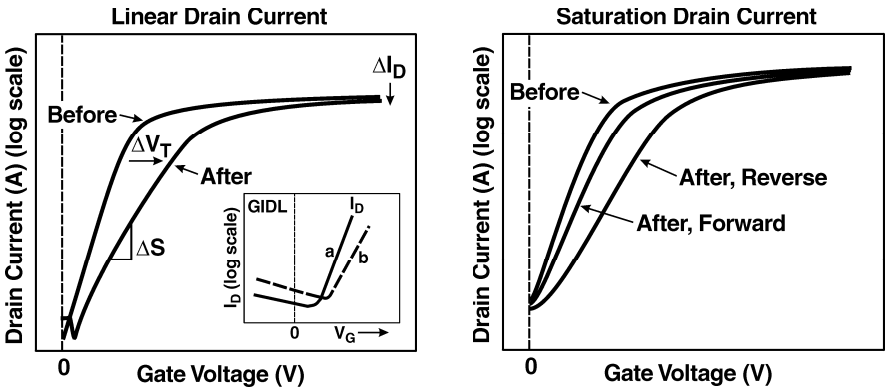
FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- End of Life circuit effects
  - For SRAM type circuits
    - Self timed circuits have increase in internal circuit delays resulting in increased access time
    - Susceptible to cell stability issues
    - Read or write fails
    - Asymmetric stress from frequent read of static data
    - Series resistance changes from blocked implant defects

FEOL WEAROUT MECHANISMS

- Hot Carriers



FEOL WEAROUT MECHANISMS

- Hot Carriers

- Reliability Prediction Model is a function of
  - the rate of bond breakage and rate of Si and H recombination
  - DC device stress vs. chip lifetime
    - Stress occurs in typical static CMOS logic circuits only during switching transients

FEOL WEAROUT MECHANISMS

- Hot Carriers

- Factors that influence lifetime
  - Reduce Isub / Id ratio
    - Reduce Vds
    - Drain engineering
  - Improve Si-SiO2 Interface quality
    - Intrinsic properties
    - "Harden" interface

FEOL WEAROUT MECHANISMS

- Hot Carriers

- Reduce Vds options
  - Operate at lower Vdd ➔ Impractical due to reduced performance
  - Better control and tolerance on power supplies
    - Use a lower nominal voltage
      - 5% power supply tolerance
      - Shift nominal point down 5%
      - Maintains same worst case Vddmin
      - 10X better lifetime that 10% power supply
  - Stack devices ➔Splits voltage across multiple devices
    - However, performance and area penalties
    - Can improve lifetime by 3-5 orders of magnitude

FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- Drain engineering options
  - Graded junction
    - Reduces Isub/Id by reducing peak electric field
    - Many methods
      - Double diffused drain
      - Lightly doped drain
      - Gate overlapped drain
    - Can result in reduced circuit performance due to higher series resistance and/or higher overlap capacitance
    - Can lead to severe shifts in series resistance due to hot carriers

FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- Improve Si-SiO2 interface options
  - Enhance Intrinsic properties➔ Minimize the number of Si-H precursors
    - Affected by
      - Oxidation conditions
      - Plasma, charging damage
      - Water related species
  - Interface "hardening"
    - Reduces probability of generating interface states
    - Incorporate Nitrogen at the Si-SiO2 interface
      - Can have undesired effects on device parametrics
    - Replace Hydrogen with Deuterium
      - Potential for >100X lifetime improvement
      - No direct impact of device electrical characteristics

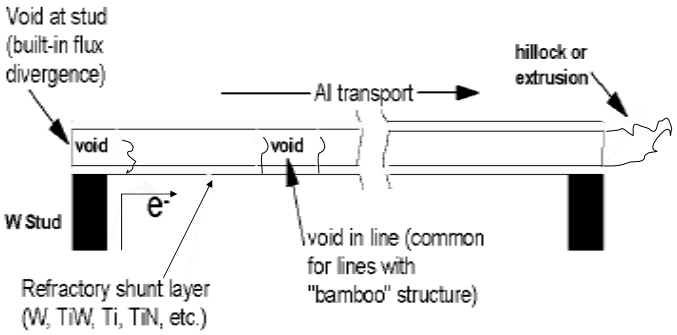
FEOL WEAROUT MECHANISMS

- **Hot Carriers**

- Product Design strategy
  - Simulate all basic Logic blocks for shift for the range of
    - Application corners (V and T)
    - Process corners (Long/Short Leff)
    - Rise/fall times
  - Modify design to keep delay shifts within specified range
    - Provide adequate timing margin
    - Incorporating delay shifts into timing tools
  - Perform Performance screening on product

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**



- Atomic transport caused by electron "wind"
- Voids and hillocks form at flux divergence sites
- Failure occurs by open circuit or resistance increase
- Accelerated testing performed at elevated temp. and current levels
- Data used to define current ground rules for each metal level

BEOL WEAROUT MECHANISMS

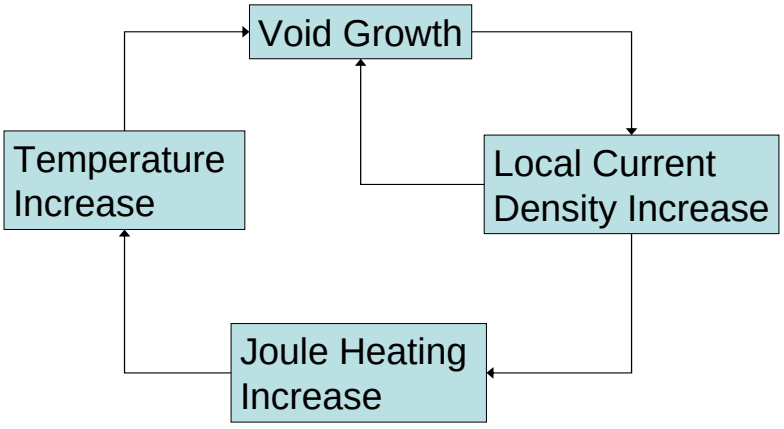
- **Electromigration (EM)**

- Metallization microstructure, current density in the line, interfacial integrity, and chip operating temperature influence the rate of EM
- Fails are due to
  - Open line (void)
  - Short to neighboring line (extrusion)
  - Resistance increase (e.g., 20%) – circuit timing
- Once the EM process starts, the damage accelerates due to localized increase in temperature due to current crowding
  - The presence of a void causes the current density to increase in the vicinity around itself because it reduces the cross sectional area of the conductor
  - The whole process continues until the void is large enough to break the line

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

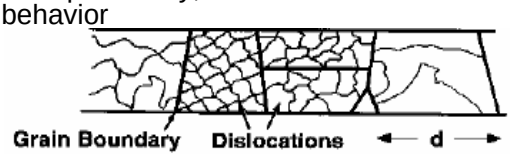
THERMAL ACCELERATION DURING VOID GROWTH



BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

- As mentioned previously, metalization microstructure plays a role in EM behavior



- Uniform lattice structures➔ hardly any momentum transfer between the conduction electrons and the metal ions.
- Lattice order is disrupted at grain boundaries and material interfaces➔ leads to more effective momentum transfer at these locations
  - Vacancies are more frequent, and metal ions in these areas are bonded more weakly enabling atomic transport along the boundaries in the direction of the electron wind.
- Atomic transport is the result of grain boundary, bulk, and surface diffusion.

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

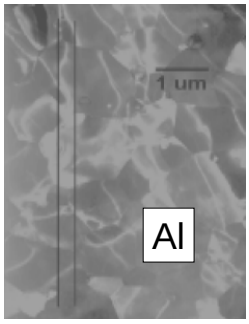
- Size of grains = width of line ➔ bamboo structure, retards EM
  - This confines mass transport mostly to interfacial diffusion, thereby reducing the atomic flux and electromigration failure rate.

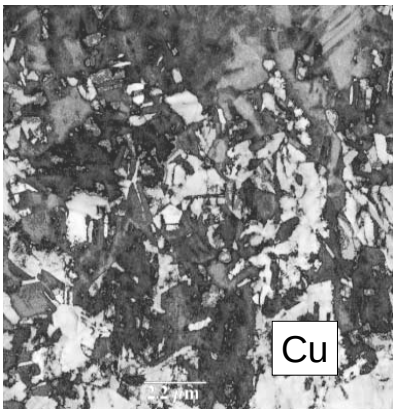
- Small Grains (d<W)

- Large Grains (d>W: Bamboo Structure)

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**



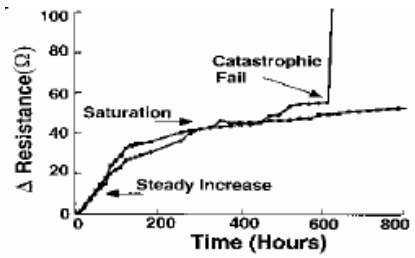


- **Narrower distribution in grain size**
- **Grain boundary diffusion**
- **Wide range of grain sizes, shapes**

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

- AlCu was basic material used for interconnects for a long time.
  - EM more influenced by grain boundary diffusion
  - Had incubation time / delay before void growth started (due to Cu precipitates)

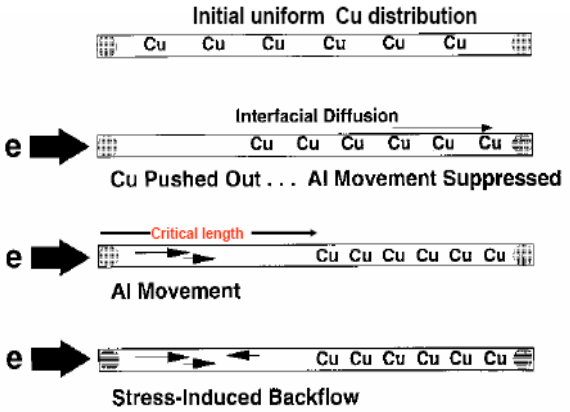


  - Considerable volume needed to cause extrusion short
  - Tight distribution of failures compared to Cu
  - More heating in upper layer of metal
    - More risk for damage due to electrical overload

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

Failure Dynamics in AlCu (incubation time)



Critical length = length below which EM does not occur (Blech length)

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

- Cu provided superior "delays" when compared to AlCu (wiring limitations were hampering circuit performance).
- Became widely used once "device poisoning" solutions developed
  - Cu/cap interface is primary EM diffusion path
- Improved EM performance due to superior electrical and thermal conductivity and higher melting point
- However, some of that advantage lost with
  - greater width of failure distribution ➔larger fraction of failures prior to the targeted EOL
  - No incubation time ➔reduces EM advantage as temp. rises
  - Weak interfaces ➔ more susceptible to extrusion failure
  - Use of lower dielectric constant interlevel insulators has influenced EM performance
    - much lower thermal conductivity
    - More heating in upper layer of metal
    - More risk for damage due to electrical overload

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

- Accelerated stressing (increased temperature and current density) is employed to study the behavior.
  - Factors are established so that the data can be related to use conditions using a LogNormal Distribution assumption

- Failure rate is modeled using Black's Equation:

$$t_{50} = CJ^{-n}e^{(Ea/kT)}$$

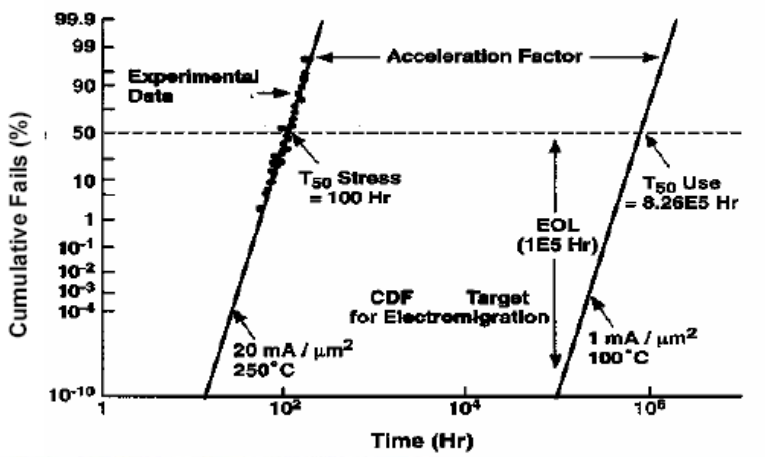
where:

t_{50} = the median lifetime of tested lines
C = a constant based on metal line properties
J = current density
n = current density exponent with value between 1 and 2
T = temperature in deg K
k = Boltzmann's constant
Ea = activation energy = 0.5 - 0.7 eV for pure Al

BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**

Bridge to Use Conditions

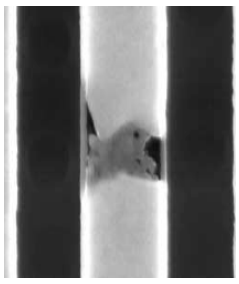


BEOL WEAROUT MECHANISMS

- **Electromigration (EM)**
- In the design of the technology/product
- Particular attention must be paid to vias and contact holes
  - Current crowding occurs above and below W vias and in Cu
  - Multiple vias are often used to compensate - organized such that the resulting current flow is distributed evenly over all the vias.
- Electromigration can be prevented by
  - proper device design to equilibrate and limit current densities in all parts of the circuit
  - increasing of the grain sizes of the metal lines such that these become comparable to their widths (whereby bamboo structure is achieved)
  - good selection and deposition of the passivation or thin films placed over the metal lines in order to limit extrusions caused by electromigration.

BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**



- High hydrostatic tensile strain
  - In Al, due to thermal expansion mismatch between Al and SiO2 produces high strain energy at operation temperature
  - In Cu due to microstructural evolution during thermal processing
- Metal seeks to reduce its strain energy by relaxation ➔ voids
- Unconstrained Al Shrinks with temperature decrease
  - Passivated Al prevented from shrinking

BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**

- Cu "pluses"
  - Higher resistance to stress migration vs Al
  - Lower resistance, smaller lines with same current carrying capability ➔ circuits can be packed closer together
- Cu "minuses"
  - High diffusivity through dielectrics
    - Must be encapsulated in a barrier film (usually a derivative of Ta or Ti) to prevent copper from diffusing into transistors
  - Denser circuits➔ extra parasitic capacitance ➔ use of lower dielectric constant dielectrics
    - The spin-on-coat process of low-k dielectric material requires furnace annealing to cure the film
    - Microstructural changes in Cu occur that increase the tensile strain in the Cu lines ➔ can lead to stress induced voiding during chip operation
    - Voids increase the resistance➔ lead to chip failure.

BEOL WEAROUT MECHANISMS

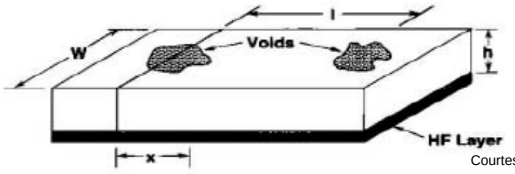
- **Stress Induced Voiding**

- Modeling the behavior is a multi-part process
  - Need a model for void growth
  - Need the thermal dependence
  - Need the stress dependence
  - Need acceleration factors
  - Need resistance measurements
  - Need the effect of microstructure

BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**

- Void growth model
  - metal line w wide, h thick
  - refractory underlayer
  - 2 small voids l apart, along x-direction



Courtesy of Tim Sullivan, IBM

- Need
  - Void volume
  - Distribution of separation between voids
  - Distribution of void sizes

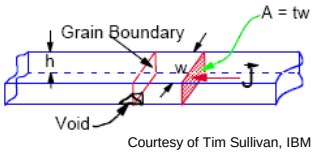
BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**

- Void volume is described by

For Randomly Spaced Voids with Average Separation = $\bar{\ell}$

$$V(t) = 3\varepsilon_0 wh\bar{\ell}\ S(z) = \bar{V}_t\ S(z)$$



Courtesy of Tim Sullivan, IBM

- Distribution of separation between voids
  - Assume exponential distribution

    $P(l) = 1/l_m\ (e^{-l/l_m})$

    where l_m = mean void separation

- Distribution of void sizes

  $\mu(t) = \lambda_f M(Z_m)$

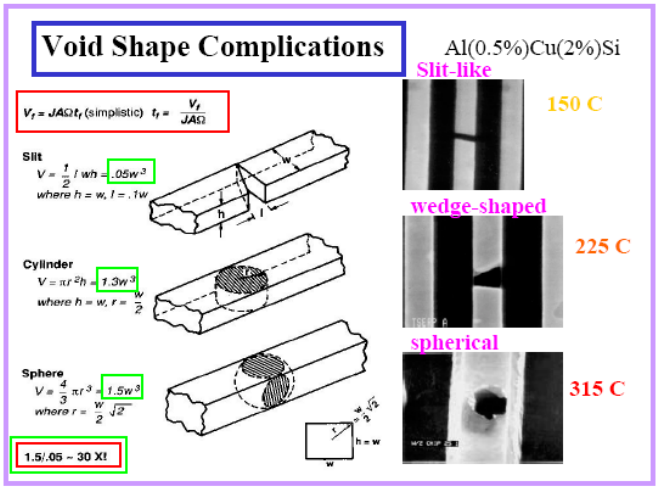
BEOL WEAROUT MECHANISMS

- Stress Induced Voiding

- What happens if you have different void shapes????
  - Could be off up to 30X in volume

BEOL WEAROUT MECHANISMS

- Stress Induced Voiding

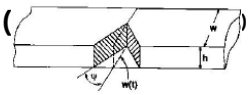


Courtesy of Tim Sullivan, IBM

BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**
  - Need the thermal dependence

$$T_{fails} = (\quad) (1/\Delta T^2)(e^{\Delta heff/kT})$$



  - Need the stress dependence

$$(N_v = N_0\, e^{-\Delta hf/kT}\ ;\ D = A\, N_v\, e^{-\Delta ht/kT})$$

  - Need acceleration factors

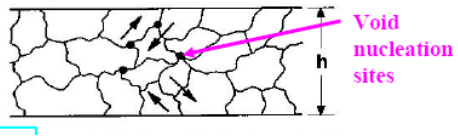
$$AF = \left(\frac{\Delta T_s}{\Delta T_u}\right)^2 e^{\frac{-\Delta h_{eff}}{k}\left(\frac{1}{T_s}-\frac{1}{T_u}\right)}$$

  - Need resistance measurements – taken empirically

BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**

- Need the effect of microstructure
  - For small grains (d<h-metal thickness)
    - Grain boundary cracking/sliding <- rate limiting
      - Acts quickly at lower temperatures
      - Candidate mechanism for void nucleation sites

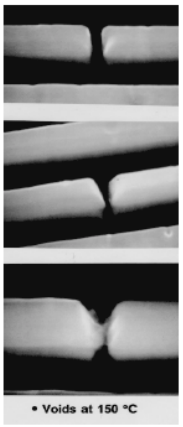


    - Plastic Flow (dislocation generation and motion)
    - Diffusion (grain boundary and lattice)
      - Void growth through grain boundary diffusion

BEOL WEAROUT MECHANISMS

- Stress Induced Voiding

Void shape and failure time



t_f=500 hr

t_f=1250 hr

t_f=2196 hr

- All three voids are wedge-shaped
- All three taken off stress together
  - Same wafer, same temperature
  - Separation betw. Line ends represents time since failure
- Volume is similar for all three

Distribution in grain orientation at boundaries where voids nucleate accounts for much variation in failure time.

Courtesy of Tim Sullivan, IBM

BEOL WEAROUT MECHANISMS

- Stress Induced Voiding

- Other considerations –
  - Passivation effects➔ Thickness, Bending
  - Alloy composition
  - Local Environment

BEOL WEAROUT MECHANISMS

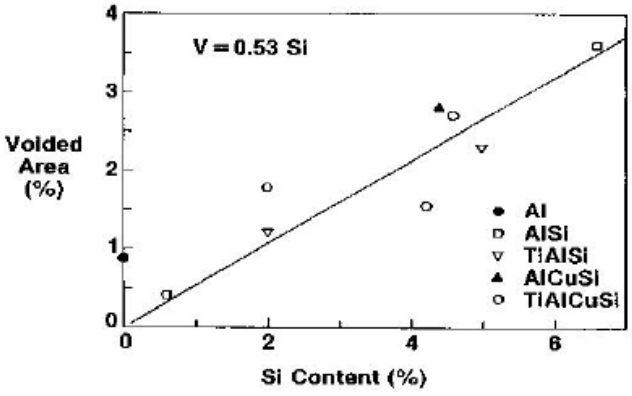
- **Stress Induced Voiding**
- Passivation effects
  - Percent fallout after stress

Temperature	Passivation Thickness (μm)		
	0.25	0.5	3.0
150	2	1	82
225	0	0.6	92
285	86	36	46
315	97	98	100

0.6 μm, Al(Cu,Si), SiN Passivation

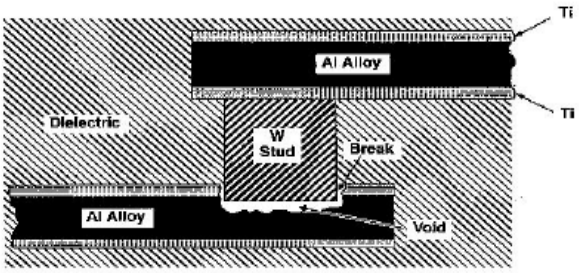
BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**
- Alloy composition



BEOL WEAROUT MECHANISMS

- **Stress Induced Voiding**
- Local Environment



- **Local Stress Risers = W stud**
  - $W_{TCE} > \alpha SiO_2$
  - $E_W > E_{SiO_2}$
  - **Hot W Deposition**
- **Preferential Void Nucleation**

BEOL WEAROUT MECHANISMS

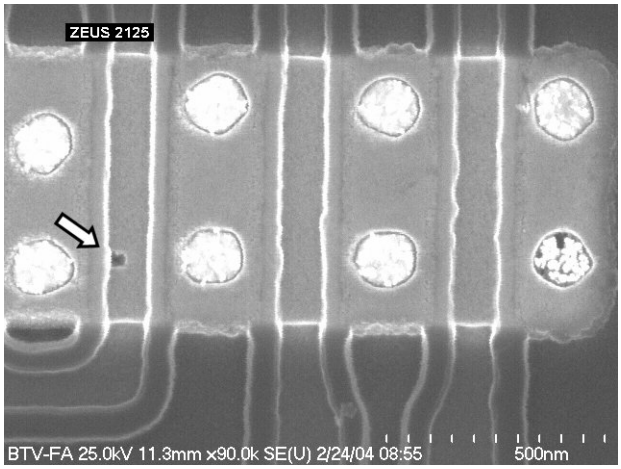
- **ILD TDDB (Inter-level Dielectric Time Dependent Dielectric Breakdown)**

- A lot of the same issues / concerns as gate oxide breakdown

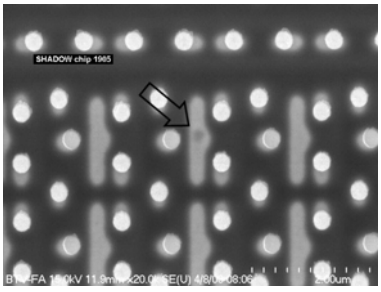
EXAMPLES OF RANDOM and SYSTEMATIC DEFECTS

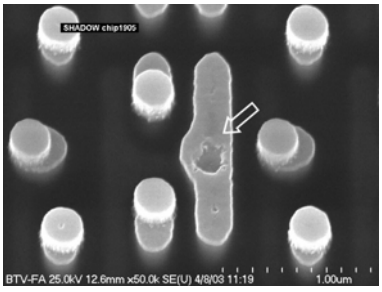
- Gate Oxide defect
- PC level defect
- FM causing MC-MC short
- NFET Vt mismatch due to FM blocking implants
- High resistance contact
- M1 Short due to Tungsten “Puddle”
- BEOL scratches causing short

GATE OXIDE DEFECT

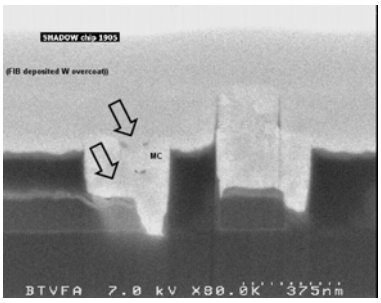


PC LEVEL DEFECT

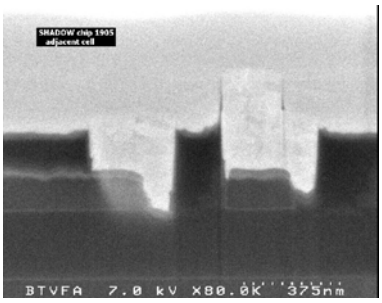




PC DEFECT (con't)

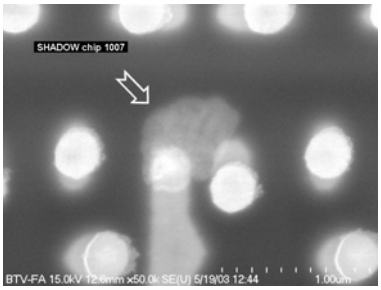


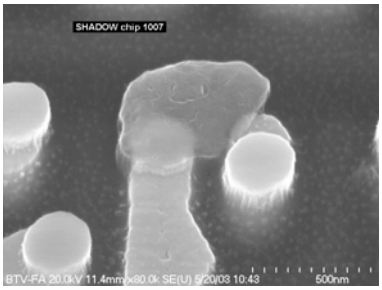
Failing chip



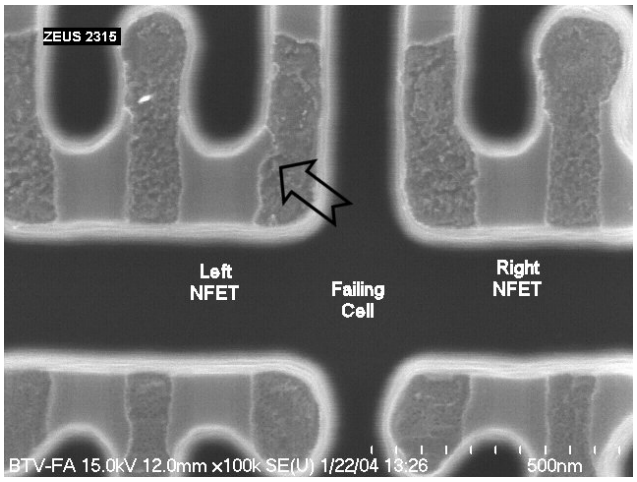
Good chip

FM CAUSING MC-MC SHORT

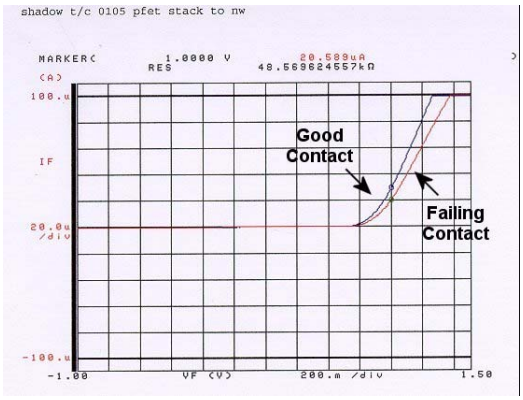




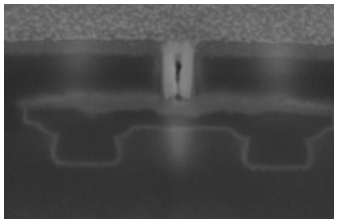
NFET Vt MISMATCH DUE TO FM BLOCKING IMPLANTS



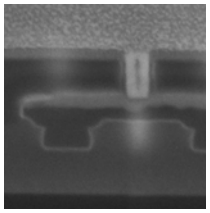
HIGH RESISTANCE CONTACT



HIGH RESISTANCE CONTACT (con't)

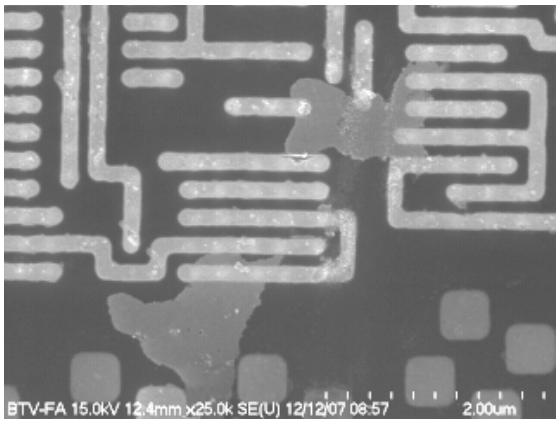


Bad contact

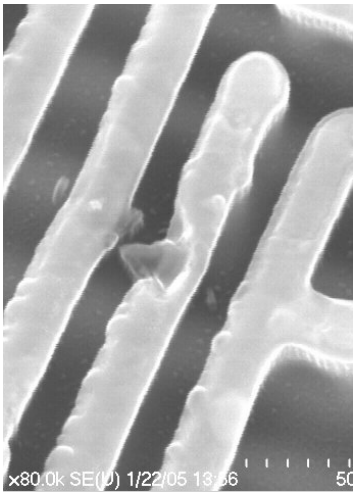


Good contact

M1 SHORT DUE TO TUNGSTEN "PUDDLE"



BEOL SCRATCHES CAUSING SHORT



RELIABILITY STRESSING/MODEL

- Qualification Cycle
- Reliability "Categories“
  - “Technology” RE mechanisms
  - “Defect” / ”Product” RE mechanisms
- Building a Reliability Model
  - Product Stress Profiles/Measurements
  - Effects of Screens
- Reliability Modeling
  - FITs, Chi-Squared, etc.

BUILDING A RELIABLITY MODEL

- **Need:**
  - **Defect distribution in time (Weibull)**
  - **Acceleration factors**
  - **Effect of screening**

DEFECT DISTRIBUTION IN TIME

- **Weibull Expression**

$$F_V(T,V,t) = 1 - e^{[\alpha_V t]^{\beta}}$$

For small F,

$$F_V(T,V,t) = \alpha_V t^{\beta}$$

Where α_V = a constant
t = time
β = Approximately 0.2 (usually empirically derived)

ACCELERATION FACTORS

- **Temperature Acceleration**

$$A_T = e^{[\Delta_H /k((1/Tuse) - (1/Tstress))]}$$

Where Δ_H = a constant (usually empirically derived)
k = Boltzmann's Constant
T is in degrees Kelvin

- **Voltage Acceleration**

$$A_V = e^{[\chi_V (V_{stress} - Vuse)]} \quad \text{OR}$$

$$A_V = (V_{stress}/V_{use})^2$$

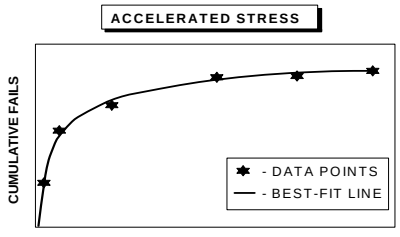
Where χV = a constant (usually empirically derived)

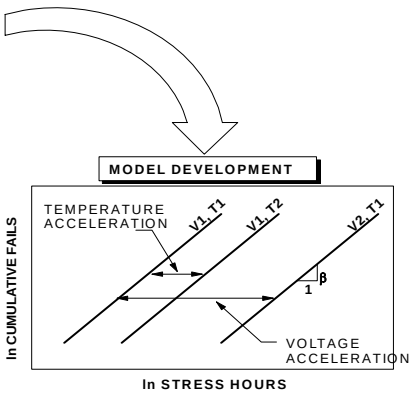
ACCELERATION FACTORS

- **Thermal Cycle Acceleration**

$$A_c = (\Delta T_{stress}/\Delta T_{use})^4$$

EMPIRICALLY DERIVING ACCELERATION FACTORS





- o NO-BURN-IN DEVICES
- o CUM. FAILS = α (HOURS)$^{\beta}$
- o DEVELOP V, T ACCELERATION FACTORS
- o DEFINE/VALIDATE BURN-IN CONDITIONS
- o VERIFY NO WEAROUT
- o PREDICT USE FAILURE RATES

"POPULAR" STRESS PROFILES

- **"3-CELL"**
  - Used to determine acceleration factor constant(s)
  - 3 "cells" with only one parameter (temperature or voltage) varied between any 2 cells
    - Cell 1 - Voltage 1 (V1) / Temperature 1 (T1)
    - Cell 2 - Voltage 1 (V1) / Temperature 2 (T2)
    - Cell 3 - Voltage 2 (V2) / Temperature 1 (T1)
- **"STEP"**
  - Acceleration factors known / assumed
  - Start with lower conditions first to guard against "surprises" & then "step" to higher conditions
- **"HIGH CELL"**
  - Acceleration factors known / assumed
  - Stress run at "high" conditions

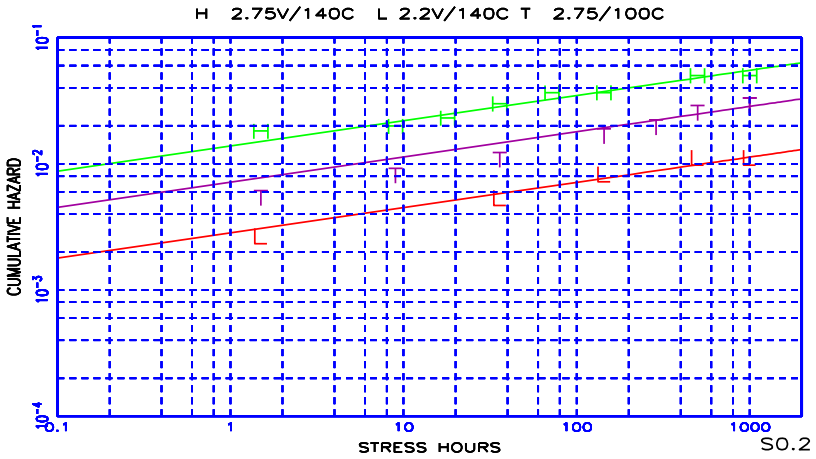
STRESS SAMPLE SIZE "RULE of THUMB"

- The following assumes you are "king of the world":
- **"3-CELL"** - expect at least 10 fails in each cell

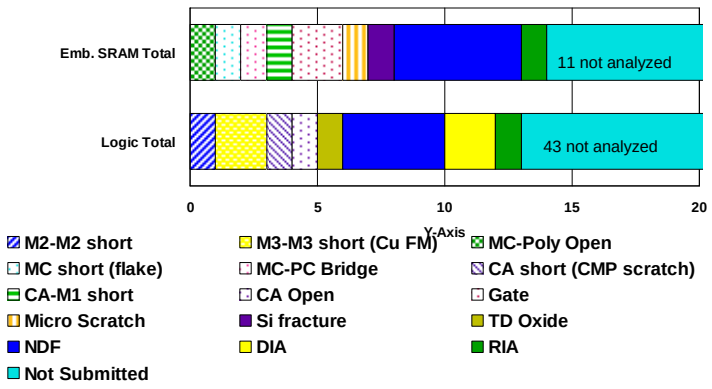
	T1	T2 > T1
V2 > V1	1/3 s/s	1/6 s/s
V1	1/2 s/s	

- **"STEP" / "HIGH CELL"** - expect 10 fails in the high step portion

TEMPERATURE/VOLTAGE MODELING



FA RESULTS



"COMPOSITE" vs. "BY DEFECT" MODEL

- **COMPOSITE**
  - Acceleration factors derived from the mix of defects
  - Needs less stress samples to accomplish
- **BY DEFECT**
  - Acceleration factors are derived for each mechanism
  - Requires a LOT more stress samples to get enough fails of each mechanism and to determine proportion of each mechanism in the sample
  - Once parameters are determined, just end up adding all the mechanisms together to derive overall behavior anyway

BUILDING A RELIABLITY MODEL

- **Have:**
  - Defect distribution in time (Weibull)
  - Acceleration factors
- **Need:**
  - Effect of screening

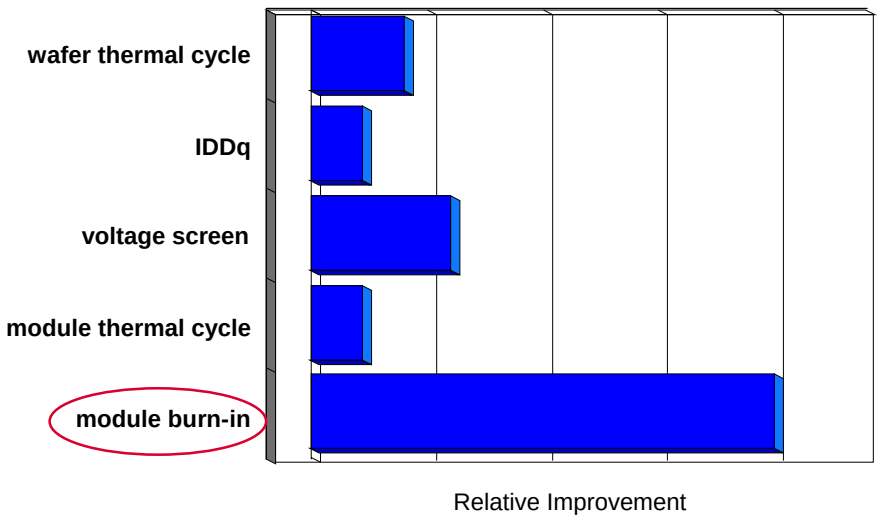
MANUFACTURING RELIABILITY SCREENS

- Burn-in
- Voltage Screens
  - Enhanced Voltage Screen (EVS)
  - Dynamic Voltage Screen (DVS)
- Thermal Cycle
- Iddq/Other
- Maverick Screens

RELIABILITY SCREENS EFFECTIVENESS SUMMARY

SCREEN	RELATIVELY EFFECTIVE	RELIATIVELY INEFFECTIVE
BURN-IN & VOLTAGE SCREEN	▪ ELECTRICAL SHORTS	▪ METAL OPENS ▪ FM OPENS ▪ ELECTROMIGRATION OPENS ▪ BLOCKED CONTACTS
THERMAL CYCLE	▪ Mx SEAMS ▪ FM OPENS	▪ ELECTRICAL SHORTS ▪ ELECTROMIGRATION OPENS ▪ BLOCKED CONTACTS
MAVERICK SCREEN	▪ BLOCKED CONTACTS ▪ POTENTIAL FOR ALL DEFECT TYPES	

RELIABILITY SCREENS RELATIVE IMPROVEMENT



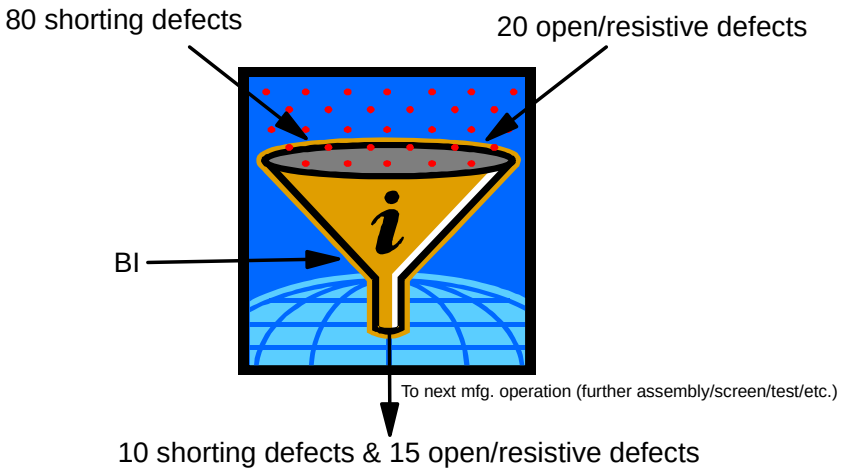
BURN-IN SCREENS

- Screens such as burn-in count on:
  - Having devices with defects that the screen can accelerate
  - Acceleration over use conditions
  - Being efficient
  - Being "perfect"

DEFECT ACCELERATION

- Not all defect types accelerate the same
  - Shorts - Very voltage accelerated
    - Example (2.5V/60C application):
    - 5hr/3.5V/140C BI = **83K** poh
  - Opens - Not as voltage accelerated
    - Example (2.5V/60C application):
    - 5hr/3.5V/140C BI = **1.1K** poh

EFFECT OF SCREENING ON DEFECT MIX



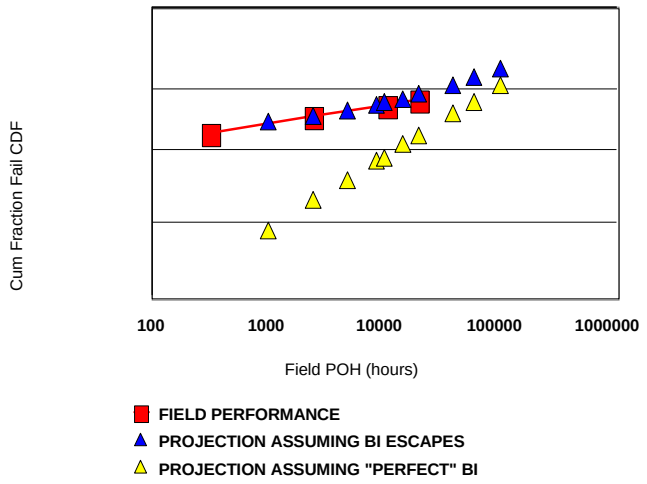
BURN-IN TYPES

- **STATIC**
  - DC bias, high temperature
  - High bipolar stress efficiency
  - 2X improvement
- **LIMITED MONITOR INSITU (a.k.a. "Dynamic")**
  - 1.5xVdd / 140C T**chip** (goal)
  - Functionally running w/expects (at least one output monitored)
  - Typically 10X improvement
- **INSITU**
  - 1.5xVdd / 140C T**chip** (goal)
  - Functionally running w/expects (all outputs monitored (goal))
  - Reduces "escapes" due to equipment and product
  - Identifies marginal, recoverable fails
  - Typically >30X improvement

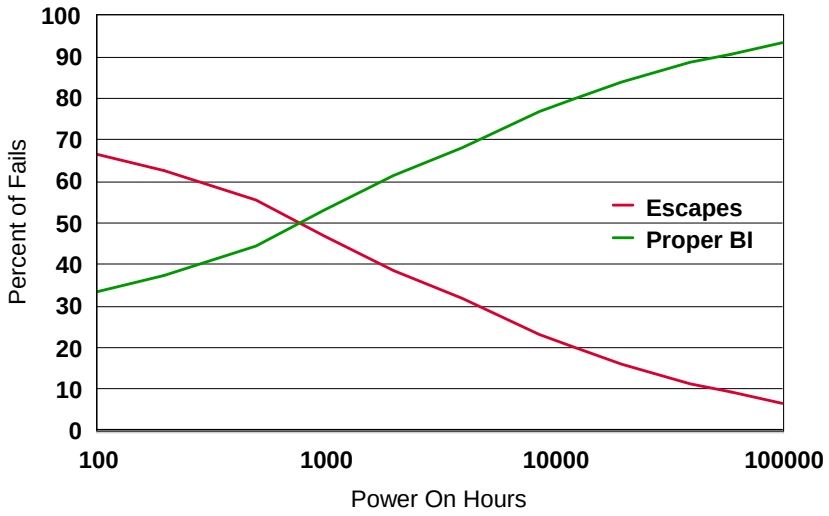
"TYPES" of BURN-IN "ESCAPES"

- **Pattern**
  - Insufficient stress patterns or circuit/electrical nodes not exercised/toggled
- **Functional**
  - Device not functional at Burn-in conditions
- **Recoverable**
  - Fails recover before tests are performed
- **Bias**
  - Defects not significantly accelerated by temperature and/or voltage
- **Operational**
  - Failure to apply required stress conditions (equipment/procedural/etc.)

FIELD PERFORMANCE vs. BURN-IN ESCAPE ASSUMPTION



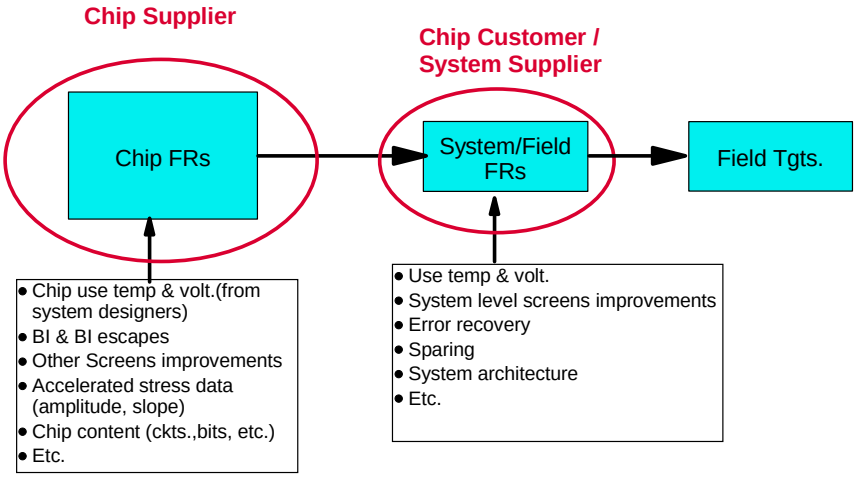
EFFECT OF BURN-IN ESCAPES ON FIELD PERFORMANCE



RELIABILITY STRESSING/MODEL

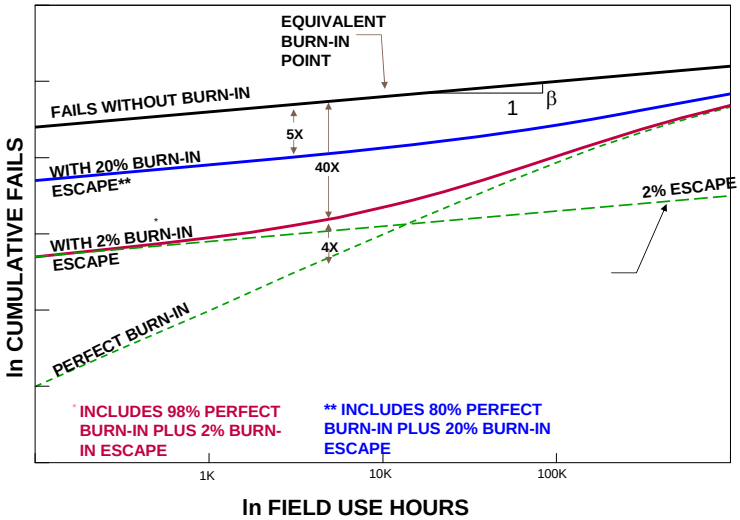
- Qualification Cycle
- Reliability "Categories“
  - “Technology” RE mechanisms
  - “Defect” / ”Product” RE mechanisms
- Building a Reliability Model
  - Product Stress Profiles/Measurements
  - Effects of Screens
- Reliability Modeling
  - FITs, Chi-Squared, etc.

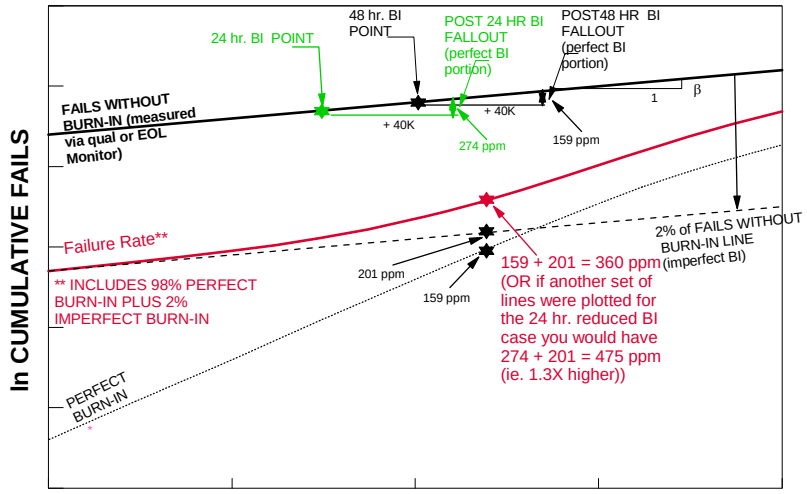
DEFECT BASED FAILURE RATES (Chip level to System level)



MODELLING

- **Have:**
  - Defect distribution in time (Weibull)
  - Acceleration factors
  - Effect of screening





FITs

- Fails In Time
- In units of ppm/KPOH (ie. a rate)
- Assumes a constant failure rate over a given time interval
- Not physically correct, but math is easy

Failure Rate Calculation using Chi Squared Exponential

- Assumes a **constant** failure rate....again, math is simple, physically not what is going on.
- The relationship between failure rate and the Chi Squared Distribution is as follows:

$$k = \xi^2(a,df) / (2t) = (\xi^2(a,df) \times 109) / ((2(dh))$$

where:

k = Failure Rate

t = time

dh = Device Hours representing equivalent use hours

= (s/s)(stress hours)(AF**T**)(AF**V**)

$\xi^2(a,df)$ = The Chi-Squared distribution for a given confidence interval (ξ^2 (a, df))

where:

a = The Chi-Squared confidence interval

df = Degrees of freedom (2r+2)

(r = Number of observed stress fails)

Failure Rate Calculation using Chi Squared Exponential (An Example)

- Given:

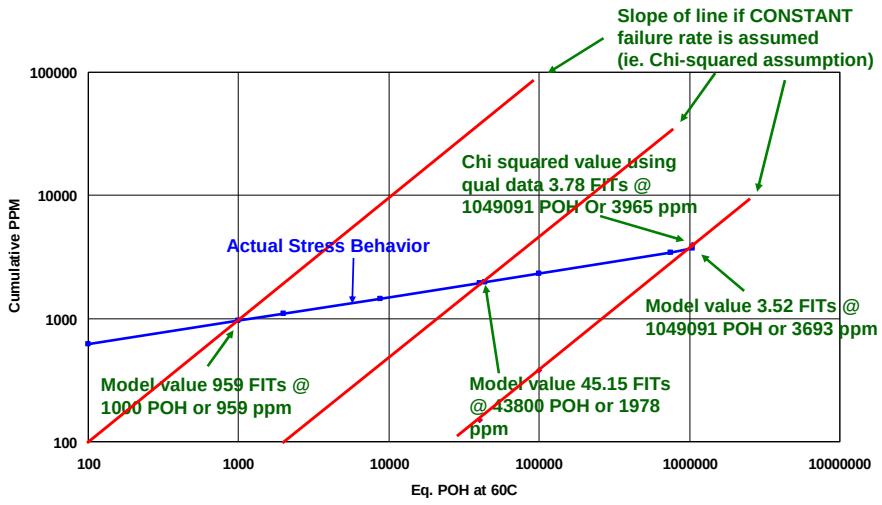
- 509 devices through functional stress
- Stress was at 5.1V, 140C, 5 hours and then 4.3V, 140C, 48 hours
- 1 fail was observed
- Use conditions of 3.3V, 60C
- DH = 0.7eV and cV = 4.0V-1
- Chi-Squared distribution with 60% confidence interval

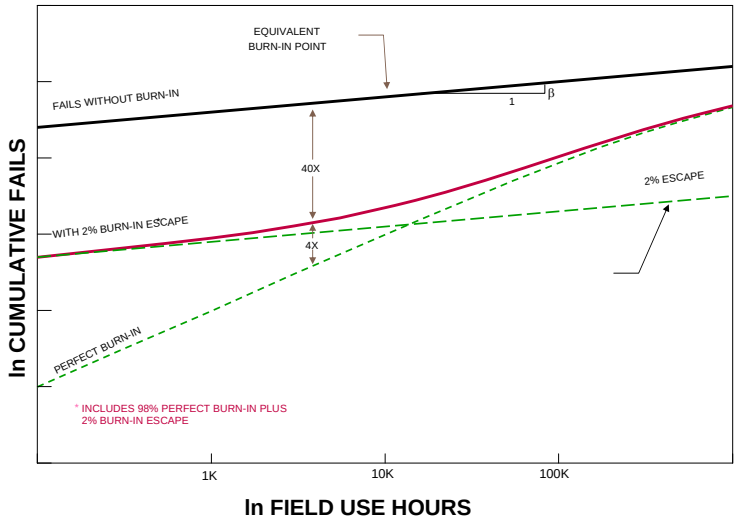
$$k = \xi^2(a,df) / (2t) = (\xi^2(60,4) \times 109) / ((2)[dh])$$

$$k = (4.04 \times 109) / (2[(509)(5)(1339.4)(112.6) + (509)(48)(54.69)(112.6)])$$

k = 3.78 FIT (over the POH interval 0 - 1.05M (end of stress))

"Model" vs. Chi-Squared Exponential





OUTLINE

- Reliability Stressing/Model
  - Qualification Cycle
  - Reliability "Categories“
    - “Technology” RE mechanisms
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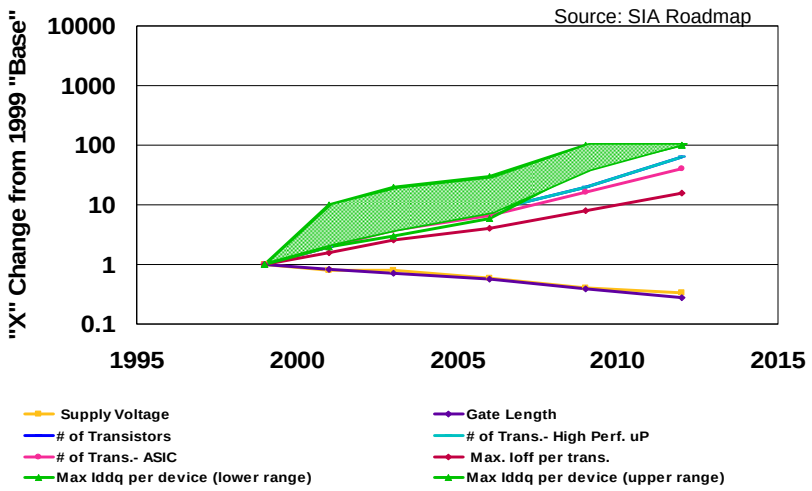
  - Reliability Modeling
    - FITs, Chi-Squared, etc.
- Manufacturing Screens
- Reliability Monitoring

MANUFACTURING RELIABILITY SCREENS

- Burn-in
- Voltage Screens
  - Enhanced Voltage Screen (EVS)
  - Dynamic Voltage Screen (DVS)
- Thermal Cycle
- Iddq/Other
- Maverick Screens

TRENDS



POWER, NOT JUST A QUALIFICATION OR END OF LINE MONITOR ISSUE

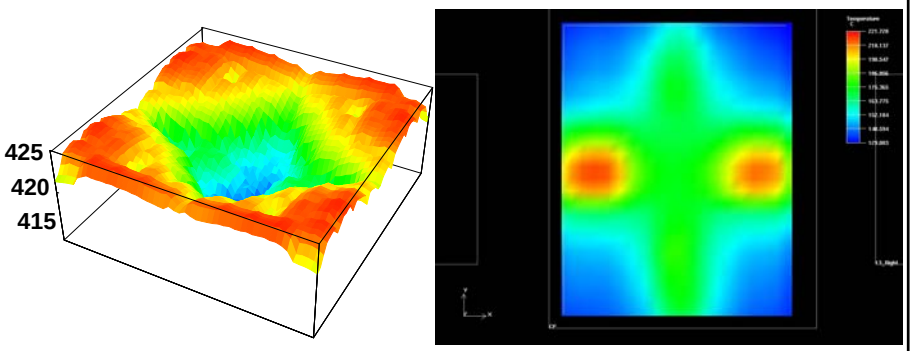
- "By 2007, many companies will be spending more on powering and cooling their data centers than on the technology they put into them. In 2000, power costs were only 5 to 10 percent of overall systems costs".

Bernie Meyerson, IBM Fellow, VP Strategic Alliances and Chief Technologist, STG

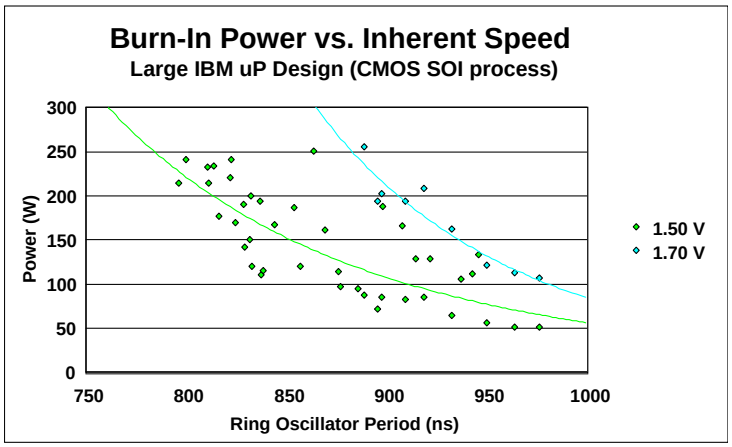
THE IMPACT OF POWER ON RE WORK

- Product RE's (and others) need to be
  - Familiar with technology RE issues
  - Familiar with tooling and product capabilities
- Tooling / product behavior directly impacts stress conditions achieved and therefore the "goodness" of the qual information and the "goodness" of the manufacturing screens

KNOW YOUR PRODUCT's POWER BEHAVIOR

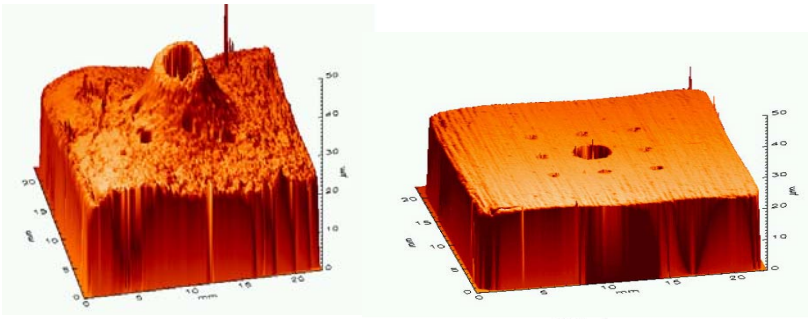


KNOW THE INFLUENCE OF MFG PROCESS



KNOW YOUR TOOLING/FIXTURING

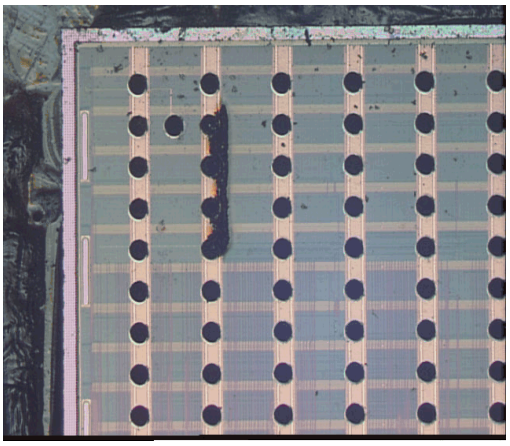
(CAN IMPACT STRESS CONDITIONS ACHIEVED)



3D view

Better Flatness Heatsink

OTHERWISE YOU END UP WITH THIS



OTHER CONCERNS

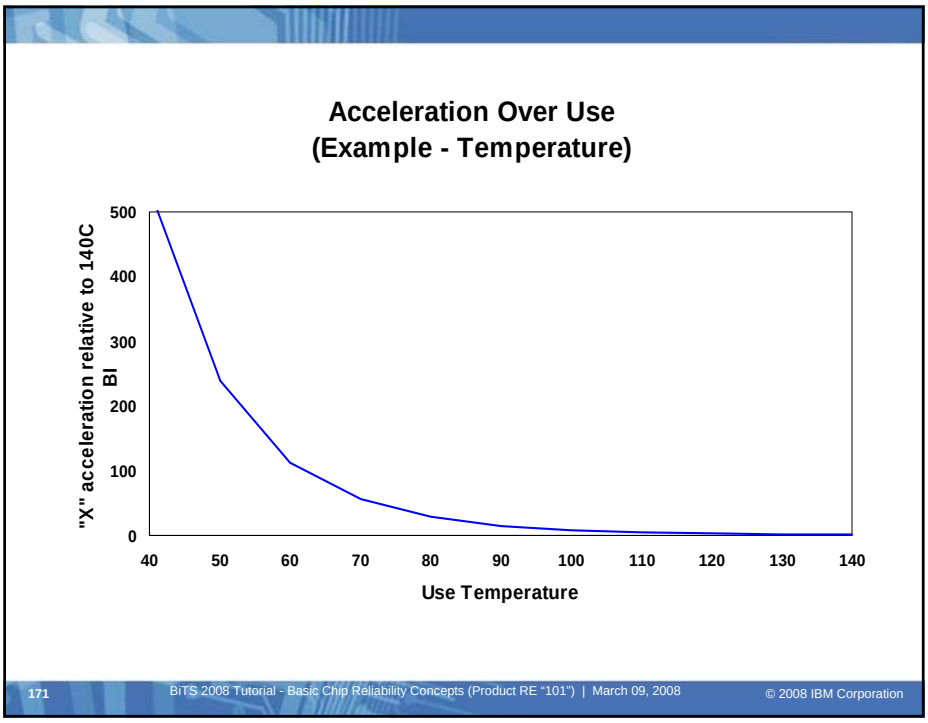
- Potential problems for Voltage Dependent Screens like Burn-in, Voltage Screen, Iddq
  - Less screenable defects
  - Loss of acceleration
  - Less efficient
  - Less "perfect"

DEFECT ACCELERATION

- To date, shorting mechanisms cause most fails
- Will trend be towards more open/resistive related fails?
  - New materials
  - More contacts/vias
  - Higher functional speeds
  - New circuit design techniques

APPLICATION TEMPERATURES

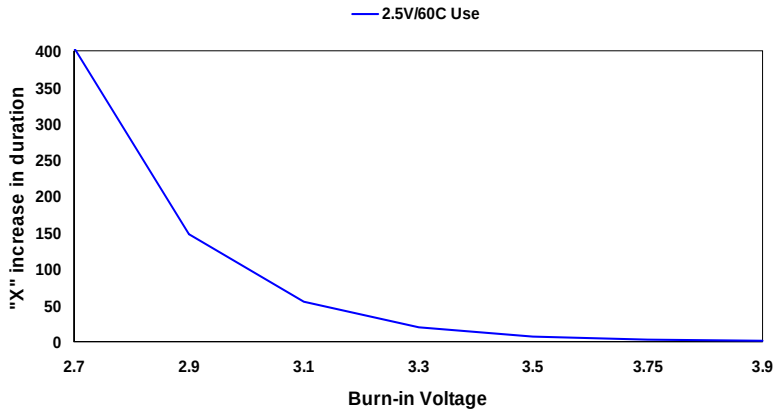
- Could climb over time due to
  - Cost cutting
  - Higher Ioff/more circuits per device
  - New materials



BURN-IN EFFICIENCY

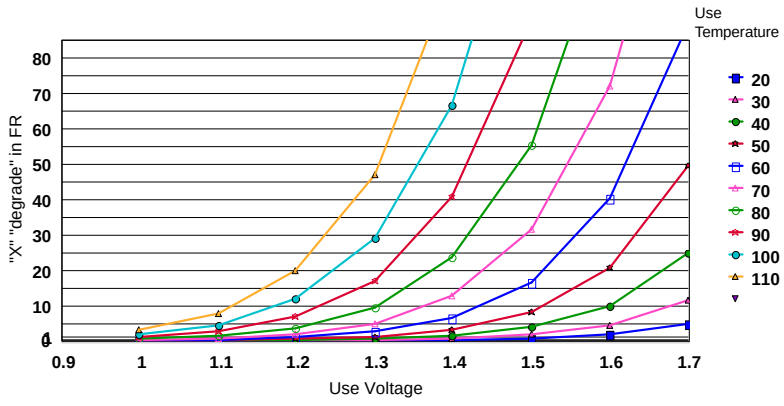
- Could decrease due to
  - Higher Ioff / Power
  - New design techniques
  - New materials

Effect of BI Voltage & Duration to Maintain Acceleration



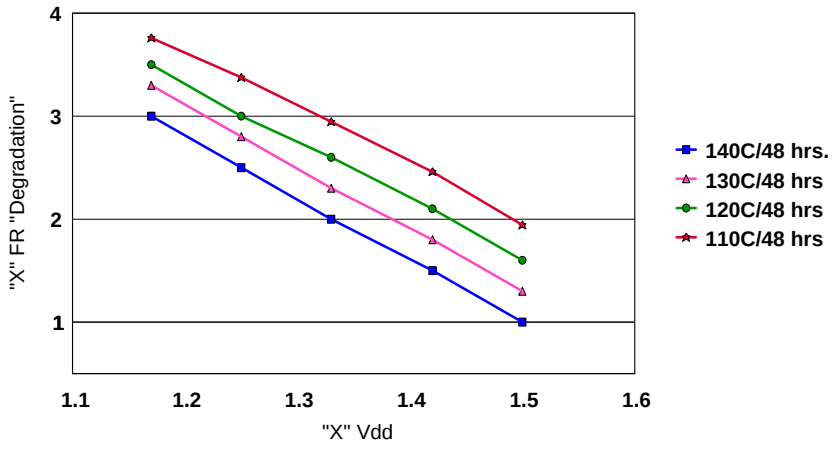
USE VOLTAGE and USE TEMPERATURE vs. TEMP/VOLT FR IMPACT for BURNED-IN PRODUCT

(Assume 1.2V/60C use operation / 1.8V/140C BI)

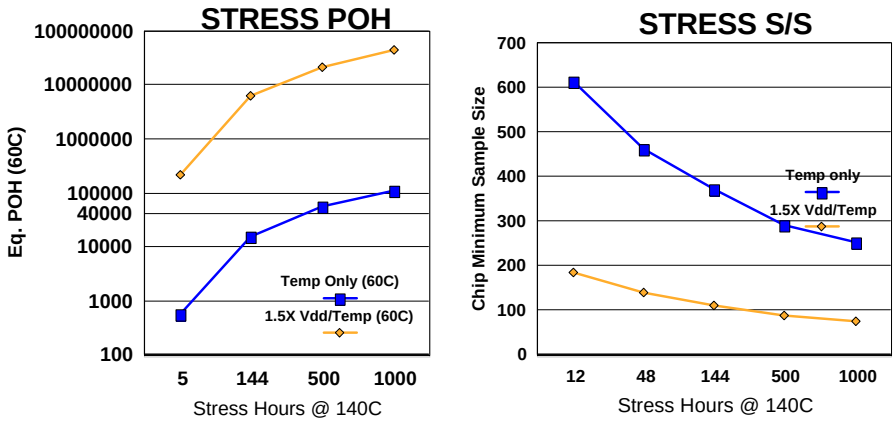


BI VOLTAGE vs. TEMP/VOLT FR IMPACT

(Assume: 1.3V/85C/60K use, 1.8V/140C/48 hr BI)



QUAL ACCELERATION IMPLICATIONS



VOLTAGE SCREEN

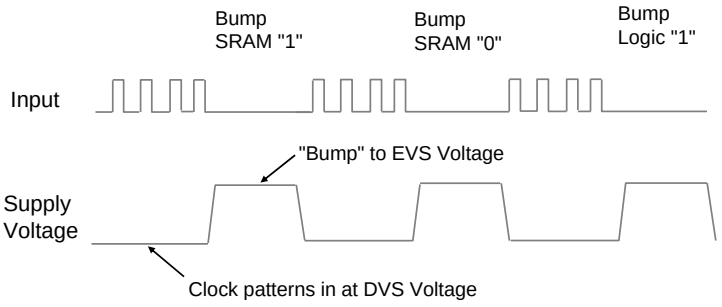
- Description
  - Application of high voltage at test temperature usually as part of WFT
    - > Burn-in voltage
    - 10mS --> 3 sec.
- Most effective for gate oxide and conductor-conductor defects

VOLTAGE SCREEN

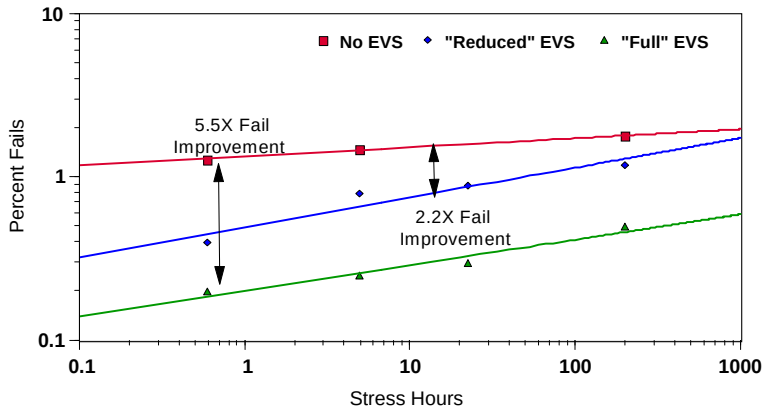
- Types
  - Dynamic (DVS)
    - Voltages greater than BI
    - Functionally running while at high voltage
    - Good pattern coverage
  - Enhanced (EVS)
    - Voltages higher than DVS
    - Static bumps to EVS voltage; no clocks at high Vdd
    - Limited patterns

DVS/EVS Screen Description

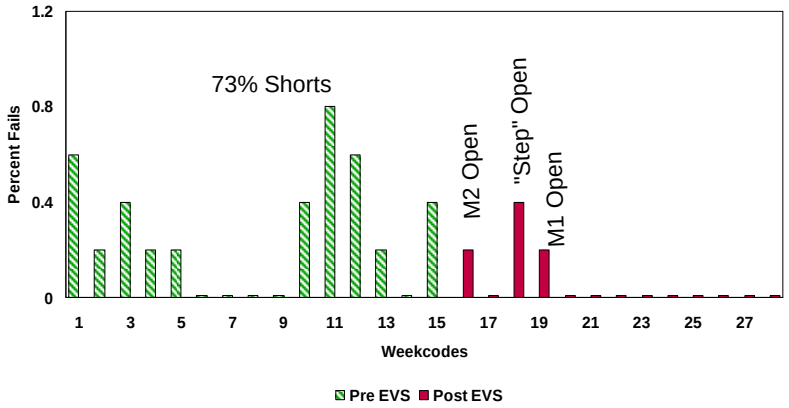
Alternate Between Segments of DVS & EVS



EVS Voltage Effectiveness



Monitor Performance
Pre/Post EVS Installation

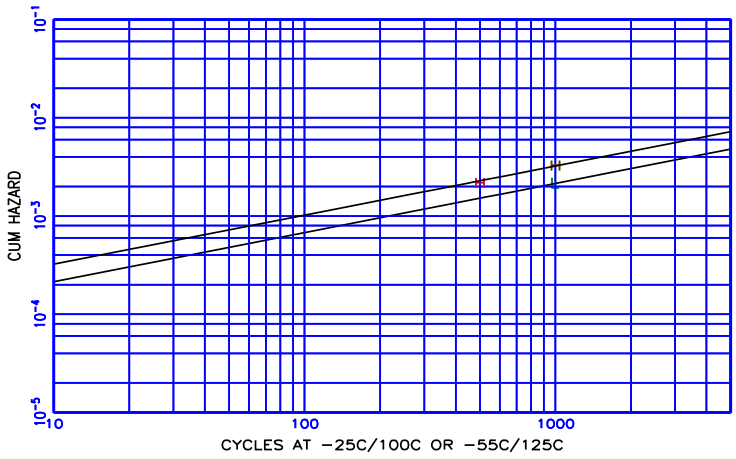


Pre EVS - 0.267% vs. Post EVS - 0.0615%
(4.33X Improvement)

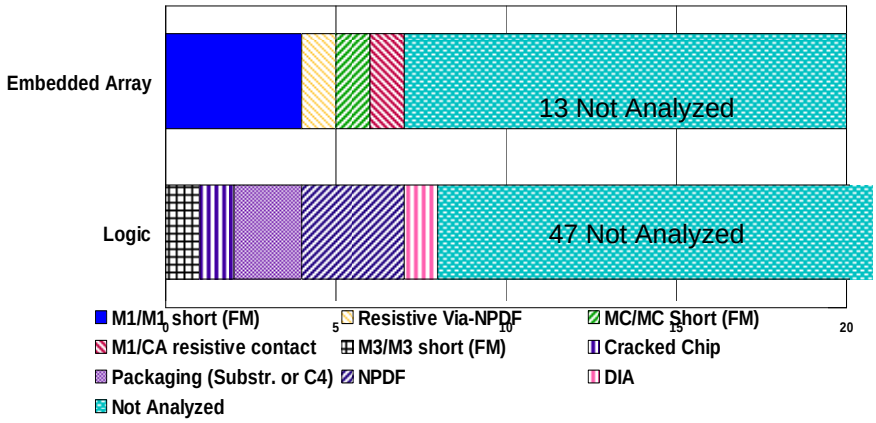
THERMAL CYCLE

- **Description**
  - Sequence of extreme thermal excursions without bias
- **Types**
  - Wafer
  - Module (typically lower temperature delta excursion than wafer)
- Culls out fails due to chip and package mechanical stress
- Most effective for interconnect and wiring defects and package defects (module)

TC MODELLING



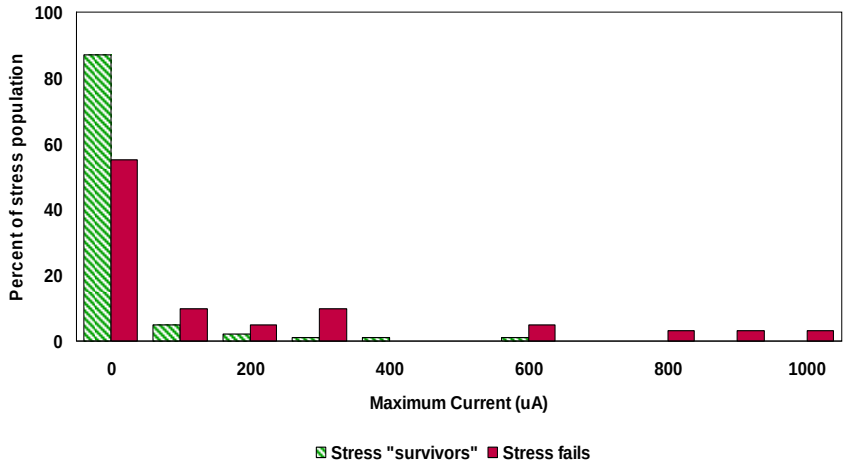
TC FA



"IDDq"

- Has been used more widely on Logic/SRAM vs. DRAM (Picoamps of current cause DRAM fails)
- Traditional technique
  - Put device in known quiescent state
  - Measure current draw
  - Reject "abnormal" devices
- Experiments have shown "abnormal" devices less reliable

Maximum Current Distributions
Good Devices and Reliability Fails



TRADITIONAL "IDDq" DAYS NUMBERED?

- Traditional technique getting "noisy“
  - Number of transistors per device going up
  - Leakage per transistor going up
  - More variability due to process variables (i.e. "short" vs. "long" Leff fabricated devices)

IDDq "EXTENSIONS"

- IDDq "signatures"
- IDDq vs. Vdd
- IDDq vs. temperature
- Lower voltages
- Transient IDD (IDDt)
- Design partitioning
- ???

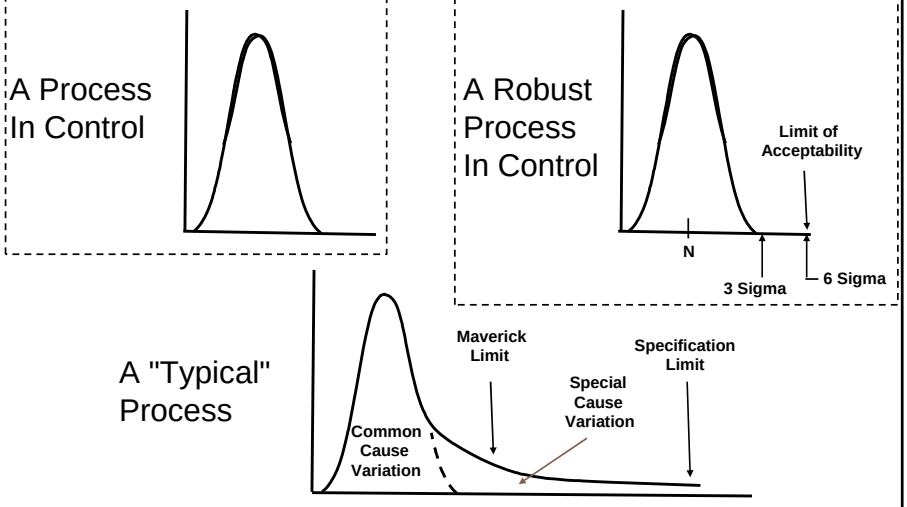
IDDq "SIGNATURES"

- Reported upon in several papers
- Example from Gattiker/Maly, et. al. 1996 IEEE IDDq Testing Workshop

MAVERICK CONTROL

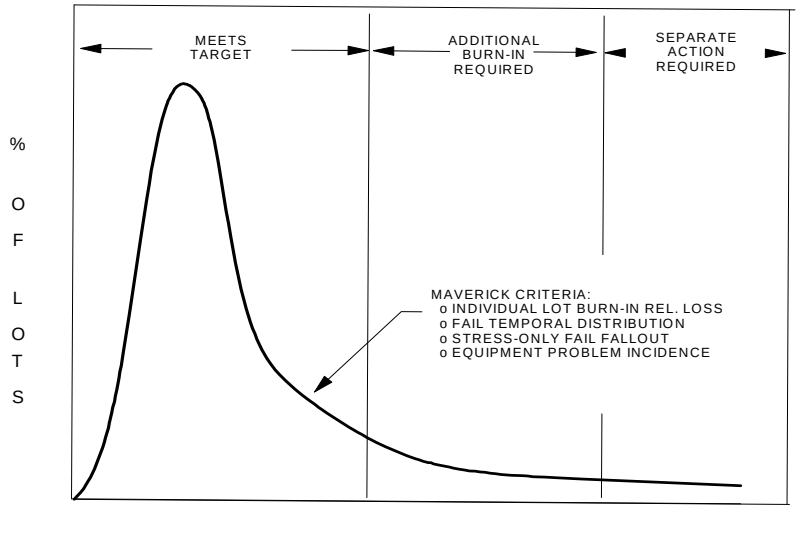
- Product screened by lot and wafer
- Yields checked for "abnormal" (i.e. maverick) wafers and lots. Mavericks held.
- Goal
  - Minimize variability (not "control" failure rates)
  - Set statistically based limits
- Reality
  - Limits based on MFG "affordability"

MAVERICK CONTROL



Special Cause Variation = Mavericks

EXAMPLE OF MAVERICK LIMITS AT BURN-IN



% BURN-IN RELIABILITY LOSS

OUTLINE

- Reliability Stressing/Model
  - Qualification Cycle
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  - Reliability Modeling
    - FITs, Chi-Squared, etc.
- Manufacturing Screens
- Reliability Monitoring

RELIABILITY MONITORING

- Objectives
- Stress Profiles
- Monitor Data

WHY MONITOR?

- **MFG Line Needs**
  - Line in control
  - Defect type feedback for line learning
  - Screens effectiveness / adjustments
  - Database to satisfy customers requirements for information
  - Data base to help market product quality
- **Customer Needs**
  - Data base to judge product quality

TYPICAL MONITOR FLOW

- Product sampled after BAT
- Usually pre-End of Line screens like BI or TC
- BI and TC performed with testing before/after

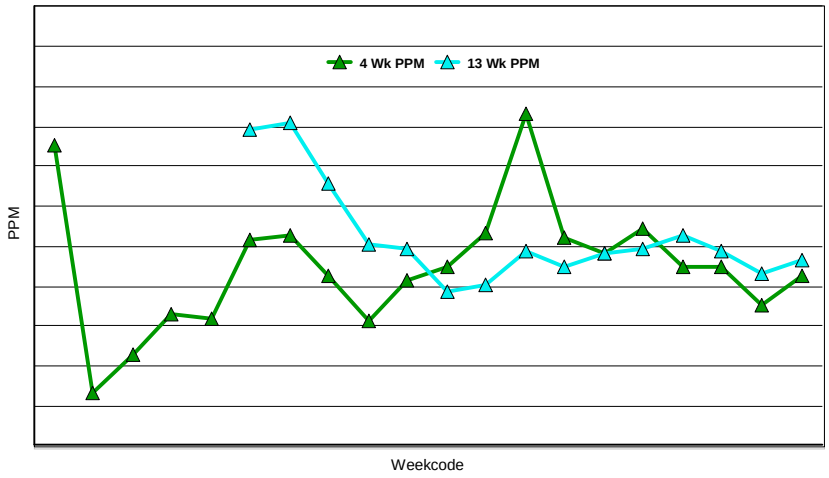
SAMPLE SIZE "RULE of THUMB"

- Sample size:
  - First, Assume you are "king of the world", again.
  - Determine performance level to monitor
  - Determine s/s (for the given stress conditions) that will give some tbd conf. level of getting at least x fails per x months

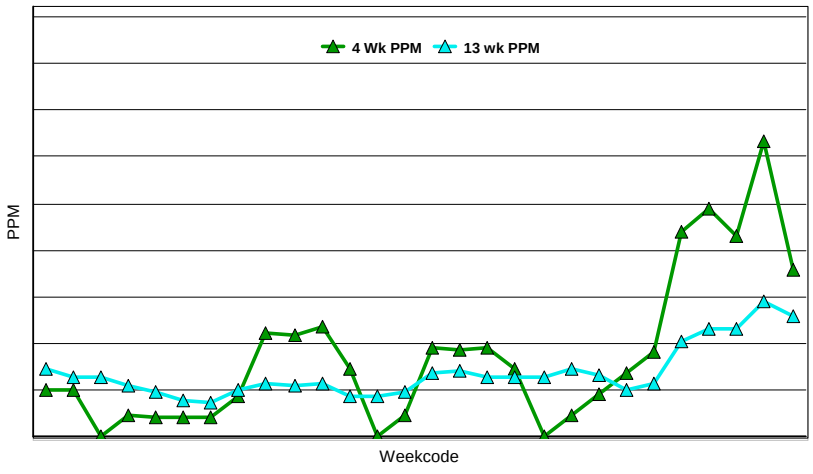
MONITOR SCOPE

- Monitor needs to factor in
  - Fab(s)
  - Technology – same/similar features/design ground rules to existing monitors
  - Same critical tool set
  - Qual data for technology
  - Enough volume to have good vintage representation
  - Is there test/stress capacity in place to support
  - Consistent In-Line/Electrical/Maverick Criteria
  - Monitor vs. other products in the technology
    - Test Coverage, Unique Tests & Screens
    - Operating Voltages
    - Design Features
    - Design Sensitivity To Defects

MONITORING TRENDS



MONITORING TRENDS



SUMMARY

- **Reliability Stressing/Model**
  - Qualification Cycle
  - Reliability "Categories“
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  - Building a Reliability Model
    - Product Stress Profiles/Measurements
    - Effects of Screens
  - Reliability Modeling
    - FITs, Chi-Squared, etc.
- **Manufacturing Screens**
- **Reliability Monitoring**

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  - Tim Sullivan
  - Al Stong
  - Ernest Wu
  - Steve Mittl
  - Ron Bolam

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