BiTS Burn-in & Test Socket Workshop 2008

Session 7

ARCHIVE 2008

HIGH FREQUENCY DEVELOPMENTS

"Challenging Device Interface - For High Speed DIMM Module Testing"

Joachim Moerbt, Rose Hu
Advantest (Europe) GmbH

"Tolerance Induced Test Socket RF Performance Variation"

Gert Hohenwarter
GateWave Northern, Inc.

"From Single-Ended to Differential"

Ryan Satrom
Everett Charles Technologies

Challenging Device Interface

for High speed DIMM Module Testing

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

Joachim Moerbt
Rose Hu
Advantest (Europe) GmbH

Contents

Motivation

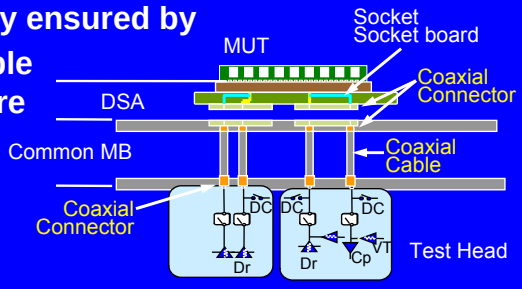
- Why presenting Device Interface Technology at BiTS
  - Contacting device to tester does not require only a high end contactor
  - Mechanical adoption crucial for contact reliability in production
  - Whole signals path from sources to sinks must be considered for performance on high speed testing

Requirements for Interface Design

- Testing memory modules on ATE
  - Ensuring testing quality – high speed
    - High frequency signals at minimized distortion
  - Increasing productivity – high parallelism
    - High quantity signals within minimum space
    - Perfect fit of test system and handling system
  - Providing highest level of flexibility
    - Keep the freedom of modifying channel connections
    - Handle different module type and form factor

Challenges to Modular Interfaces

- Current modular interface can fulfil some of those requirements:
  - Best signal integrity ensured by
    - Pure coaxial cable for ideal structure in signal path
  - Flexibility by
    - Device specific adapter
    - Test system orientated common MB



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Challenges to Modular Interfaces

- Specification for DIMM

– Parallelism:	16 DIMM
– Test chamber size:	240.4mm x 153.4mm
– Target MUT:	240 pin DIMM
– Required signals per MUT:	200 signals, 16PPS
– Coaxial connectors per MUT:	6pcs. (each 38-channel)

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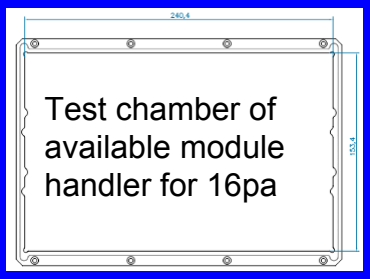
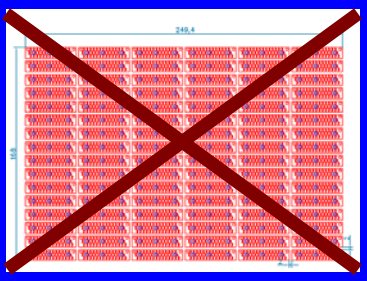
Challenges to Modular Interfaces

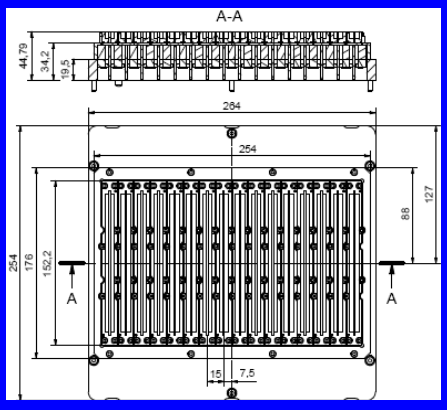
- Bottleneck
  - Mechanical conflict to handler
  - Not able to realize high parallelism with small test chamber





Goal of New Interface Design

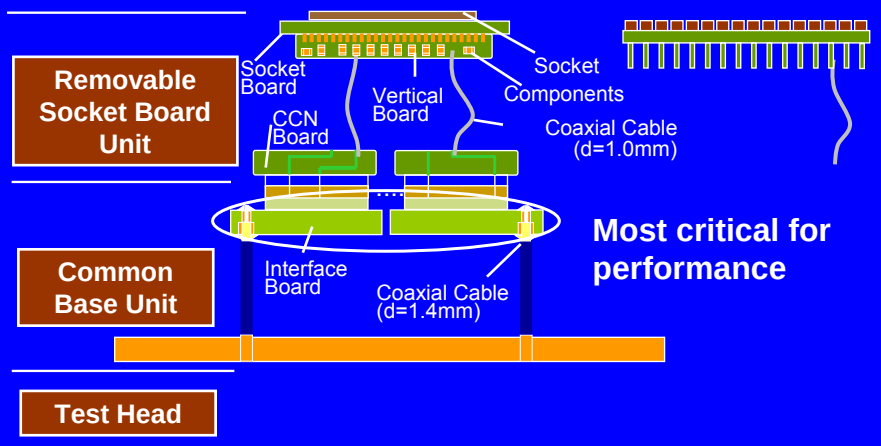
- Achieve the highest parallelism within very limited space
- Challenge the higher testing speed of memory module- up to 400MHz



Top view of module interface

New Design Concept

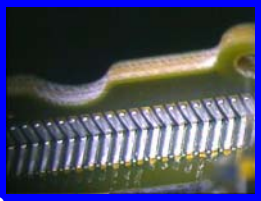
Removable socket board unit to test various devices on various platforms

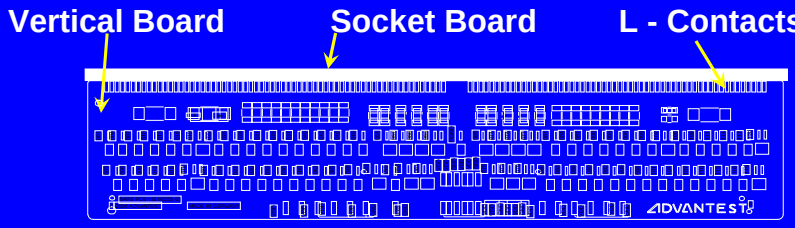


Most critical for performance

Vertical Board

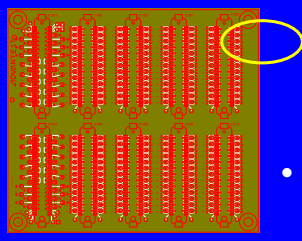
- **L- contacts to secure stable connection between socket board and vertical board**
- **Room for passive components**
- **Landing pads to connect to coaxial cables**



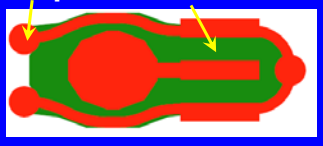


Interface Board

Interface Board



Top and Bottom view



- Signal grounding:
  - Surrounded by ground trace at top
  - Shielded by ground pattern at the bottom layer
- The coaxial cable inserted into the through hole with specific solder technology

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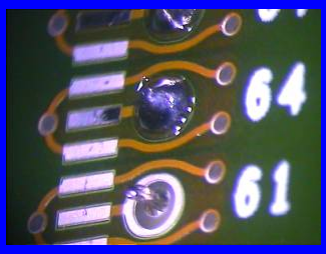
Interface Board



- Crosstalk between signals is minimized through optimal ground guidance

Top view of interface board

- The impedance distortion is minimized by optimal ground shielding
- Minimum signal T_{pd} deviation by precise hole drilling

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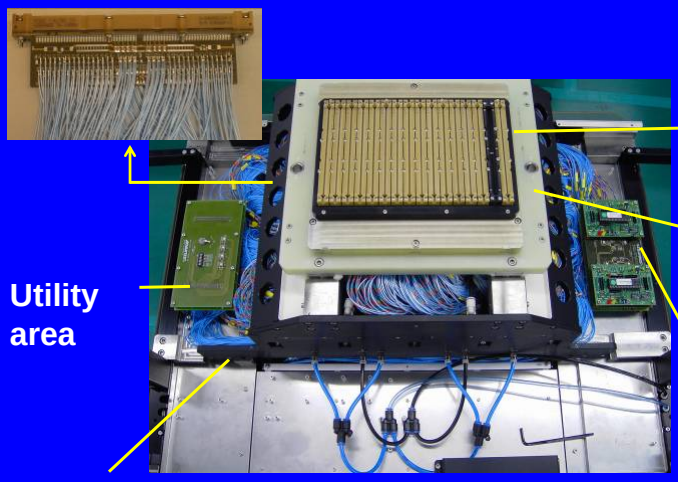
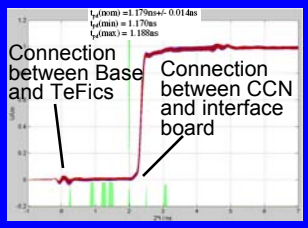
Flex Module Interface



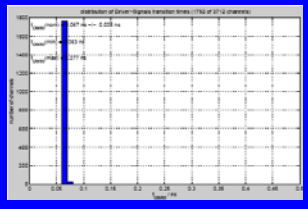
Reflection Measurement

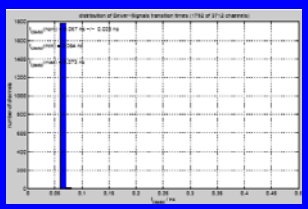
Flex Module, Common Base Unit

Standard MB with coaxial cable



Propagation delay of signal channels





Intrinsic transition time of signal channels

Comparison Results

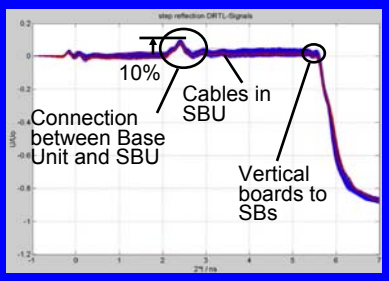
Flex Module Base Unit

- **The reflection waveform shows:**
  - **Signals are transmitted smoothly from coaxial cable to interface board without visible distortion**
- **The standard deviation of propagation delays:**
  - **As good as a standard modular interface with pure coaxial cable and coaxial connector without inter-board connection**
- **The intrinsic transition time:**
  - **Comparable to standard coaxial interface**

Reflection Measurement

Measuring the Flex Module Device Interface

Flex Module Interface with SBU, 16pa



Standard MB with DSA, 2pa

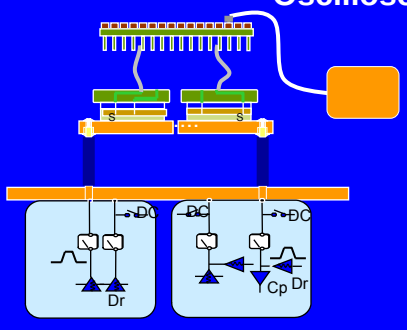
Comparison Results

Complete Flex Module Device Interface

- **Reflection measurement shows**
  - **The distortion of Flex Module Interface is mainly caused by the inter connection between base unit and socket board unit.**
  - **The distortion of standard coaxial SBC type Interface is caused by the inter connection between common MB and DSA.**
  - **The distortions are almost equivalent.**

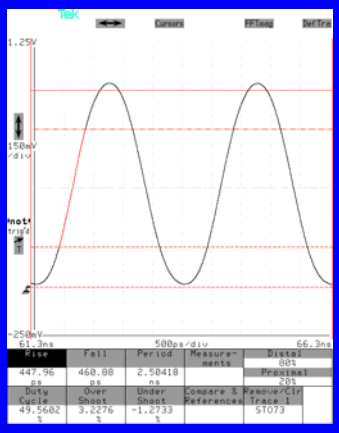
Signal Measurement at 400MHz

- **Transmission measurement at the MUT**
  - **400MHz signals generated by test system T5588**
  - **swing of 0V to1.0V.**
  - **Comparison waveform taken from a standard reference fixture used for system QA.**

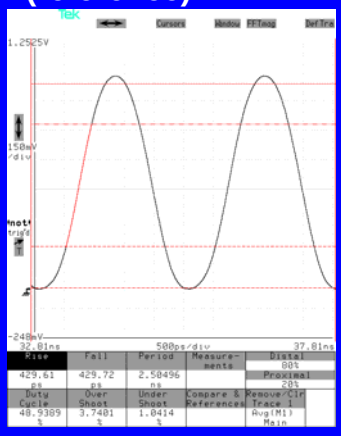


Driver Waveform Comparison

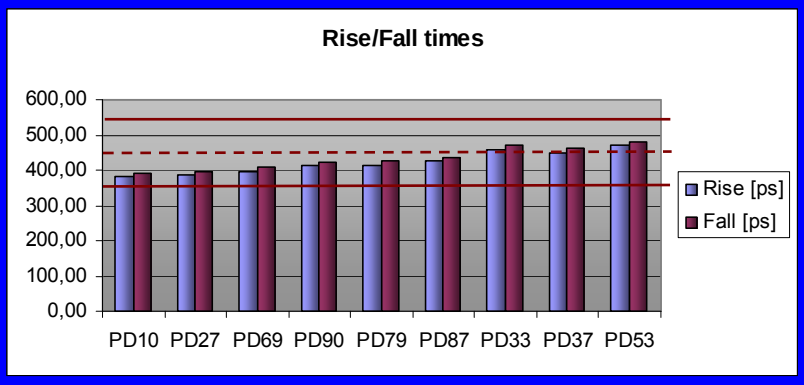
PD37 on Flex Module DIMM HiFix



PD37 on skew board (reference)



Driver Signal Performance



Best case and worst case signals:

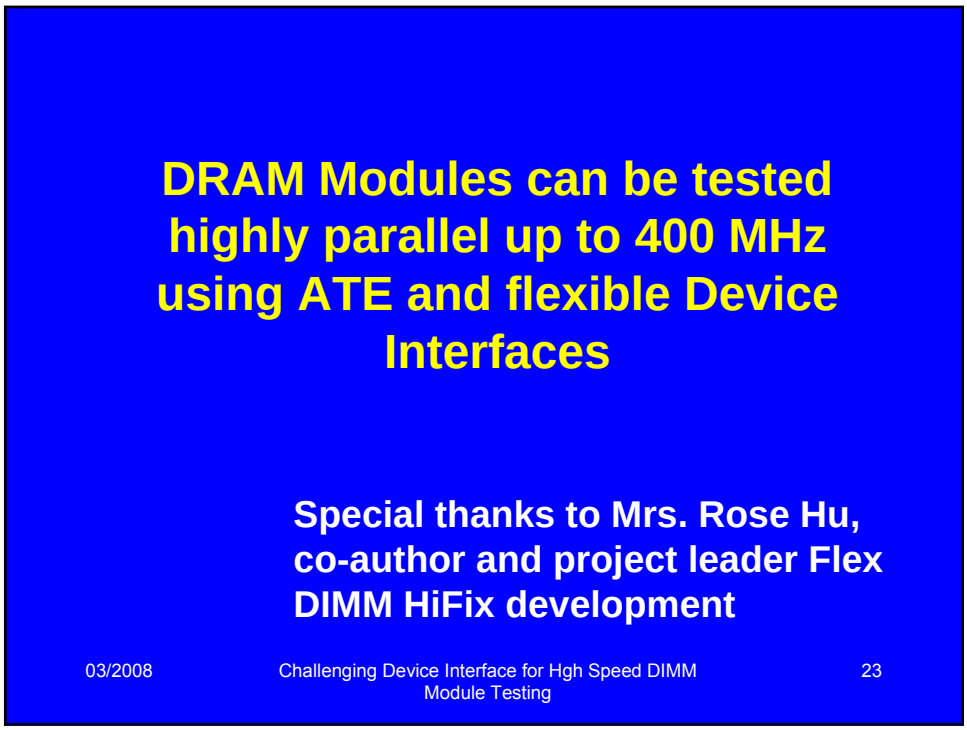
- **Matching to system specification of 450ps+/-100ps**

Result of Signal Measurement

- Good Signal quality compared to reference
- Good coherency between all signals
- Full correlation can be expected
- High repeatability in device testing
- Fulfil homogenous yield rate expectation

Conclusions

- Highest density signal transmissions by pluggable SBUs realized
- Optimum impedance control by new through-hole structure for coaxial cable into PCB connection
- Signal distortion is minimized
- Signal integrity equivalent to pure coaxial standard interface
- 400MHz testing frequency enabled for DIMM


DRAM Modules can be tested highly parallel up to 400 MHz using ATE and flexible Device Interfaces
Special thanks to Mrs. Rose Hu, co-author and project leader Flex DIMM HiFix development
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Tolerance Induced Test Socket RF Performance Variation

2008 Burn-in and Test Socket Workshop

March 9 - 12, 2008

Gert Hohenwarter
GateWave Northern, Inc.
www.gatewave.com

Objective

Socket RF Performance - What Can Compromise It ?

- Establish potential causes for variations
- Identify ways to quantify them
- Examine impact of parameter changes on RF performance

Approach

- Use simple models for generic sockets with moderate RF performance to illuminate problem

  (Sockets are shown with straight through pins for simplicity. Models and measurements cover different types of contactors. Results thus do not imply that performance of sockets constructed with spring probes is limited)
- Determine impact of misalignment on capacitance and inductance
- Provide migration path to improved techniques
- Supplement models with measurements on three different socket types and contactor technologies

3/2008 Tolerance Induced Test Socket RF Performance Variation 3

Tools Used

- *3D structure simulator (generates capacitance/inductance info from mechanical designs)*
- *SPICE circuit analysis (predicts S-parameters from above model info)*
- *Full FEA S-parameter modeling (uses entire socket/interface geometry to predict performance)*
- *VNA measurements (2port and 4port) (real world behavior verification)*

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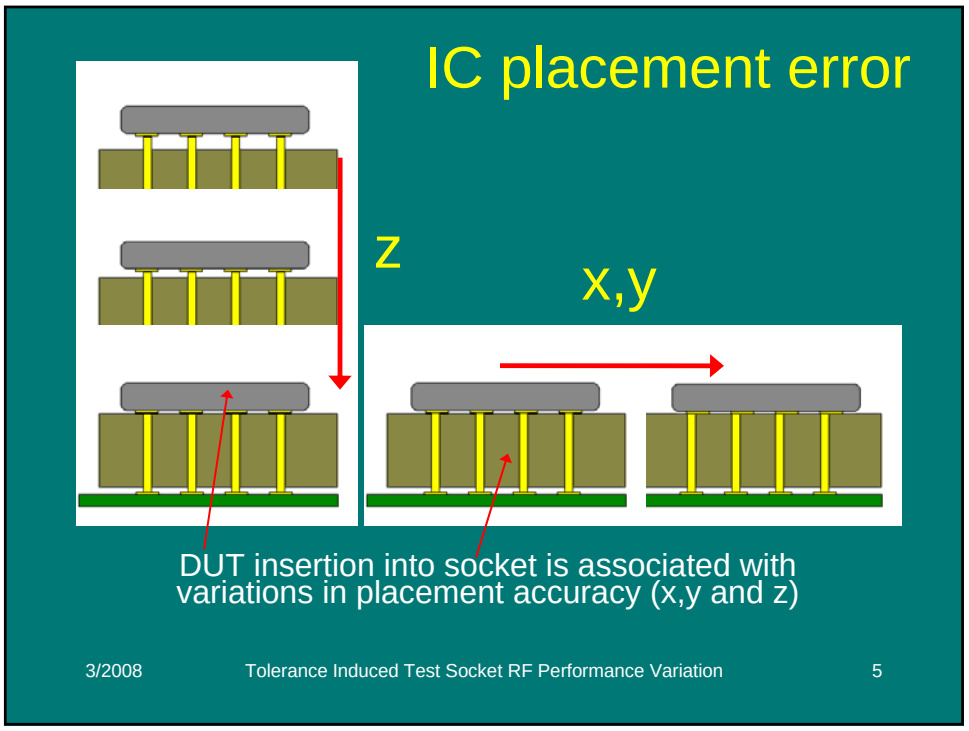
IC placement error
z
x,y
DUT insertion into socket is associated with variations in placement accuracy (x,y and z)
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Tolerance Induced Test Socket RF Performance Variation
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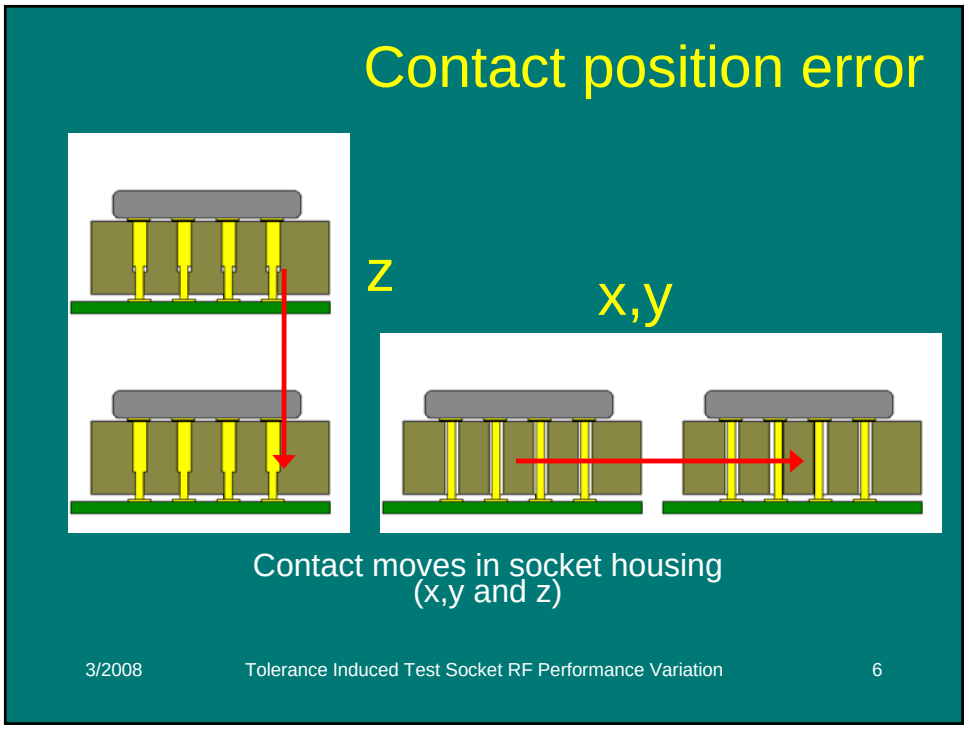
Contact position error
z
x,y
Contact moves in socket housing (x,y and z)
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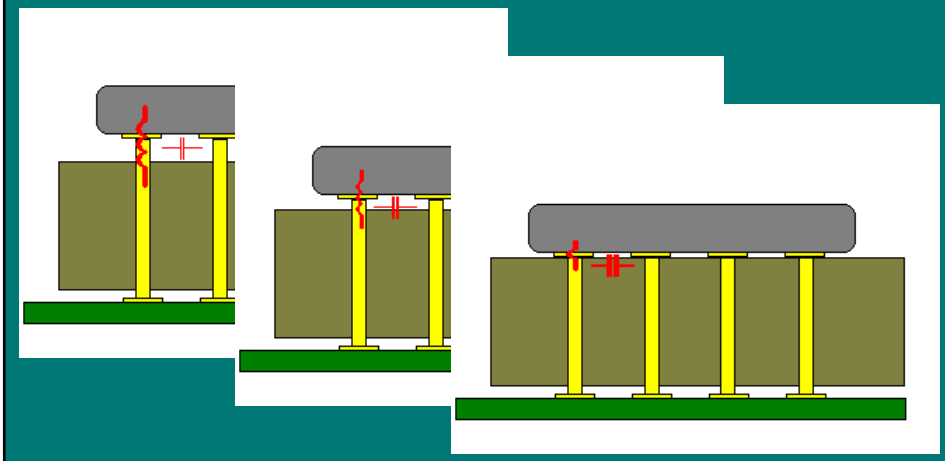
Z placement



Z position likely affects inductance as well as capacitance (plus delay)

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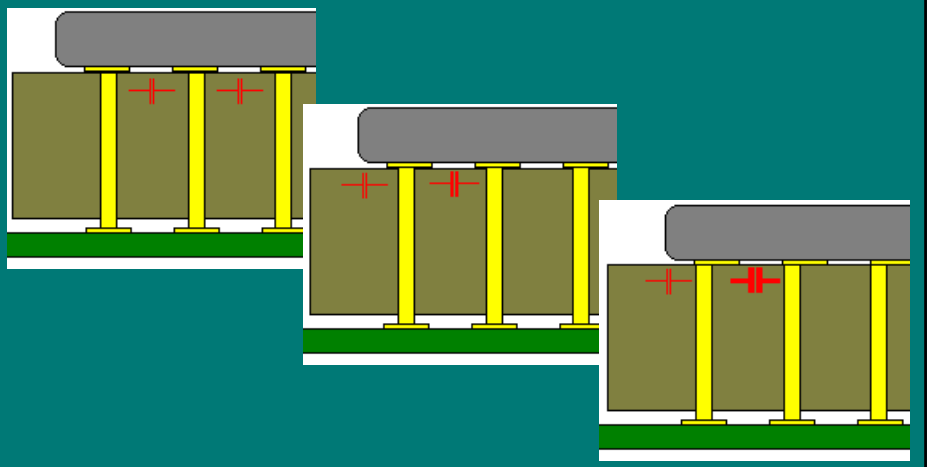
X,Y placement



X and Y position likely affect primarily pad to pad capacitance

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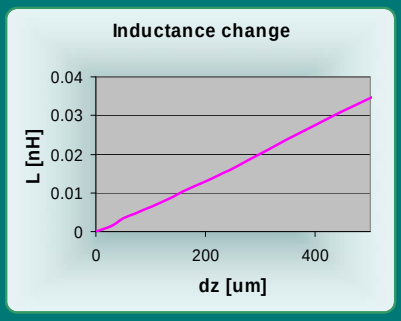
Inductance change example

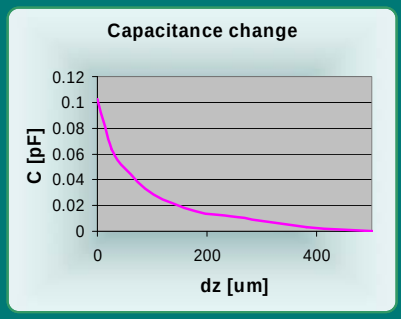


$$L = \mu_0 \frac{l}{\pi}\left(\ln\frac{d}{a} + ?\right)$$

$$L \sim l$$

Socket model: Inductance change as a function of length change

Capacitance change example 1

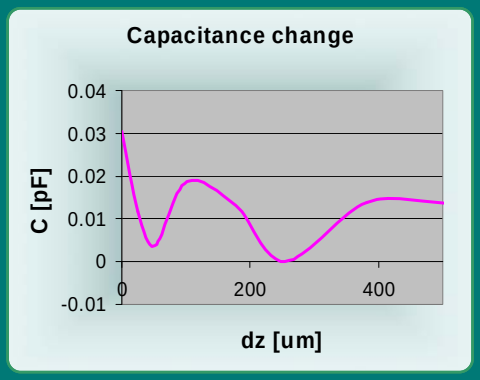


$$C = \epsilon_r \epsilon_0 \frac{A}{d}$$

$$C \sim \frac{1}{d}$$

Socket model: Capacitance change as a function of axial position change

Capacitance change example 2



Socket example: Capacitance change as a function of axial position (nominal 0.28 pF)
A monotonic capacitance variation must not be expected

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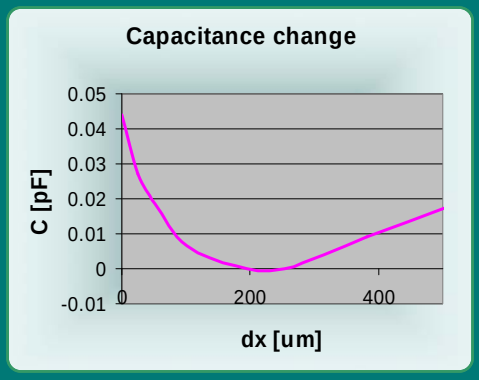
Capacitance change example 3



Socket example: Capacitance change as a function of lateral position (nominal 0.28 pF, 1mm pitch)

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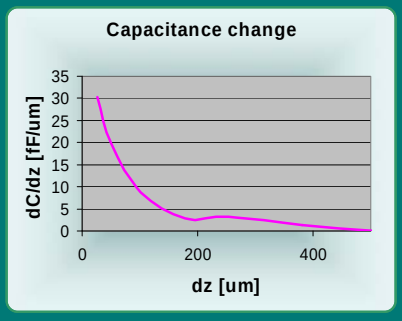
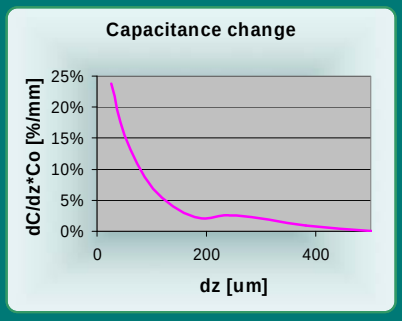
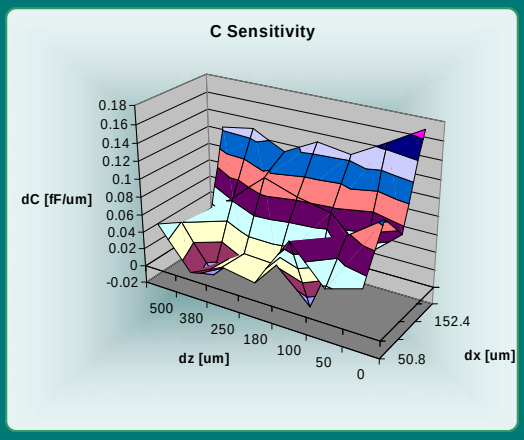
Capacitance change characterization





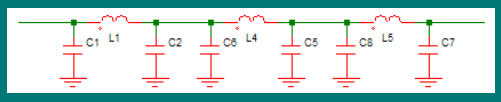
Determination of (normalized) sensitivity allows for comparison of different designs

Design optimization

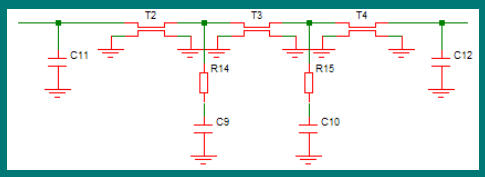


Capacitance sensitivity in x and z direction can show "sweet spot" for a given design
A similar approach can be pursued for inductance

Equivalent circuits for insertion loss model (SPICE)



Lumped model (3 sections)



Distributed model with transmission lines

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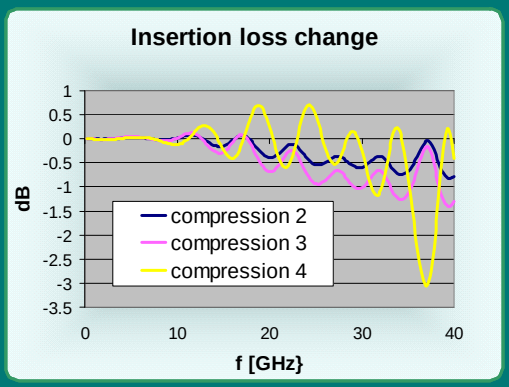
Insertion loss (SPICE)



Insertion loss (S21) changes as a result of capacitance variations
(For the graph subsequent simulation results are subtracted from the first dataset)

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Shortcomings of this approach…..

- SPICE model is only approximate
- Model may change not only value but also character during device positioning
- Cumbersome parasitics extraction

…can be overcome by complete structure simulator, albeit at the expense of….

- potential lack of understanding of the underlying mechanisms

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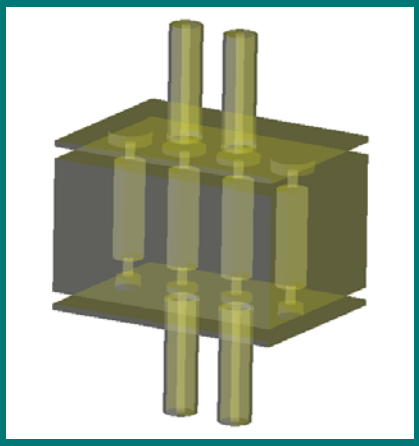
Structure Characterization



4 port arrangement that mimics testing with a network analyzer

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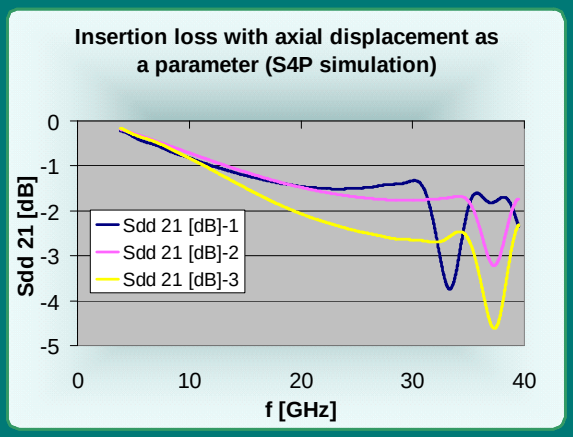
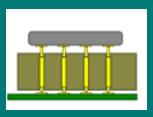
Insertion loss (FEA)

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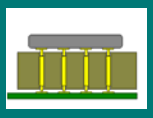
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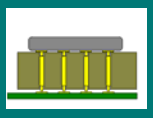
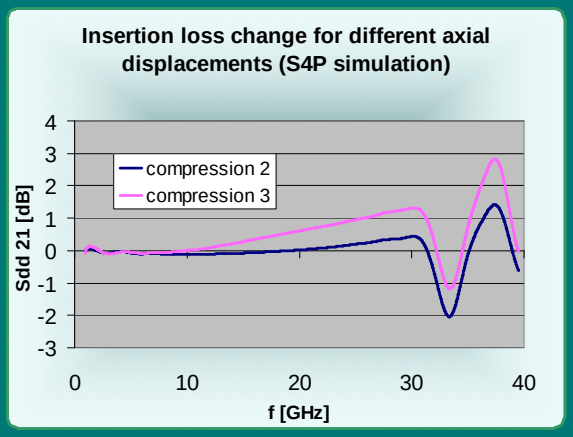
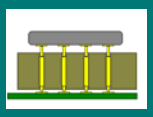

3

Insertion loss under z variation

Insertion loss changes (FEA)

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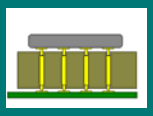
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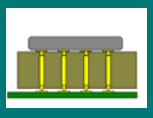
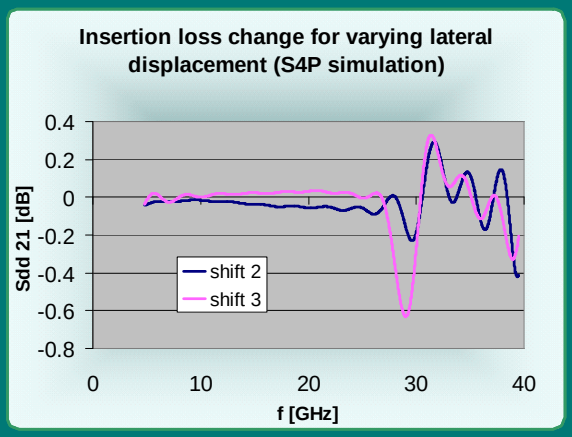
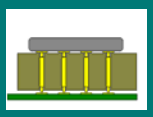

3

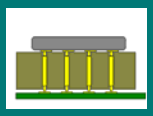
Insertion loss changes under z variation

Insertion loss (FEA)

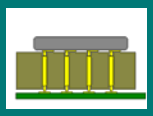




1



2



3

Insertion loss changes under x variation

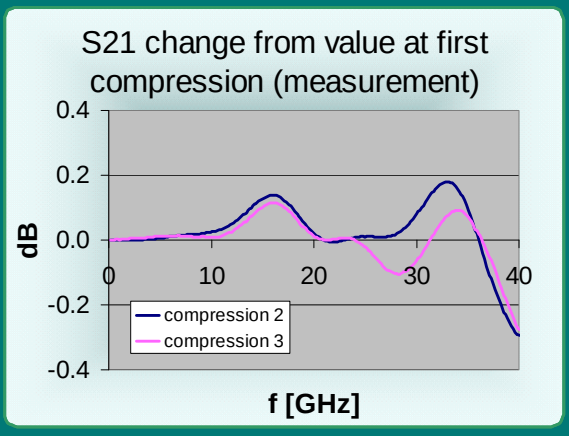
Shortcomings of this approach…..

- FEA only as good as what is entered into the model
- If mechanisms are not **completely** understood and accounted for, results will be misleading
- FEA slow and not capable of dealing with larger structures

…can be overcome by the ultimate test:
Vector Network Analyzer measurements

- Models for simulation (SPICE, IBIS) can be extracted from those tests

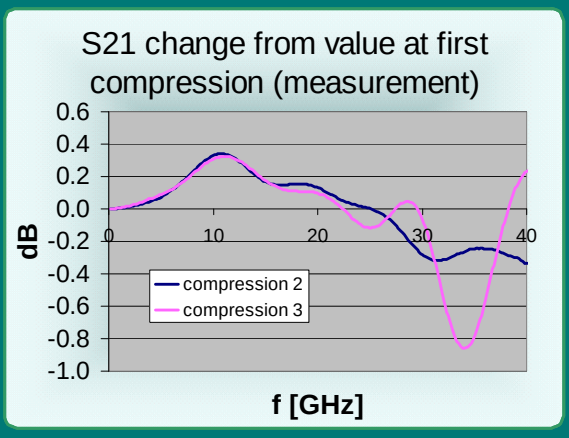
Insertion loss change (VNA)



Socket type 1 (-1dB @ 18 GHz)

3/2008 Tolerance Induced Test Socket RF Performance Variation 23

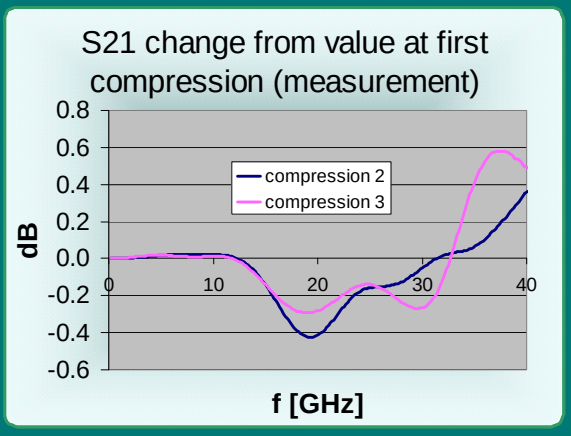
Insertion loss change (VNA)



Socket type 2 (-1dB @ 15 GHz)

3/2008 Tolerance Induced Test Socket RF Performance Variation 24

Insertion loss change (VNA)



Socket type 3 (-1dB @ 20 GHz)

Conclusion

- Examples show potentially significant impact of placement accuracy on high speed performance
- Socket designs can be optimized for minimal performance change via sensitivity analysis
- Several different tools available for performance assessment
- Other parameters that were not addressed here (such as S11 and crosstalk) change as well
- Ultimate proof for robust design is verification by actual testing (sensitivity of C,L and S21)

Thank you

From Single-Ended to Differential

Ryan Satrom
ECT - Semiconductor Test Group, MN
2008 BiTS Workshop

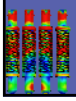
BiTS Burn-in & Test Socket Workshop

Introduction

- Differential Signaling
  - Increasingly common way of transferring data
  - Performance differs from single-ended performance
  - Performance unpredictable without simulation and careful design
- This Presentation Will:
  - Compare differential signaling in contactors to single-ended signaling in contactors
  - Describe differential signaling impact
  - Suggest ways to account for differential signaling

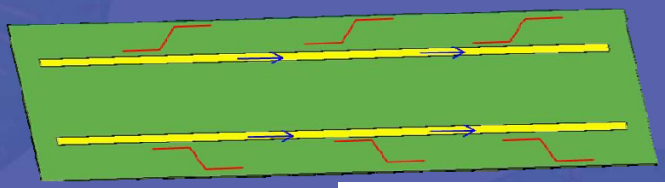
Differential Signaling

- Two Transmission Lines
  - Used to transmit a signal and its complement
  - Signal is voltage difference between the two lines
- Lines Not Necessarily Coupled
  - Differential PCB traces have little coupling
  - Differential nets in contactor have significant coupling
- Common Interfaces:
  - XAUI, SerDes, USB, PCI Express, Ethernet, HDMI



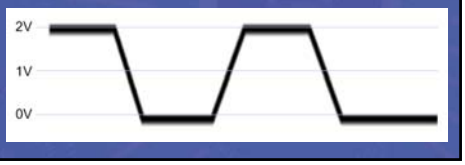
3/2008 From Single-Ended to Differential 3

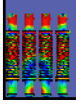
Differential Pair – Simple Example



- Signal line 1 excited with a signal
- Signal line 2 excited with complementary signal
- The result is the difference between the 2 voltages

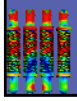
$V_{DIFF} = V_1 - V_2$





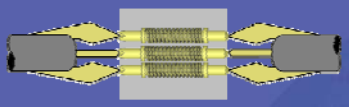
Advantages/Disadvantages of Differential Signaling

- Advantages
  - Increased immunity to return path discontinuities
  - Less susceptible to noise
- Disadvantages
  - Requires additional PCB real estate
  - Possibility of creating increased EMI

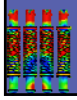


Characterization Method

1) Single-Ended VNA Characterization
   - Use industry standard G-S-G configuration
   - Direct contact approach

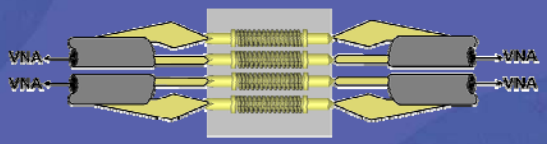


2) Single-Ended 3D Electromagnetic Simulation
   - Correlate 3D models to single-ended G-S-G contactor models
3) Create Differential Models
   - Use correlated single-ended models to create 3D electromagnetic differential simulations

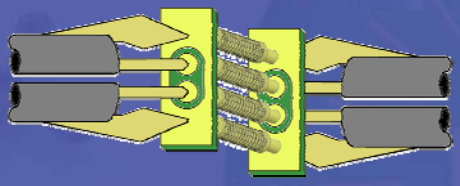


Characterization Method

- Other Characterization Approaches – 4-Port VNA



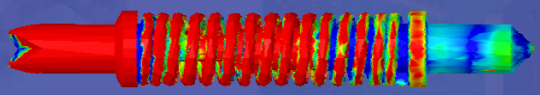
  - Incompatible with direct contact approach
  - Grounds connected at VNA – not at contactor



  - Ground-shorting PCB approach increases error
  - Must have accurate method for de-embedding

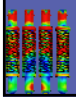
Differential Signaling – Key Concepts
(Compared to Single-Ended Signals)

1) Differential signals will not perform like single-ended signals in contactors
2) Bandwidth of differential signals in contactors is less dependent on ground proximity
3) PCB-contactor transitions will have less effect on differential signals than single-ended signals



Single-Ended vs. Differential Performance

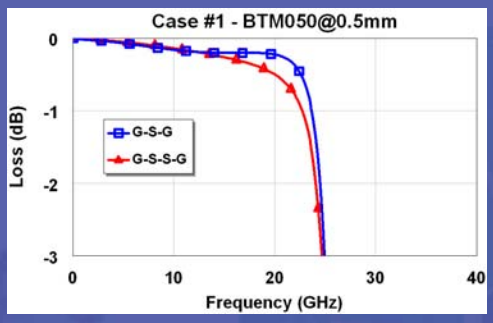
- Differential signals will not perform like single-ended signals in contactors
- Differential signal configuration always differs from single-ended configuration, affecting performance
- In order to understand contactor performance, differential specifications must be obtained from supplier
- Characterization is required for each configuration

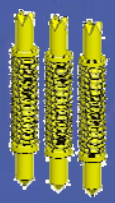


Single-Ended vs. Differential Performance

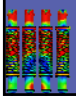
Comparison of single-ended G-S-G vs. differential G-S-S-G

- Case #1 - BTM050 @ 0.5mm - Bandwidth is unchanged





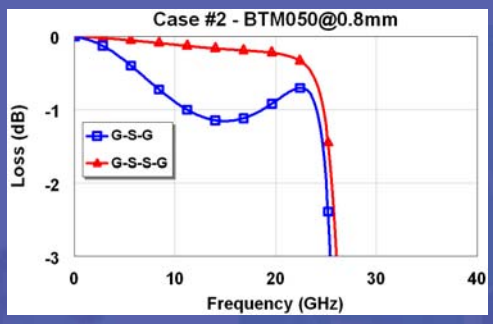
G-S-G Bandwidth (-1dB) = 23.6GHz
G-S-S-G Bandwidth (-1dB) = 22.7GHz

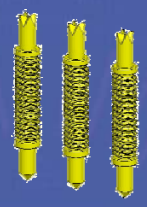


Single-Ended vs. Differential Performance

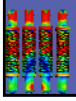
Comparison of single-ended G-S-G vs. differential G-S-S-G

- Case #2 - BTM050 @ 0.8mm - Bandwidth increases





G-S-G Bandwidth (-1dB) = 11.2 GHz
G-S-S-G Bandwidth (-1dB) = 24.7 GHz



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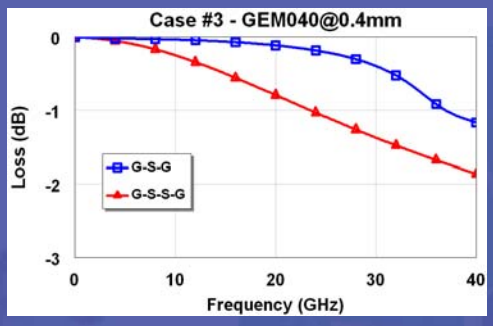
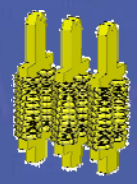
Single-Ended vs. Differential Performance

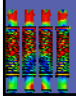
Comparison of single-ended G-S-G vs. differential G-S-S-G

- Case #3 - GEM040 @ 0.4mm - Bandwidth decreases





G-S-G Bandwidth (-1dB) = 36.9 GHz
G-S-S-G Bandwidth (-1dB) = 23.4 GHz



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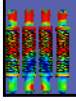
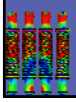
Single-Ended vs. Differential Performance

- Results Summary
  - Case #1 – Bandwidth is unchanged
  - Case #2 – Bandwidth increases
  - Case #3 – Bandwidth decreases
- There is no trend to predict differential performance based on single-ended performance



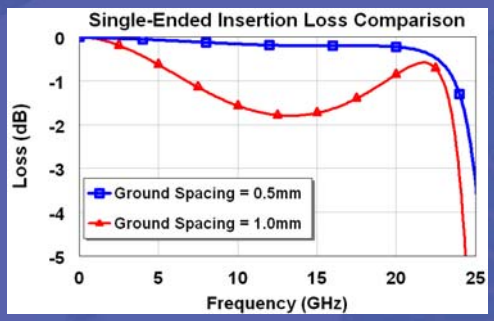
Ground Proximity

- Bandwidth is affected by proximity to nearest return path
  - Only return path of single-ended signals is nearest ground or grounds
  - Return path of differential signals is a combination of nearest ground(s) and complementary signal
- Entire differential return current can travel in complementary signal path
- Bandwidth of differential signals in contactors is less dependent on ground proximity
  - Note: Ground proximity also affects other RF parameters such as crosstalk and EMI



Ground Proximity

Comparison using ECT BTM050 high performance probes
SE #1 : Ground spacing = 0.5mm
SE #2 : Ground spacing = 1.0mm



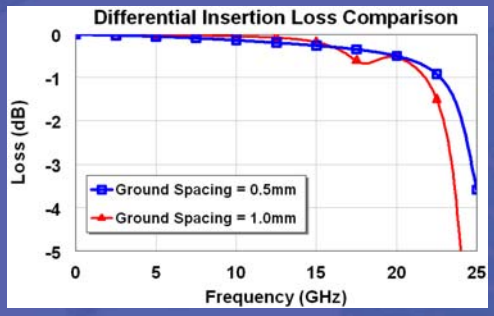
SE #1

SE #2

0.5mm Bandwidth (-1dB) = 23.6 GHz
1.0mm Bandwidth (-1dB) = 6.8 GHz

Ground Proximity

Comparison using ECT BTM050 high performance probes
DIFF #1 : Ground spacing = 0.5mm; Sig spacing = 0.5mm
DIFF #2 : Ground spacing = 1.0mm; Sig spacing = 0.5mm



DIFF #1

DIFF #2

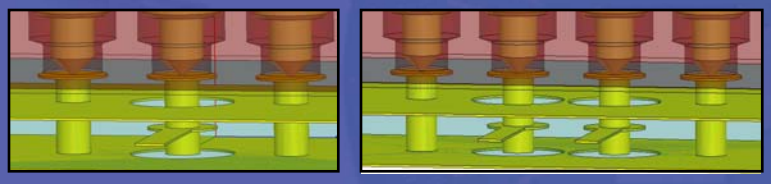
0.5mm Bandwidth (-1dB) = 22.7 GHz
1.0mm Bandwidth (-1dB) = 21.8 GHz

Ground Proximity

- Results Summary
  - Single-ended – Bandwidth decreases
  - Differential – Bandwidth unchanged
- Ground proximity has much less effect on differential signals in contactors than on single-ended signals

PCB-Contactor Transition

- The PCB-contactor transition always has an impact on performance
  - Should be modeled with 3D electromagnetic simulation*
- Differential signals have decreased dependence on ground
  - Less current travels through ground via(s)
  - This minimizes discontinuity and improves insertion loss



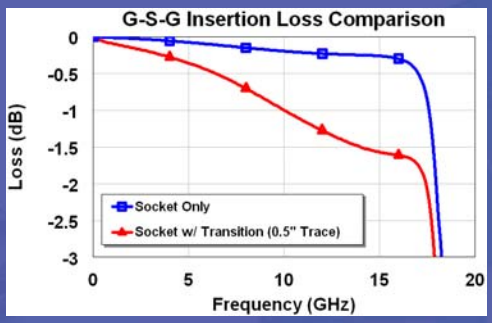
* See "Effects of the Launch on Bandwidth", Ryan Satrom, BiTS 2006

PCB-Contactor Transition

Comparison of single-ended signal – with and without transition

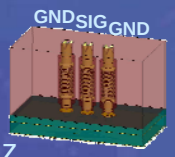
SE #1 : G-S-G – socket only

SE #2 : G-S-G with socket transition + 0.5” trace



SE #1

SE #2



Socket Only Bandwidth (-1dB) = 17.6 GHz

Socket with Transition Bandwidth (-1dB) = 10 GHz

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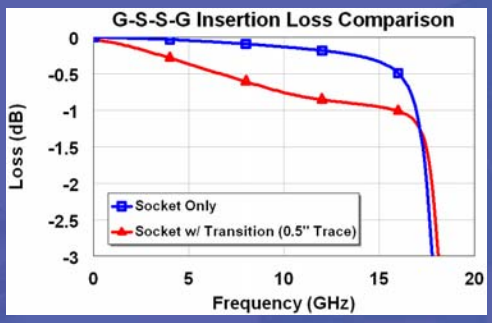
PCB-Contactor Transition

Comparison of differential signal – with and without transition

DIFF #1 : G-S-S-G – socket only

DIFF #2 : G-S-S-G with socket transition + 0.5” trace



DIFF #1

DIFF #2

Socket Only Bandwidth (-1dB) = 16.9 GHz

Socket with Transition Bandwidth (-1dB) = 15.8 GHz

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PCB-Contactor Transition

Results Summary

- Single-Ended – Bandwidth decreases significantly
- Differential – Bandwidth less affected

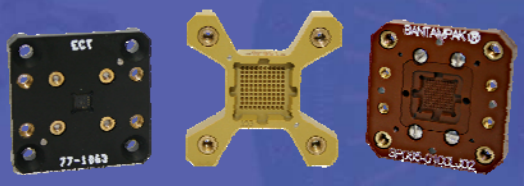
- PCB-contactor transitions will have less effect on differential signals than single-ended signals

Design Technique – Modify Dielectric

- Impedance
  - Inversely proportional to the square root of dielectric

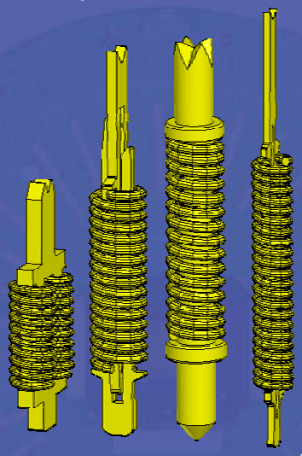
$$Z_0 \sim \frac{1}{\sqrt{\varepsilon_R}}$$

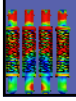
- Insertion Loss and Return Loss
  - Both highly dependent on impedance
- Modifying dielectric to match impedance will improve performance



Design Technique – Modify Probe

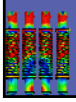
- Impedance is related to diameter of probe
- Optimal probe selection is determined by best impedance match
- Probe selection dependent on both signal-type (single-ended or differential), ground proximity, and pitch
- Simulation used to determine optimal technology for each pitch





Conclusion

- Differential signaling impacts contactor design
- Signal type must be considered in order to optimize contactor design
- Understanding the concepts of differential signaling will help improve contactor design



Thanks!

Feedback is greatly appreciated
Feel free to contact me at Ryan.Satrom@ectinfo.com