INNOVATIVE CONTACT TECHNIQUES

“Contact Pin Complexities: Valuing Performance and Cost”
Paul Schubring
Plastronics

“New Concept in Spring Probe Design”
John Winter, Larre Nelson, Amos Friedner
Rika Denshi America, Inc.

“Non-Contact System-in-Package Testing”
Jeff Hintzke, Chris Sellathamby, Brian Moore
Scanimetrics, Inc.

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Contact Pin Complexities: Valuing Performance and Cost

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

Paul Schubring
Plastronics

Agenda

• Introduction
• Technology Trends
• Cost Background
• The Conflict
• The Development Challenge
• Contact Solution Comparison
• Optimal Solution
• H-pin – Solution & Innovation
• Conclusion
Introduction

• Technology trends driving Moore’s law increasingly at odds with the economics needed to sustain past business performance
• As a percent of total product cost, tooling is low, but rising – Cost pressures never greater

Source: Evolution of a Revolution. www.intel.com
Technology Trends

- Package / Application drive secondary requirements
  - Co-planarity
  - Pin Travel
  - Life cycle requirement
  - Etc.

- Pitch / Frequency most compelling technology force
  - Today’s mainstream: 0.6 – 1.0 mm / 1 – 4 GHz
  - 2008 - 2009: 0.5 – 0.8 mm / up to 10 GHz
- Power has stabilized
- C-res – varies by application (BI/Test/Sys Test)

Cost Background

- Tooling Cost per pin improves generation to generation
  - Reached plateau based on capability of current mainstream technology (probe pins) and technology requirements (pitch / electrical)
- Next generation requirements may increase cost / pin price
• Gross margin / ASP pressures have lead to new paradigm
  – BI: Better capability at same cost / Test: Same capability at lower cost
• Need to optimize performance and cost never been greater
• Key concern is where does the envelope stop e.g. where does quality suffer at expense of cost

The Development Challenge

• Zone I: Character Building Zone
  – Often seen by early adaptors
• Zone II: Necessary Evil
  – Product must have the capability
• Zone III: Settle For Zone
  – Low cost, but sacrifice capability e.g. yield, retest, Bin split, etc.
• Zone IV: Cheap and Good
  – Does the grail of contact solutions exist?
• New tooling development = f(cost, resources, capability, lead time…)
  • Too often, mutually exclusive
The Development Challenge

- Customer Desire/Industry Goal: Migrate as many new development programs into a single technology (Zone IV)

Nature of industry is that all 4 zones will exist

- Standardization benefits all
  - Reduces development lead times / resources / costs
  - Enables economies of scale
    - Reduces manufacturing / component / assembly costs
  - Reduces product lead time & inventory costs

Contact Solution Comparison

- Three primary solutions:
  - Stamped (BI)
  - Probe / Membrane (Test/Sys Test)

<table>
<thead>
<tr>
<th>Relative Performance of Test and Burn-in Technologies</th>
<th>Stamped Socket</th>
<th>Probe Pin Socket</th>
<th>Membrane Socket</th>
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<tr>
<td>Current Carrying Capacity (Amps) (higher the better)</td>
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<td>10</td>
</tr>
<tr>
<td>Inductance (nH) (lower the better)</td>
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<td>2</td>
<td>0.4</td>
</tr>
<tr>
<td>Life of Contact (Thousands of cycles)</td>
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<td>250+</td>
<td>25</td>
</tr>
<tr>
<td>Contact Travel (mm)</td>
<td>~ 0.2 - 0.5</td>
<td>0.5+</td>
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Relative Cost: A < B, C

3/2008 Contact Pin Complexities: Valuing Performance and Cost
Contact Solution Comparison

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### Relative Performance of Test and Burn-in Technologies

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</tr>
<tr>
<td>Assembly of Socket Method - Automation or Manual</td>
<td>A</td>
<td>M</td>
<td>M</td>
</tr>
<tr>
<td>Cost</td>
<td>A</td>
<td>B</td>
<td>C</td>
</tr>
</tbody>
</table>

### Optimal Solution

- Use best technical capability as a technology target
  - Broad product envelope
- Cost – Establish breakthrough cost/performance capability
  - Lower TCoO – everything from price & delivery to probe life & yield
- Design for manufacturing
  - Automated assembly
  - Quality & reliability
**H-pin Solution**

<table>
<thead>
<tr>
<th>Attribute</th>
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<th>Probe Pin Socket</th>
<th>Membrane Socket</th>
<th><strong>H-pin</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Carrying Capacity</td>
<td>~ 1</td>
<td>2+</td>
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</tr>
<tr>
<td>Resistance</td>
<td>50</td>
<td>100</td>
<td>10</td>
<td>35</td>
</tr>
<tr>
<td>Inductance (nH, lower the better)</td>
<td>6</td>
<td>2</td>
<td>0.4</td>
<td>0.9</td>
</tr>
<tr>
<td>Life of Contact (Thousands of cycles)</td>
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<td>Assembly of Socket Method</td>
<td>A</td>
<td>M</td>
<td>M</td>
<td>A</td>
</tr>
<tr>
<td>Production Cost</td>
<td>A</td>
<td>B</td>
<td>C</td>
<td>D</td>
</tr>
<tr>
<td>Contact cost per pin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**H-pin™ Innovation**

- H-pin: Patented pin technology
  - Electrical path comparable to stamped single beam pin
  - High performance of traditional probe / economies of scale of high volume stamping process
  - Scalable for variety of pitches:
    - 0.5 mm ~1.0+ mm
    - BI / Test / Sys Test / Connector applications
H-pin™ Performance

- H-pin delivers electrical performance through full stroke
- Excellent durability / stress relaxation performance
  - Negligible contact force change after bake
  - Stable lab performance to 250K cycles

Insertion Loss

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin to Pad Resistance</td>
<td>&lt; 40mΩ</td>
</tr>
<tr>
<td>Self-Inductance</td>
<td>0.88 nH</td>
</tr>
<tr>
<td>Single-ended Insertion Loss</td>
<td>&lt; 1dB to 20 GHz</td>
</tr>
<tr>
<td>Single-ended Return Loss</td>
<td>&lt; -10dB to 20 GHz</td>
</tr>
<tr>
<td>Differential Return Loss</td>
<td>-17.5 dB @ 5GHz</td>
</tr>
<tr>
<td>Differential Insertion Loss</td>
<td>-25dB @ 11.75 GHz</td>
</tr>
<tr>
<td>Near End Cross Talk</td>
<td>-25dB @ 14.8 GHz</td>
</tr>
<tr>
<td>Far End Cross Talk</td>
<td>-25dB @ 7.5 GHz</td>
</tr>
</tbody>
</table>

0.5mm H-pin Performance

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H-pin Innovation

<table>
<thead>
<tr>
<th>Features:</th>
<th>Benefits:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.40mm to 0.70mm Travel</td>
<td>Compliance for Large Package Warpage</td>
</tr>
<tr>
<td>Flat Spring Rate</td>
<td>Stable Contact Resistance and Force</td>
</tr>
<tr>
<td>BeCu H-PIN™</td>
<td>Solid Beam Electrical Performance</td>
</tr>
<tr>
<td>Stainless Steel Core Spring</td>
<td>Compliance at High Temperatures (180°C+)</td>
</tr>
<tr>
<td>Bandwidth -1dB @ 15GHz</td>
<td>Correlated BI, System Evaluation and Test</td>
</tr>
<tr>
<td>Current Carrying Capacity</td>
<td>Reliable Power and Ground Contact</td>
</tr>
<tr>
<td>High Volume Stamping *</td>
<td>Stocked Inventory and Better Lead Time</td>
</tr>
<tr>
<td>Automated Pin Assembly *</td>
<td>High Volume Capacity and Quality Control</td>
</tr>
<tr>
<td>Reel-to-Reel Pin Insertion *</td>
<td>High Volume Capacity and Ease of Use</td>
</tr>
</tbody>
</table>

• H-pin reduces TCO
  – Single solution for wide array of applications
  – High volume process
    • Competitive price
    • Automated assembly
  – Short lead times / delivery

Conclusion

• Product enabling through technical innovation continues as our collective goal
• Technology at any cost is long gone and is now focused on best affordable capability
• Current technologies generally offer either technical capability or cost capability
• New H-pin technology is a new technology that combines both in a single solution
Thank You!

Q & A
New Concept in Spring Probe Design

RIKA DENSHI AMERICA, INC.
John Winter – Engineering Manager
Larre Nelson – General Manager
Amos Friedner – Sales Manager

Outline

- Motivation
  - Improve contact resistance
  - Improve high frequency response issue
- Solution
  - Concept
  - Customer requirements / wish list
  - Design
- Results
- Benefits
Design Objectives

• Contact resistance improvements
  – Improve contact resistance / standard deviation
  – Maintain short operating length
  – Maintain long cycle life
  – Reduce wear due to bias construction
  – Maintain consistent spring force vs. deflection

• Frequency response improvements
  – Improve signal integrity – static and dynamic

Market Requirements

• Short operating length
• Low contact resistance standard deviation
• Long travel
• Consistent and smooth spring force vs deflection
• Higher current carrying capacity
Solution - Spring Sleeve

Standard Probe   Bias Probe w/out ball

Bias Ball Probe   Probe w/Spring Sleeve
Probe with Spring Sleeve

Contact resistance

CONTACT RESISTANCE COMPARISON

<table>
<thead>
<tr>
<th></th>
<th>STANDARD TEST PROBE</th>
<th>TEST PROBE WITH SPRING SLEEVE</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Average Resistance</strong></td>
<td>27.8 mOhms</td>
<td>15.7 mOhms</td>
</tr>
<tr>
<td><strong>Standard Deviation</strong></td>
<td>32.9 mOhms</td>
<td>6.7 mOhms</td>
</tr>
</tbody>
</table>
Single ended probe

Coaxial probe with spring sleeve
Single ended x-ray image

Contact resistance

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<tr>
<td><strong>Average Resistance</strong></td>
<td><strong>Average Resistance</strong></td>
</tr>
<tr>
<td>32.1 mOhms</td>
<td>27.4 mOhms</td>
</tr>
<tr>
<td><strong>Standard Deviation</strong></td>
<td><strong>Standard Deviation</strong></td>
</tr>
<tr>
<td>47 mOhms</td>
<td>14 mOhms</td>
</tr>
</tbody>
</table>
Test probe without spring sleeve

Test probe with spring sleeve
Benefits

• Consistent electrical performance
• Improved current carrying capacity
• Consistent / smooth force vs. deflection
• Enables shorter probe designs
• Can easily be added to most probe designs
• Longer cycle life than bias constructed probe
Non-Contact System-in-Package Testing

2008 Burn-in and Test Socket Workshop

Chris Sellathamby, Brian Moore, Jeff Hintzke

Purpose

• Show how a wireless testing technique can overcome the multiple testing issues encountered with Silicon-based System in Package (SiP) devices

• Propose applications for wafer-level and package burn-in
Outline

• Silicon-based System-in-Package (SiP) technology
• SiP testing challenge
• Non-contact test access technology
• SiP testing by WiTAP™
• Wafer-level burn-in of SiPs
• Summary

Silicon Substrate System in Package

• Silicon serves as chip carrier
• Substrate contains interconnect and passive components
• Built using IC technologies
• SiP assembled on the wafer
• Package often built like wafer level package
Example of Silicon Based SiP Substrate

Bare SiP Substrate

Silicon Based SiPs

1 Chip
42 passives
3cm x 3cm

1 Chip + Si-based Substrate
1cm x 1cm

2 Chips
86 passives
4cm x 8cm

2 Chip + Si-based Substrate
3cm x 3cm

1 Chip
42 passives
3cm x 3cm

2 Chip + Si-based Substrate
3cm x 3cm

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SiP Testing Issues

- Internal nodes hidden
- SiPs don’t use BIST or DFT
  - Individual die often have scan
- Substrate Damage from probing
- 3D
  - Varied topologies
    - Stacked die, wirebonds, flipchip
- Burn-in of assembled devices

Non-Contact Interconnect Technology

- Wireless chip-scale communications
- Distances < 100 µm
- Micro TX/RX on chip
- One TX/RX per I/O
- Fully CMOS compatible
- Power via standard probe, all other signals wireless
- Data scales to > 1 Gbps
Innovative Contact Techniques

Receiver

Data Out
RF (AM) In

Non-contact Test Example

Non-contact JTAG enquiry and response

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Alignment Sensitivity

- BER vs. Alignment
- 120um antennas
- 20MHz Clock
- The zone inside the curve has an error rate less than one error per $10^{10}$ bits.

WiTAP™ Chip

- Standard 130nm CMOS Process
- 1.1mm x 1.2mm
- JTAG Test controller
- 3 Independent scan chains
- 1.8V input supply
- 1.2V and 1.8V output supplies
- Intelligent power control
WiTAP™

- Wireless Test Access Port for SiP
- JTAG and Boundary Scan testing
- Replaces probes with wireless transceivers
- All SiP power supplied through WiTAP™ chip
- Allows test during build, before final packaging
- Allows testing of hidden test points
- Can be used with stacked chips

SiP Testing with the WiTAP™

- JTAG test controller with Integrated RF transceivers
- Assembled on the SiP substrate early in the assembly process
- Test the SiP assembly multiple times during the process
- Higher Yields
- Faster Production Ramps
- Lower manufacturing costs
WiTAP™ Advantage

- Technology is “non-contact” for data signals
  - manufacturing process can be monitored
  - chips can be smaller
  - more chips can be tested at once
- Test when/where no test was possible before
- Reduce SiPs production costs
- Enables wafer-level burn-in
  - Very high parallelism is possible

Probing with WiTAP™
Probecard - Top View

Probecard – Bottom View

Probe Transceivers

Cantilever Power Pins
Package Burn-in Concept

- Wireless channels communicate through package
- Power/Gnd by simplified burn-in socket

Conclusions

- WiTAP™ solution for SiP testing application
- Parallel WiTAP™ SiP x4 in production
- High parallel Wafer-level burn-in possible