2008 Session 5

ARCHIVE 2008

INNOVATIVE CONTACT TECHNIQUES

"Contact Pin Complexities:
Valuing Performance and Cost"
Paul Schubring
Plastronics

"New Concept in Spring Probe Design"
John Winter, Larre Nelson, Amos Friedner
Rika Denshi America, Inc.

"Non-Contact System-in-Package Testing"
Jeff Hintzke, Chris Sellathamby, Brian Moore
Scanimetrics, Inc.

Contact Pin Complexities:

Valuing Performance and Cost

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

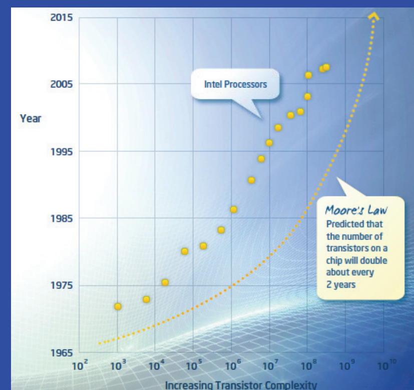
Paul Schubring
Plastronics

Agenda

- Introduction
- Technology Trends
- Cost Background
- The Conflict
- The Development Challenge
- Contact Solution Comparison
- Optimal Solution
- H-pin – Solution & Innovation
- Conclusion

Introduction

- Technology trends driving Moore's law increasingly at odds with the economics needed to sustain past business performance
- As a percent of total product cost, tooling is low, but rising
  - Cost pressures never greater

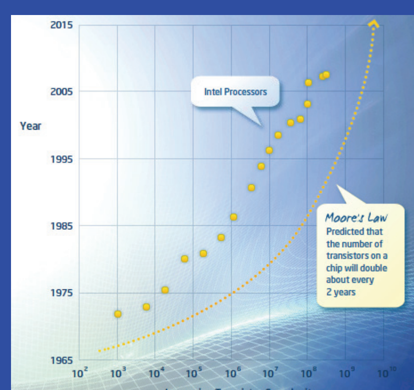


Source: Evolution of a Revolution.
www.intel.com

3/2008 Contact Pin Complexities: Valuing Performance and Cost 3

Introduction

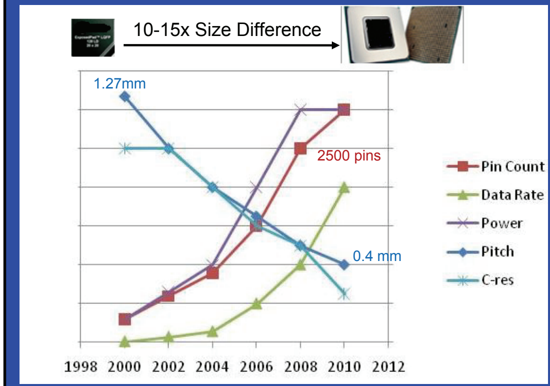
- Technology at any price is gone and best capability at lowest price is now the goal
- Any solutions to minimize this conflict?



Source: Evolution of a Revolution.
www.intel.com

3/2008 Contact Pin Complexities: Valuing Performance and Cost 4

Technology Trends

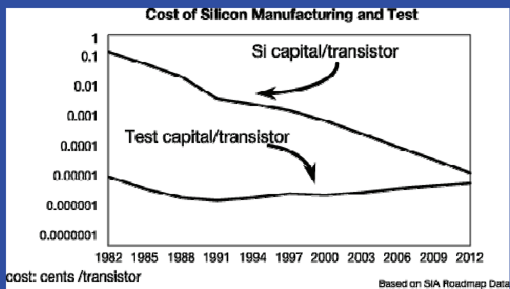


- Package / Application drive secondary requirements
  - Co-planarity
  - Pin Travel
  - Life cycle requirement
  - Etc.

- Pitch / Frequency most compelling technology force
  - Today's mainstream: 0.6 – 1.0 mm / 1 – 4 GHz
  - 2008 - 2009: 0.5 – 0.8 mm / up to 10 GHz
- Power has stabilized
- C-res – varies by application (BI/Test/Sys Test)

3/2008 Contact Pin Complexities: Valuing Performance and Cost 5

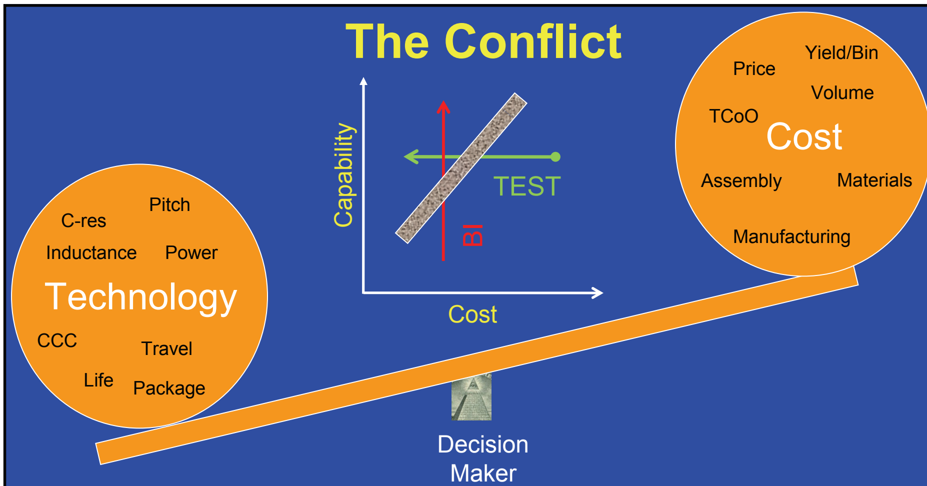
Cost Background



- Tooling Cost per pin improves generation to generation
  - Reached plateau based on capability of current mainstream technology (probe pins) and technology requirements (pitch / electrical)
- Next generation requirements may increase cost / pin price

3/2008 Contact Pin Complexities: Valuing Performance and Cost 6

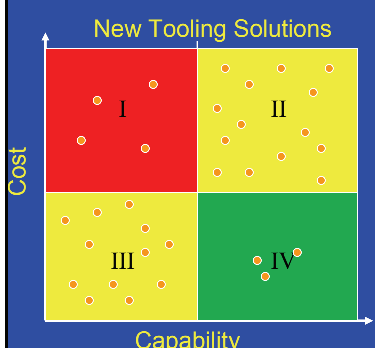
The Conflict



- Gross margin / ASP pressures have lead to new paradigm
  - BI: Better capability at same cost / Test: Same capability at lower cost
- Need to optimize performance and cost never been greater
- Key concern is where does the envelope stop e.g. where does quality suffer at expense of cost

3/2008 Contact Pin Complexities: Valuing Performance and Cost 7

The Development Challenge

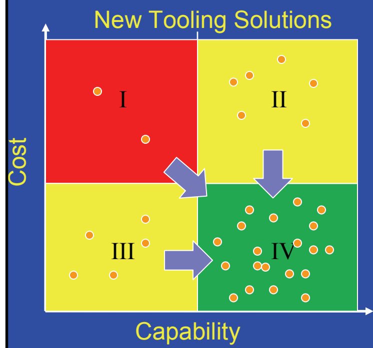


- Zone I: Character Building Zone
  - Often seen by early adaptors
- Zone II: Necessary Evil
  - Product must have the capability
- Zone III: Settle For Zone
  - Low cost, but sacrifice capability e.g. yield, retest, Bin split, etc.
- Zone IV: Cheap and Good
  - Does the grail of contact solutions exist?

- New tooling development = f(cost, resources, capability, lead time…)
- Too often, mutually exclusive

3/2008 Contact Pin Complexities: Valuing Performance and Cost 8

The Development Challenge



- Customer Desire/Industry Goal: Migrate as many new development programs into a single technology (Zone IV)

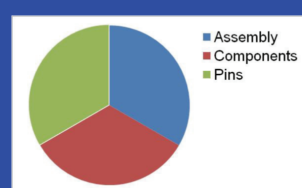
Nature of industry is that all 4 zones will exist

- Standardization benefits all
  - Reduces development lead times / resources / costs
  - Enables economies of scale
    - Reduces manufacturing / component / assembly costs
  - Reduces product lead time & inventory costs

3/2008 Contact Pin Complexities: Valuing Performance and Cost 9

Contact Solution Comparison

- Three primary solutions:
  – Stamped (BI)
  – Probe / Membrane (Test/Sys Test)



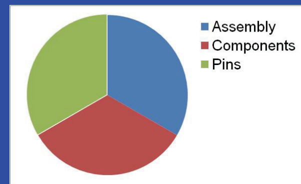
	Relative Performance of Test and Burn-in Technologies			
		Stamped Socket	Probe Pin Socket	Membrane Socket
Electrical	Current Carring Capacity Amps (higher the better)	~ 1	2+	2+
Electrical	Resistance mOhms (lower the better)	50	100	10
Electrical	Inductance nH (lower the better)	6	2	0.4
Mechnical	Life of Contact Thousands of cycles	10	250+	25
Mechnical	Contact Travel (mm)	~ 0.2 - 0.5	.50+	0.10
Production Costs	Assembly of Socket Method - Automation or Manual	A	M	M
Production Costs	Cost Contact cost per pin	A	B	C

Relative Cost: A < B, C

3/2008 Contact Pin Complexities: Valuing Performance and Cost 10

Contact Solution Comparison

- Three primary solutions:
  - Stamped (BI)
  - Probe / Membrane (Test/Sys Test)



	Relative Performance of Test and Burn-in Technologies			
		Stamped Socket	Probe Pin Socket	Membrane Socket
Electrical	Current Carring Capacity Amps (higher the better)	~ 1	2+	2+
Electrical	Resistance mOhms (lower the better)	50	100	10
Electrical	Inductance nH (lower the better)	6	2	0.4
Mechnical	Life of Contact Thousands of cycles	10	250+	25
Mechnical	Contact Travel (mm)	~ 0.2 - 0.5	.50+	0.10
Production Costs	Assembly of Socket Method - Automation or Manual	A	M	M
Production Costs	Cost Contact cost per pin	A	B	C

Relative Cost:
A < B, C

3/2008 Contact Pin Complexities: Valuing Performance and Cost 11

Optimal Solution

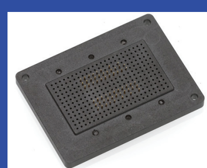
	Attribute	*Optimal pin?*
Electrical	Current Carring Capacity Amps (higher the better)	2+
Electrical	Resistance mOhms (lower the better)	35
Electrical	Inductance nH (lower the better)	0.9
Mechnical	Life of Contact Thousands of cycles	250+
Mechnical	Contact Travel (mm)	.50+
Production Costs	Assembly of Socket Method - Automation or Manual	A
Production Costs	Cost Contact cost per pin	D

- Use best technical capability as a technology target
  - Broad product envelope
- Cost – Establish breakthrough cost/ performance capability
  - Lower TCoO – everything from price & delivery to probe life & yield
- Design for manufacturing
  - Automated assembly
  - Quality & reliability

3/2008 Contact Pin Complexities: Valuing Performance and Cost 12

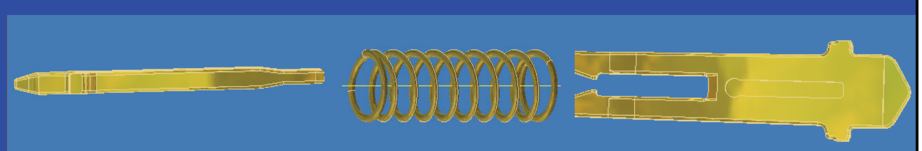
H-pin Solution

	Relative Performance of Test and Burn-in Technologies				
	Attribute	Stamped Socket	Probe Pin Socket	Membrane Socket	*H-pin*
Electrical	Current Carring Capacity Amps (higher the better)	~ 1	2+	2+	2+
	Resistance mOhms (lower the better)	50	100	10	35
	Inductance nH (lower the better)	6	2	0.4	0.9
Mechnical	Life of Contact Thousands of cycles	10	250+	25	250+
	Contact Travel (mm)	~ 0.2 - 0.5	.50+	0.10	.50+
Production Costs	Assembly of Socket Method - Automation or Manual	A	M	M	A
	Cost Contact cost per pin	A	B	C	D

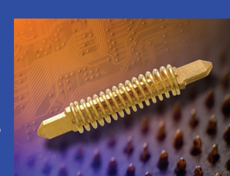


3/2008 Contact Pin Complexities: Valuing Performance and Cost 13

H-pin™ Innovation

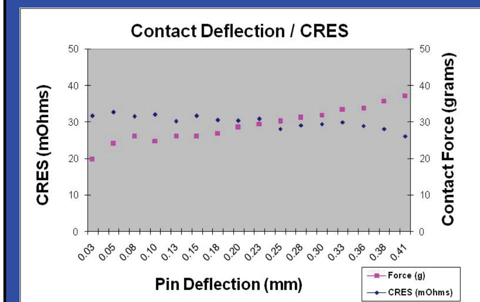


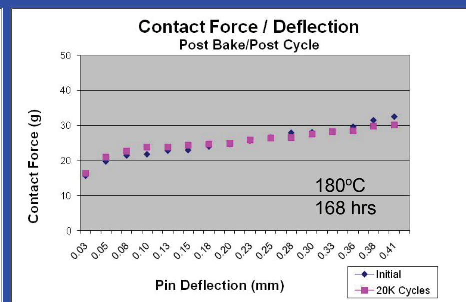
- H-pin: Patented pin technology
  - Electrical path comparable to stamped single beam pin
  - High performance of traditional probe / economies of scale of high volume stamping process
  - Scalable for variety of pitches:
    - 0.5 mm ~1.0+ mm
  - BI / Test / Sys Test / Connector applications



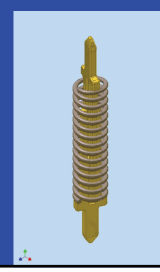
3/2008 Contact Pin Complexities: Valuing Performance and Cost 14

H-pin™ Performance





- H-pin delivers electrical performance through full stroke
- Excellent durability / stress relaxation performance
  - Negligible contact force change after bake
  - Stable lab performance to 250K cycles



3/2008 Contact Pin Complexities: Valuing Performance and Cost

H-pin™ Performance

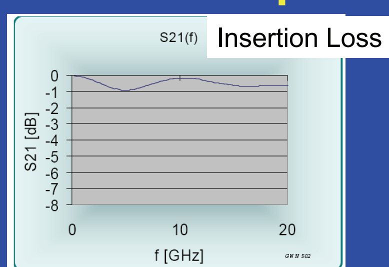


Figure 23 Insertion loss S21 (f) and S12 (f)

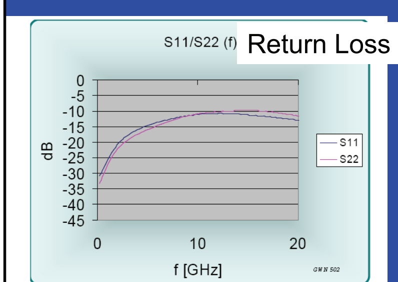


Figure 25 S11 magnitude (f) for the thru measurements into a 50 Ohm probe

0.5mm H-pin Performance

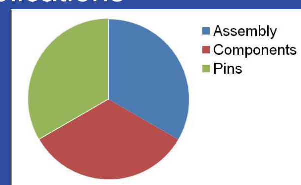
Attribute	Performance
Pin to Pad Resistance	< 40mΩ
Self-Inductance	0.88 nH
Single-ended Insertion Loss	< 1dB to 20 GHz
Single-ended Return Loss	< -10dB to 20 GHz
Differential Return Loss	-17.5 dB @ 5GHz
Differential Insertion Loss	-25dB @ 11.75 GHz
Near End Cross Talk	-25dB @ 14.8 GHz
Far End Cross Talk	-25dB @ 7.5 GHz

3/2008 Contact Pin Complexities: Valuing Performance and Cost 16

H-pin Innovation

Features:	Benefits:
0.40mm to 0.70mm Travel	Compliancy for Large Package Warpage
Flat Spring Rate	Stable Contact Resistance and Force
BeCu H-PIN™	Solid Beam Electrical Performance
Stainless Steel Core Spring	Compliancy at High Temperatures (180C+)
Bandwidth -1dB @ 15GHz	Correlated BI, System Evaluation and Test
Current Carrying Capacity	Reliable Power and Ground Contact
High Volume Stamping *	Stocked Inventory and Better Lead Time
Automated Pin Assembly *	High Volume Capacity and Quality Control
Reel-to-Reel Pin Insertion *	High Volume Capacity and Ease of Use

- H-pin reduces TCO
  - Single solution for wide array of applications
  - High volume process
    - Competitive price
    - Automated assembly
  - Short lead times / delivery



3/2008 Contact Pin Complexities: Valuing Performance and Cost 17

Conclusion

- Product enabling through technical innovation continues as our collective goal
- Technology at any cost is long gone and is now focused on best affordable capability
- Current technologies generally offer either technical capability or cost capability
- New H-pin technology is a new technology that combines both in a single solution

3/2008 Contact Pin Complexities: Valuing Performance and Cost 18

Thank You!

Q & A

3/2008 Contact Pin Complexities: Valuing Performance and Cost 19

New Concept in Spring Probe Design

RIKA DENSHI AMERICA, INC.
John Winter – Engineering Manager
Larre Nelson – General Manager
Amos Friedner – Sales Manager

BITS Workshop
March 9-12, 2008

Outline

- Motivation
  - Improve contact resistance
  - Improve high frequency response issue
- Solution
  - Concept
  - Customer requirements / wish list
  - Design
- Results
- Benefits

Design Objectives

- Contact resistance improvements
  - Improve contact resistance / standard deviation
  - Maintain short operating length
  - Maintain long cycle life
  - Reduce wear due to bias construction
  - Maintain consistent spring force vs. deflection
- Frequency response improvements
  - Improve signal integrity – static and dynamic

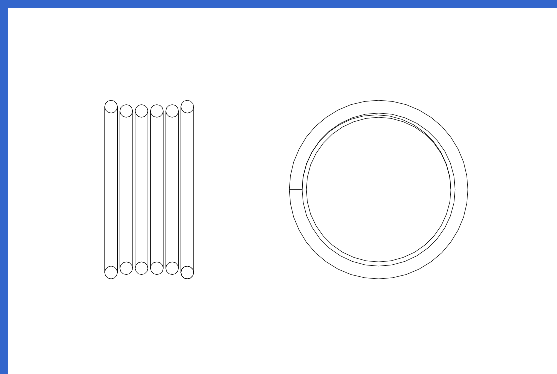
3/2008 New Concept in Spring Probe Design 3

Market Requirements

- Short operating length
- Low contact resistance standard deviation
- Long travel
- Consistent and smooth spring force vs deflection
- Higher current carrying capacity

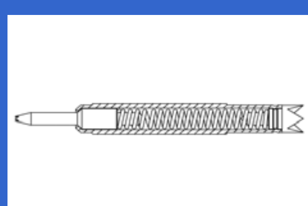
3/2008 New Concept in Spring Probe Design 4

Solution - Spring Sleeve

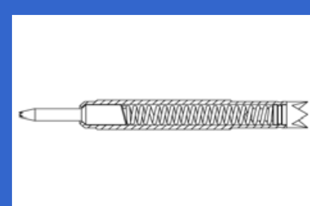


3/2008 New Concept in Spring Probe Design 5

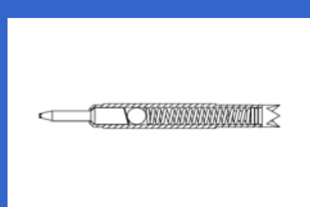
Standard Probe



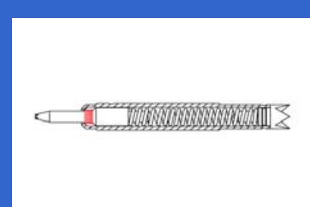
Bias Probe w/out ball



Bias Ball Probe



Probe w/Spring Sleeve

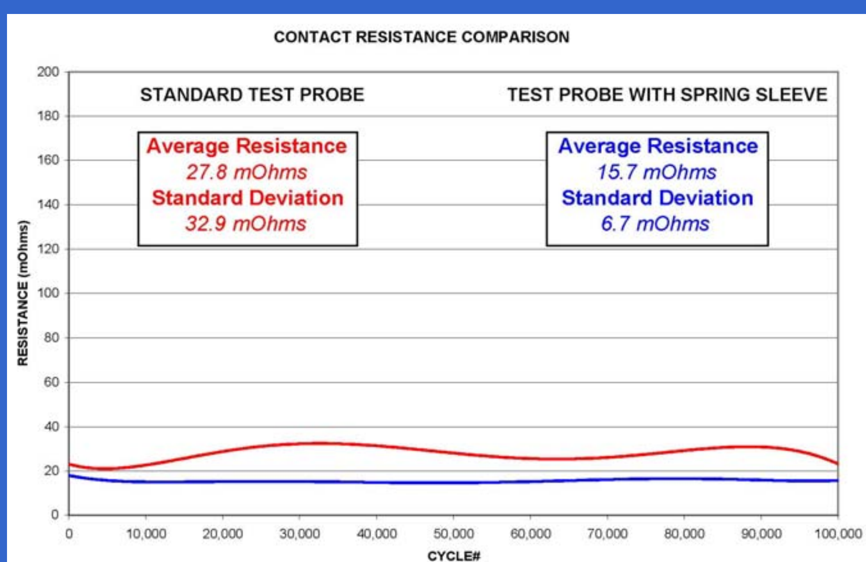


3/2008 New Concept in Spring Probe Design 6

Probe with Spring Sleeve

3/2008 New Concept in Spring Probe Design 7

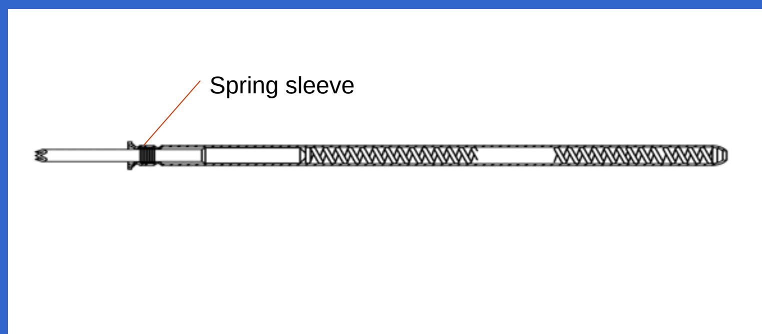
Contact resistance



3/2008 New Concept in Spring Probe Design 8

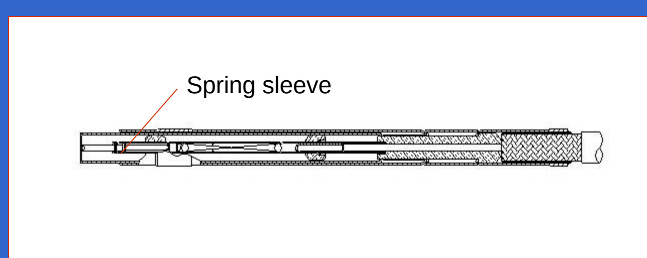
Paper #2

Single ended probe



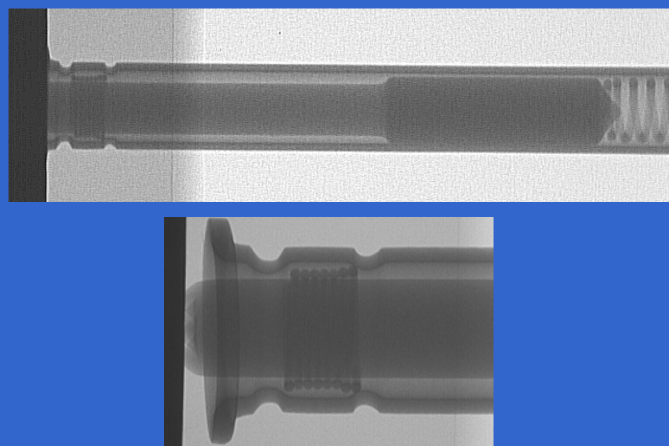
3/2008 New Concept in Spring Probe Design 9

Coaxial probe with spring sleeve



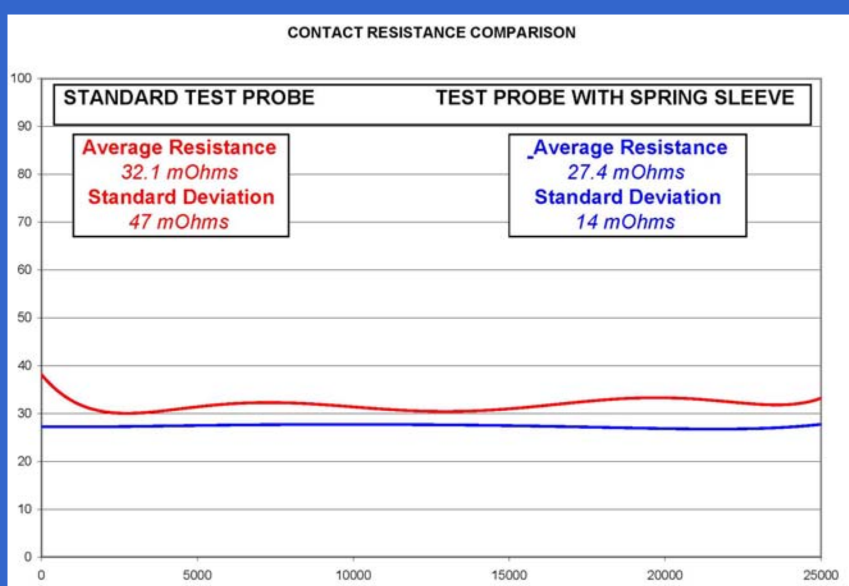
3/2008 New Concept in Spring Probe Design 10

Single ended x-ray image



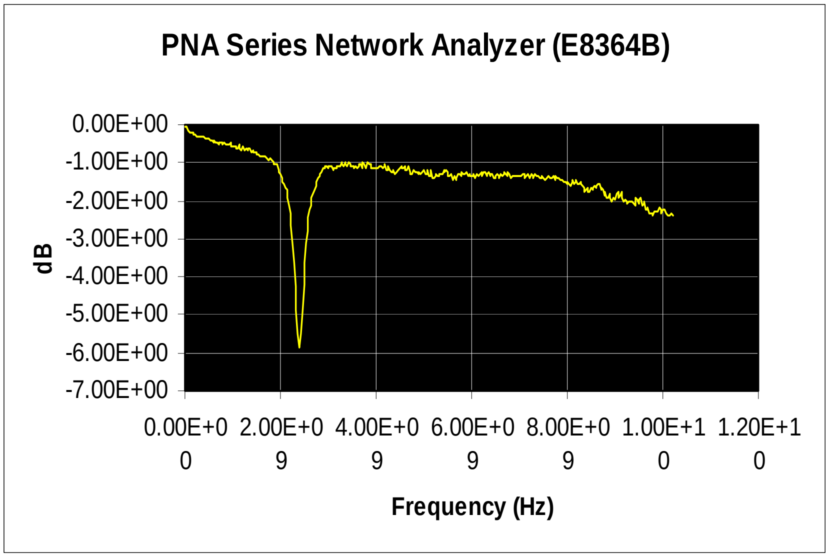
3/2008 New Concept in Spring Probe Design 11

Contact resistance



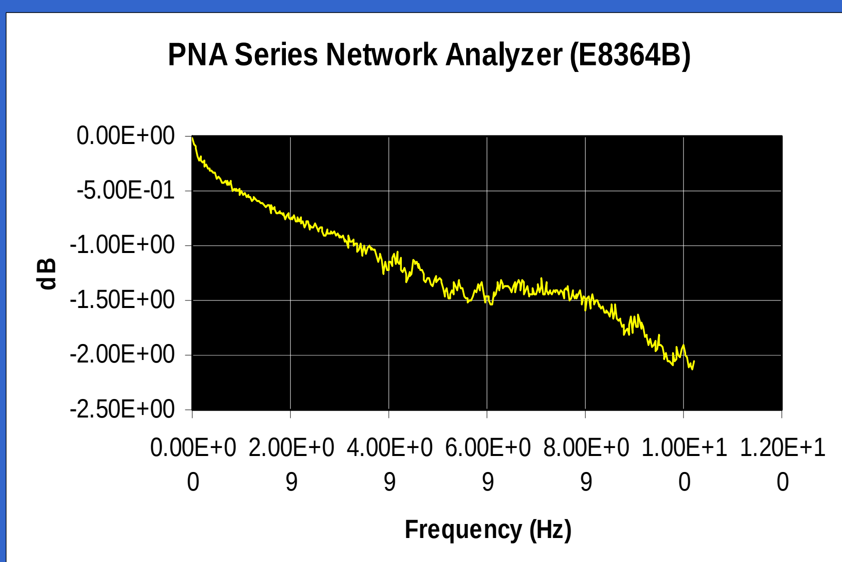
3/2008 New Concept in Spring Probe Design 12

Test probe without spring sleeve



3/2008 New Concept in Spring Probe Design 13

Test probe with spring sleeve



3/2008 New Concept in Spring Probe Design 14

Benefits

- Consistent electrical performance
- Improved current carrying capacity
- Consistent / smooth force vs. deflection
- Enables shorter probe designs
- Can easily be added to most probe designs
- Longer cycle life than bias constructed probe

3/2008 New Concept in Spring Probe Design 15

Non-Contact System-in-Package Testing

SCANIMETRICS

2008 Burn-in and Test Socket Workshop

Chris Sellathamby, Brian Moore, Jeff Hintzke

Purpose

- Show how a wireless testing technique can overcome the multiple testing issues encountered with Silicon-based System in Package (SiP) devices
- Propose applications for wafer-level and package burn-in

03/2008 Non-Contact System-in-Package Testing 2

Outline

- Silicon-based System-in-Package (SiP) technology
- SiP testing challenge
- Non-contact test access technology
- SiP testing by WiTAP™
- Wafer-level burn-in of SiPs
- Summary

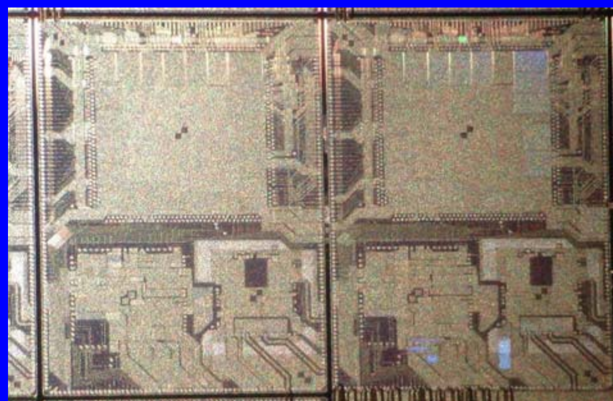
03/2008 Non-Contact System-in-Package Testing 3

Silicon Substrate System in Package

- Silicon serves as chip carrier
- Substrate contains interconnect and passive components
- Built using IC technologies
- SiP assembled on the wafer
- Package often built like wafer level package

03/2008 Non-Contact System-in-Package Testing 4

Example of Silicon Based SiP Substrate



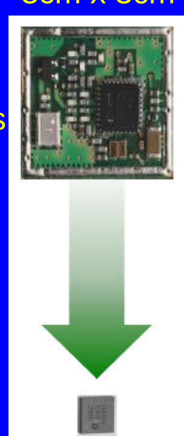
Bare SiP Substrate

03/2008 Non-Contact System-in-Package Testing 5

Silicon Based SiPs

3cm x 3cm

1 Chip
42 passives

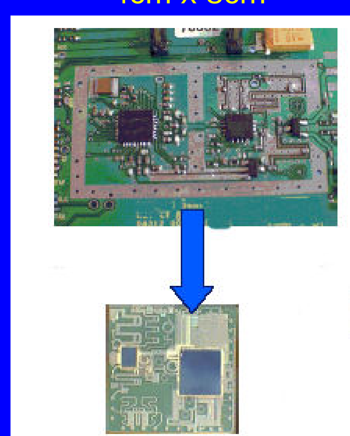


1 Chip +
Si-based
Substrate

1cm x 1cm

4cm x 8cm

2 Chips
86 passives



2 Chip +
Si-based
Substrate

3cm x 3cm

03/2008 Non-Contact System-in-Package Testing 6

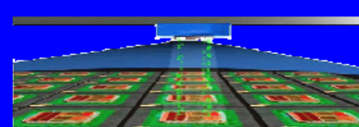
SiP Testing Issues

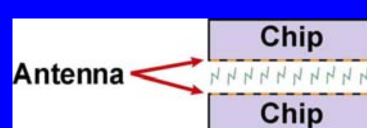
- Internal nodes hidden
- SiPs don’t use BIST or DFT
  - Individual die often have scan
- Substrate Damage from probing
- 3D
  - Varied topologies
    - Stacked die, wirebonds, flipchip
- Burn-in of assembled devices

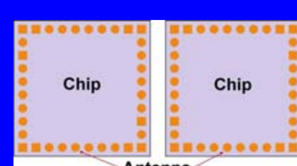
03/2008 Non-Contact System-in-Package Testing 7

Non-Contact Interconnect Technology

- Wireless chip-scale communications
- Distances < 100 µm
- Micro TX/RX on chip
- One TX/RX per I/O
- Fully CMOS compatible
- Power via standard probe, all other signals wireless
- Data scales to > 1 Gbps

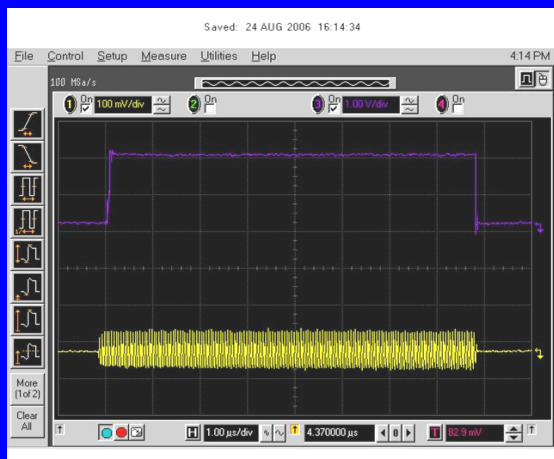






03/2008 Non-Contact System-in-Package Testing 8

Receiver



Data Out

RF (AM) In

03/2008 Non-Contact System-in-Package Testing 9

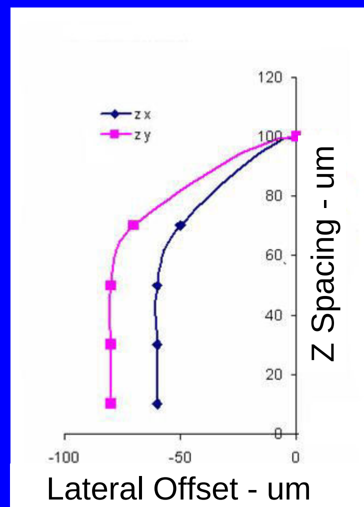
Non-contact Test Example

Non-contact JTAG enquiry and response

03/2008 Non-Contact System-in-Package Testing 10

Alignment Sensitivity

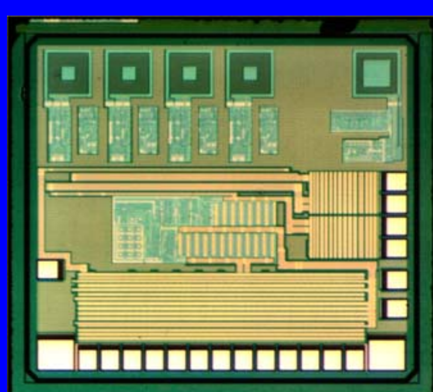
- BER vs. Alignment
- 120um antennas
- 20MHz Clock
- The zone inside the curve has an error rate less than one error per 10^10 bits.



03/2008 Non-Contact System-in-Package Testing 11

WiTAP^{TM} Chip

WiTAP™ - Wireless Test Access Port



- Standard 130nm CMOS Process
- 1.1mm x 1.2mm
- JTAG Test controller
- 3 Independent scan chains
- 1.8V input supply
- 1.2V and 1.8V output supplies
- Intelligent power control

03/2008 Non-Contact System-in-Package Testing 12

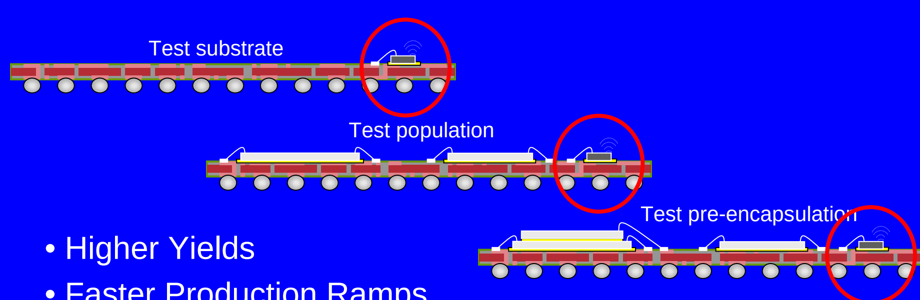
WiTAP™

- Wireless Test Access Port for SiP
- JTAG and Boundary Scan testing
- Replaces probes with wireless transceivers
- All SiP power supplied through WiTAP™ chip
- Allows test during build, before final packaging
- Allows testing of hidden test points
- Can be used with stacked chips

03/2008 Non-Contact System-in-Package Testing 13

SiP Testing with the WiTAP™

- JTAG test controller with Integrated RF transceivers
- Assembled on the SiP substrate early in the assembly process
- Test the SiP assembly multiple times during the process



- Higher Yields
- Faster Production Ramps
- Lower manufacturing costs

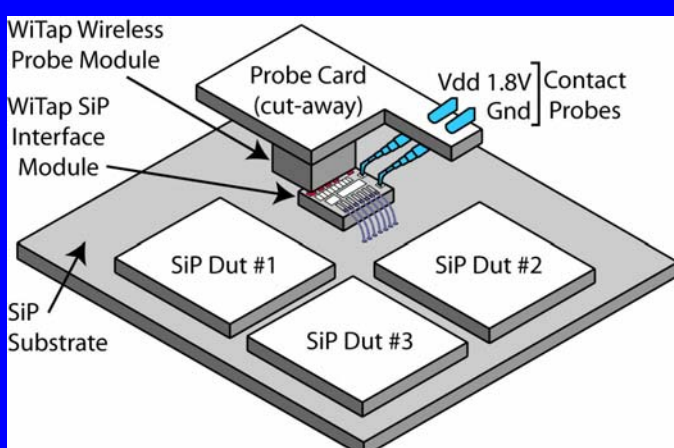
03/2008 Non-Contact System-in-Package Testing 14

WiTAP™ Advantage

- Technology is “non-contact” for data signals
  - manufacturing process can be monitored
  - chips can be smaller
  - more chips can be tested at once
- Test when/where no test was possible before
- Reduce SiPs production costs
- Enables wafer-level burn-in
  - Very high parallelism is possible

03/2008 Non-Contact System-in-Package Testing 15

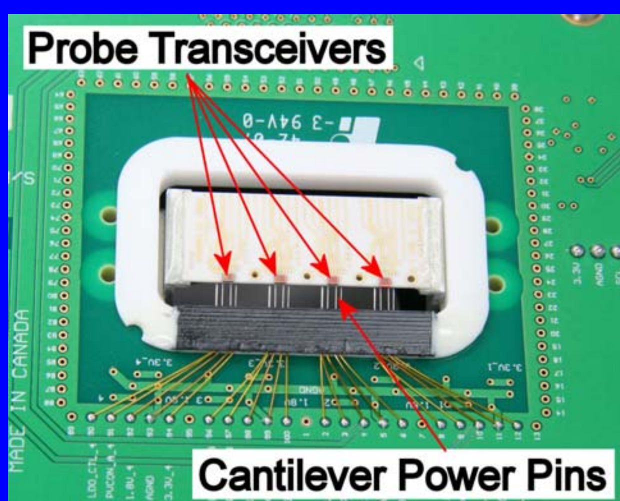
Probing with WiTAP™



03/2008 Non-Contact System-in-Package Testing 16

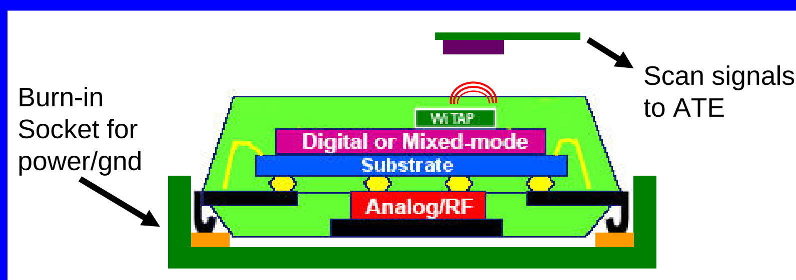
Probecard - Top View

Probecard – Bottom View



Package Burn-in Concept

- Wireless channels communicate through package
- Power/Gnd by simplified burn-in socket



03/2008 Non-Contact System-in-Package Testing 19

Conclusions

- WiTAP™ solution for SiP testing application
- Parallel WiTAP™ SiP x4 in production
- High parallel Wafer-level burn-in possible

03/2008 Non-Contact System-in-Package Testing 20