



2008

Session 4

ARCHIVE 2008

THERMAL ISSUES - A BETTER UNDERSTANDING

“Thermal Design and Analysis”

Harlan Faller

Johnstech International

“Chasing Die Temp—What Impacts the Actual Die Temp in Burn-in? How About the Socket?”

Mike Noel, Doug Grover, Doug Laing, Dan Wilcox

Freescale Semiconductor

“Metal Interface Materials for Burn-in Applications”

Jordan Ross

Indium Corporation

“Optimized Air Cooled Test Socket”

Grant Wagner, David Gardell

IBM Microelectronics

March 9 – 12, 2008

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Thermal Design and Analysis

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008



Harlan Faller, P.E.
Johnstech International

Johnstech[®]

Agenda

- Introduction
- Concepts of Heat & Heat Transfer
- Thermal Characteristics of Selected Materials
- Critical Factors of Thermal Paths
- Thermal Analysis of DUT/Test Socket/LB
- Case Study With Data
- Conclusions
- Glossary of Terms
- Appendix

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Introduction

- **Objective of this Presentation:**
 - To demonstrate how Thermal Concepts and Laws are applied to Test Socket Analysis.
- **Goal:**
 - To provide a Set of Guidelines to users of the methodology presented herein.
- **Future Work:**
 - Expand on the Guidelines and formalize them into a spreadsheet.

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Concepts of Heat & Heat Transfer

- **Thermodynamics**
 - Deals with Systems in Equilibrium
 - Will predict State Change in Equilibrium
 - Won't predict Rate of Change of a System not in Equilibrium
- **Heat Transfer**
 - Will predict Energy Transfer between Material Bodies resulting from Thermal difference
 - Will predict Rate of Heat Exchange
 - Obeys the Laws of Thermodynamics

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Laws of Thermodynamics

- **Zeroth Law**
 - If two Thermodynamic Systems are in Thermal Equilibrium with a third, they are in Thermal Equilibrium with each other.
- **First Law**
 - In any process, the Total Energy of the Universe remains constant.
 - Energy cannot be created or destroyed.

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Laws of Thermodynamics

- **Second Law**
 - Energy Systems have a tendency to increase their Entropy (Heat Transfer Content) rather than decrease it.
- **Third Law**
 - As the Temperature approaches absolute zero, the Entropy of a System approaches a constant.

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Mechanisms of Heat Transfer

- **Conduction:** $Q = -kA(\Delta T)/L$
- **Convection:** $Q = h_c A(T_s - T_m)$
- **Radiation:** $Q = \epsilon \sigma F_{1,2} A(T_1^4 - T_2^4)$

-
- Q = Quantity of Heat Transferred (Watts)
 - k = Thermal Conductivity of Material (W/m-K)
 - A = Cross-Sectional Area (m²)
 - ΔT = Temperature Difference (°C)
 - L = Length of Heat Transfer Path (m)
 - h_c = Coefficient of Convective Heat Transfer (W/m-K)
 - T_s, T_m = Temperature of Surface and Media (°C)
 - ε = Emissivity of radiating Surface (dimensionless)
 - σ = Stefan-Boltzmann Constant (5.67x10⁻⁸ W/m²-K⁴)
 - F_{1,2} = Shape Factor between Surface Area of Body 1 & 2 (≤1.0)
 - T_{1,2} = Surface Temperature of Bodies (Kelvin)

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Thermal Characteristics of Materials

MATERIAL	CONDUCTIVITY	SPECIFIED HEAT
Ag	429.0 W/m-K	235 J/Kg-K
Cu	401.0	384
Au	319.0	129
Al	237.0	903
W	173.0	125
Ni	90.4	444
Be-Cu	90.0	420
Fe	80.4	450
Pt	71.6	133
Sn	66.8	227
Pb	35.3	128

Source: Ruben, S., Handbook Of The Elements (Open Court: La Salle, IL 1996)

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Reasons for Cooling DUT's in Test

- Heat causes Noise in Electronic Circuits.
- Non-Dissipated Heat increases Junction Temperature of the Die.
 - +150°C max. for GaAs
 - +175°C max. for Silicon
- Cooling can increase Semiconductor Performance, Life and Reliability.
- Every 10°C increase in Junction Temperature reduces Life by 50%.

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Critical Factors of Thermal Paths

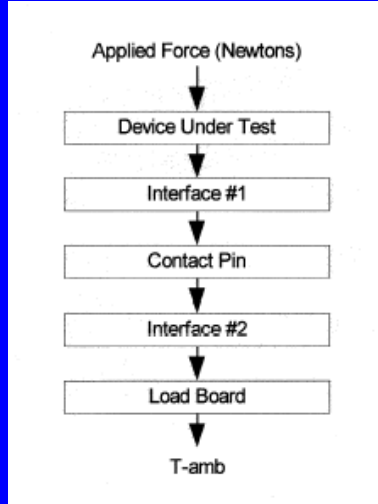
- Pressure at the Interface
- Hardness of the Contact Surfaces
- Size of the Contact Surface Asperities
- Geometry of Contacting Surfaces
- Average Gap Thickness of Void Spaces
- Thermal Conductivity of Fluid in Void Spaces
- Thermal Conductivity of Contact Materials

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Interface Geometry for DUT/TS/LB



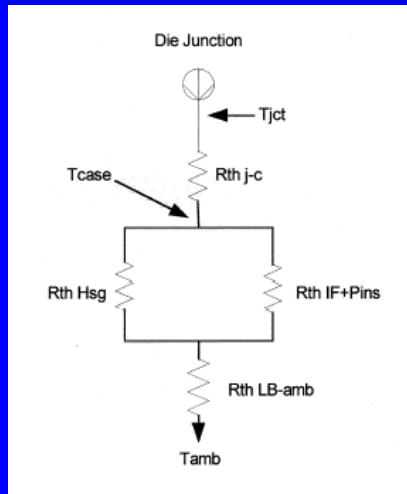
Block Diagram of Interface Geometry

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Interface Geometry for DUT/TS/LB



Schematic Diagram of Interface Geometry

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Interface Geometry for DUT/TS/LB

- Per Schematic Diagram on previous slide:

$R_{th_{j-c}} = \theta_{j-c}$ = Thermal Resistance,
Die Junction to Case

$R_{th_{if-pins}} = \theta_{if-pins}$ = Thermal Resistance,
Interfaces + Contacts

$R_{th_{hsg}} = \theta_{hsg}$ = Thermal Resistance of
Socket Housing

$R_{th_{LB-amb}} = \theta_{LB-amb}$ = Thermal Resistance,
Load Board to Ambient Air

$\theta_{Total} = \theta_{j-c} + [\theta_{if-cp} \parallel \theta_{hsg}] + \theta_{LB-amb}$

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Interface Geometry for DUT/TS/LB

- For Semiconductors, θ_{j-c} is an internal function of Design and Manufacturing Techniques.
- Plastic Semiconductor Cases are often used for low-power Devices. In some cases, θ_{j-c} could be $>50^{\circ}\text{C/W}$.

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Thermal Resistance

- Heat Transfer can be defined in terms of Thermal Resistance, θ :
 - $\theta = \Delta T/Q$ °C/W
 - Q = Quantity of Heat Transferred (Watts)
 - ΔT = Temperature Difference between two Surfaces (°C)
 - θ characterizes the Transmission of Heat through the Heat Transfer Path

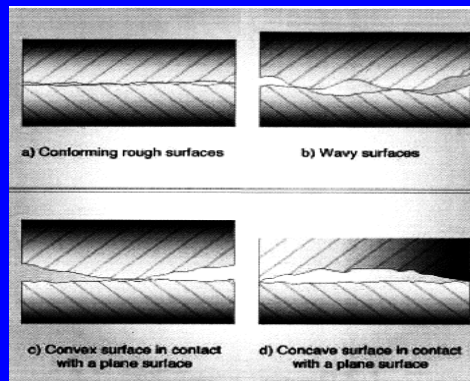
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Mounting Interface

- Mounting Interface is a critical area of Heat Transfer.
- Heat is conducted when Surfaces touch. \longrightarrow
 - Usually only 1% - 5% of Total Surface Area



Source: *Electronics Cooling Magazine*, May 1997

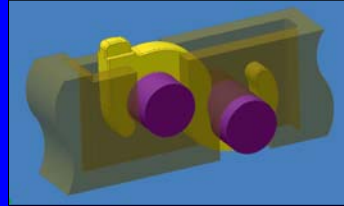
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Case Study:

Heat Transfer through 2mm “S” Contacts to Ambient Air for DUT / TS / LB



- DUT: 7x7mm, 48 TQFN, 2.95 Watt Device
 - $\theta_{j-c} = 2^{\circ}\text{C/W}$
- Heat Load: ~2.9 Watts
- Contacts: 2mm, 0.508mm wide “S” type
- 10 Contacts in Torlon™ Housing from DUT Pad to Load Board
- Typical Thermal Resistance:
 - $\theta_{\text{Torlon}^{\circledR}} = 120^{\circ}\text{C/W}$
 - $\theta_{\text{LB-Air}} = 12^{\circ}\text{C/W}$
 - $\theta_{\text{Amb Air}} = +27^{\circ}\text{C}$

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Simplified Methodology for Case Study

- **Determine or calculate the following:**
 - Cross-Sectional Area of Contact
 - Thermal Resistance of the Contact
 - Thermal Resistance of Pad-Contact Interface
 - Thermal Resistance of Contact-Load Board Interface
 - Total Thermal Resistance of the Heat Path
- **Plug in the numbers and crank**

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Calculation of Contact's Thermal Resistance

- Determine these Contact characteristics:
 - **Volume**
 - **Mass** (dependent on Volume and Density of Material)
 - **Cross-Sectional Area** of Contact to Heat/Current Flow
- Thermal Resistance is defined as:
 - $\theta = L/kA$
 - L = Length of the Contact (m)
 - k = Thermal Conductivity of Contact material (W/m-K)
 - A = Cross-Sectional Area of the Contact (m²)

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Interface Thermal Resistance of DUT-Contact & Contact-Load Board

- Determine the following factors:
 - **Apparent and Real Area** of Contact of Interface Surfaces (m²): $A_{\text{real}} = 0.3 \times A_{\text{apparent}}$
 - **Force of Contact** (Newtons)
 - **Contact Material and Finish** (microns)
 - **Pressure on Contact** at IF (N/m²)
 - **Average Surface Roughness** of Materials at Interface (microns)
 - $\sigma_{\text{avg}} = (\sigma_1^2 + \sigma_2^2)^{1/2}$
 - σ_1 = Surface Finish of Material 1 (microns)
 - σ_2 = Surface Finish of Material 2 (microns)

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Interface Thermal Resistance of DUT-Contact & Contact-Load Board

- Determine the following factors:
 - Average Thermal Conductivity (W/m-K)
 - $k_{avg} = 2k_1k_2/(k_1 + k_2)$
 - k_1 = Thermal Conductivity of Material 1 (W/m-K)
 - k_2 = Thermal Conductivity of Material 2 (W/m-K)
 - Average Asperity Angle, $Tan \Phi$
 - $Tan\Phi_{avg} = (Tan^2\Phi_1 + Tan^2\Phi_2)^{1/2}$
 - $Tan\Phi_1$ = Asperity Angle of Material 1 (dimensionless)
 - $Tan\Phi_2$ = Asperity Angle of Material 2 (dimensionless)

Source: Remsburg, R., *Advanced Thermal Design of Electronic Equipment* (Chapman & Hall: New York, 1998)

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Heat Transfer through an Interface

- $h_i = 1.45k_{avg}(P/H)^{0.985}Tan\Phi_{avg}/\sigma_{avg}$
 - h_i = Heat Transfer Coefficient (W/m²-K)
 - P = Pressure at Interface (N/m²)
 - H = Hardness of Softer Material at Interface (N/m²)
- $h_{ga} = k/y = k/[(y/\sigma) \times \sigma_{avg}]$ W/m²-K
 - k = Thermal Conductivity of Gap Media (air = 0.0252 W/m-K)
 - y/σ = Constant (use "8" as an average for machined surfaces)
- $h_a = h_i + h_{ga}$ (W/m²-K)
- $\theta_a = (h_a \times A_{app})^{-1} \text{ } ^\circ\text{C/W}$

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Case Study Data:

- | <u>Parameters</u> | <u>DUT Pad</u> | <u>Contact</u> | <u>Load Board</u> |
|-------------------------------------|----------------------|----------------------|----------------------|
| Surface Finish (microns) | 1.6x10 ⁻⁶ | 1.6x10 ⁻⁶ | 1.6x10 ⁻⁶ |
| TanΦ _n | 0.15 | 0.15 | 0.15 |
| Thermal Cond. (W/m-K) | 66.8 | 90.0 | 319.0 |
| Mat'l. Hardness (N/m ²) | 0.5x10 ⁸ | 5x10 ⁸ | 5x10 ⁸ |
- **Pressure @ Interface 1: 4.597x10⁷ N/m²**
 - **Pressure @ Interface 2: 3.798x10⁷N/m²**
 - **Other pertinent data on Slides 17 & 29**

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Summation of Thermal Resistances for Heat Path

- **Thermal Resistance of Interface 1 & Interface 2:**
 $\theta_{IF1} = (h_{a1} \times A_{real\ IF1})^{-1} \text{ } ^\circ\text{C/W}$
 $\theta_{IF2} = (h_{a2} \times A_{real\ IF2})^{-1} \text{ } ^\circ\text{C/W}$
- **Total Thermal Resistance of Interfaces plus Contact:**
 $\theta_{IFs+pin} = \theta_{IF1} + \theta_{pin} + \theta_{IF2} \text{ } ^\circ\text{C/W}$
- **Sum Total of Thermal Resistance for DUT/TS/LB:**
 $\theta_{j-amb} = \theta_{j-c} + [\theta_{IF-cp} \parallel \theta_{hsg}] + \theta_{LB-amb} \text{ } ^\circ\text{C/W}$
- **@T_{amb} the Die Temperature is defined as:**
 $T_{die} = T_{amb} + (\theta_{j-amb} \times P_{diss}) \text{ } ^\circ\text{C}$
 $P_{diss} = \text{Heat Conducted away from Device Die}$

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Case Study Result Calculations:

Reference: Slide 17, 2.9 Watt, 48 TQFN Device with 2mm, 0.508mm wide "S" Contacts

- $\theta_{pin} = 98.8^{\circ}\text{C/W}$
- $\theta_{IF1} = 2.6^{\circ}\text{C/W}$
- $\theta_{IF2} = 15.1^{\circ}\text{C/W}$
- $\theta_{IFs-pin} = 116.5^{\circ}\text{C/W}$
- $\theta_{c-LB} = 10 \text{ pins @ } 116.5^{\circ}\text{C/W} \parallel 120^{\circ}\text{C/W} = 10.6^{\circ}\text{C/W}$
- $\theta_{j-amb} = \theta_{j-c} + \theta_{c-LB} + \theta_{LB-amb} = 2 + 10.6 + 12 = 24.6^{\circ}\text{C/W}$
- $T_{die@+27^{\circ}\text{C}} = +27 + (24.6 \times 2.9) = 98.3^{\circ}\text{C}$
- Measured Test Results gave a **Die Temperature of 96°C.**
- The **difference** between Calculated and Measured Values is **2.3°C.**

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Conclusions

- Heat Transfer obeys the Laws of Thermodynamics.
- It is crucial to remove Heat from DUTs.
- It is possible to calculate the Heat Flow from DUTs through the Test Socket to the Environment.
- Equations were presented to use in Heat Calculations.
- Results of the Case Study were in good agreement with Measured Results.

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THANK YOU
for your time and attention!

Any Questions?

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Glossary of Terms

- **Terms and units used in Heat Transfer**
 - Heat Flux $J/m^2\cdot s$
 - Heat Transfer Rate $dQ = qA(W/m^2)$
 - Mass Density, ρ Kg/m^3
 - Specific Heat, c_p $J/Kg\cdot k$
 - Thermal Conductivity, k $W/m\cdot k$
 - Thermal Energy $Q(Joules)$
 - Thermal Resistance, θ $^{\circ}C/W$
 - Thermal Time Constant, γ $seconds$

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Appendix

Physical Properties of C110 Copper & C172 BeCu

<u>Property</u>	<u>C110 Copper</u>	<u>C172 BeCu</u>
Density	8,940 Kg/m ³	8,321.4 Kg/m ³
Elect. Resistivity	1.71x10 ⁻⁸ Ω-m	7.68x10 ⁻⁸ Ω-m
Hardness	4-9x10 ² N/mm ²	5-10x10 ² N/mm ²
Melting Point	1082.8°C	982.2°C
Specific Heat	384 J/Kg-K	420 J/Kg-K
Tensile Strength	44 Ksi	90-112 Ksi
Thermal Cond.	401.0 W/m-K	90.0 W/m-K

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Chasing Die Temp – What impacts the actual die temp in burn-in? How about the socket?

Michael Noel
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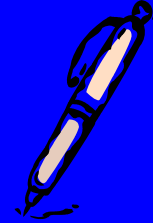


Introduction

- **Burn-in**
 - **Definition:**
 - The process of exercising an integrated circuit at elevated voltage and *temperature*
 - **Challenges**
 - Knowing temperature *of the die*
 - Minimize understress
 - Do we miss some we should have caught?
 - Minimize overstress
 - Do we damage some with too much stress?

BI Factors

- Example
 - Burn-in model targets 145 °C die temp (Tj)
 - Assume 5 °C error in temperature
 - A sample device Variation
 - Duration of BI at 140 °C = 124 Hrs
 - Duration of BI at 145 °C = 103 Hrs
 - Duration of BI at 150 °C = 87 Hrs



Significant Difference...

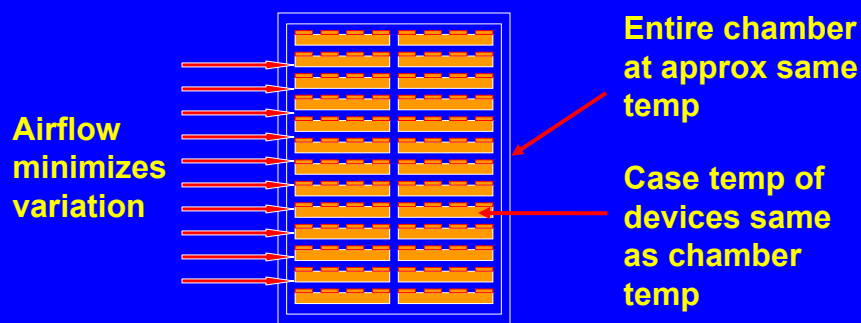
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Low power devices

- Burn-in for low power devices was simpler



- Minimal power, minimal heat rise from internal stress
- Most devices very close to same temp

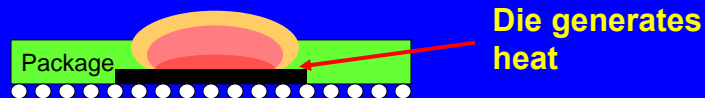
But....
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Thermal Factors

- Device technology changes
 - Smaller gates, more leakage
 - More leakage, more heat
 - More heat, more thermal issues



- As die generates heat, issue is now cooling
- Simple airflow is not enough

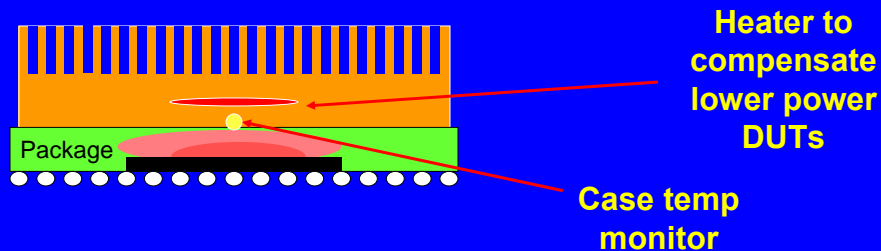
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Thermal Factors

- Not all devices are created equal
 - Variation in power consumed by each DUT
 - Controlling chamber is not enough
 - We need to **Control Each Device**
 - We install some type of active thermal control



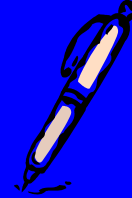
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Case temp

- Can we use case temp?
 - Power variation of 3 Watts
 - Package with 6 °C/W / TjC
 - Control all devices to a case temp
 - Temperature of junction could be 18 °C different
 - Depends on knowing TjC
 - Could be a separate topic alone
 - We could have much more variation in device power



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Chasing Die Temp

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Diode or Resistor

- We can monitor die temp using a diode or resistor
 - Are they available?
 - They require calibration
 - How do we calibrate?
 - How reliable are they?
 - What impacts the readings?
- More importantly....
 - Monitoring is not enough... we still need to **control** the temp



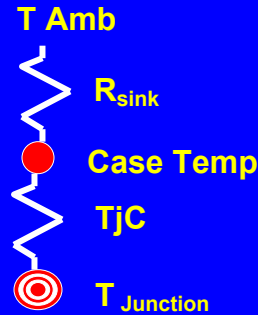
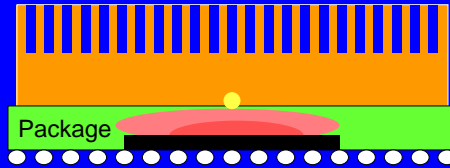
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Basic Model

- **Basic TjC model**
 - Set/Monitor case temp
 - Calculate die temp based on power and TjC



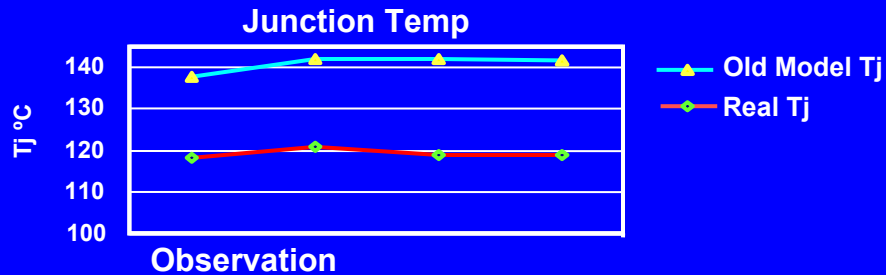
- **Two Questions:**
 - *Is this accurate enough?*
 - *What is missing.....*

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Real world example



- **Is this accurate enough?**
 - Example device shows a die temp difference of up to 25 °C

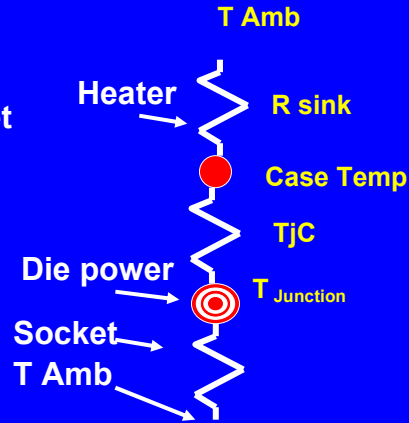
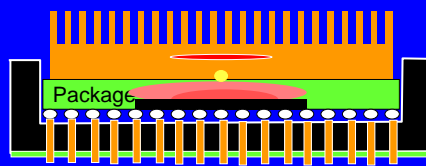
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Chasing Die Temp

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Additional considerations

- Lots of variables are missing
 - Heater in thermal path
 - Device generates heat
 - Heat path through socket
 - Ambient temperature



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Chasing Die Temp

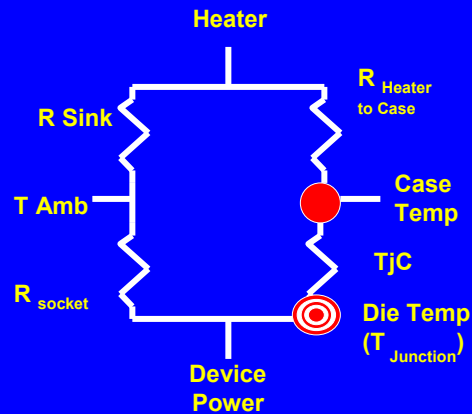
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Improved model

- A different model – one way to look at it

- Include additional variables

- Heater power
- Ambient temp
- $R_{\text{Heat sink}}$
- R_{Socket}



- How do these factors impact die temp?

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Chasing Die Temp

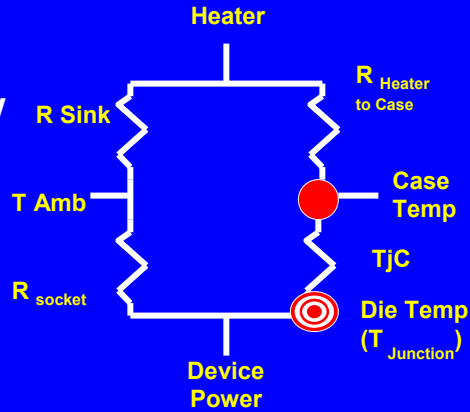
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Build a way to explain it

- Convert thermal activity to Ohms law equivalents

$V = I * R$
Becomes

$T_2 - T_1 = P * R$



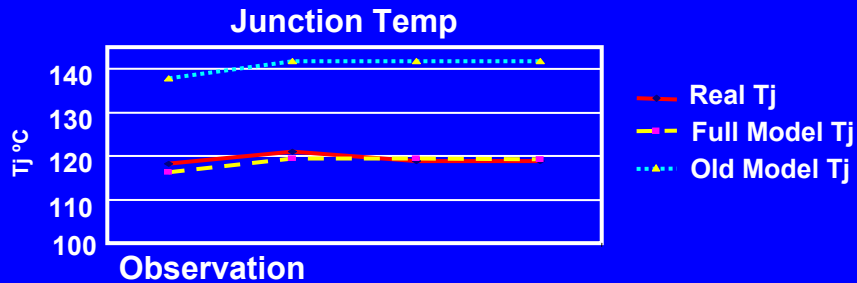
Now we can better predict behavior....

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Real world example



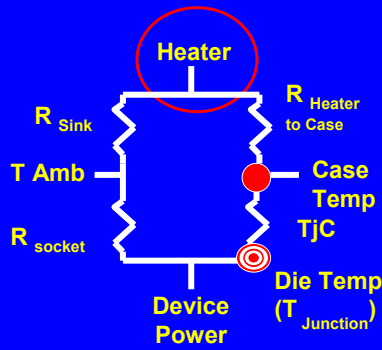
- Including additional variables increases accuracy of our predictions
- Lets look at the pieces....

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Impact of having a heater



- Heater power can have significant impact
- We now have two heat sources, one trying to add heat, the other trying to dissipate heat

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Impact of having a heater

- Ta	75 °C	75 °C
- R _{sink}	1 °C/w	1 °C/w
- TIM	0.5 °C/w	0.5 °C/w
- T _{jc}	6 °C/w	6 °C/w
- HTR	40 w	5 w
- R _{socket}	20 °C/w	20 °C/w

Die power		
Through lid	40 %	70 %
Through socket	60 %	30 %

For a 5w package, Tj Error = 8 °C

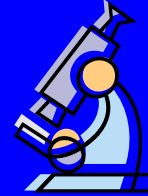
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Can we see impact of heater?

- Try an experiment:
 - Load chamber
 - Set ambient
 - Device power is off
 - Increase heater power to achieve target temp
 - Monitor diode temp
 - Repeat over several temperature ranges



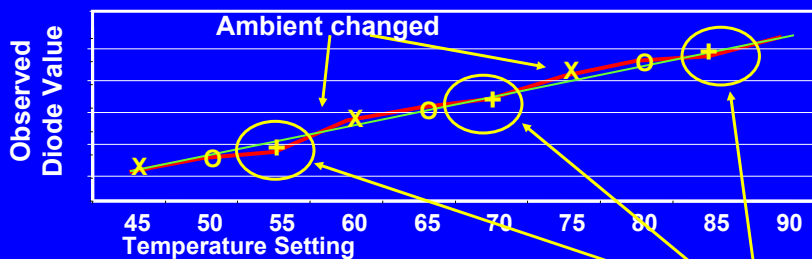
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Testing Impact of Heater

Observed Diode Value at various set points



Heater Power

- X – Approx 12 Watts
- O – Approx 18 Watts
- + – Approx 24 Watts

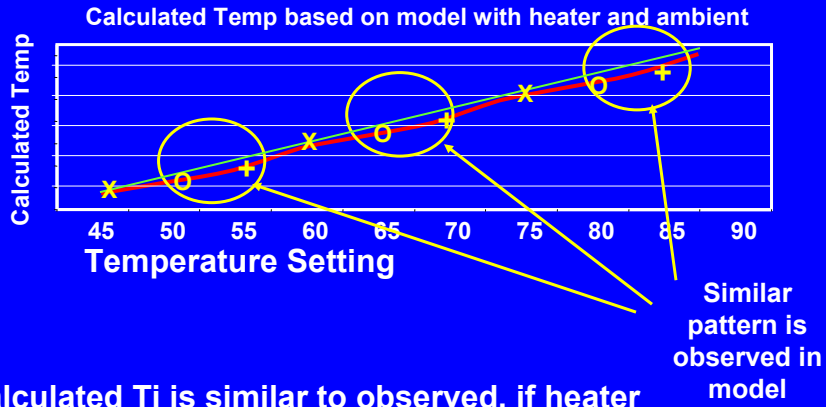
Heater Duty Cycle is changing

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What does the model predict?



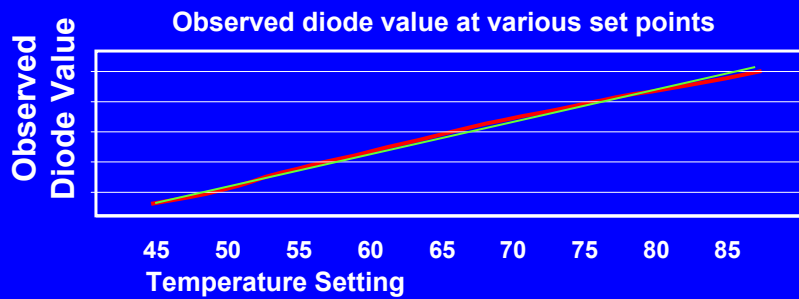
- Calculated T_j is similar to observed, if heater duty cycle and oven ambient are included
- T_j Error Increases with heater power

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Diode with no heater



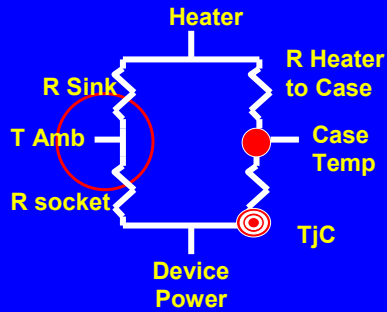
- Same device, same temps ambient only
- Die temp is much more consistent across various temps

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Impact of ambient temp



- As ambient increases, so does die temp with equal case temps
- Impacts thermal distribution between case and socket paths

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Chasing Die Temp

21

Impact of T_{ambient}

- T _{ambient}	75 °C	25 °C
- R _{sink}	1.5 °C/W	1.5 °C/W
- T _{jc}	6 °C/W	6 °C/W
- R _{socket}	60 °C/W	60 °C/W

- 5w device, set case temp to 95 °C (for planned T_j of 125 °C) gives:

- T_j Actual with
 - Ambient 75 121 °C Error of 4 °C
 - Ambient 25 116 °C Error of 9 °C

Lower values of oven ambient increase calculated error when not factored in

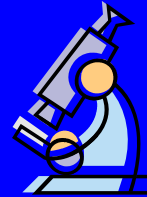
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Chasing Die Temp

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Can we see the impact of ambient?

- Try an experiment:
 - Load chamber
 - Set case temperature to fixed value
 - DUT power is on
 - Increase ambient temp in oven
 - Monitor diode temp



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Chasing Die Temp

23

Observed impact of ambient



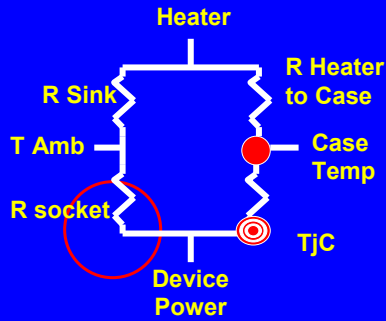
- As ambient is raised, die temp increases even if case temp if held constant
- Some impact from chicken/egg (current & temp both increasing influence each other)

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Chasing Die Temp

24

What about the socket itself?



Lower R_{socket} values give much greater error when they are not factored in

Very high R_{socket} values approximate basic model

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Chasing Die Temp

25

Impact of R_{socket}

- T_a	75 °C	75 °C	75 °C
- R_{sink}	1.5 °C/W	1.5 °C/W	1.5 °C/W
- T_{jC}	6 °C/W	6 °C/W	6 °C/W
- HTR	40 W	40 W	40 W
- R_{socket}	20 °C/W	60 °C/W	∞
T_j with T_{jC} of 6	131 °C	144 °C	148 °C
T_j with T_{jC} of 2	124 °C	129 °C	132 °C
T_{jC} of 6 Error:	17 °C		
T_{jC} of 2 Error:	4 °C		

T_{jC} has large effect, lower values minimize impact of R_{socket}

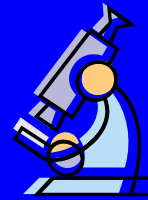
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Chasing Die Temp

26

Can we see the impact of R_{socket} ?

- Try an experiment:
 - Load chamber
 - Set case temperature to fixed value
 - DUT power is on
 - Monitor diodes
 - Remove several socket pins
 - Repeat the experiment
 - Compare the results

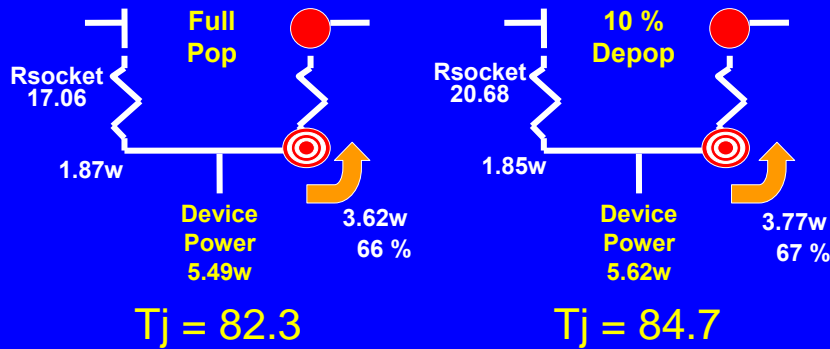


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Chasing Die Temp

27

Observed with R_{socket} change



- Increasing R_{socket} changes the thermal path
- As R_{socket} increases, die temp error increases compared to traditional model

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Chasing Die Temp

28

Observed with R_{socket} change

- Removing roughly 10% of the socket pins had a visible impact on R_{socket}
- If R_{socket} increases enough, error is minimized and T_j approaches predicted die temp from simple model
- Other factors can impact R_{socket}
 - Board composition, copper density
 - Airflow across the bottom of the board

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Chasing Die Temp

29

Summary

- Several factors impact die temp
 - Heaters
 - Heaters in thermal path can increase error
 - Ambient air temperature
 - Changing ambient air temp can impact die temp, even when case temperature is held constant
 - R_{socket}
 - Lower R_{socket} values increase error, higher values approach basic model
- Several other factors can be considered

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Chasing Die Temp

30

Summary

- Controlling die temp
 - Using thermal diodes (or resistors) is the most accurate way to monitor junction temperature

But....

If using thermal diodes, be careful to calibrate as much as possible using ambient or, if using heater, apply full model to compensate for errors

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Chasing Die Temp

31

Summary

It is possible to predict thermal behavior using a mathematical model however, the model needs to include the variables discussed earlier



There are no absolutes, all these variables interact with each other and need to be characterized

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Chasing Die Temp

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Metal Interface Materials for Burn-in Applications

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

Jordan Ross
Market Manager
Thermal Applications
Indium Corporation



Metal Interface Materials for Burn-in Applications

- Indium Corporation
- An Introduction to Metal TIMs
- The Needs in Burn-in
- Thermal Resistance vs. Pressure in Metal TIMs
- Discussion and Questions

Applications of Solder & Compressible TIM

- TIMs for the burn-in process
 - Indium
 - Indium silver
 - Indium and aluminum
- Solders for evaporators & heaters in the stack up
 - Engineered melting temps for step soldering
 - High conductivity alloys to help efficiency of design

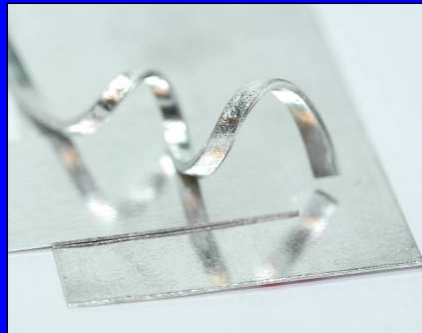
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Metal Interface Materials for Burn-in Applications

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Types of Metal TIMs for Burn-in

- Compressible Metal
 - Pure indium
 - Indium silver
 - Indium/aluminum clad



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Metal Interface Materials for Burn-in Applications

4

Attributes

- Compliant
- High conductivity
- 86W/mK
- Durable, many cycles

Material	Thermal Conductivity (W/mK)	Flow Stress (psi)
Indium	86	280
Copper	385	4800
Lead	35	1800
LMA	20	-
Grease	2	-



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Metal Interface Materials for Burn-in Applications

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Burn-in Head with Metal TIM Applied



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Features of Metal TIMs for Burn-in

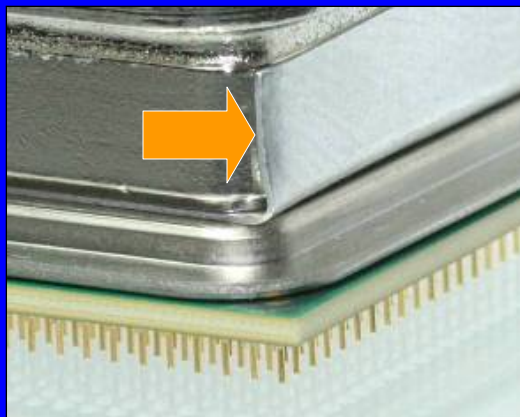
- Tabs for attach
- Custom shapes
- Custom thicknesses based on application
 - Bare die
 - Lid package
- Custom cladding
- Clean
- Faster thru put
- Longer yields

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Tabs for Attach

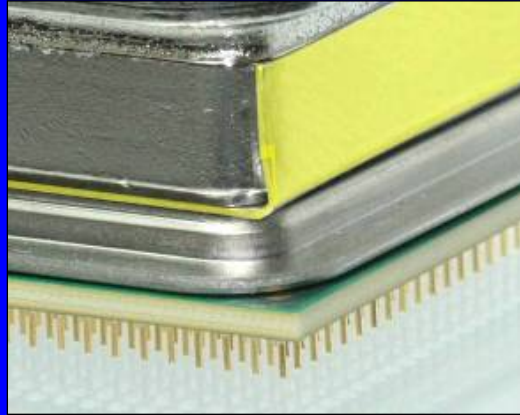


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Tabs for Attach

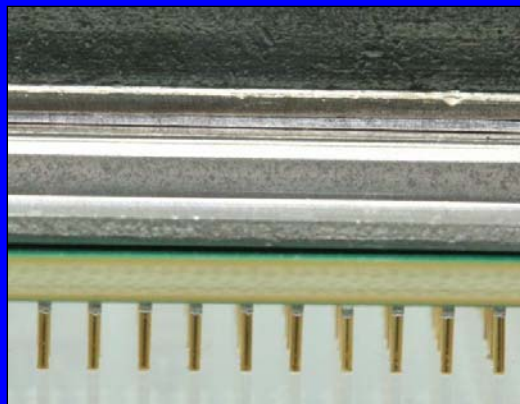


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Compliant

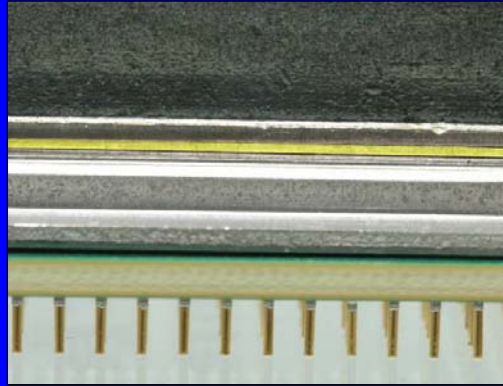


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Compliant

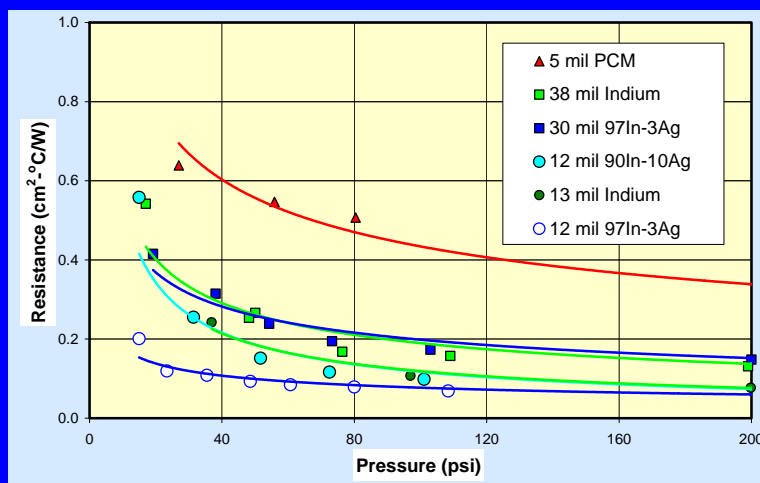


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Metal Interface Materials for Burn-in Applications

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Resistance: Baseline of Burn-in TIMs

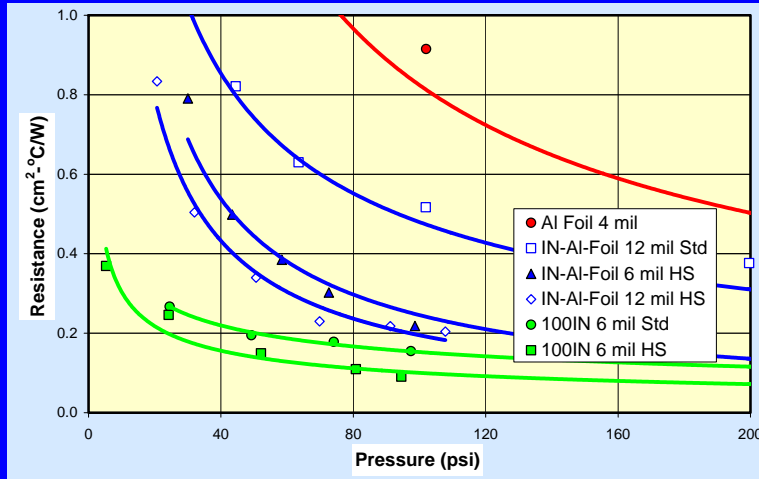


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Metal Interface Materials for Burn-in Applications

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Thermal Resistance of Metal TIMs



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Metal Interface Materials for Burn-in Applications

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Increasing Durability for Cycling, Cleanliness

- Alloy indium with silver
- Aluminum clad for no residue

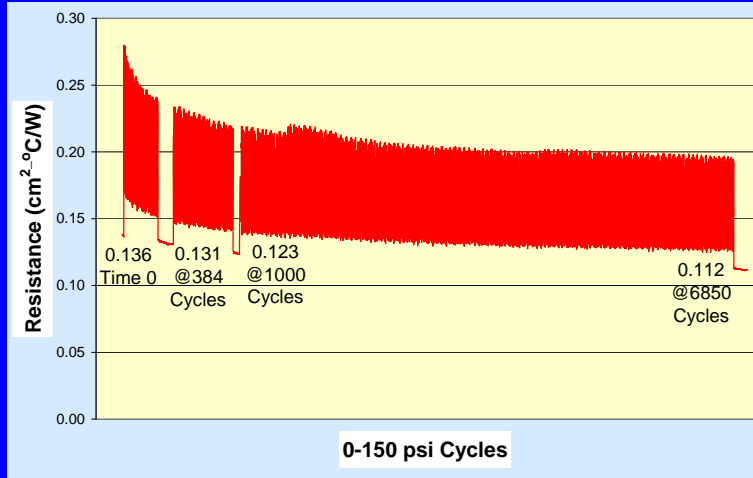


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12 mil 90In/10Ag Cycling Tests



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Metal Interface Materials for Burn-in Applications

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Solder in Burn-in Equipment

<i>Alloy</i>	<i>Melting Point (°C)</i>	<i>Composition</i>					
19	60	51	In	32.5	Bi	16.5	Sn
1E	118	52	In	48	Sn		
281	138	58	Bi	42	Sn		
290	143	97	In	3	Ag		
201	199	91	Sn	9	Zn		
238	217	90	Sn	10	Au		
121	221	96.5	Sn	3.5	Ag		
182	280	80	Au	20	Sn		
183	356	88	Au	12	Ge		
184	363	96.8	Au	3.2	Si		
176	382	95	Zn	5	Al		
186	424	55	Ge	45	Al		

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Metal Interface Materials for Burn-in Applications

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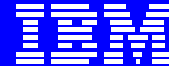
Summary

- Burn-In speed can be enhanced by high performance thermal interfaces.
- High performance thermal interfaces can accommodate multiple contacts without making a "mess" on the chips.
- Cladding or altering the alloy can increase durability and usefulness of the Metal TIM.
- The evaporator/heater stack benefits from multiple thermal interfaces made through step solder processes - without this solder, the system would not function efficiently.

Optimized Air Cooled Test Socket

2008 Burn-in and Test Socket Workshop
March 9-12, 2008

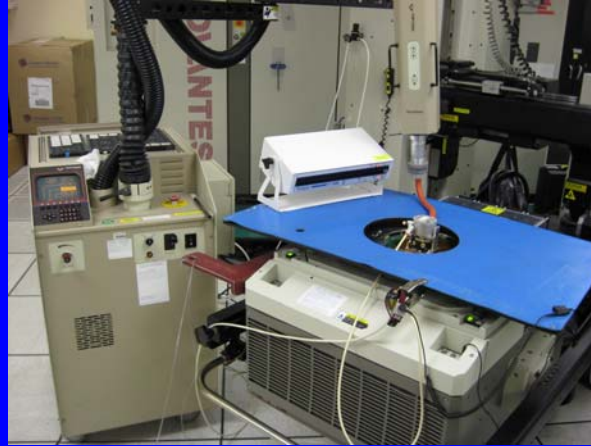
Grant Wagner - IBM
David Gardell - IBM



Overview

- Hand plug test sockets
- Historical development
 - Thermal chamber
 - Single jet impingement (UT2)
 - Multiple jet impingement
 - Liquid cooled
- Measured data
 - Thermal test chip
 - Noise
 - Pressure and flow

Handplug Test



- Used for engineering characterization
- Low volume manufacturing where automated handler not justified

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Current Test Equipment

- Dry compressed house air
- Meriam Laminar Flow Element (LFE) 50MW20-1 ½ with Smart Flow gage 2110F
 - LFE accurate to +/- 0.72% of reading
 - Accurate to +/- 0.1% FS (+/-0.06 cfm)
- Absolute pressure measured with Meriam gage
- Gage air pressure – Omega DPG1002
 - 0 to 100 psi, accuracy = 0.25% FS
 - Inlet to UT2 body at barb fitting
- SCFM flow rate calculated from measured flow corrected for:
 - Viscosity, absolute pressure, absolute temperature

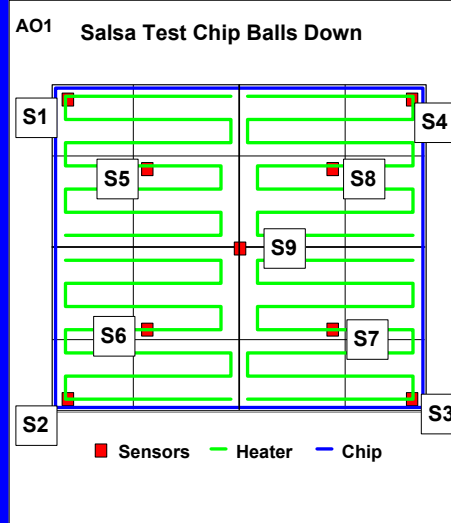
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Bare Die Thermal Test Chip

- 8.8 x 8.8 mm chip
- Flip chip attach
- 42.5 sq x 4.5 mm ceramic substrate
- 9 temperature sensors
- Serpentine heater pattern
- Various chip sizes

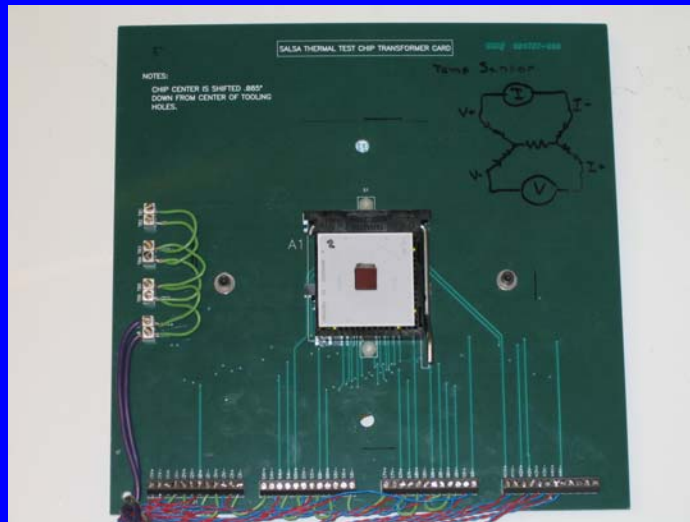


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Salsa Thermal Test Board



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Thermal Chamber

Socket Force

Exhaust Air Air Inlet Temperature Controlled

Product chip
Product Substrate
Test Socket
Interface board

- Part heats up above chamber temperature as power is increased

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Thermal Chamber

Chip to air Thermal Resistance, 14 mm bare die chip

Resistance (C/W) or psi

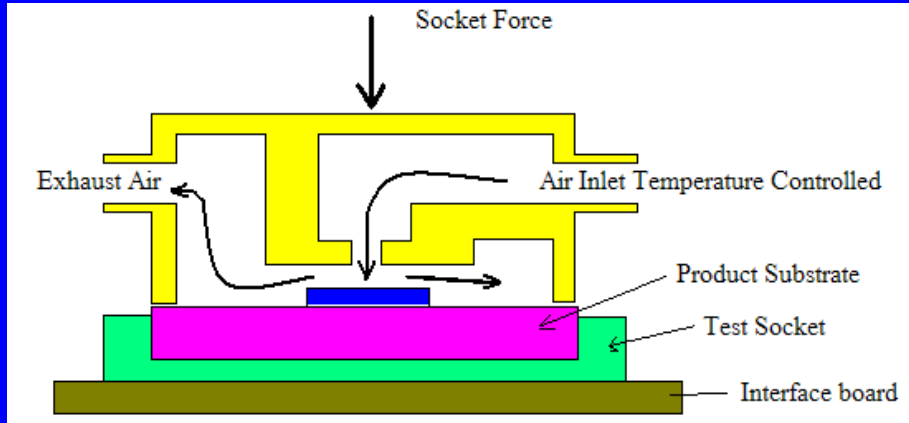
Air Flow (scfm)

■ Chip Ctr
▲ PSI

- Thermal Resistance = $(\text{max chip temp} - \text{air temp}) / \text{total chip power}$

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Single Jet Development



- Airflow directed to chip center

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Single Jet Development UT2



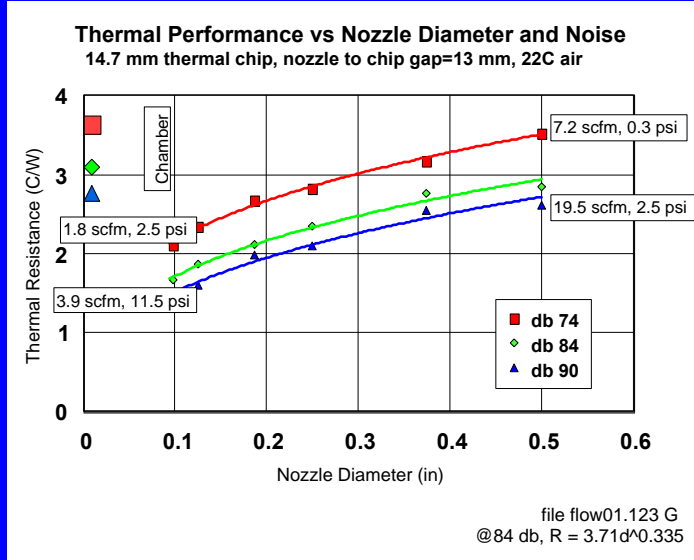
- Small central hole for high velocity air jet
- Optional spring loaded thermocouple

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Resistance vs Nozzle Diameter

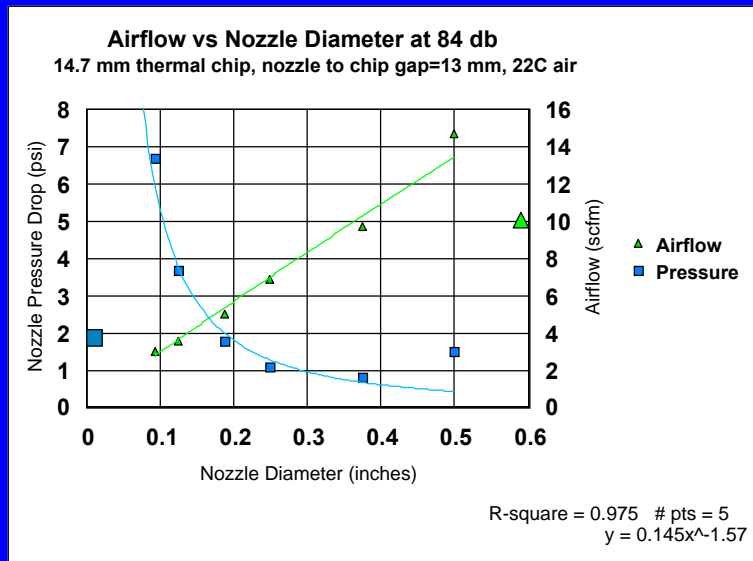


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Pressure & Flow vs Diameter

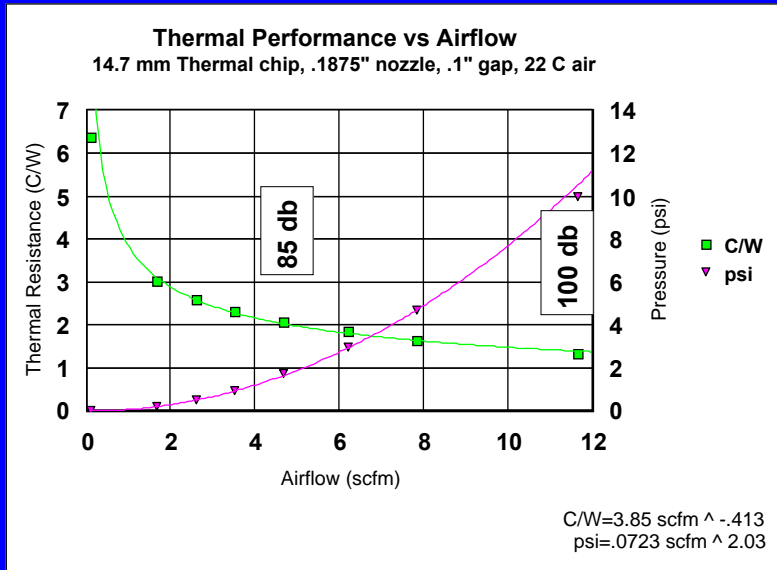


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Resistance vs Flow

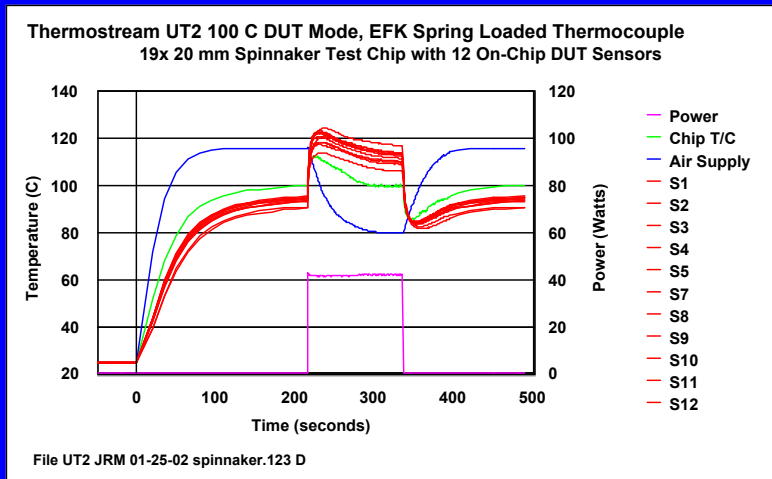


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UT2 – Active Thermal Control



- Good performance, $\Delta T = 20 \text{ C} @ 42 \text{ W}$ on 20 mm chip
- Response time limitations

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Multiple Jet Development

- A matrix of small holes for jet impingement
 - Interstitial holes for air exhaust
 - Exhaust from one hole does not effect flow from adjacent holes
- 10 mm square array
- Thermal data measured on 8.8 mm chip
- Data compared to UT2
 - Single 0.18” diameter jet

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Multiple Jet Development

- Calculate “thermal resistance” based following:
$$R = (\text{avg chip temp} - \text{air inlet temp}) / \text{chip power}$$
- Total chip power is uncorrected for heat loss to fixture
- Air inlet temperature is uncorrected for adiabatic air temperature decrease
- Resistance measured at high power approximates slope of line
 - Indicates performance in manufacturing

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Mezzo LIGA Process, Nickel

1) X-ray lithography

2) Electroplating

3) Molding

4) Metallization

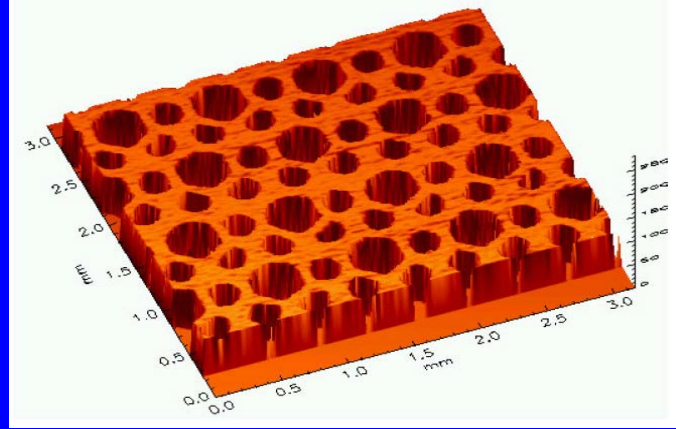
5) Polymer removal

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<p style="text-align: center;">1. Target</p>	
2(a) Schematic of the MJCA concept	2(b) Side view of the fabricated MJCA. The conduit connecting top and lower surface are the jet inflow conduits. The holes in the lower surface are the exhaust ports.
2(c) Fabricated 1x1 sq. cm MJCA	2(d) Bottom view of the MJCA with the jet impingement holes (large holes) surrounded by the exhaust ports (small holes)

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Mezzo MJCA Measured with FRT Tool



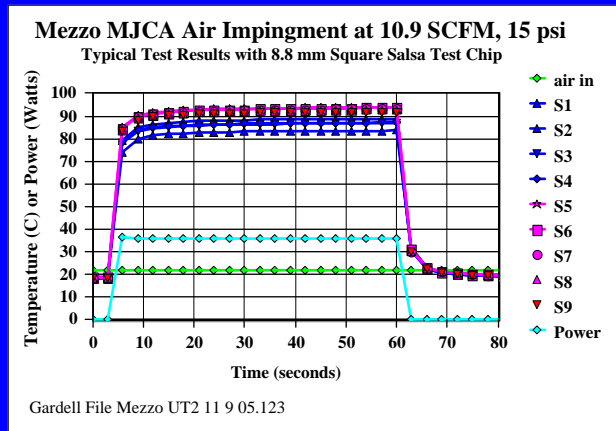
- Supply holes are approximately 345+/-20 microns
- Return holes are approximately 165+/-40 microns

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Typical Thermal Test Results



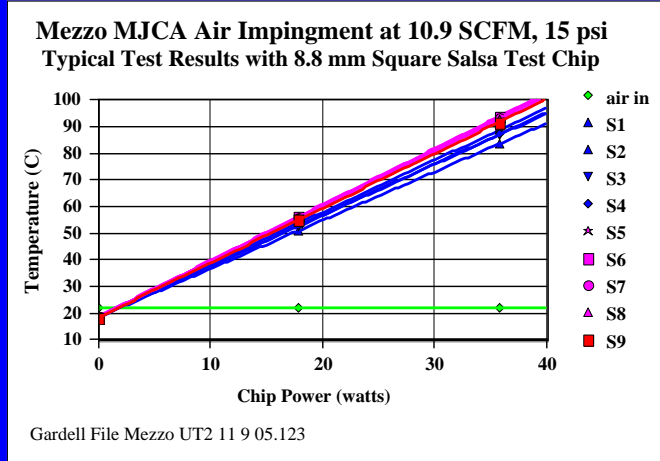
- Measure all temperatures during a 60 second step power
- Temperatures reach steady state, 380 micron gap
- Chip temperature initially below air inlet at high pressure

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Temperature vs Power, Several Tests



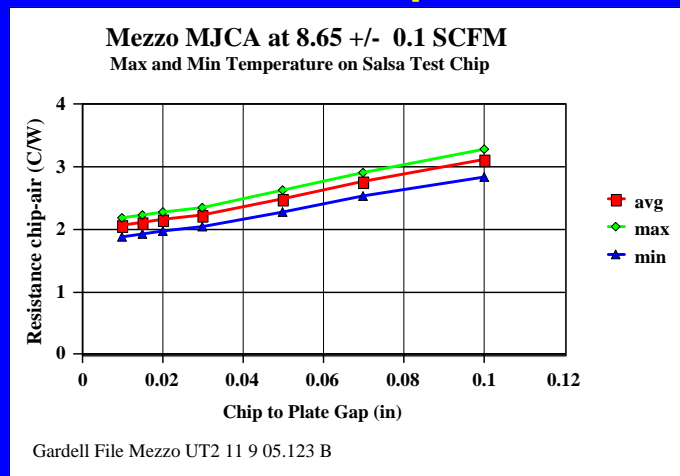
- Plot steady state temperature vs power
- Chip temperature initially below air inlet at high pressure

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Resistance vs Chip-to-Plate Gap



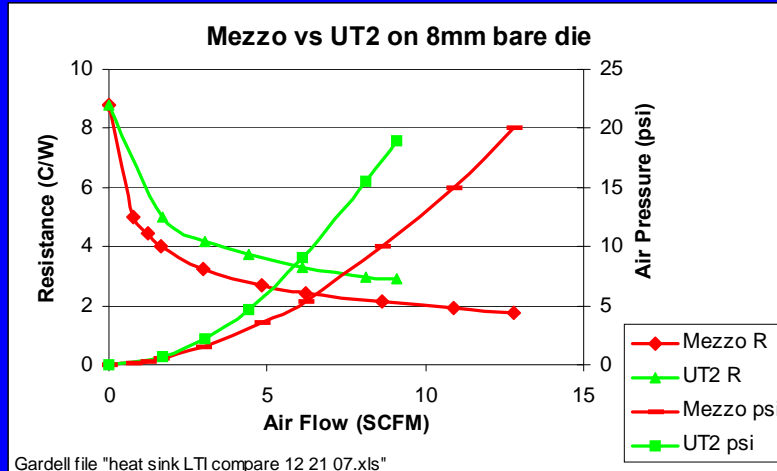
- Thermal performance improves at closer spacing
- Tolerance and pressure concerns at extremely small gaps

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Mezzo vs UT2 on 8.8 mm Salsa Chip



- Mezzo has lower resistance, lower noise and lower pressure at same flow as single jet impingement

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3 Tests Determine Heat Flow Paths

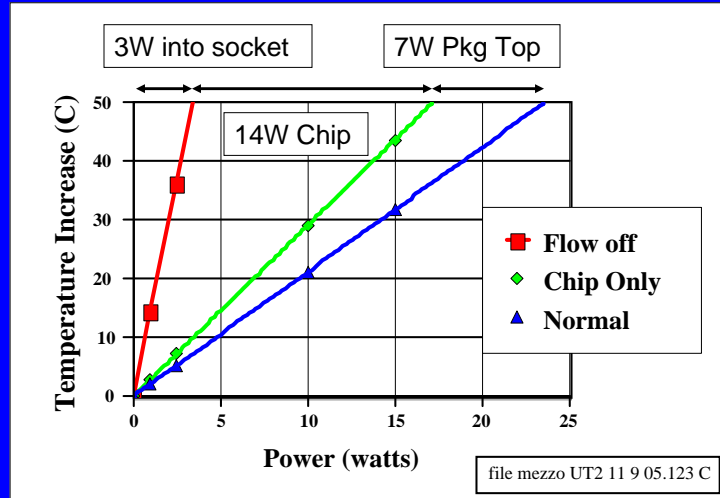
1. Normal test, no insulation, heat flows into:
 - Chip surface and air flow
 - Chip to substrate surface to airflow
 - Chip to substrate to socket to board to ambient air
2. Insulate only top surface of ceramic substrate, airflow only onto top of chip
 - Difference from test 1 is heat flow from substrate
3. Insulate top surface of chip and substrate
 - All heat is forced into test socket, board, and ambient air

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Mezzo at 8.7 scfm on Salsa



- Only 58% of heat is lost from chip top surface

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Microchannel Liquid Cooled Heat Sink for Bare Die

- Nickel plated Cu
- Undersized pedestal
 - Polished surface
- Coaxial bellows
 - Fluid inlet & outlet
 - Compliance & die force

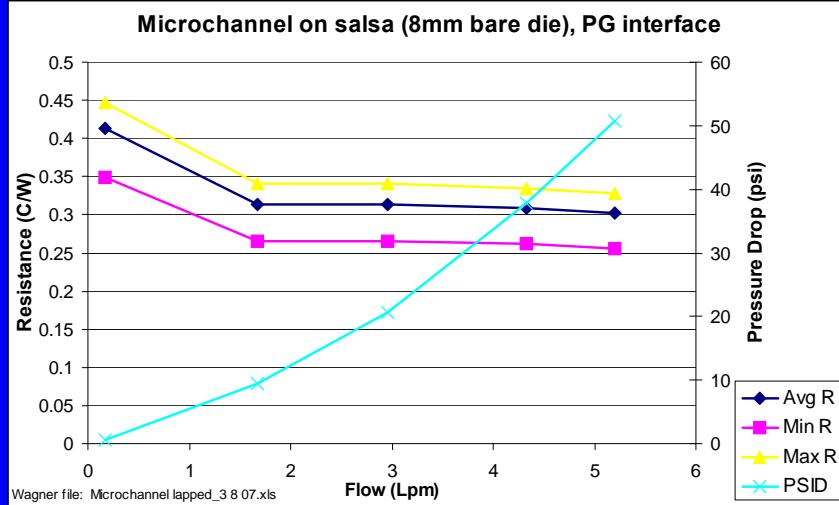


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Resistance & Pressure vs Flow



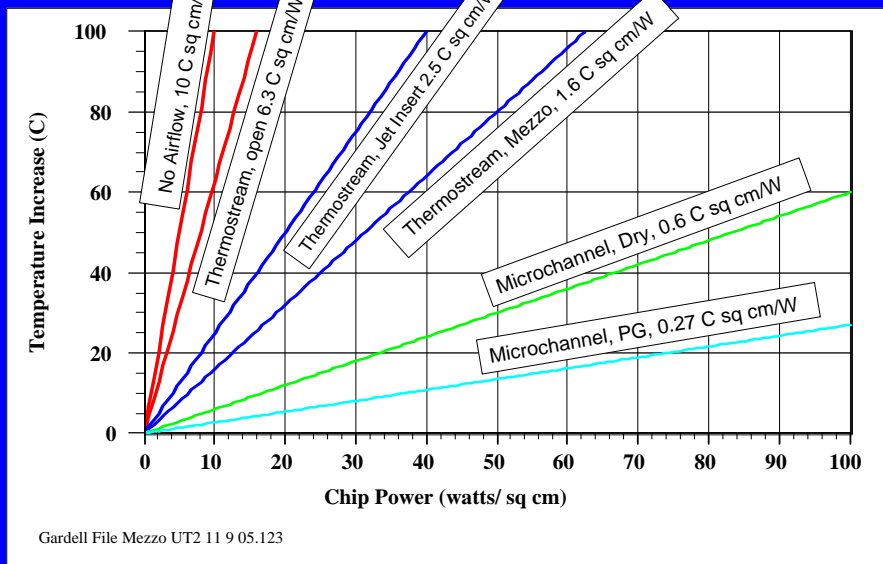
- Point of diminishing return, 45/55 PG/water

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Avg. Chip Temp, 8.8 mm Bare Die Chip



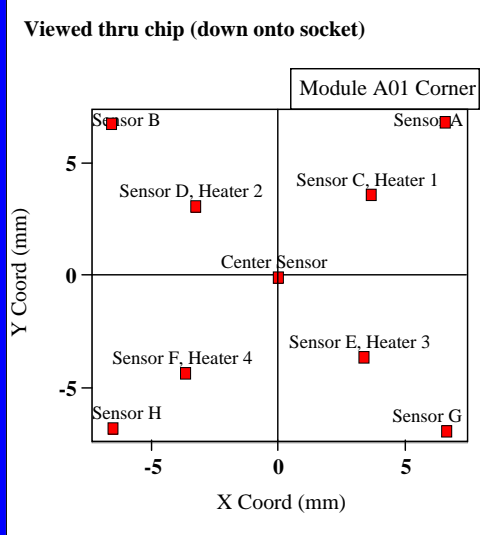
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TV994 – Lidded Thermal Module

- 14.7 mm square chip
- 42.5 mm ceramic substrate
- Aluminum DLA lid 2 mm thick
- 4 heater elements
- 9 temperature sensors



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DLA Impingement Designs

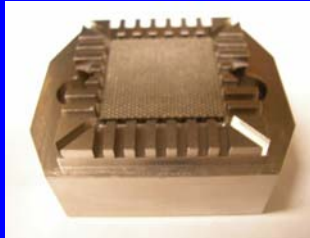
Plastic DLA



Cu DLA



Cu Mezzo DLA – 20mm array

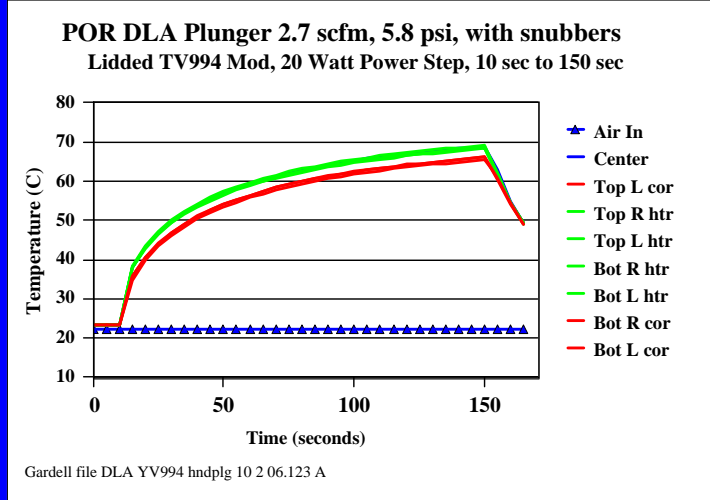


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Plastic DLA Transient Response



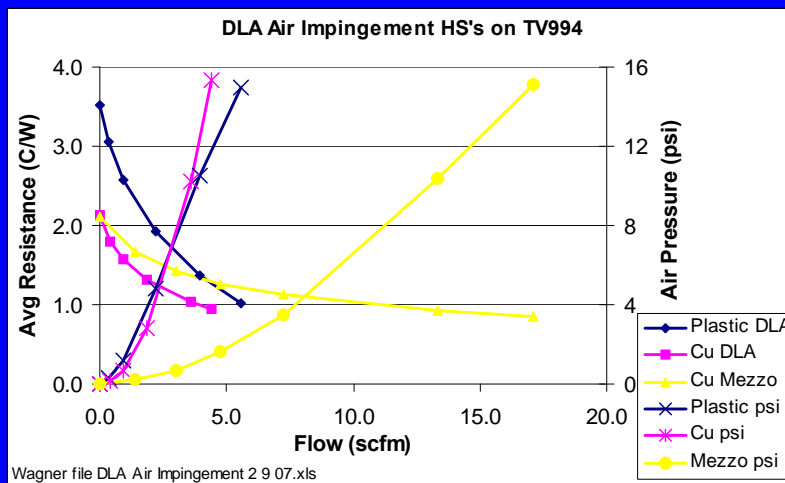
- Thermal resistance is 2.2 C/W at 2 minutes

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Resistance & Air Pressure Vs Flow




- Mezzo flow/pressure is limited by inlet fitting

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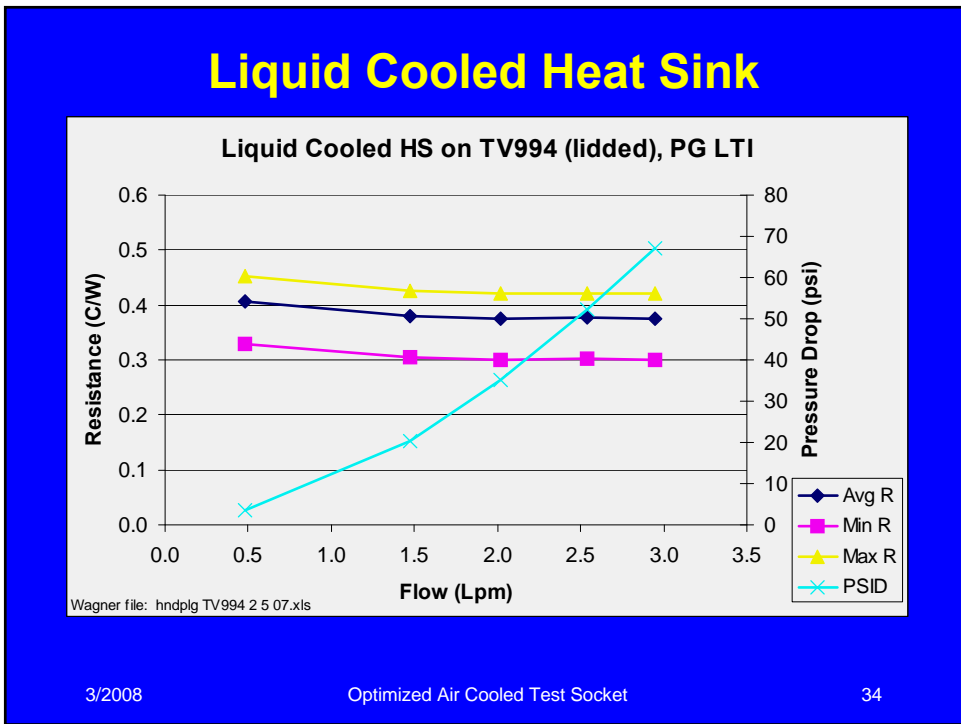
32

Liquid Cooled Heat Sink for Lidded Modules

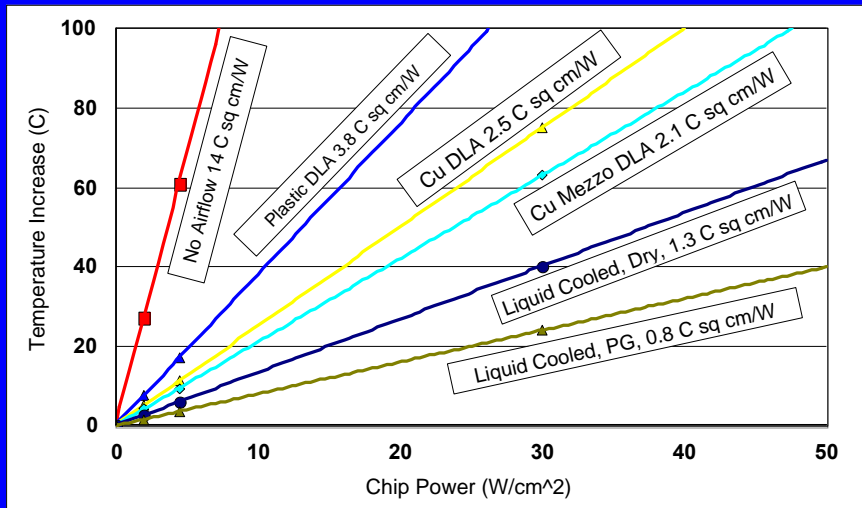


- Nickel plated copper
- Serpentine channel pattern
- Spring loaded thermocouple

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Avg. Chip Temp, 14.7mm Lidded Die



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Conclusions

- Single jet nozzle diameter and nozzle-to-chip gap were optimized
 - Smaller diameters result in improved thermal performance at the cost of higher pressure
- Multi-jet arrays outperform single jets on small bare die test modules
- On large lidded packages, multi-jet arrays require high airflow for optimum performance
 - Investigate use of high pressure blowers
- Air cooled solutions are still inferior to liquid cooled solutions in terms of thermal performance, but can be a good low cost, non contact alternative for low power applications

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