ARCHIVE 2008

FINE PITCH PCB CHALLENGES

"Super-Sockets: Integration of Technology From Test Board Into Socket Assembly"

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"Column Failure on Memory Burn-In Boards"

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Super-Sockets: Integration of Technology from Test Board into Socket Assembly

March 9 - 12, 2008

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When Technologies Reach Their Limits, A New Paradigm Must Emerge

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Overview

- Smaller, Faster, Less Expensive
- Shifting the Burden
- Removing Restraints
- Integrating Components
- Impact on Cost of Test

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Smaller, Faster, Less Expensive… The Trend Continues

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What's Next?

Needs of Manufacturers

Smaller
- Packages
- Pitches

Faster
- Higher Freq
- Lower Inductance
- Lower Contact Resistance

Less Expensive
- Board Costs
- Socket Costs (price per pin)
- Down Time

Robbing Peter to Pay Paul

- There are currently individual solutions to each need
- Where is the comprehensive solution?

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Have Load Board Manufacturers Met Their Match?

0.4 mm pitch:

- 100 microns drilled holes + no change in board thickness =

  High Aspect Ratio

- How do we get to 0.4 mm pitch and beyond for high layer count, thick load boards?

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What if We Could Shift the Burden?

- What if…
  - …the footprint of the DUT no longer dictated the pitch and layout of the load board
  - …test board design could remain static
  - …standard test boards could be used
  - …there was no compromise to performance or space of the socket

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Removing Footprint Restraints

- By incorporating test board technology into the socket assembly:
  - Footprint restraints are removed
  - Pitch is no longer an issue!
- How is this done?
  - Two methods

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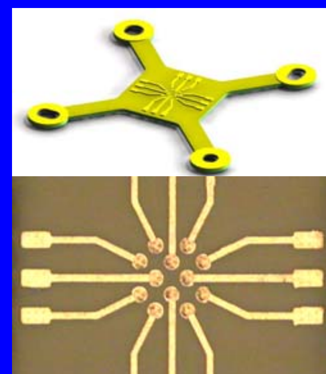
Method 1: Fan-Out Using Printed Interconnect

- Traces are printed on a polyimide substrate
- Traces transform pitch and footprints (ie. 0.3 mm device pitch to 0.8 mm board pitch)



0.3 to 0.5 mm Fan-Out Socket Interconnect

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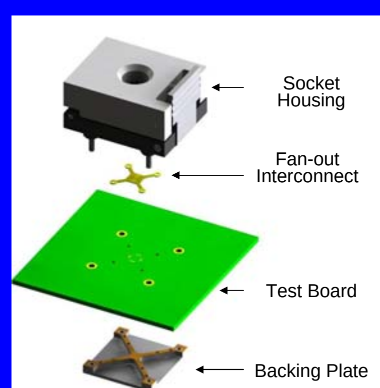
Method 1: Fan-Out Using Printed Interconnect

- Ideal for QFN/MLF style packages
- Can also be used for low pin count BGA packages



0.3 to 0.5 mm Fan-Out Socket Assembly

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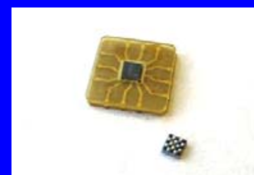
Method 1: Fan-Out Using Printed Interconnect

- Printed fan-outs as a socket insert



Top View

Bottom View

Fan-Out Socket Insert: 0.3 mm Device Pitch to 0.5 mm Socket Pitch

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Method 2: Space Transformer

- Multilayer PCB in the socket assembly
- Transforms pitch and footprint or descrambles pin layout
- Compression mounts to load board
- Can be used with most compression mount sockets

Socket Assembly with Space Transformer

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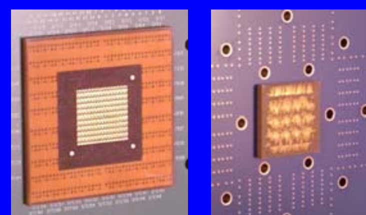
Space Transformer Applications

- 0.4mm pitch package test enabler
- Mother / Daughter
  - Multiple part numbers
- Mother / Daughter
  - Multiple systems



Space Transformers in Probe Applications

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Space Transformer Applications

- Descrambler
  - Pin out change
- Re-utilization

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Space Transformer Attributes

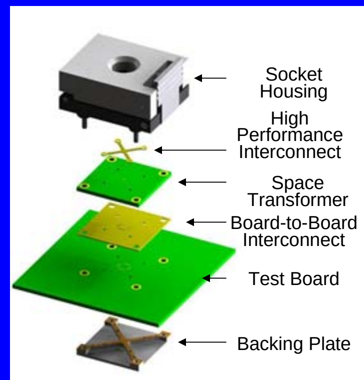
- Organic Materials
  - Matched to load board
- Impedance Controlled
  - 63.5µ Line/Space
- Hi Pin Count - 400+

Space Transformer Attributes

- .25mm pitch capable
- Thru Hole to HDI Buildup
  - Micro-drilling to laser micro-via's
- Zero 'Z' axis increase
  - Integrated in socket

Solution For High-Performance, Fine Pitch Socket Assemblies

- High performance socket housing and interconnect
- Space Transformer with impedance control
- Low inductance compression mount board-to-board interconnect



ConnectFlex™ with Space Transformer High Performance, 0.3 mm Device Pitch, 0.8mm Board Pitch Socket Assembly

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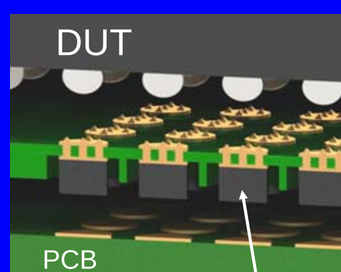
Printed Interposer: An Enabling Technology

- Fan-out uses printed interposer technology
- Pin contactors are printed on polyimide
- No spring pins or stamped contactors
- Uses a conductive compliant material



Conductive Compliant Material

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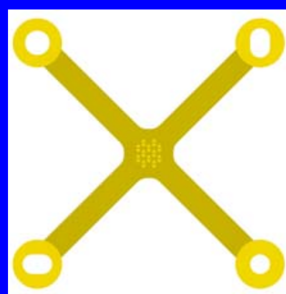
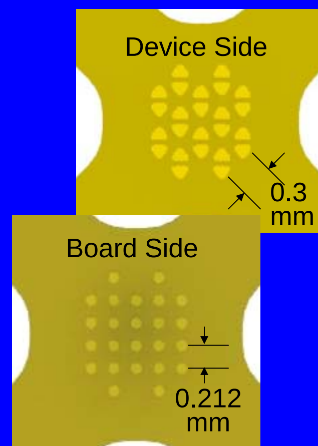
Printed Interposer: Kelvin Made Easy

- Kelvin for QFN or BGA down to 0.3 mm pitch





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Printed Interposers: Fine Pitches

- Pitches down to 0.2 mm

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Integrating Other Elements of the Test Board

- Decoupling under the DUT (bottom side)
- Decoupling near the device (top side)
- Resistors to tune circuits
  - What if you could put these in the socket?

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Passives in the Socket Assembly

- Passives can be placed right next to devices under test
- Possibilities of increased performance for high speed devices
- Benefits are still under debate

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Cost of Test

- Current economic driver
  - Price per pin
  - Socket Pitch
  - Number of insertions
  - Load Board Pitch

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Cost of Test

- Changing the socket architecture creates a new economic driver
  - Price per insertion
- New factors that lower costs
  - Less expensive machined socket housings
  - Less expensive molded socket tooling costs ($10,000 vs $100,000)
  - Standard Test Boards
    - Less expensive test boards
    - Reusable test boards
    - Increased life of test boards

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Summary

- Need for smaller, faster, and less expensive
- Integration of technology from test board into socket assembly
- Burden shifted away from load board
- A new paradigm in test socket architecture will enable IC Manufacturers

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Acknowledgements

Afshin Nouri, Contech Solutions, Inc

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Column Failure on Memory Burn-In Boards

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

Yogesh Ahuja
Pycon Inc.
Santa Clara, CA

Introduction

- Capacity, Capacity, & Capacity determines Burn-in Board design.
- Large boards crowded with up to 400 sockets
- Average design ties half the board address lines. (200 devices)
- Average design ties two columns together for I/O's. (50 devices)
- Phantom failures can take out 15% or 50% of capacity
- Severe problems lead to complete abandonment of the Vendor, Engineer or Product Line

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Assumptions

- Fully functioning design
  - Tuned
  - Bring-Up problems eliminated
- System Reads/Writes to the Complete Memory Map
  - System reports Good Vs. Bad devices
  - Monitored BI
- All Channels on the DUT are isolated with Resistors

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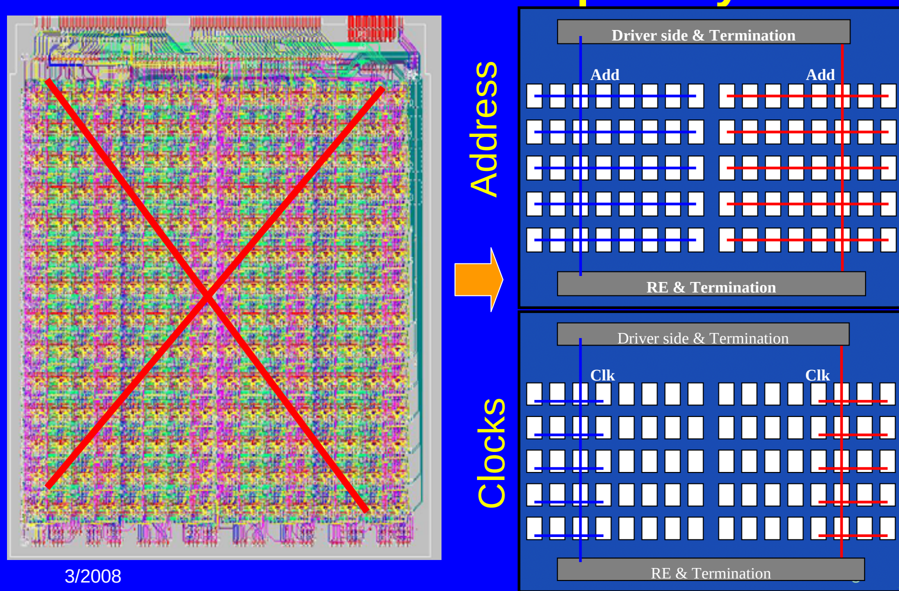
Part 1

Gather Information

Understand The Simple Layout



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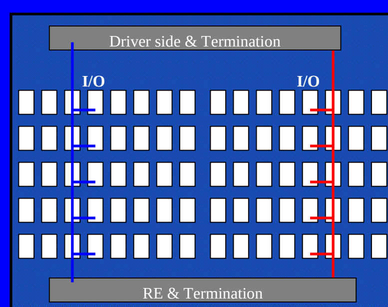
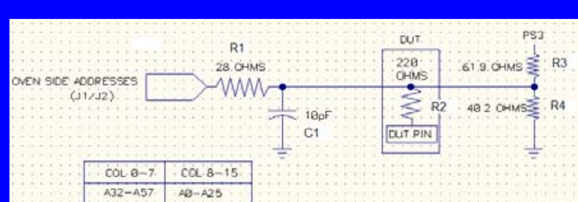
Understand Layout Cont'

- Address 8 Col X 16 Rows
- Clocks 4 Col X 16 Rows
- I/O's 2 Col X 16 Rows
- CS, GE, etc…
- FE & RE Terminations





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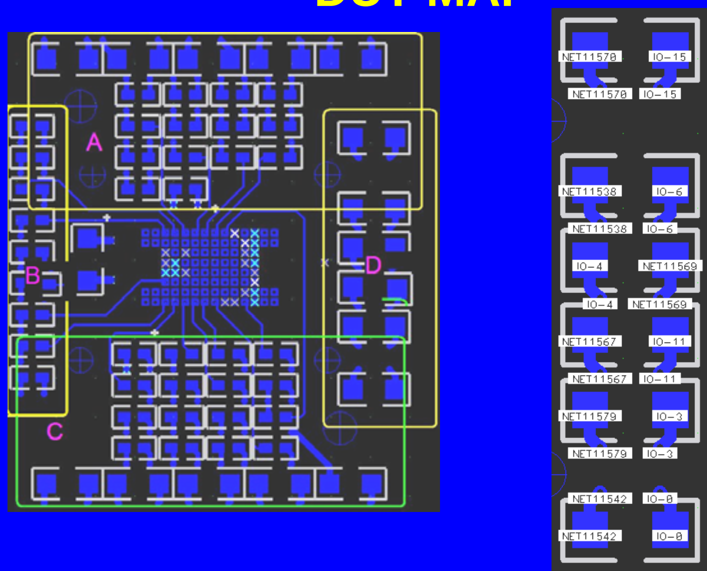
DUT MAP



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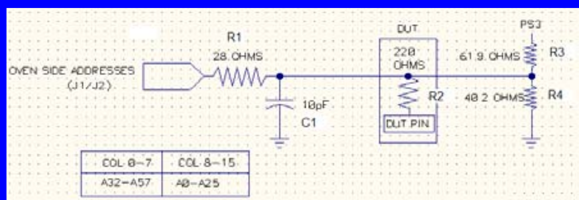
Part 2

Eliminating Simple Failures

Uni-Directional Signal Failures

- Address, Clock & CS propagate from Driver to DUT only
- DUT is protected using isolation resistors
- Device Failures
  - Dead Short in the DUT: Adr to GND results in a loss of few mV of VOH to DUT. No Column Failures
  - Dead Short in the DUT: Adr to VCC results in a gain of few mV of VOL to DUT. No Column Failures



This example has a +/- 60mV change

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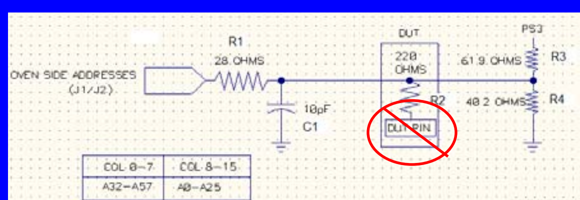
Uni-Directional Failures Cont'

- If Column failures show up on Uni-Directional signals the problem is outside of the DUT region.
  - Corrupt Tuning/Termination components.
  - Bad VIAS
  - Opens/shorts on traces
  - Gross failures



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Solution

- Corrupt Tuning/Termination components.
  - Run a Static (RLC) test to find bad components
  - Simple test, eliminates problems quickly
- Via Problem
  - Run a Static test to find location
  - Only board manufacturer can fix problem
  - CAF & cracked barrels are mostly incurable
- Opens/shorts on traces
  - Open traces are rare and signify mishandling
  - Shorts are common on poorly maintained boards
  - PM & Cleaning can eliminate problem

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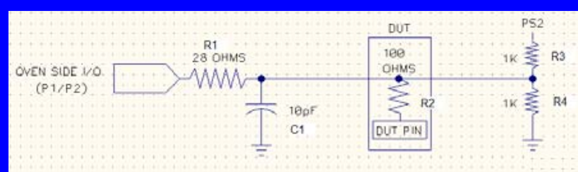
Part 3

Eliminating Complex Failures

BI-Directional Signal Failures

- I/O Lines have bi-directional data
- DUT is protected using isolation resistors
- System Writes with >100mA of current
- Device Writes with <10mA of current
- Frequency of failure (Ascending order)
  - Gross Failures (See Uni-Directional Failures)
  - Burn-In Board quality issues, CAF, PM
  - Device I/O Stuck at High/Low



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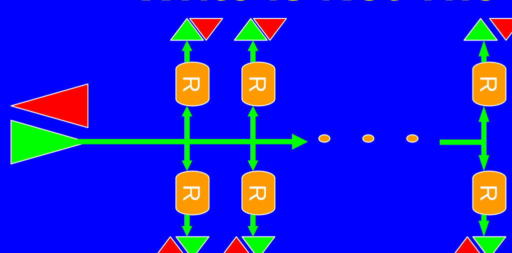
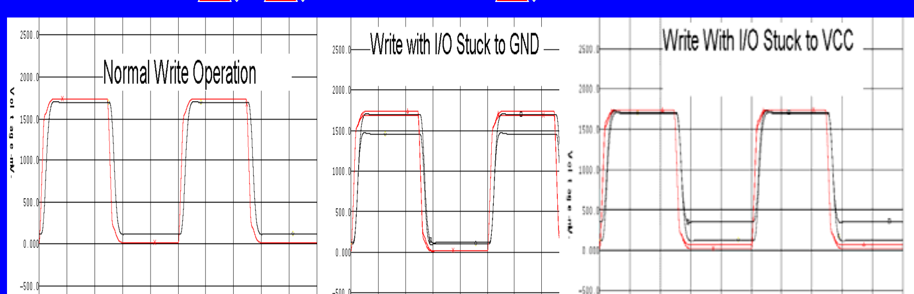
Write is Not The Problem



Write (100mA) is always successful



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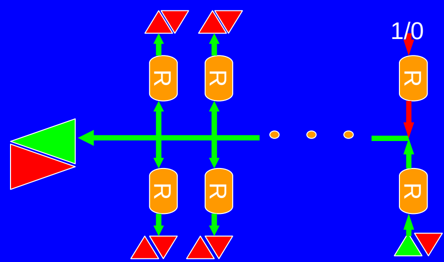
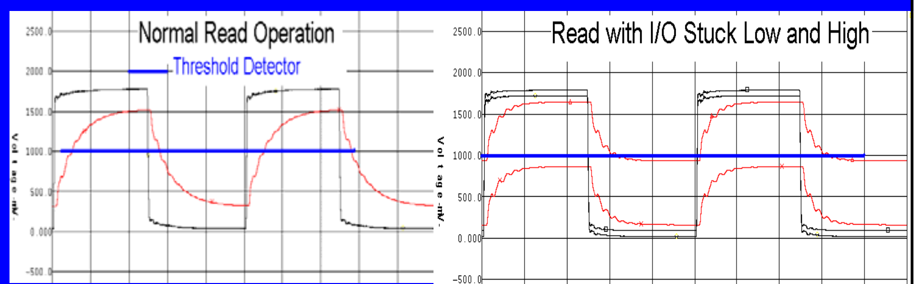
Read is The Problem



- -Read (5mA) is weak
- -One DUT drives all others
- -Threshold level invalid



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Solution Without Devices

- Line stuck High or Low
  - The same error can also be caused by socket pins being physically shorted on the board
  - PM, Cleaning Static test can eliminate the problem
  - CAF cannot be eliminated
  - Run an empty board with 0000 to weed out bad BIB
    - Column failures predict physical damage with BIB
    - Detects socket I/O pins shorted to VCC

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Solution With Devices

- Line stuck High or Low
  - Run fully loaded bib with 0000 to weed out bad Devices
  - Column failures predict device stuck high
  - Run fully loaded bib with 1111 and lowering threshold level to weed out bad devices
  - Column failures predict device stuck low
  - Possible to continue BI with lower threshold level
- Physical Location Probe Using DMM
  - All but one I/O will show the same Resistance to GND/VCC
  - DUT side of Resistor on one location will be dead short

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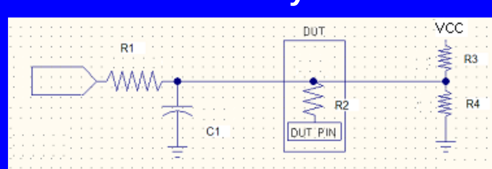
Add fault tolerance in the system

- Determine the amplitude of the signal with the fault.
  - No Short
    - Vh = (R4/((R3//R2)+R4)) x VCC
    - Vl = (R4//R2)/((R4//R2) +R3)) x VCC
  - Short to GND
    - Substitute R4 with Rx = R4//R2
  - Short to VCC
    - Substitute R3 with Ry = R3//R2



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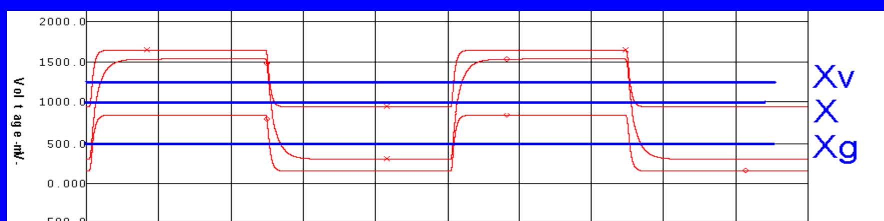
Add fault tolerance Cont’

- Six values determine three threshold levels
    - Vh Vl Normal Operation: X
    - Vh Vl Short to Gnd: Xg
    - Vh Vl Short to VCC: Xv
- Dynamically adjust threshold level in system
    - Set Threshold level to X
    - If (2 Column Failures) then
        - Xg -> X and retest
        - If (2 Column Failures) then
        - Xv -> X and retest



Conclusion

- Understand the simple style layout
- Almost all failures will resemble the channel assignment
- Unidirectional failures are outside of the socket region
- Bidirectional failures are inside the socket region
- Prescreen empty boards with 0000 to find BIB faults
- PM boards regularly to avoid debug hours
- Implement fault tolerance at system level

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Thank You

Q/A