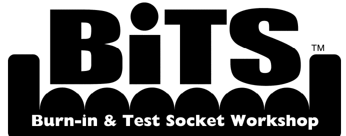

2008 **Keynote Speaker**

ARCHIVE 2008

"Packaging & Assembly in Pursuit of Moore's Law and Beyond"

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Vice President and Senior Fellow
Advanced Packaging Systems Integration Laboratory
Freescale Semiconductor

As the semiconductor industry continues in its pursuit along the curve of Moore's Law from 65 nm to 45 nm, 32 nm and beyond, the challenges for packaging and assembly technologies are becoming significant. Packaging can no longer be thought of as a back end process largely independent of the silicon and product definition. The assembly and packaging technologies have become an integral component in the overall performance, figures of merit and cost competitiveness of these new generations of products. Further, market trends and customer expectations are moving rapidly into higher levels of system integration and system solutions. This trend is moving products toward greater levels of integration and diversification beyond the scaling of Moore's Law.

Rapid market growth in areas beyond the traditional drivers for the semiconductor industry, such as computer and industrial applications, into consumer applications with semiconductor based systems becoming pervasive in all aspects of our lives is placing additional demands on packaging. These demands include but are not limited to lower cost, shorter time to market and greater flexibility and reuse.

This presentation addresses these new challenges, the trends in packaging and assembly and some unique solutions that are being developed and implemented. A broad spectrum of products solutions from system-on-chip, 3D, system-in-package as well as "wafer level" assembly are discussed.

Dr. Johnson leads the Advanced Packaging Systems Integration Laboratory (APSL) within the Freescale Technology Solutions Organization. This laboratory is responsible for the development and implementation of a broad spectrum of packaging advances in support of Freescale Semiconductor's business and strategy. These innovations are in areas which include analog power, RF and sensor modules, automotive applications and advanced wirebond and flip chip packages.

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Agenda

- Packaging Evolution
- Market / IDM Evolution
- Challenges
- Advanced Package Development
- Freescale's Redistributed Chip Package (RCP)
- Conclusion

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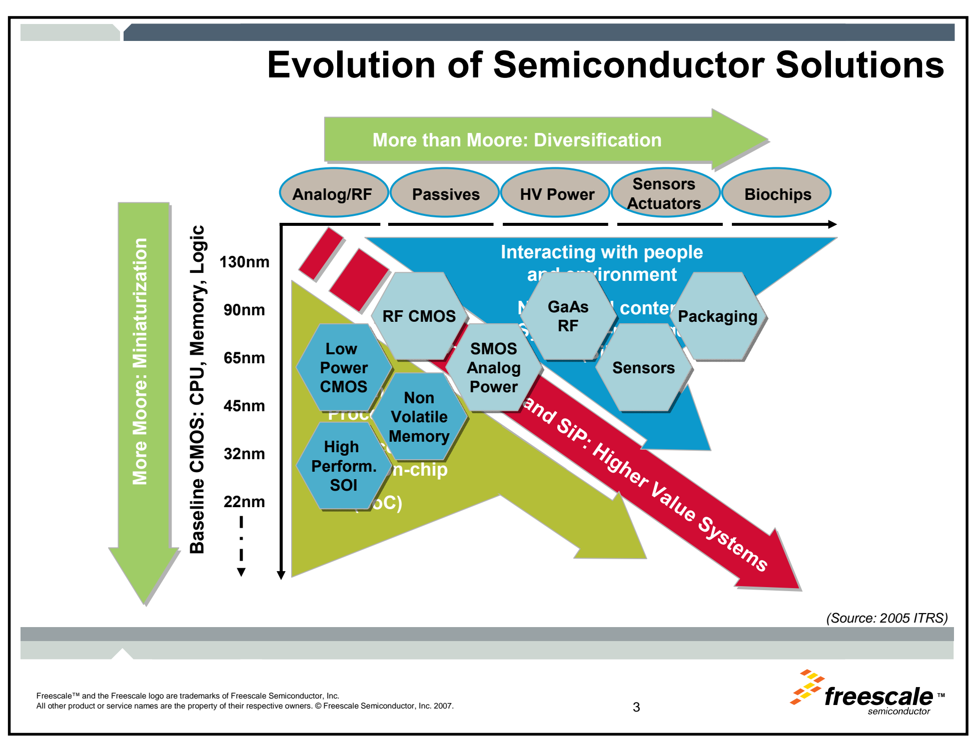
Evolution of Semiconductor Solutions
More than Moore: Diversification
Analog/RF
Passives
HV Power
Sensors Actuators
Biochips
More Moore: Miniaturization
Baseline CMOS: CPU, Memory, Logic
130nm
90nm
65nm
45nm
32nm
22nm
Interacting with people
RF CMOS
GaAs RF
Packaging
Low Power CMOS
SMOS Analog Power
Sensors
Non Volatile Memory
High Perform. SOI
and SiP: Higher Value Systems
(Source: 2005 ITRS)
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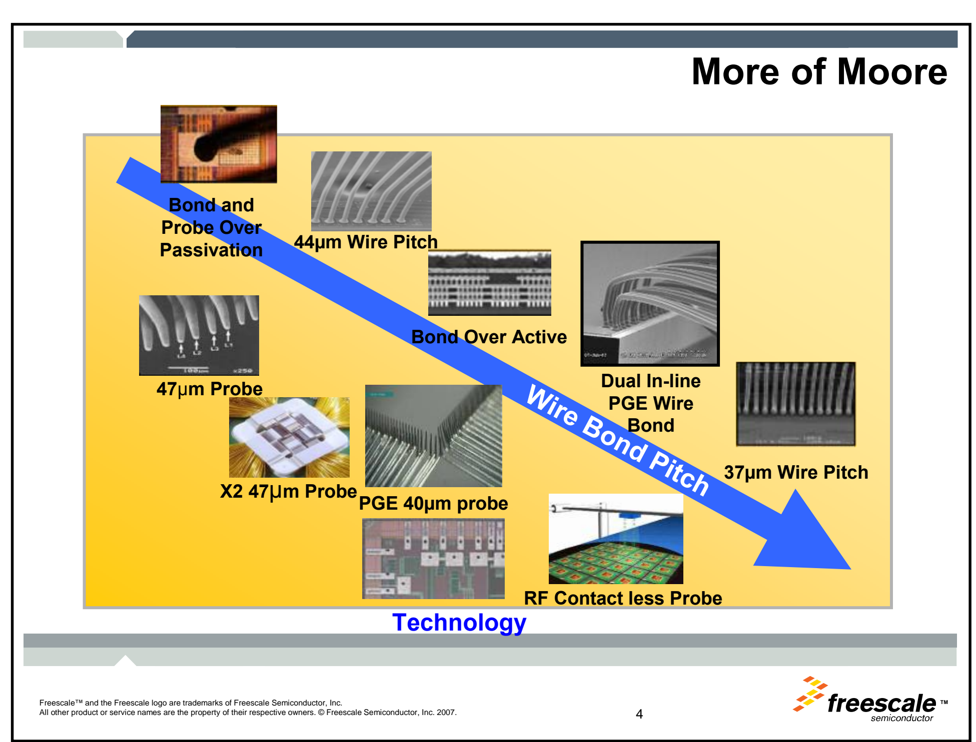
More of Moore
Bond and Probe Over Passivation
44µm Wire Pitch
Bond Over Active
Dual In-line PGE Wire Bond
47µm Probe
X2 47µm Probe
PGE 40µm probe
Wire Bond Pitch
37µm Wire Pitch
RF Contact less Probe
Technology
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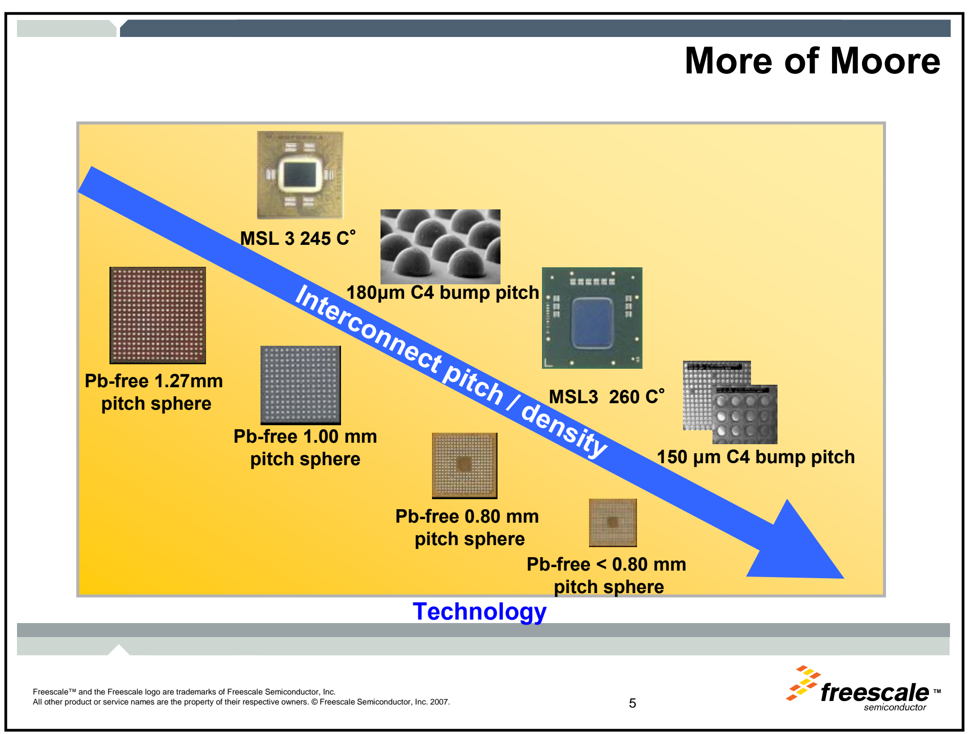

Market / IDM Evolution

- **The market drivers have evolved:**
  - Industrial
  - Computer
  - Wireless
  - Automotive
  - Customer
- **The market demands system solutions**
  - Greater functionality with software
  - Faster Time to Market (product refresh)
  - Cost, Cost, Cost
  - Flexibility and reuse
- **Society demands “Green” solutions**

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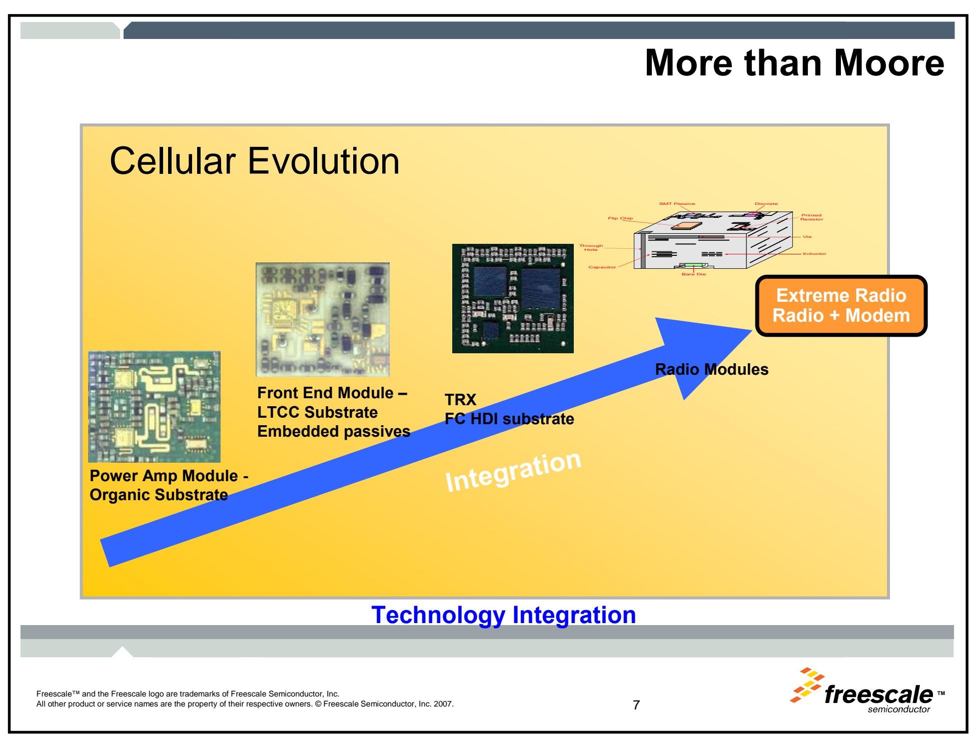
More than Moore
Cellular Evolution
Extreme Radio
Radio + Modem
Radio Modules
TRX
FC HDI substrate
Front End Module –
LTCC Substrate
Embedded passives
Power Amp Module -
Organic Substrate
Integration
Technology Integration
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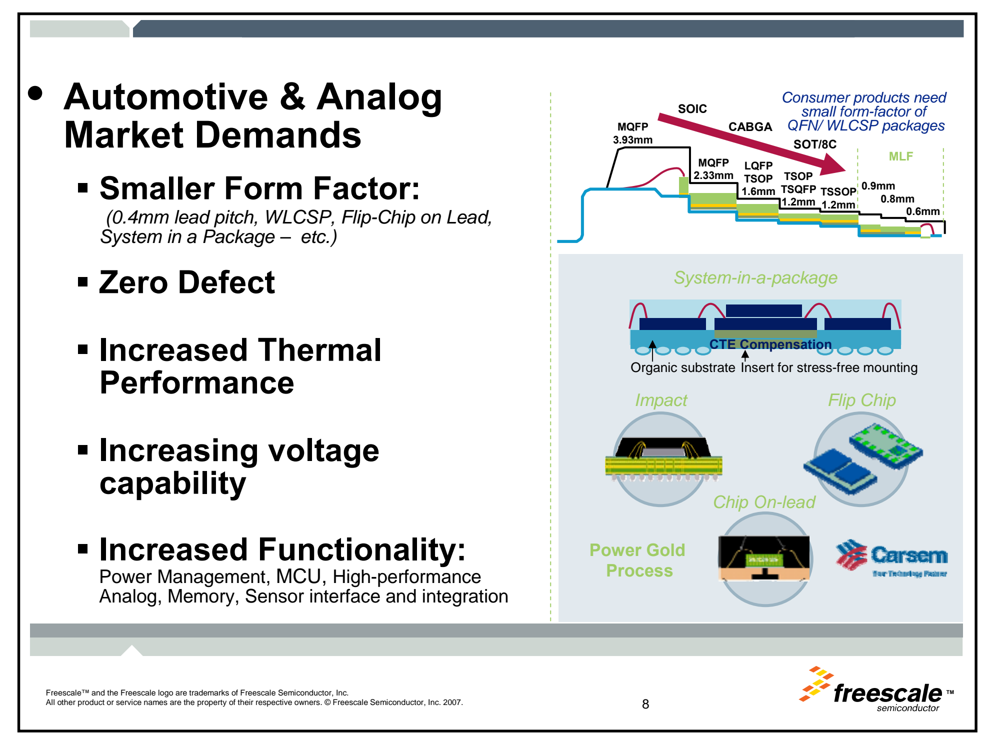
• Automotive & Analog Market Demands
▪ Smaller Form Factor:
(0.4mm lead pitch, WLCSP, Flip-Chip on Lead, System in a Package – etc.)
▪ Zero Defect
▪ Increased Thermal Performance
▪ Increasing voltage capability
▪ Increased Functionality:
Power Management, MCU, High-performance Analog, Memory, Sensor interface and integration
Consumer products need small form-factor of QFN/ WLCSP packages
SOIC
MQFP
3.93mm
CABGA
SOT/8C
MLF
MQFP
2.33mm
LQFP
TSOP
1.6mm
TSOP
TSQFP
1.2mm
TSSOP
1.2mm
0.9mm
0.8mm
0.6mm
System-in-a-package
CTE Compensation
Organic substrate
Insert for stress-free mounting
Impact
Flip Chip
Chip On-lead
Power Gold Process
Carsem
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Challenges

- System on a Chip (More of Moore)
  - Compromised subsystem performance
  - Signal integrity
    - parasitics, cross coupling
  - Power and ground (core @ 1.0 volt)
    - Parasitics – inductances to ground, IR drop
  - Design Cost
  - Time to Market
  - Decreasing flexibility and reuse
  - Pad Limited Designs

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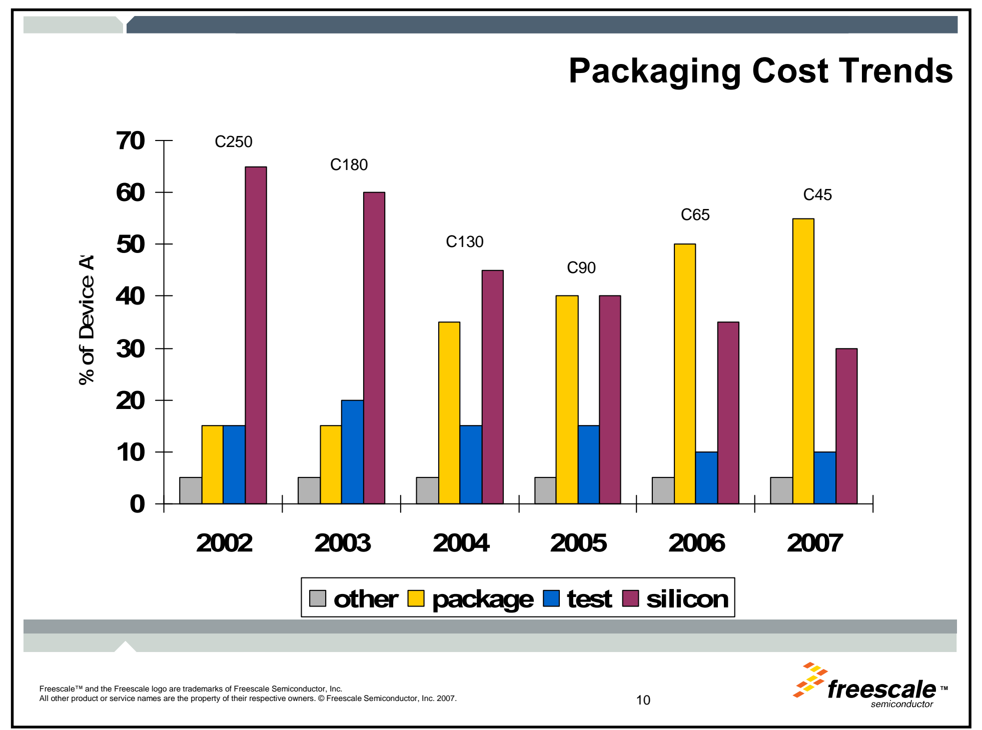

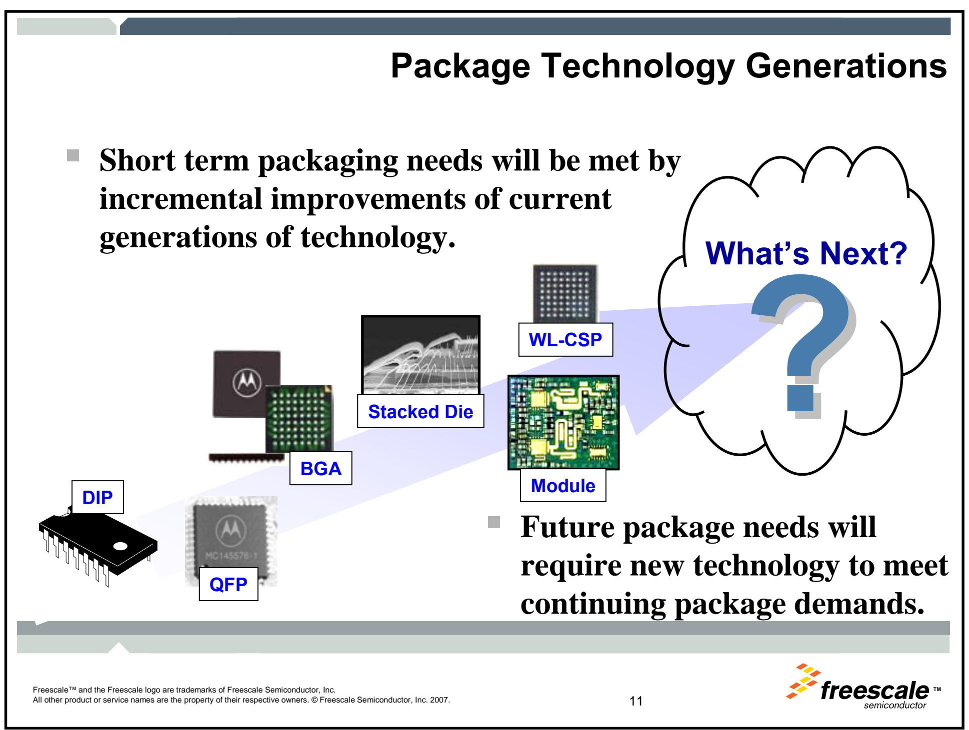
Package Technology Generations
Short term packaging needs will be met by incremental improvements of current generations of technology.
What's Next?
?
WL-CSP
Stacked Die
BGA
Module
DIP
QFP
Future package needs will require new technology to meet continuing package demands.
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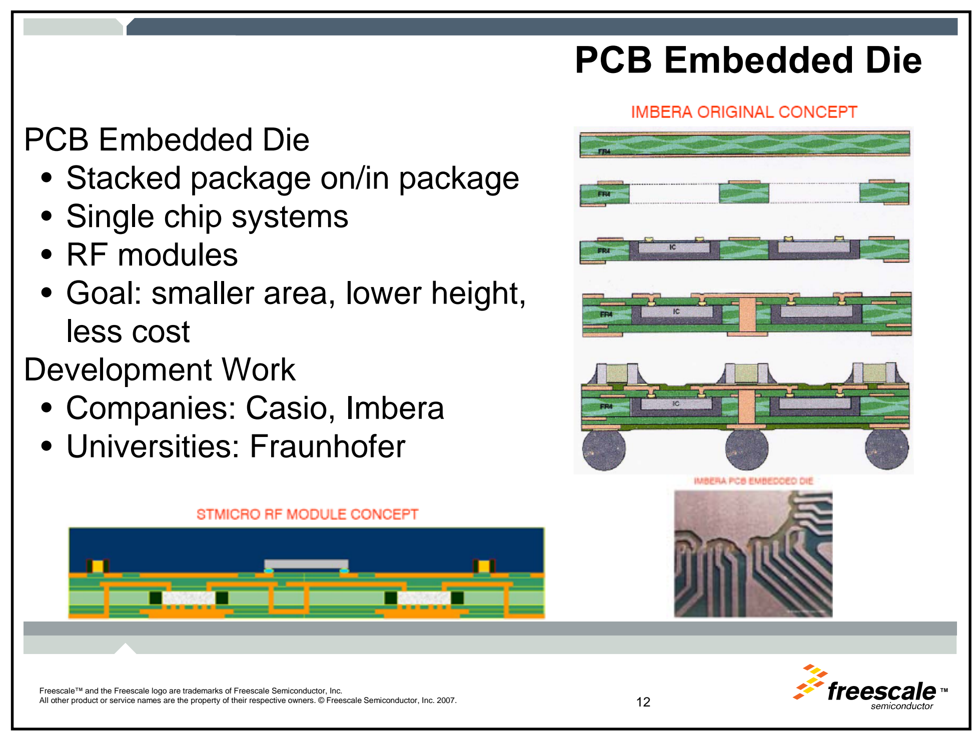
PCB Embedded Die
IMBERA ORIGINAL CONCEPT
PCB Embedded Die
• Stacked package on/in package
• Single chip systems
• RF modules
• Goal: smaller area, lower height, less cost
Development Work
• Companies: Casio, Imbera
• Universities: Fraunhofer
STMICRO RF MODULE CONCEPT
IMBERA PCB EMBEDDED DIE
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Casio EWLP RF Module

Main die embedded in PCB (EWLP)

- Other die on top of board (WLP)
- Passives/packaged discretes on top of board (SMT)
- Target: phones, Bluetooth, GPS, TV tuner
- Joint development of Casio and CMK

10mm x 10mm Module with 1 EWLP, 7 WLP, 31 SMT

WLP (SMT) Passive Devices EWLP

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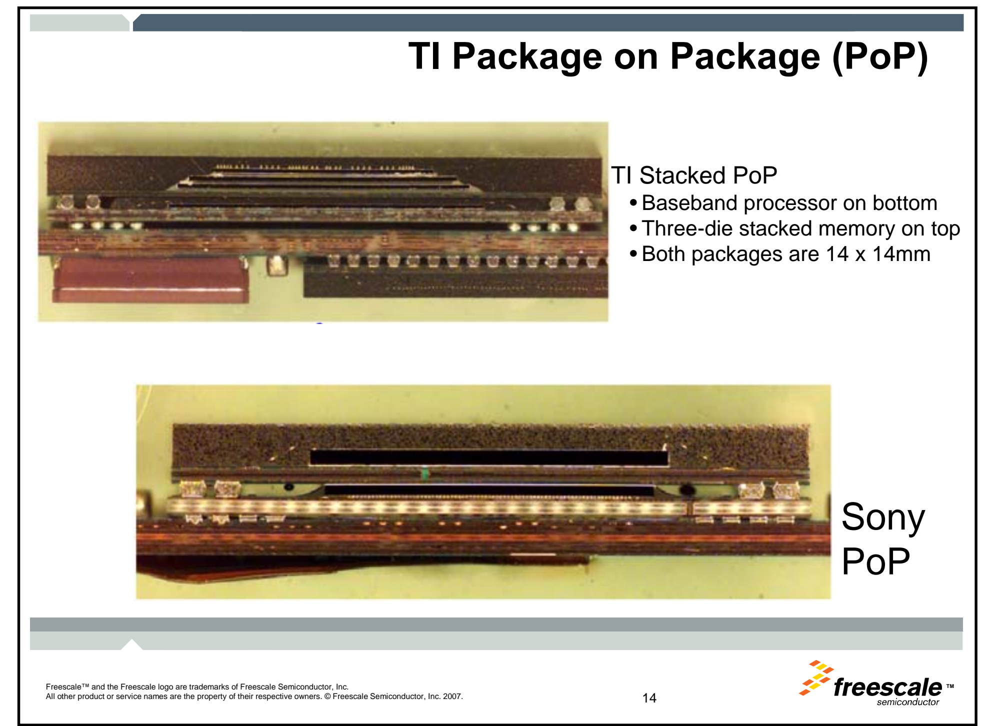

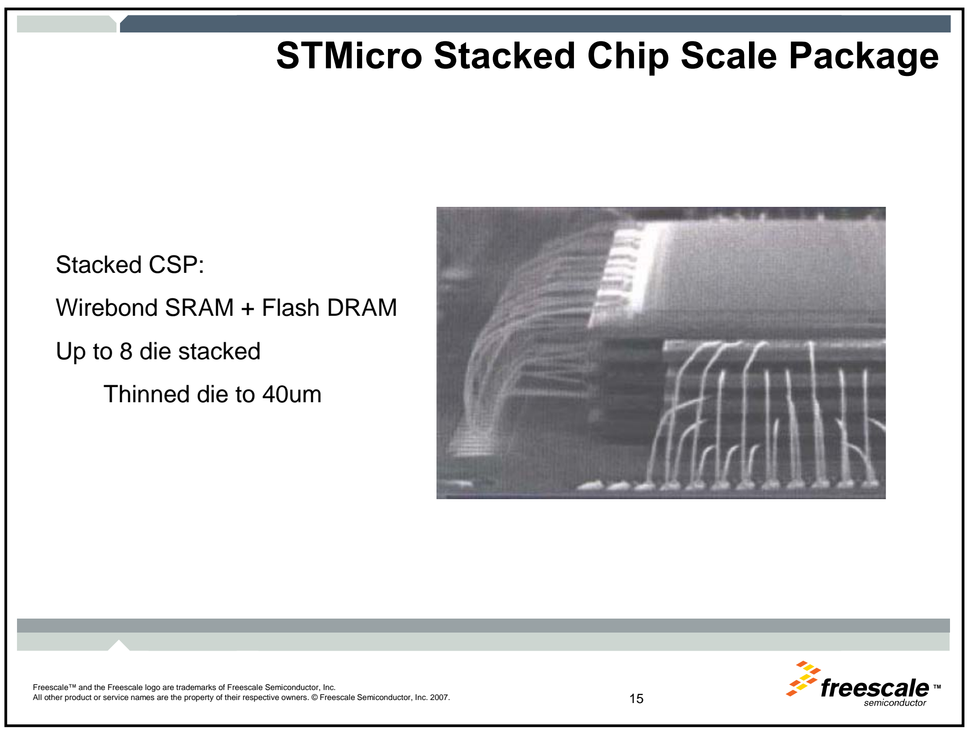
STMicro Stacked Chip Scale Package
Stacked CSP:
Wirebond SRAM + Flash DRAM
Up to 8 die stacked
Thinned die to 40um
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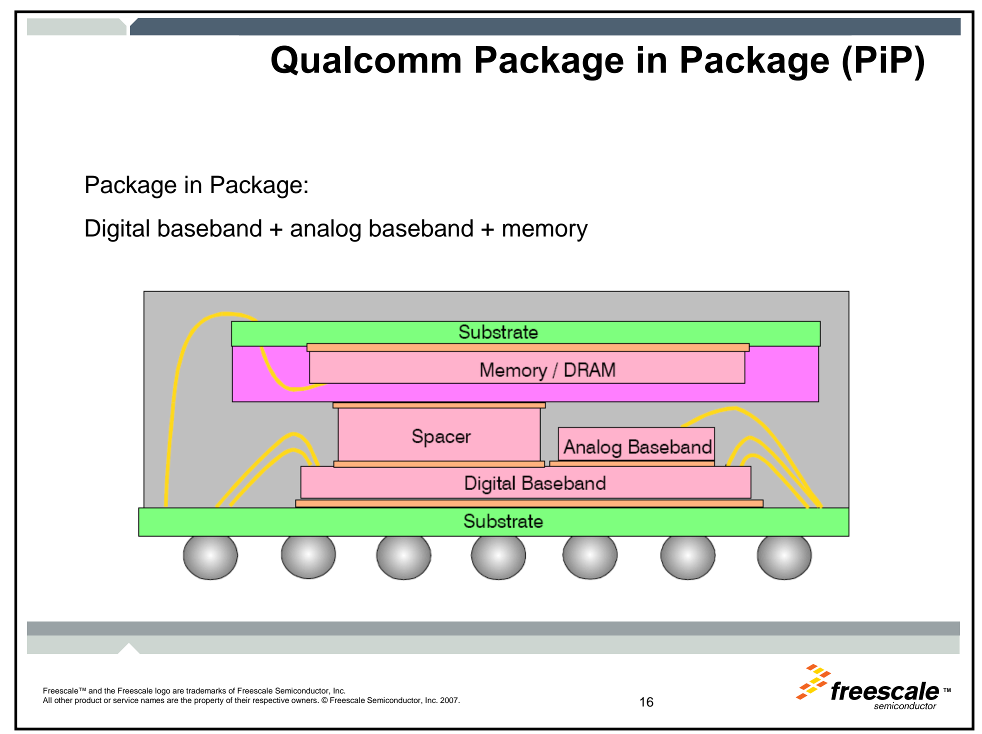
Qualcomm Package in Package (PiP)
Package in Package:
Digital baseband + analog baseband + memory
Substrate
Memory / DRAM
Spacer
Analog Baseband
Digital Baseband
Substrate
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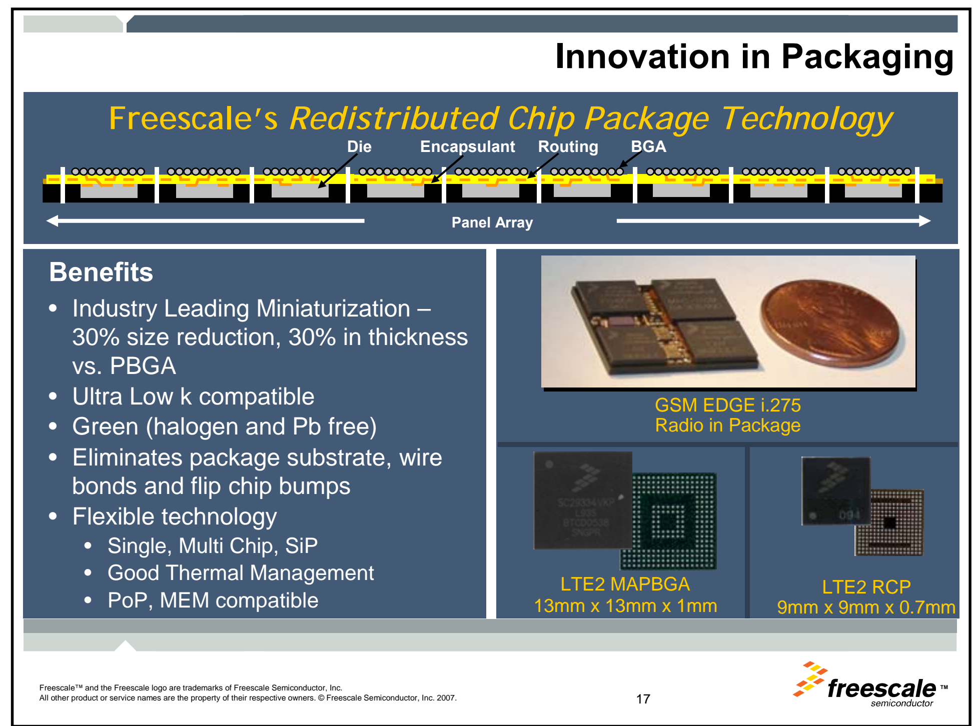
Innovation in Packaging
Freescale's Redistributed Chip Package Technology
Die
Encapsulant
Routing
BGA
Panel Array
Benefits
Industry Leading Miniaturization – 30% size reduction, 30% in thickness vs. PBGA
Ultra Low k compatible
Green (halogen and Pb free)
Eliminates package substrate, wire bonds and flip chip bumps
Flexible technology
Single, Multi Chip, SiP
Good Thermal Management
PoP, MEM compatible
GSM EDGE i.275
Radio in Package
LTE2 MAPBGA
13mm x 13mm x 1mm
LTE2 RCP
9mm x 9mm x 0.7mm
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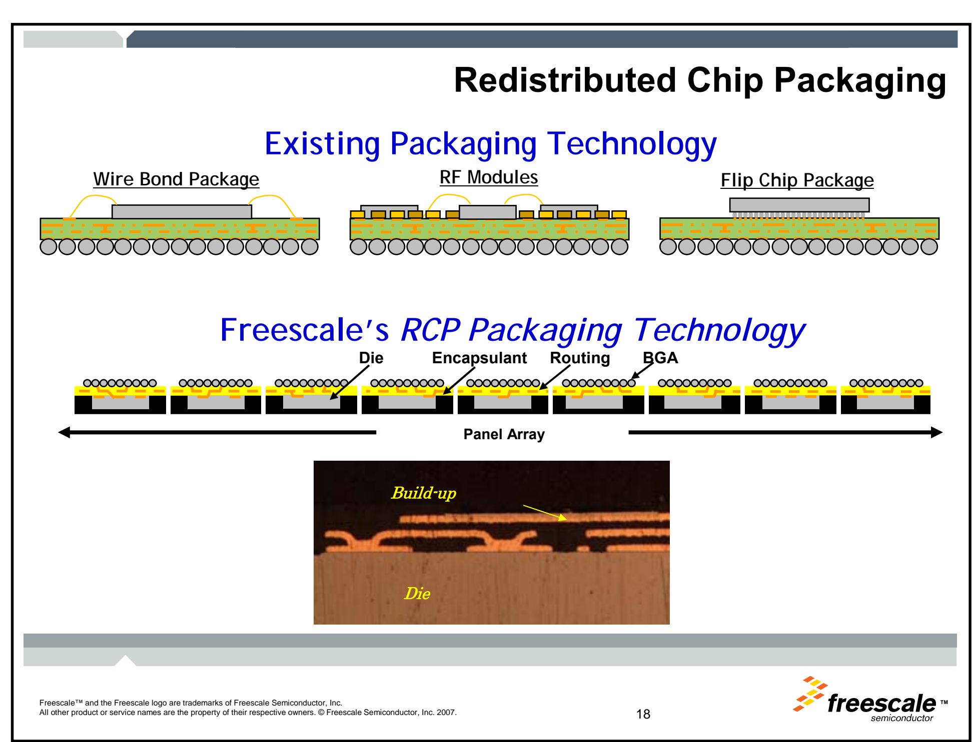
Redistributed Chip Packaging
Existing Packaging Technology
Wire Bond Package
RF Modules
Flip Chip Package
Freescale's RCP Packaging Technology
Die
Encapsulant
Routing
BGA
Panel Array
Build-up
Die
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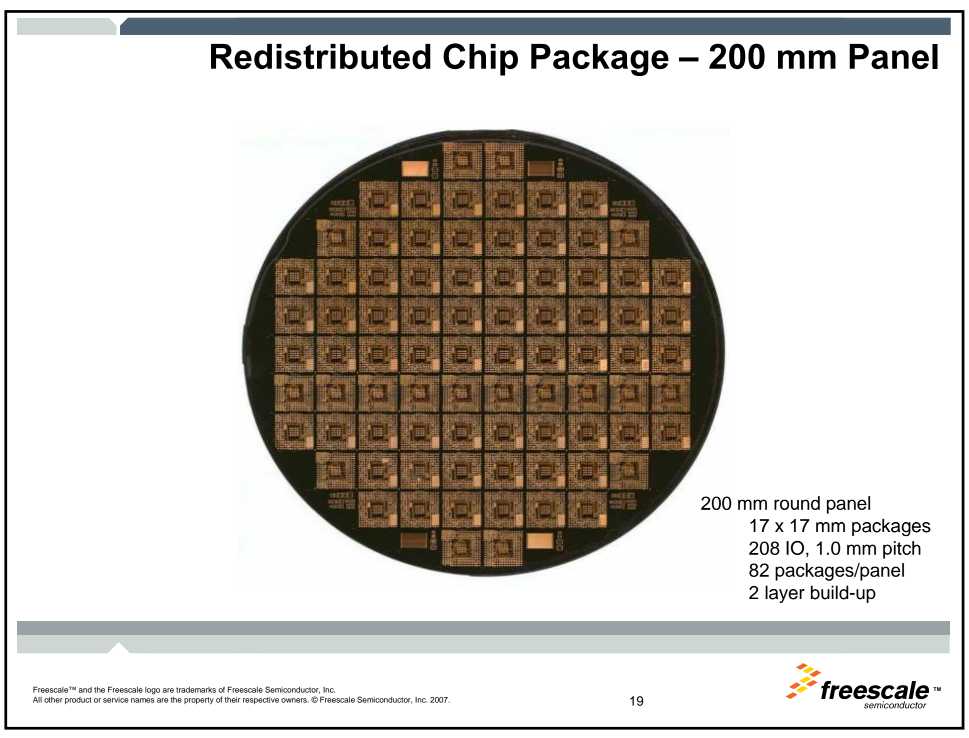
Redistributed Chip Package – 200 mm Panel
200 mm round panel
17 x 17 mm packages
208 IO, 1.0 mm pitch
82 packages/panel
2 layer build-up
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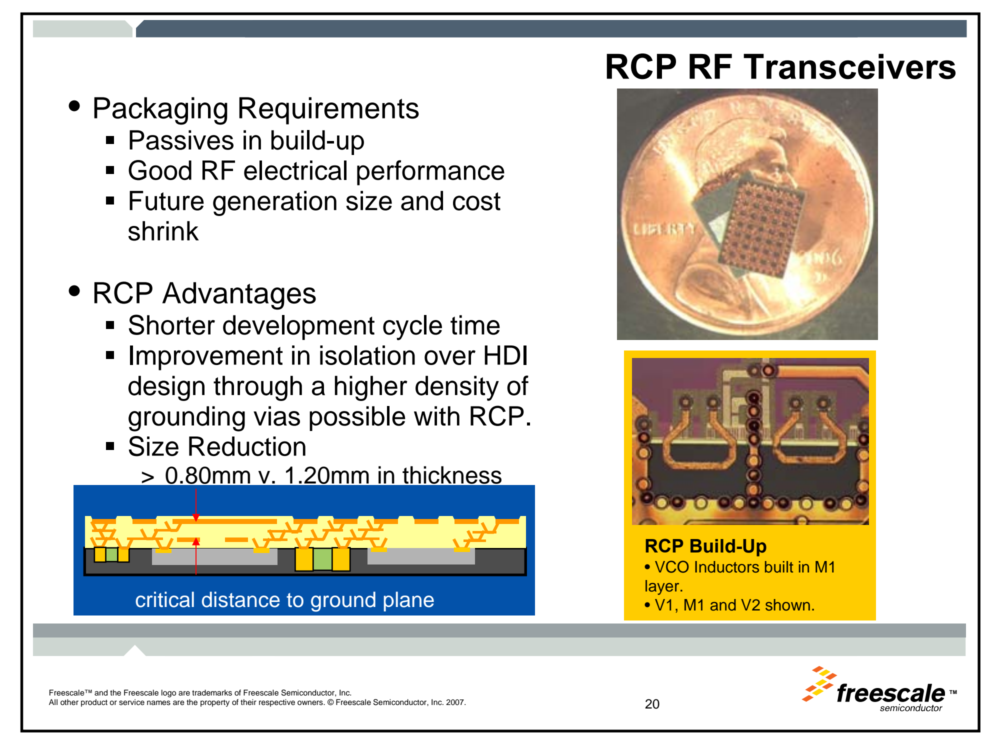
RCP RF Transceivers
• Packaging Requirements
▪ Passives in build-up
▪ Good RF electrical performance
▪ Future generation size and cost shrink
• RCP Advantages
▪ Shorter development cycle time
▪ Improvement in isolation over HDI design through a higher density of grounding vias possible with RCP.
▪ Size Reduction
> 0.80mm v. 1.20mm in thickness
critical distance to ground plane
RCP Build-Up
• VCO Inductors built in M1 layer.
• V1, M1 and V2 shown.
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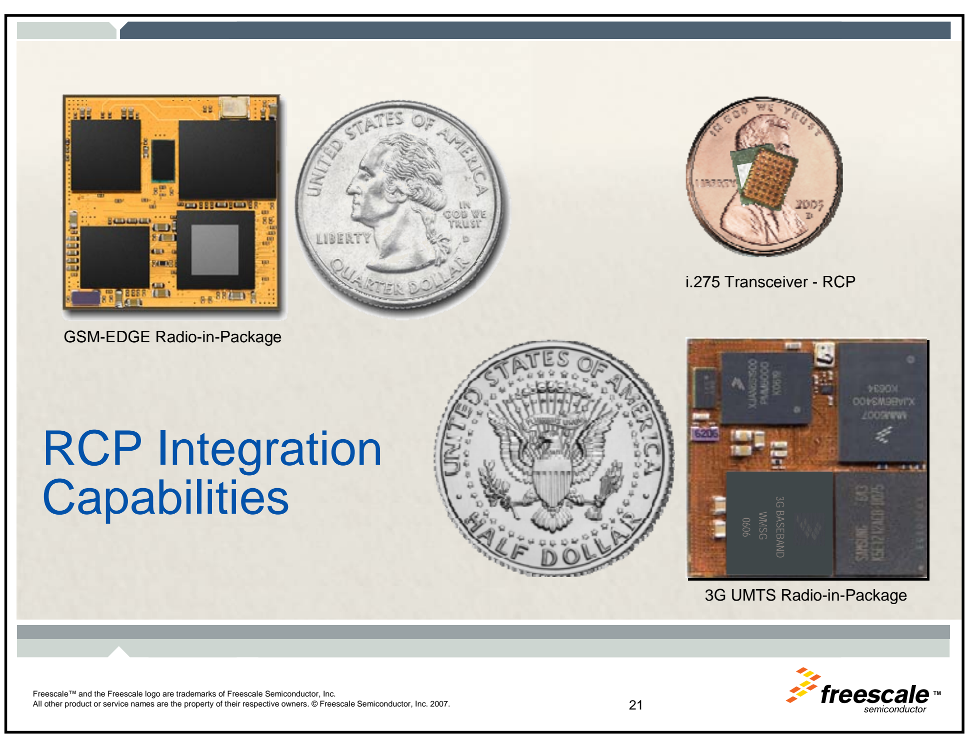
GSM-EDGE Radio-in-Package
i.275 Transceiver - RCP
RCP Integration Capabilities
3G UMTS Radio-in-Package
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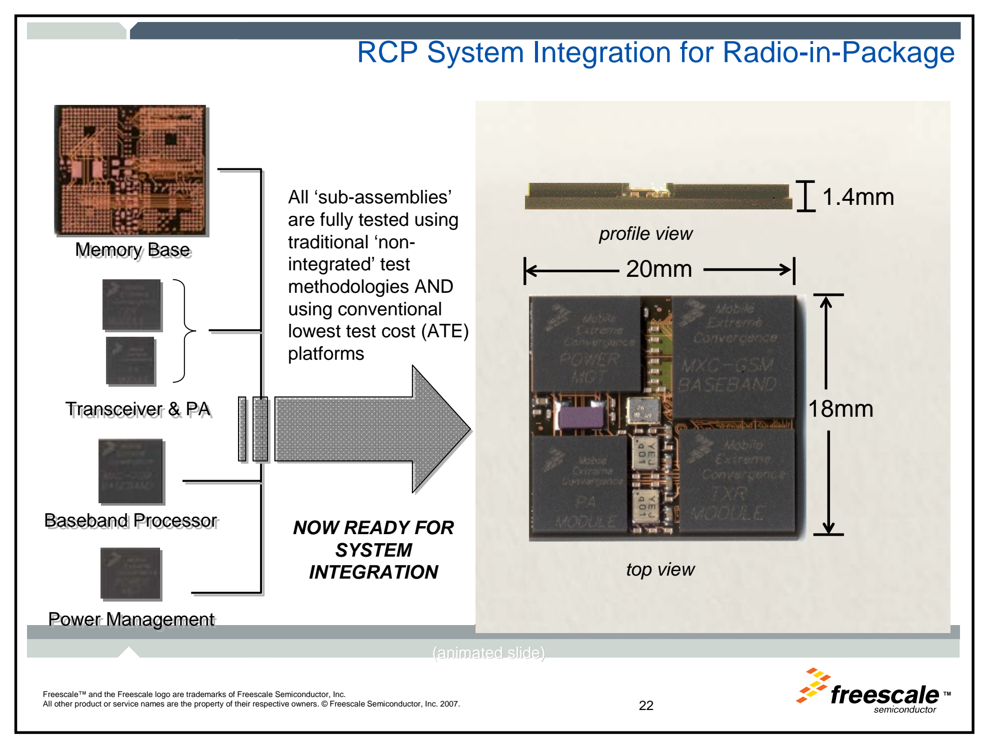
RCP System Integration for Radio-in-Package
Memory Base
Transceiver & PA
Baseband Processor
Power Management
All 'sub-assemblies' are fully tested using traditional 'non-integrated' test methodologies AND using conventional lowest test cost (ATE) platforms
NOW READY FOR SYSTEM INTEGRATION
1.4mm
profile view
20mm
18mm
top view
(animated slide)
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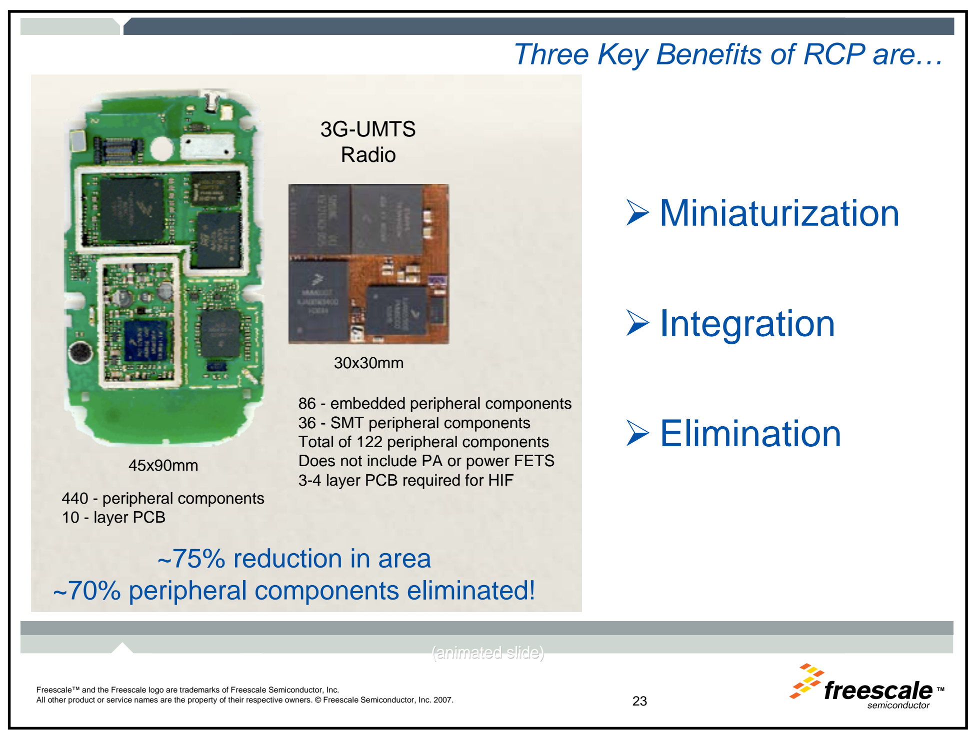

Conclusions

Market Demands:

- **Systems Integration with increasing functionality**
- **Speed of design (Time to Market)**
- **Flexibility**
- **Reuse**
- **Cost, Cost, Cost**

Are necessitating a revolution in packaging and assembly technologies

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