“Catching the Mobile Wave: Packaging is Going 3D”
Dr. Belgacem Haba
Fellow and CTO of Advanced Packaging and Interconnect
Tessera Inc.

Hand-held communication and entertainment products will continue to dominate the consumer markets worldwide, and with each generation offering more and more features and/or capability, system level integration and miniaturization becomes more of a priority. And even though the actual applications and functionality of the new product offering expands, the customer is expecting each generation to be smaller and lighter than its predecessor.

The cell phone is a great example of how new technologies and techniques can be applied to maintain performance improvements over time. The explosion of the cell phone market over the last few years is a testament to the increase of functionality and complexity of miniaturization. However, this has led to some serious issues, especially mechanical, thermal and shielding problems. Less than one part in 1,000 of the volume of an electronic product is occupied by transistors. The remaining volume consists of mechanical structure, air, passive elements, cables and connectors. 3D stacking is a natural way to reduce the system volume. Die fabricated at different process geometries can be brought together in a 3D stack, thus avoiding some of the cost issues associated with system-on-chip (SoC) designs.

This presentation focuses on the different alternatives available for 3D packaging as well as new ideas that people are planning for the mobile phone revolution to continue.

Dr Haba is responsible for overseeing next-generation research and development activities for Tessera, Inc. Dr. Haba was a founder of SiliconPipe Inc. His previous positions include managing the packaging research and development division at Rambus, managing advanced research and development projects at the NEC Central Research Laboratories in Japan and, before that, he worked for IBM at its T.J. Watson Research Center in New York. He holds 93 U.S. patents, and over 150 worldwide patents and patent applications. Dr. Haba was awarded the Most Inspirational Paper award at the 2006 BiTS Workshop.
Catching the Mobile Wave: Packaging is Going 3D

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

Belgacem Haba, Ph.D.
Tessera

Outline

• Introduction
• Driving forces and limitations
• 3-D package stacking
• 3-D wafer-level stacking
• 3-D by embedding technologies
• 3-D in optics
• Conclusion
Packaging is the key

- About 1cm cube of silicon
- The rest is Packaging

Mobile Phone Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>1970s</th>
<th>1980s</th>
<th>1990s</th>
<th>Today</th>
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<tbody>
<tr>
<td>Price</td>
<td>~$5000</td>
<td>~$4000</td>
<td>~$300</td>
<td>Free Voice, Data</td>
</tr>
<tr>
<td>Voice</td>
<td>Voice</td>
<td>Voice</td>
<td>Voice</td>
<td></td>
</tr>
</tbody>
</table>
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Evolution of Memory

- 5MB IBM hard drive, 1956

Jan 7th PR: SanDisk Announces the 12-Gigabyte microSDHC Card – the World's Largest Capacity Card for Mobile Phones

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The Inside of Mobile Phones

Mobile Phone Components
- Camera Module
- Display
- LEDs
- Substrate
- Discretes
- Subsystem
- Connector

Mobile Phone Distribution of BOM
- IC Packaging 6%
- ICs 35%
- Other 22%
- Off-Chip Electronics
- Displays 17%
- Connectors 3%
- Substrates 5%
- Discretes & LEDs 4%
- Cameras 8%

Source: Portelligent, Tessera

2007 ITRS & iNEMI Updates
Packaging is now a limiting factor but it is enabling for More than Moore

- Packaging has become the limiting element in system cost and performance
- The Assembly and packaging role is expanding to include system level integration functions.
- As traditional Moore’s law scaling become more difficult innovation in assembly and packaging can take up the slack.

Source: ITRS & iNEMI 2007 updates
Which way to go?  
System Integration

Cost / function  
Time to market

System on Chip  
Bio-Interface  
MEMS  
SIP and 3D Packaging  
Power supply

System complexity

Source: ITRS Assembly & Packaging WG, April ’07

Mobile Phone

Source: Portelligent

March 9 - 12, 2008
### Phone Thickness Drivers

- Voltage control inductors
- High-value Capacitors
- Filters
- Oscillators
- Camera
- Connectors
- Battery
- Package stacking

Source: Portelligent.

### Integrated Hermetic Packaging

- SAWs, crystal oscillators and many MEMS oscillators require hermetic packaging
- Hermetic packaging is difficult to integrate into typical low-cost electronic assemblies

Source: Portelligent.
Main Board of Camera

Cameras are too thick

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Interconnect Pitch Limitations

Die size: 150 µm
Die pitch:

Package size: 500 µm
Package pitch:

SFT Silicon Interposer

60 µm Pitch Flip Chip
Silicon on Silicon Interposer
3D Electronics (like Human Evolution)

2D development 3D improves density and efficiency

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Third direction: Z direction

- As many die as possible in z-direction
- 3 solutions:
  - Wire bondable die stacking in single package
  - Package stacking (POP: package on package)
    - Ball-Stack
    - Fold over
  - Through via die stacking

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Different Stacking Technologies

- Package stacking technologies
  - Solder ball
  - Cu pin
- Die stacking technologies
  - Wire bond stacking
  - Through Silicon Via stacking
  - Edge bond stacking

3-D: When to Die Stack vs. Package Stack

- % of Applications
- Vertical Die Qty
- Cumulative Die Yield
- Die Cost
- Source: Amkor / Sharp

Source: Amkor / Sharp
Package on Package

Addressing the Challenges – Reliability

- Mobile phones drop tests increasingly difficult to pass
- Underfill is a necessity – increases cost and effective size
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Latest High Die Stacking Press Releases

- **Samsung**
  - 16 die stacked
  - 8Gb NAND flash chips, can enable up to 16 gigabyte (GB) MCP solution
  - Wafer-thinning technology to only 30 micrometers (µm) (65% thickness of 10 chips)
  - November 01, 2006

- **Akida Elpida**
  - 20 stacked NAND Flash Chips @1.4mm thickness
  - Die Thickness: 30µm
  - April 23, 2007

- **Hynix**
  - 20 stacked NAND Flash Chips @1.4mm thickness
  - Die Thickness: 25µm
  - May 06, 2007

High die stacking (beyond 4-6) has substantial manufacturing challenges:
- High cost
- Compound yield
- Complex assembly process
- Questionable reliability performance

Challenges With Wire Bond Stack

- Grinding very thin die
- Handling of very thin die
- Wire bonding of thin die overhang
- Compound yield
- Testing and burn-in
“Via first” and “Via last” process flow

Via first

Via last

Through Silicon Vias

Eight Stacked Chips (WSP)

8-die Stack
Challenges with Through Silicon Vias

- Grinding very thin die especially at 12 inch wafers
- Handling of very thin die
- Rigidity in via design and via real estate
- Testing and burn-in
- Availability of infrastructure

Stacking By Edge Connect

16-die Flash Stack

8-die Flash Stack

16-die Flash Stack
Wafer Level Edge Contact
From Tessera

Support wafer

Final Product
(Ready For Wire Bond)

<table>
<thead>
<tr>
<th>Item</th>
<th>Thickness</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die</td>
<td>~25 µm</td>
<td>a, b, c, d, e</td>
</tr>
<tr>
<td>Adhesive</td>
<td>~3 µm</td>
<td>e, f, g, h</td>
</tr>
<tr>
<td>Carrier</td>
<td>30 µm</td>
<td>i</td>
</tr>
</tbody>
</table>

Total Package Thickness ~ 155 µm
Final Product (Ready For Surface Mount)

Ultra thin 4 x Die stack

Six, 4-Die Stacks Within a Pkg
(24 die < 1 mm)

3D schematic

Wire bond to 6 WLSP

SD Card Footprint

Cross Sectional SEM

Toward 32 die in < 1 mm
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IMBERA Embedded Process

1. Component placement
2. Component placement 2
3. Stacking
4. Pressing
5. Plating
6. Patterning
7. Solder mask and surface finish

Source: Imbera
FREESCALE RADIO-IN-PACKAGE USING RCP

General Process Flow

1. Fabricate Memory Base with embedded components
2. Add Stacked Pkgs
3. Attach solder balls, Singulate, final test

Source: Freescale

FREESCALE RCP RADIO IN PACKAGE

All 'sub-assemblies' are fully tested using traditional 'non-integrated' test methodologies AND using conventional lowest test cost (ATE) platforms

NOW READY FOR SYSTEM INTEGRATION

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OCCAM Process

- Components placed on temporary or permanent base
- Components and base are overmolded with insulating material
- Component leads are accessed (e.g., by laser driling)
- Vias are plated along with circuit layer
- Circuits are coated with insulating material and access to terminations provided
- Additional circuits are plated and additional layers built up to create needed connections
- Final assembly: circuits not used for connection are protected with insulating material

Source: Verdant

Nokia Miniaturization Roadmap

- Packaging Roadmap
- 1988
- SIP
- Die Stack
- POP
- TSV memory
- Future POP
- Substrate
- Complementing S-interposer
- 2004
- 2007
- 2017
- Phone core electronics TSV
- True 3D system

Source: Nokia, ITR 2007
Embedded DRAM

 liquor 12: MCP with substrate embedded DRAM

Source: Intel

Likelihood of Evolution of POP

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Main Board of Camera
Cell Phone Camera Module

Passives
Image processor and memory

Source: Prismark

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COB Assembly
Smaller pixels - More particle problems

Lower Resolution
Larger Pixels
Particle has small effect on pixel

Higher Resolution
Smaller Pixels
Particle has large effect on pixel

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COB vs WLP Module Yield

![Graph showing COB vs WLP Module Yield](chart)

- **Package Yield (%)**
  - WLP
  - COB

- **Image Resolution**
  - VGA
  - 1.3M
  - 2M
  - 3M

- **Particle Contamination During COB Manufacturing Decreases Yield at Higher Resolution**

Wafer Level Camera Modules

**From This...**
- Digital Optics
- Shellcase

**To This...**
- Lenses
- IR Filters
- Wafer

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Revolutionizing the Camera Module

Conventional camera phone → OptiML™ wafer level technology

Image Without EDOF

1 Meter Away

Infinity

10 Centimeters Away
Conclusion

- Packages are getting thinner and thinner
- Contact pitch are getting smaller and smaller
- Multiple die packages will become the norm
- See more and more embedded passives and some actives
- Packages would have contacts from top and bottom
- Expect complex testing schemes