BiTS™ Burn-in & Test Socket Workshop

2008 HOT TOPICS

ARCHIVE 2008

FROM EVALUATION TO PRACTICE

"Keeping It Real: Simulating QFN and BGA Probe Performance in the Test Lab"

Kevin Deford, Nick Argyros, Jon Diller
Synergetix

"Finite Element Analysis Using Elastic Membrane Technique for Test Socket Design Optimization"

K. Prabakaran, Ila Pal
Antares Advanced Test Technologies

"High-Performance Contactors for Wafer-Level Test (WLT)"

Jim Brandes
Everett Charles Technologies

"A Latch System for the Delicate IC Package"

Hideyuki Takahashi, Hide Furukawa
Sensata Technologies, Inc.

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SYNERGETIX

Keeping It Real:

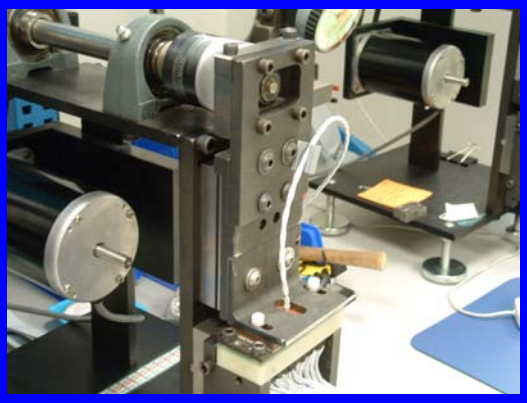
Simulating QFN and BGA Probe performance in the Test Lab

Authors:
Kevin DeFord, Nick Argyros & Jon Diller

Presented by:
Kevin DeFord

BiTS Burn-in & Test Socket Workshop 2008

Conventional Test Method



- Gold substrate
- Avg R < .05 Ω
- > 1KK Contacts
- Perfect world!

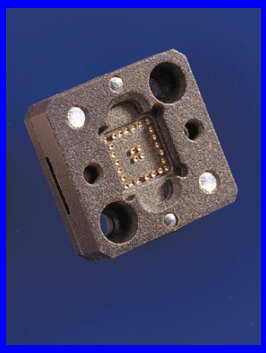
Paper #1

- Pros
  - Reliable method
  - Repeatable
  - Free from artifacts
  - Low/predictable cost
- Cons
  - Application life expectancy
  - Meaningful maintenance cycles
  - Fretting engine

Design Challenge #1

- Simulate application life
- Virgin hit every contact
- Measure individual 4-wire resistance
- Flexibility
- > 500,000 virgin contacts

Lead Free Contact Materials



QFN Copper Lead Frame

- Matte Sn
- NiPd/Au
- Pd/Au
- SAC 105

03/2008 Keeping it Real: Simulating QFN and BGA Probe performance in the Test Lab 5

Handler Simulation Test System

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Handler Simulation Test System

Fixture Stack Up

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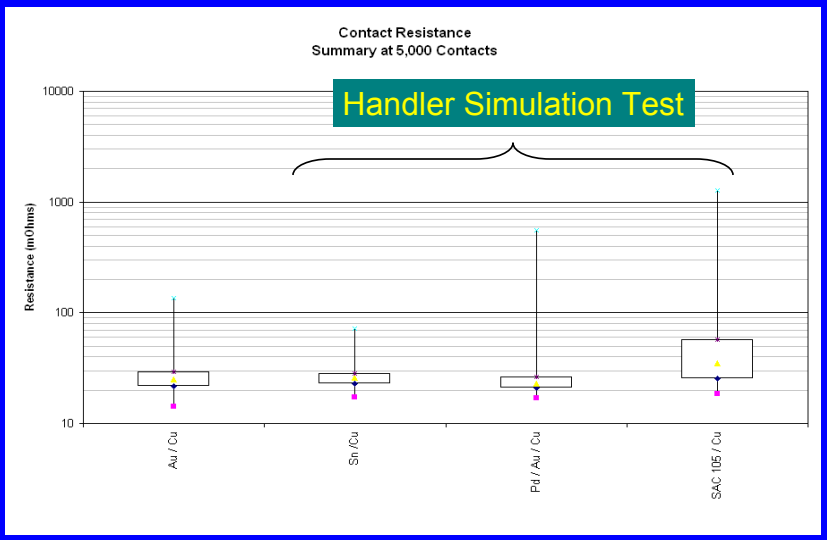
Comparison of Contact Resistance



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Cons

- Inverted design
- Limited to spring pin contacts
- Can't simulate BGAs
- Socket artifacts

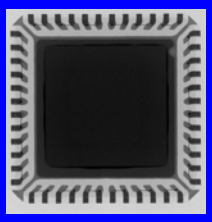
Design Challenge #2

- Test socket applications
- Pick and place devices
- Focus on SAC family of alloys
- Test against BGAs and QFNs
- Cross different contactor platforms

Lead Free Devices, 0.5 mm Pitch

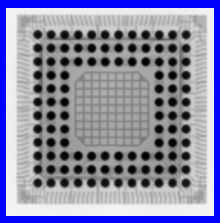
QFN

- Matt Sn



BGA

- SnAgCu
  - 105
  - 305



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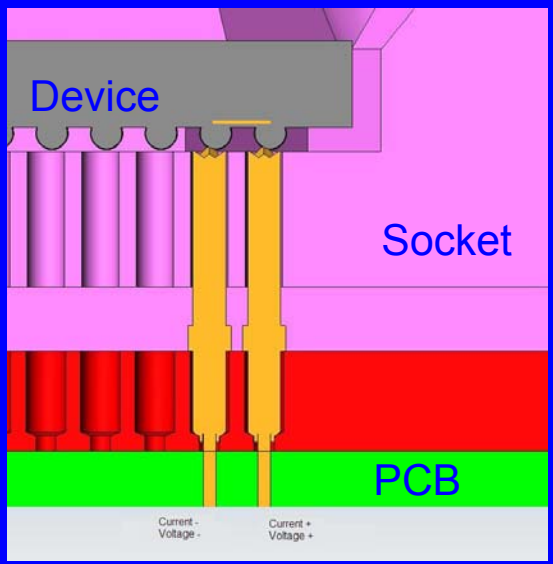
- Daisy chain devices
- Loop 4-wire resistance
- Socket provides device alignment



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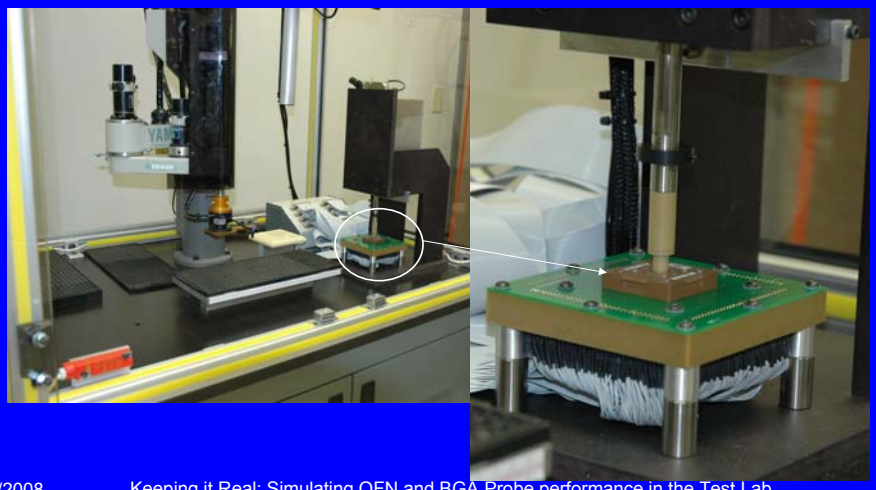
Handler Simulation Tester for Sockets



Test parameters

- Device insertion – Pick n place into socket
- Insertion Force – 7.25 Kg
- Current – 25 mA
- Device – Pick up – Drop – Plunge
- Test virgin devices at scheduled stops

- Pros
  - Physical interaction with BGAs
  - Cross over platforms
  - Socket/device wear characteristics
- Cons
  - High Cost
  - 5-10K contacts/day
  - Must recycle devices

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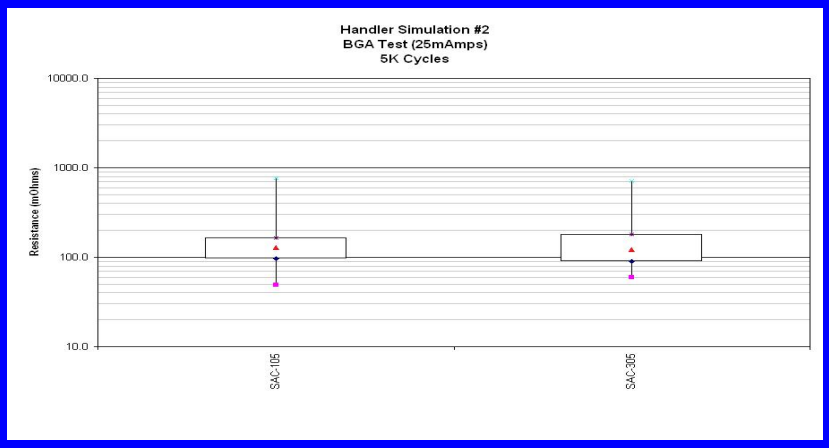
SAC Comparison in HST2



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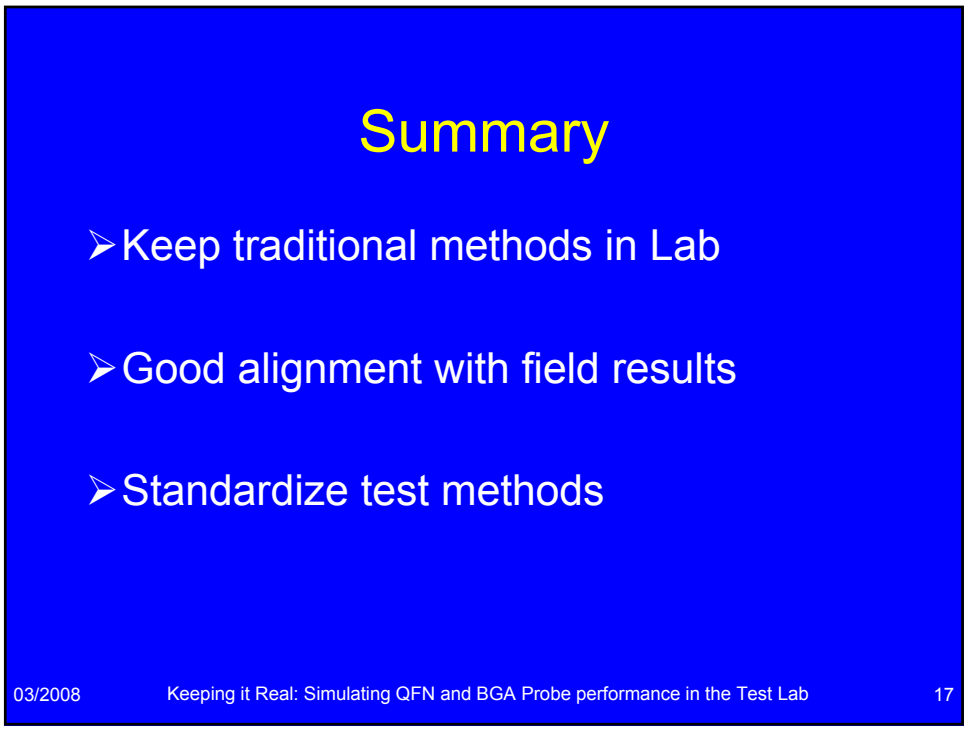
Summary
Keep traditional methods in Lab
Good alignment with field results
Standardize test methods
03/2008
Keeping it Real: Simulating QFN and BGA Probe performance in the Test Lab
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Finite Element Analysis Using Elastic Membrane Technique for Test Socket Design Optimization

2008 Burn-in and Test Socket Workshop
March 9 - 12, 2008

(Praba) K. Prabakaran
Ila Pal
Antares Advanced Test Tech.

Overview

- FEA
- Assumptions
- Socket
- Pin – Free and Test State
- Problem
- Solution
- Validation
- Conclusion

FEA

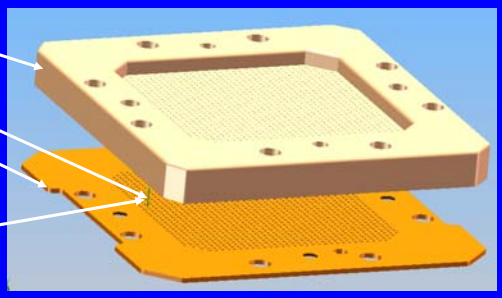
- Computer model of a material/design that is stressed and analyzed for specific results
- Load -> Deformation -> Strain -> Stress
- Excellent tool for design comparison
- Easy to determine design modifications to avoid failure – deformation, stress
- Young Modulus (E) and Poisson's Ratio (ν)
- Shear Modulus calculated, G = E/(2*(1+ν))

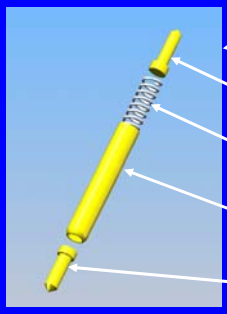
Assumptions

- Linear Analysis
- Don't allow large deformation
- Don't have stress-strain curve for material
- Isotropic (properties are same in any direction)
- Homogeneous (consistent properties throughout)

Package Test Socket

Socket Body
Spring Pin
Retainer Plate





Terminal
Spring
Barrel
Plunger

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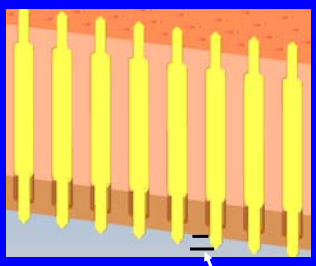
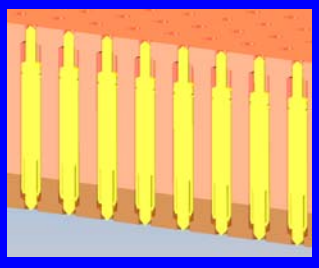
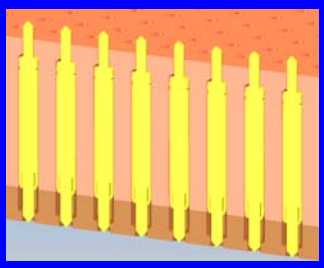
Pin - Free and Test State

Free State
PreLoad State
Test State
(Device and LoadBoard not shown)







PreLoad
Travel

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Problem

- When socket mounted to the load board, pins push the socket body to bow
- Socket bowing causes preload to vary from high (outer edge) to low (center), even no preload, if deformation is high
- No preload may tilt and jam the pin inside the cavity
- No preload may damage the load board pad due to cyclic loading

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Solution

- The deflection value should be known in order to design the socket properly
- Use of Elastic Stiffener (membrane technique) to balance varying preload
  - To predict deformation
  - To predict stress values

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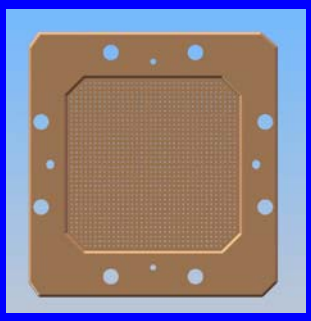
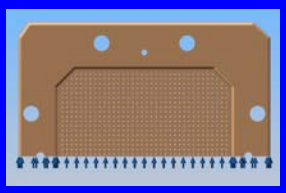
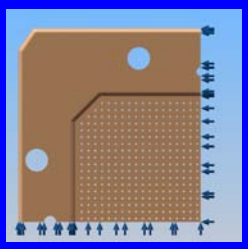
FEA: Symmetry

Use of quarter CAD model for more mesh and faster solution, if symmetry:

- Design
- Load
- Support







Full, 1/ 2, 1/4, 1/8 model …..

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FEA: Analysis

- Preload varies from low (center) to high (outer edge)
- Elastic Stiffener (membrane technique) to counteract varying preload
- Preload 8gf/pin
- Pin Spring Constant, *k* = 25 gf/mm
- Total 1,000 pins, 250 pins for 1/4 th model
- Preload = 250*8 = 2,000 gf
- Elastic Stiffness, *K* = 250*25 = 6,250 gf/mm

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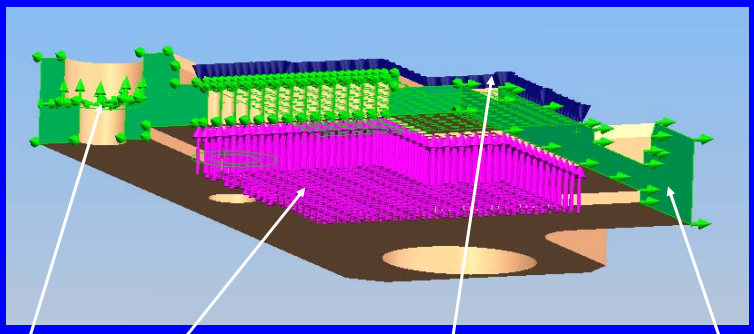
FEA: BC



Bolted (Fixed)

Preload (Bot. Surface)

Elastic Stiffness (Top Surface)

Symmetry (Two Planes)

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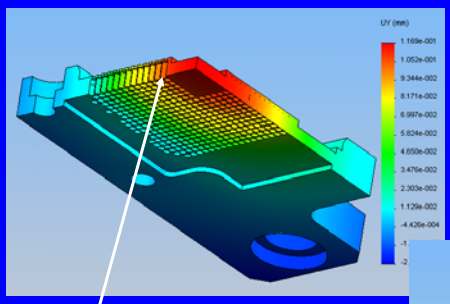
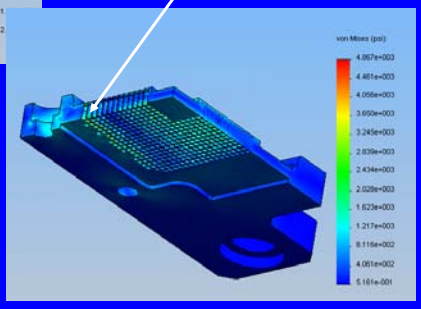
FEA: Results



Max. vonMises Stress is 4,800 psi



Max. deflection at Pin location is 3.9 mil

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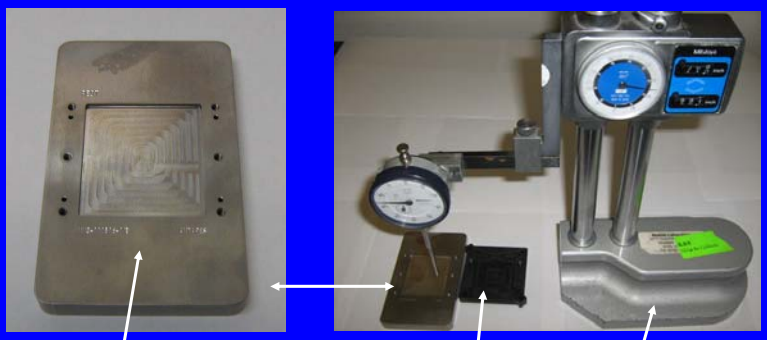
Validation



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Deflection

Socket	Measured	FEA (Membrane)	FEA (No-Membrane)
Project 1	3.2 mil	3.9 mil	5.5 mil
Project 2	3.5 mil	3.7 mil	4.6 mil
Project 3	1.2 mil	1.4 mil	1.6 mil

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Conclusion

- Elastic membrane technique predicts deformation value close to measured value
- Failure mechanism is mostly caused by higher deflection than stress, due to Preload
- Optimized socket design
- Reduced prototype and testing cost

High-Performance Contactors for Wafer-Level Test (WLT)

By
Jim Brandes

BiTS Presentation
March 11 2008

Agenda

- Traditional model: test devices at least twice
  - Once (or more) at the wafer level
  - Again after packaging
- New paradigm of final test at wafer level (Wafer-Level Test – WLT) eliminating test after singulation
  - Suitable package types (packaged at wafer level)
  - Economic advantages of eliminating one test
- WLT similar to both probe and package test
- WLT mechanically similar to probe

Agenda

- WLT must be identical to package test
- Mechanical challenges of wafer-level test
  - Fine-pitch requirements
  - Support for high parallelism (vertical contact)
- Electrical challenges of wafer-level test
  - High current, low resistance
  - Low inductance, high bandwidth
- High-performance probes and contactors for wafer-level test

3/2008 High-Performance Contactors for Wafer-Level Test (WLT) 3

Traditional Test Method

- Devices historically tested *at least* twice
  - Wafer probe
  - Final (package) test
  - Majority of devices only tested twice
- Some devices tested more
  - Military (high & low temperature)
  - Industrial (high temperature)
  - Burn-In (value-added process)

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Traditional Test Method

Wafer Probe

- Confirms device functionality
- Cannot be a complete and thorough test
  - Devices' parametric performance is affected by packaging
  - Contacting constraints exist with traditional methods
  - Testing at-speed possible, but expensive
- Performed to increase probability that only good die are packaged
  - Packaging adds significant cost
  - Prefer to screen rejects at the wafer level

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Traditional Test Method

Final (Package) Test

- Performed at device specification limits
  - DC tests
  - AC tests (measurements or high-speed functional)
  - Functional at specified I/O levels
- Confirms performance with packaging effects included
  - Bonding wires or other internal paths
  - Package material as dielectric
- Checks for packaging defects
- Traditionally last test step before shipping

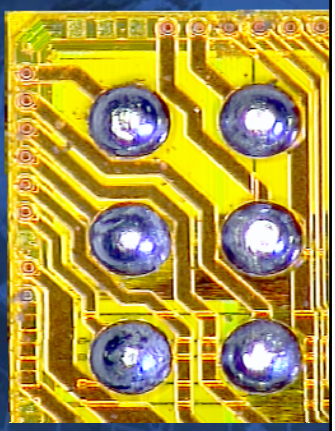
3/2008 High-Performance Contactors for Wafer-Level Test (WLT) 6

New Method – Final Test on Wafer

Wafer Level Packaging (WLP)

- Redistribution layer
- Encapsulation
- Ball attach or contact pad plating
- Ready to be diced, boxed and shipped

- Packaging at wafer level allows testing at wafer level



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New Method – Final Test on Wafer

Economic Advantages

- Testing traditionally >10% of cost of device manufacture
- Testing once rather than twice has potential to halve this
- Advantage less profound, but still present for those devices tested more than twice
- Improved possibilities of parallelism
- Shorter time to market

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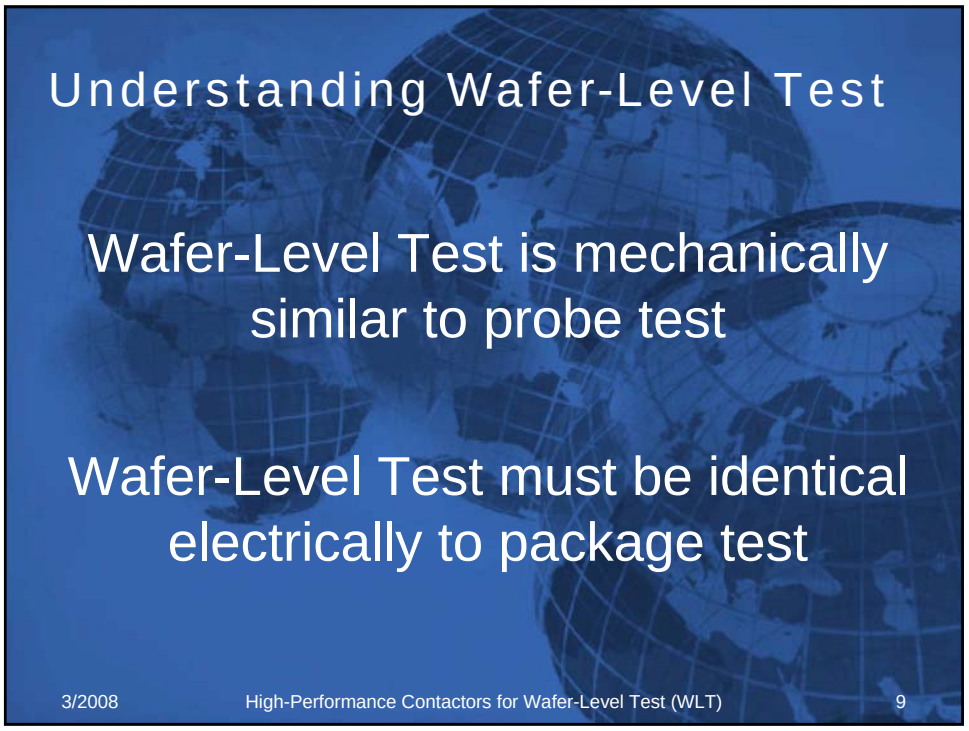
Understanding Wafer-Level Test
Wafer-Level Test is mechanically similar to probe test
Wafer-Level Test must be identical electrically to package test
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High-Performance Contactors for Wafer-Level Test (WLT)
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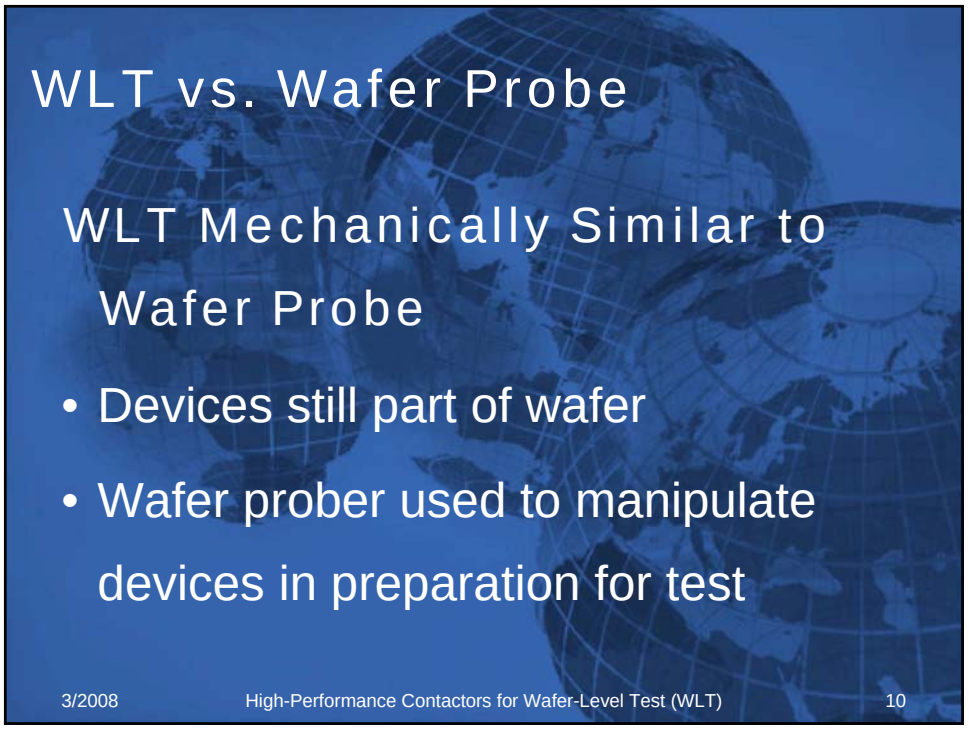
WLT vs. Wafer Probe
WLT Mechanically Similar to Wafer Probe
• Devices still part of wafer
• Wafer prober used to manipulate devices in preparation for test
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WLT vs. Wafer Probe

Wafer-Level Test *Is* Final Test

- DC tests
  - High current
  - High voltage
  - Accurate force values
  - Accurate measure values

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WLT vs. Wafer Probe

Wafer-Level Test *Is* Final Test

- Functional tests
  - Drive minimum V_{IH}
  - Drive maximum V_{IL}
  - Confirm minimum V_{OH} @ I_{OH}
  - Confirm maximum V_{OL} @ I_{OL}
  - Power supplies at minimum / maximum

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WLT vs. Wafer Probe

Wafer-Level Test *Is* Final Test

- Timing / AC tests
  - Full clock speed
  - Worst-case input timing combinations
  - Confirming input-to-output timing
  - Time measurements
  - RF tests (gain, SNR, THD, etc.)

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WLT vs. Wafer Probe

WLT Challenges - Mechanical

- Fine-pitch requirements
  - Currently at 0.4 and 0.3 mm pitch
  - 0.25 mm and smaller soon
- Vertical Contact
  - Support for high parallelism
  - Support for area arrays
- Adequate force requirements
  - More force required than wafer probe
  - 20 g - 30 g to pierce solder oxide and debris

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WLT vs. Wafer Probe

WLT Challenges - Mechanical

- Stack height
  - Probers not capable of plunging to board
  - Additional height diminishes performance
- Cleaning
  - Abrasive scrub for cantilever probe not appropriate
  - New cleaning techniques required
- Compliance
  - Bumped wafers not as coplanar as wafer pads

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WLT vs. Wafer Probe

WLT Challenges - Electrical

- High current requirements
- Low, consistent resistance
- Low inductance requirements
- High bandwidth requirements
- *Everything that is required for final test*

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WLT vs. Wafer Probe

Traditional Spring Pins
(Probes / Pogo® Pins)

- Address most challenges
  - Adequate forces
  - High currents
  - Vertical contact
  - Compliance
- Cost effective

WLT vs. Wafer Probe

Traditional Spring Pins
(Probes / Pogo® Pins)

- Might not meet some requirements
  - Fine pitch
  - Low inductance
  - Long life
- Cannot meet all simultaneously

New-Generation Spring Pins Meet All the Requirements

New Architecture Spring Probes

–High electrical performance

–High mechanical performance

–Cost-effective manufacturing method

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New-Architecture Probe

New Architecture

– Single-ended
  - Made of two pieces and spring
  - No barrel
– All external surfaces allow excellent plating quality and consistency
– Scalable architecture suitable for 0.2 mm and below

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New-Architecture Probe

High Electrical Performance

- Short, wide signal paths
- Low, consistent resistance
- Low inductance
- High bandwidth

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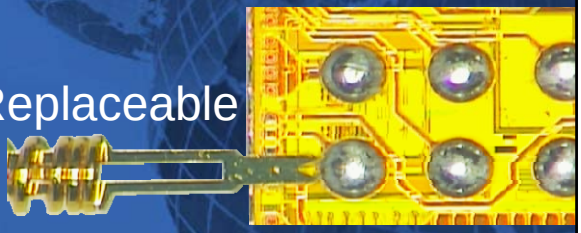
New-Architecture Probe

High Mechanical Performance

- Good force
- High compliance for a small probe
- Long life
- Individually Replaceable



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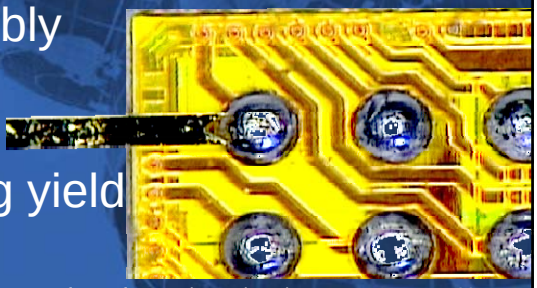
New-Architecture Probe

Cost-Effective Probe

- Fewer probe parts
- Lower cost than turned parts
- Easier assembly
- Better plating improves manufacturing yield



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New-Architecture Probe

Sample Specifications Electrical

	0.4 mm	0.3 mm
Bandwidth	25.8 GHz @ -1 dB*	12.4 GHz @ -1 dB*
Loop Inductance	0.91 nH*	1.12 nH*
Continuous Current	1.2 A @ 20° C rise	TBD
	1.7 A @ 40° C rise	TBD
Current @ 1% duty cycle	7.7 A @ 20° C rise	TBD

* Native pitch, GSG, Vespel dielectric

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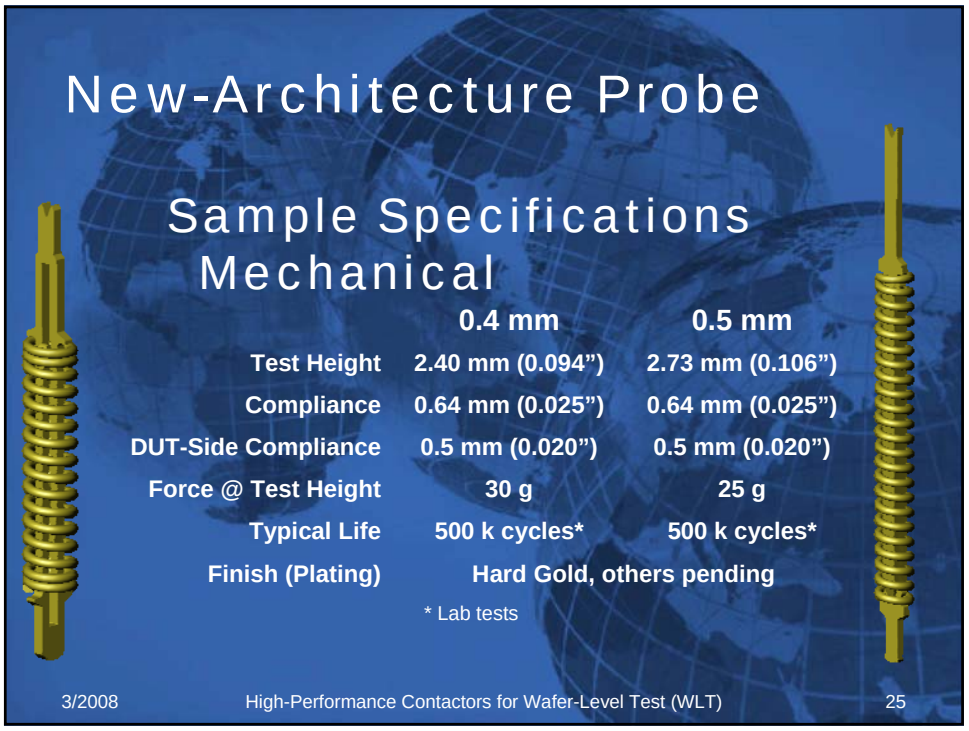
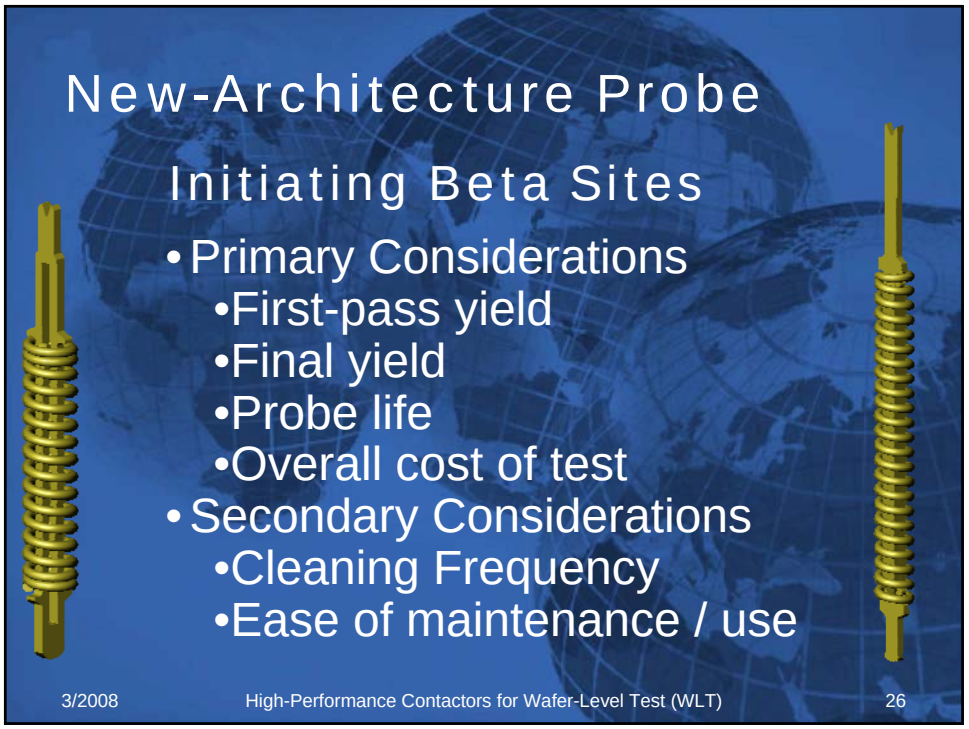

New-Architecture Probe
Sample Specifications
Mechanical
0.4 mm
0.5 mm
Test Height
2.40 mm (0.094")
2.73 mm (0.106")
Compliance
0.64 mm (0.025")
0.64 mm (0.025")
DUT-Side Compliance
0.5 mm (0.020")
0.5 mm (0.020")
Force @ Test Height
30 g
25 g
Typical Life
500 k cycles*
500 k cycles*
Finish (Plating)
Hard Gold, others pending
* Lab tests
3/2008
High-Performance Contactors for Wafer-Level Test (WLT)
25


New-Architecture Probe
Initiating Beta Sites
• Primary Considerations
•First-pass yield
•Final yield
•Probe life
•Overall cost of test
• Secondary Considerations
•Cleaning Frequency
•Ease of maintenance / use
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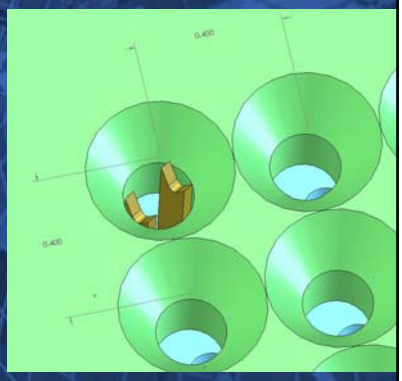
Future

- Highly scalable Architecture
- Probes designed for:
  - 0.2 mm pitch
  - 0.4 mm Kelvin Arrays



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High-Performance Contactors for Wafer-Level Test

Discussion

Thank You

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A Latch System for the Delicate IC Package

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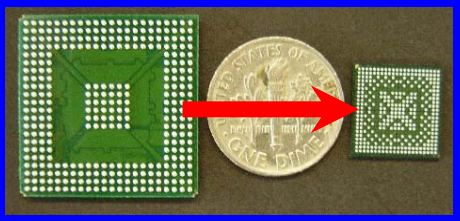
Japan / Attleboro, MA

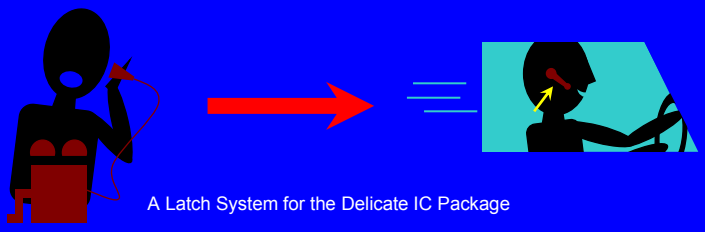
Overview

- IC Package Trend
- Burn In Test Socket Trend along with IC
- Typical Failure of IC at Burn in Process
- New Latch Solution
- Test Result (Actual and FEA)

IC Package Trend

IC package becomes smaller and thinner with technology change….



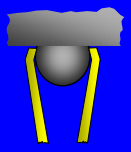


03/2008 A Latch System for the Delicate IC Package 3

Contact Technologies (1)

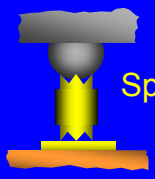
Contact needs to be changed due to the narrow pitch

0.65mm pitch and above

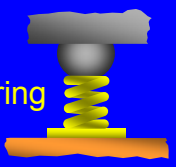


Pinch type

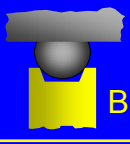
0.65mm pitch and below



Spring probe



Helical spring



Buckling beam

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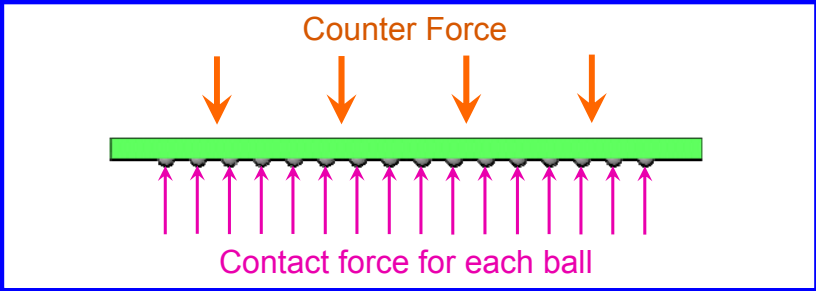
Contact Technologies (2)

Contact force from a compression style requires force on the top side of IC



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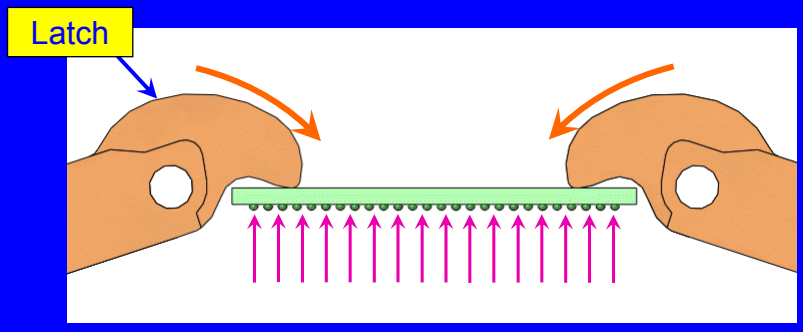
Current Latch System

The latch system is used to apply force to the IC in an open top burn in socket.



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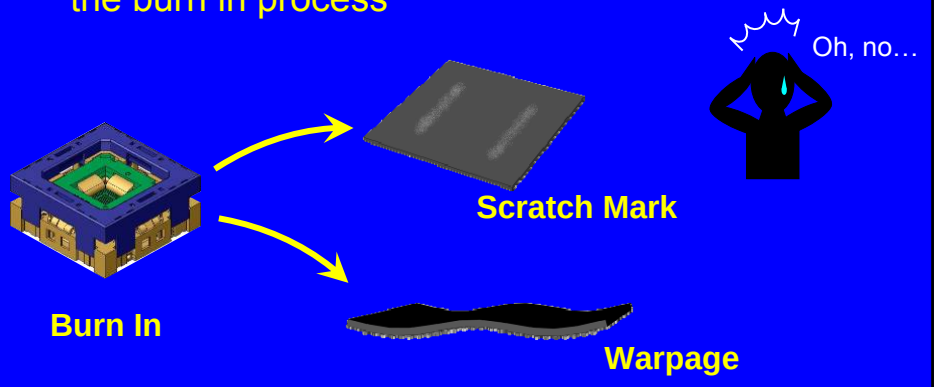
IC Failure at Burn In Process (1)

Miss matching of the latch and the delicate IC may cause undesirable result to the IC during the burn in process



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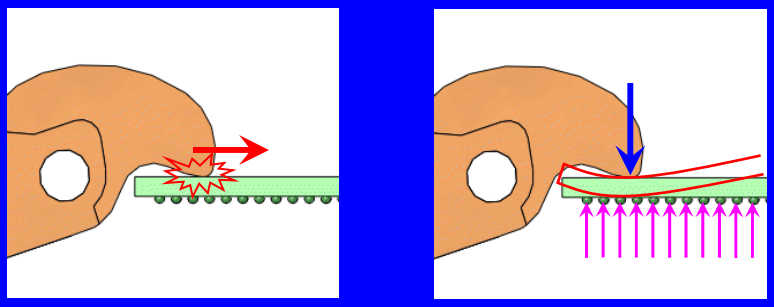
IC Failure at Burn In Process (2)

Potential latch design effects on delicate IC:

- Horizontal movement → Potential for Scratch mark
- Concentrated force → Potential for Warpage



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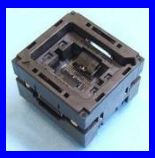
IC Failure at Burn In Process (3)

Current solution for these problems:

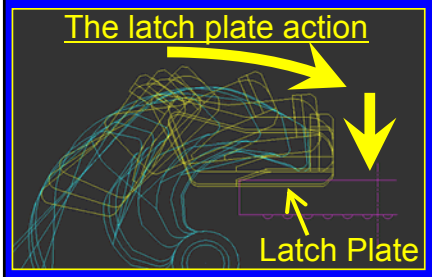
- Use lubricated plastic material on Latches
  → Plastic also contains glass filler
- Latch surface coating for lubrication
  → Coating comes off easily
- Rocking latch plate
  → Works for warpage, but not for scratch mark

Vertical Action Latch (1)

"Vertical Touch" – Latch system

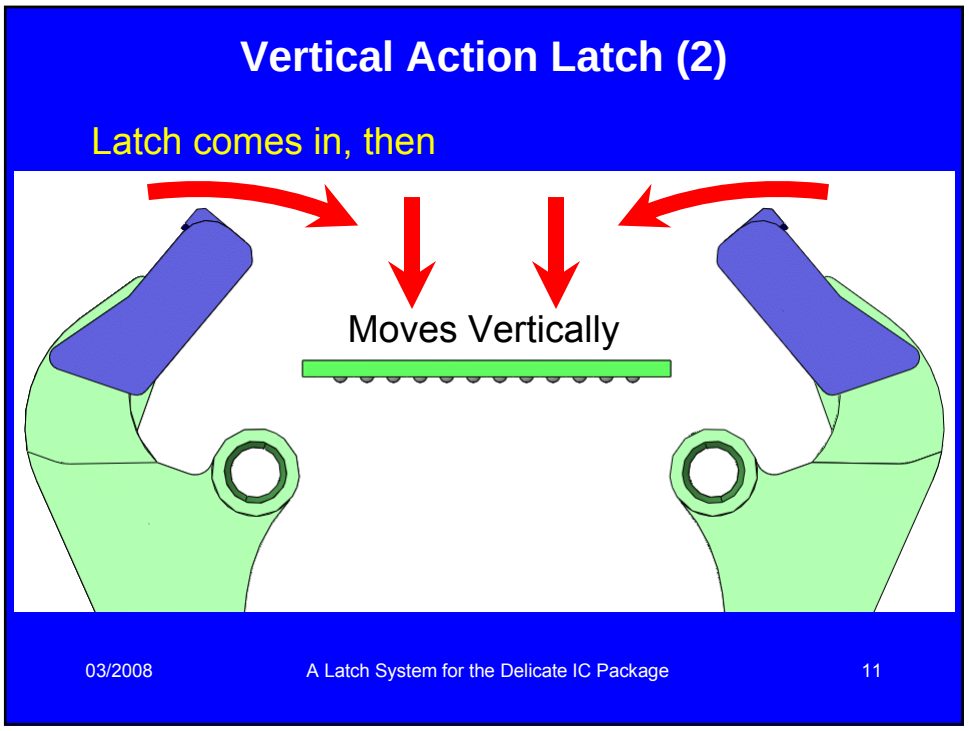


The latch pushes down on the IC with completely vertical action. (Patent pending)



The **vertical action** avoids any scratch mark on the IC surface.

The **latch plate** distributes the latch force to a wider area.


Vertical Action Latch (2)
Latch comes in, then
Moves Vertically
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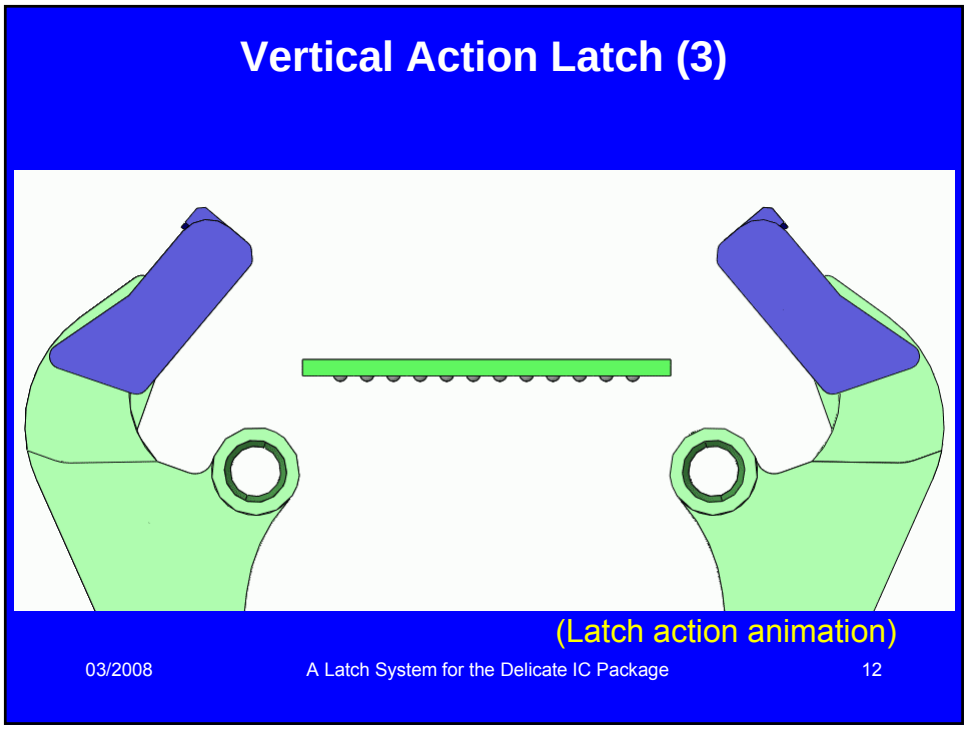
Vertical Action Latch (3)
(Latch action animation)
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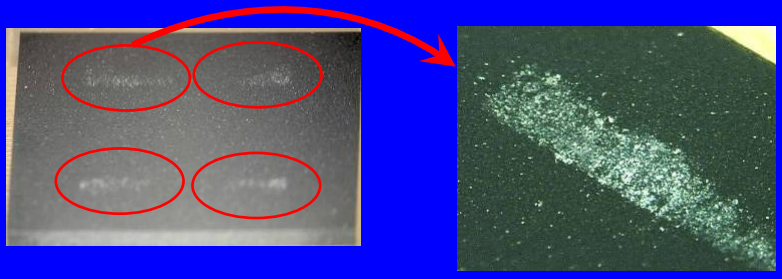
Test Result (1)

Scratch mark result (current latch)

After 10 cycles



The scratch mark is very visible and significant.

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Test Result (2)

Scratch mark result (Vertical Touch)

After 100 cycles

After 5000 cycles

After **10000 cycles**

No scratch mark even after 10000 cycles.

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Test Result (3)

Test results (IC warpage, 140 deg.C / 24 hours)

Without Latch Plate

With Latch Plate

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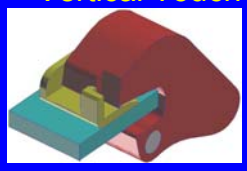
FEA Result (1)

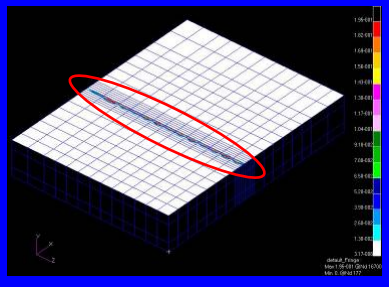
Force distribution

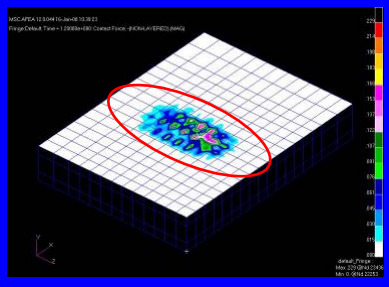
Current Latch

Vertical Touch distributes the force to 10 times larger area than current design.

Vertical Touch







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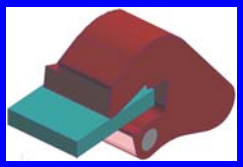
FEA Result (2)

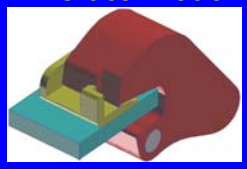
Deformation analysis

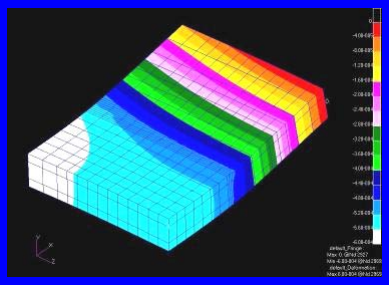
Current Latch

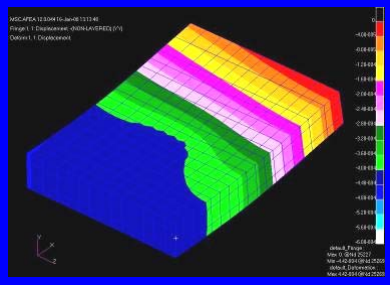


Vertical Touch improves deformation by 27%.

Vertical Touch







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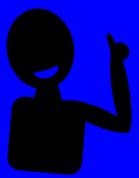
Applications

"**Vertical Touch**" – Latch system

Distributing the force over a **large area** with **Non horizontal** movement avoids scratch marks and warpage on the IC.

Vertical Touch latch system is good for

- **Soft mold IC**
- **Bare die IC**
- **Thin IC**
- **PoP IC** / etc.



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Q&A

Thank you !