BiTS™ Burn-in & Test Socket Workshop

2007 TUTORIAL

ARCHIVE 2007

TUTORIAL 2

"AN OVERVIEW OF CRITICAL ISSUES IN IC PACKAGING"

by

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SEMICONDUCTOR PACKAGING has become increasingly critical as the package becomes the limiting factor in integrated circuit (IC) performance. This tutorial provides insight into the important aspects of these critical packaging issues. Topics include an overview of the IC packages used in volume production, trends in IC packages such as body size, pin count, and package pitch. Materials and test issues will also be addressed.

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IC Package Technology Trends

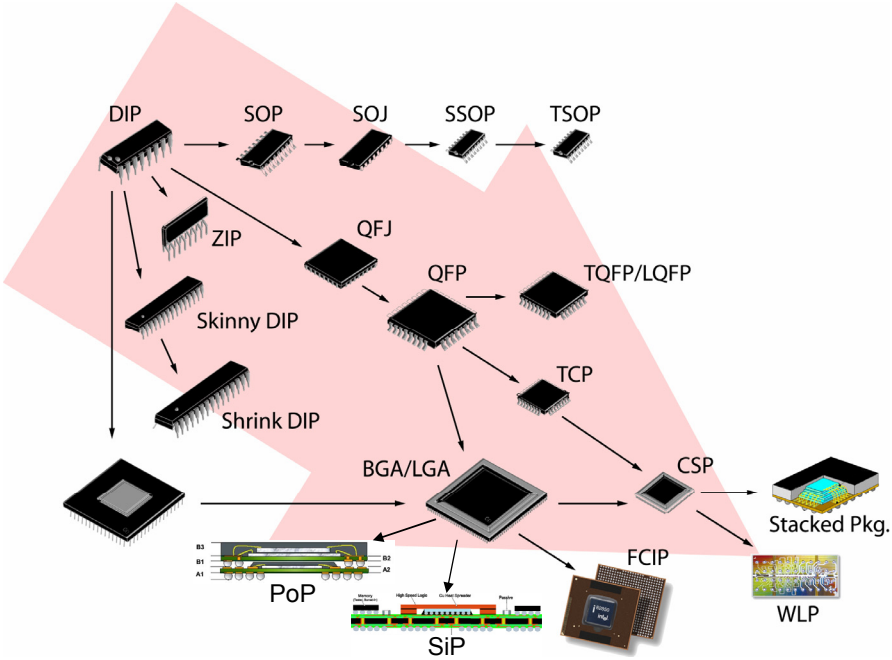
- Packaging of ICs is no longer the mundane process that took place at the end of the chip supply chain. For most products, today's packaging requires high level coordination between silicon and package designers.

- The proliferation of package technologies can be attributed to technical (performance) and cost demands being placed on the package by the device and system engineers.

- The high performance, increased functionality and space-sensitive applications have resulted in an increased rate of advanced IC package solutions to satisfy the demand.

- As a result of the extreme cost pressure that has been exerted on the electronic industry, package solutions that offer the minimum level of performance at the lowest cost will continue to be in demand.

Package Technology Evolution



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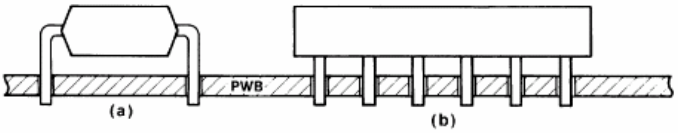
Package Technology Evolution

1960 – 1985	1986 – 1995	1996 – 2000	2001 – 2005
CDIP, PDIP+	SOIC, PLCC, QFP+	BGA, QFN, SiP+	Modules, Cards, Stack
> 50 pkg types	> 250	> 1000	> 1500

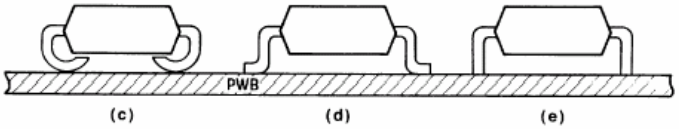
Source: Amkor

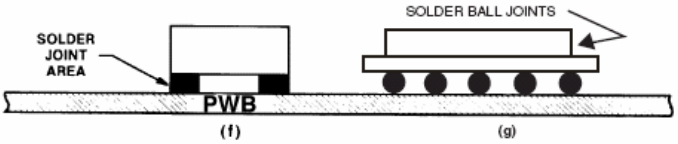
Board Level Packaging

Through Hole Mount Technology



Surface Mount Technology





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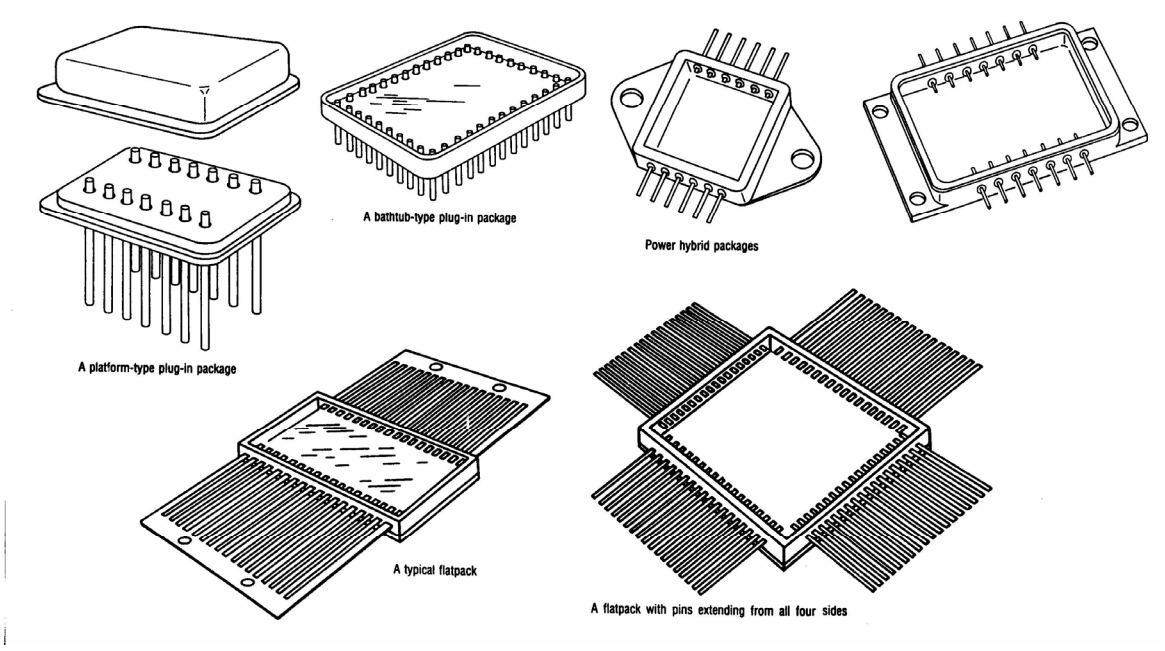
Prefabricated Metallized Ceramic Packages



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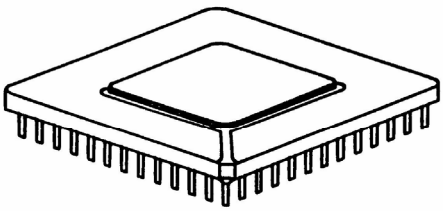
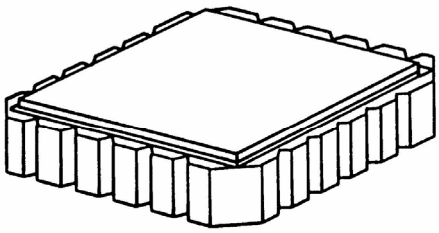
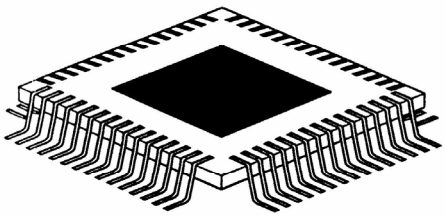
Prefabricated Ceramic/Plastic Packaging



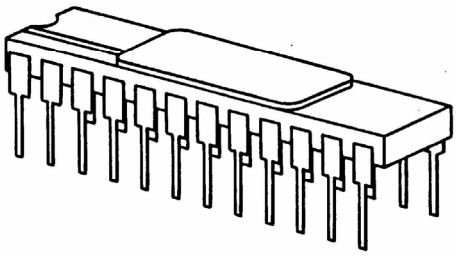
Ceramic PGA package outline



LLCC package outline



Ceramic Quad Flatpack



Side-brazed package outline

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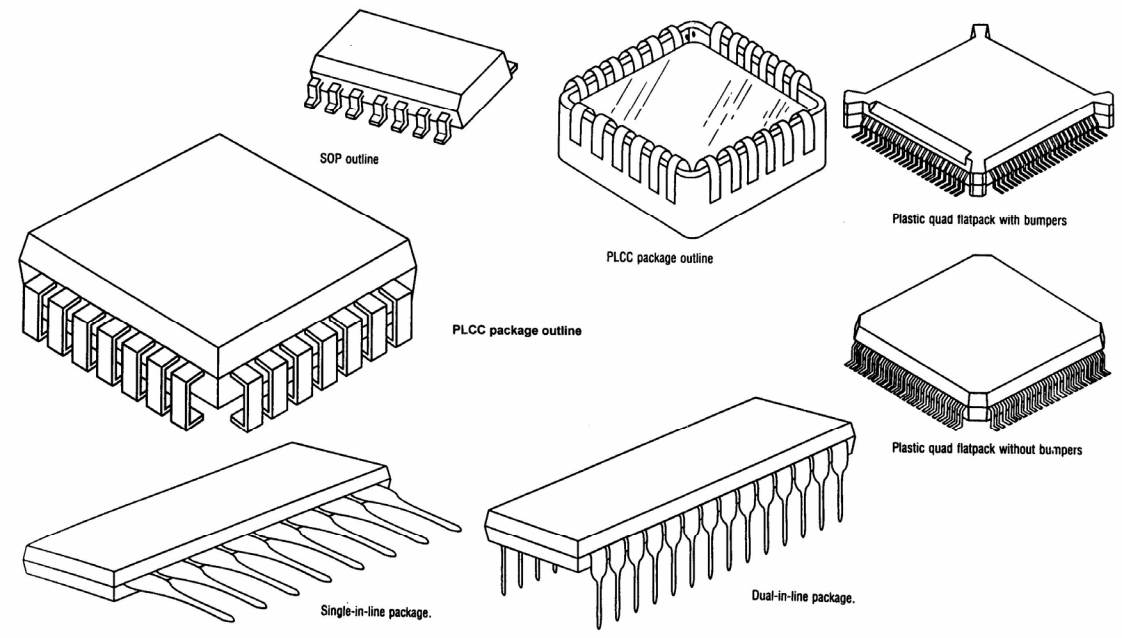
Postmolded Plastic Packaging



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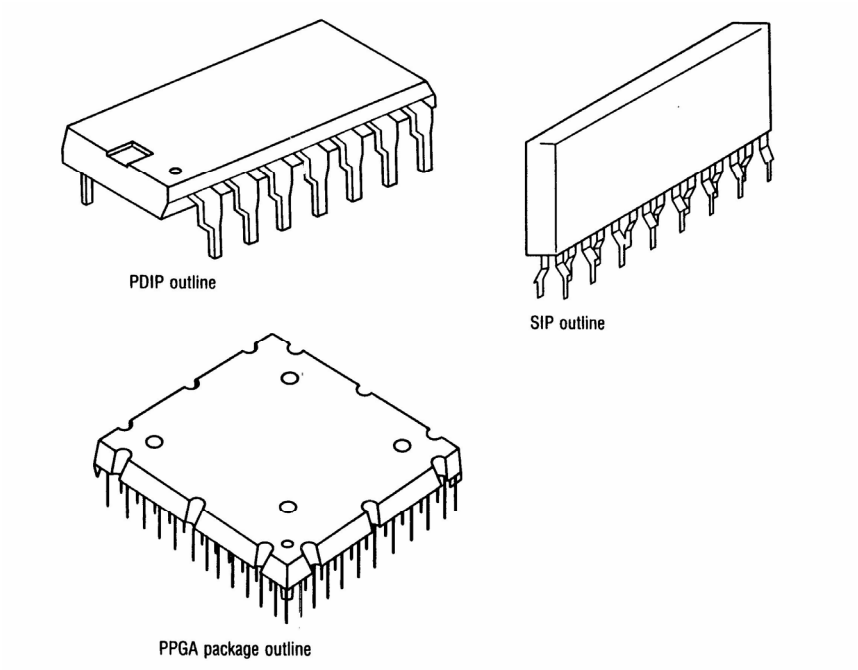
Postmolded Plastic Packaging



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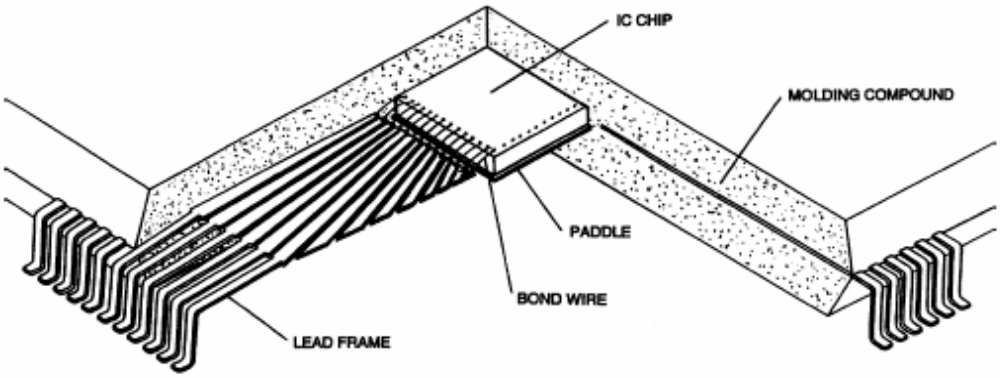
Typical QFP in a Postmolded Plastic Technology



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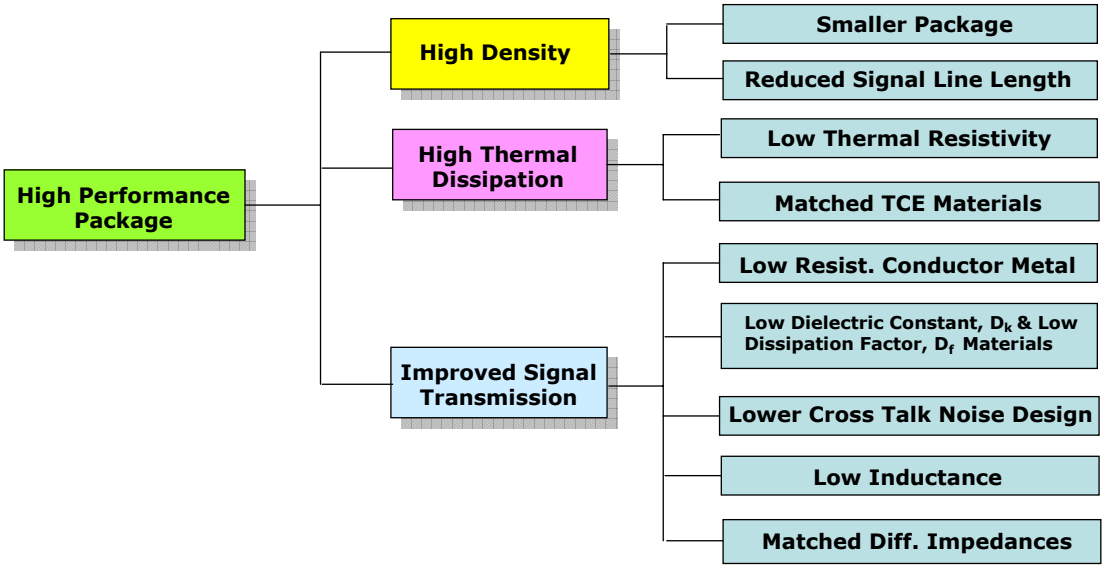
Driving Forces in Package Selection

- Product Application
- Silicon Technology
- Operating Frequencies
- No. of Input/Output Requirements
- Power Dissipation
- Environmental Operating Conditions
- Package Size
- Board Packaging Density
- Board Level Packaging Technology (Surface Mount/Through-Hole Mount)
- Compatibility with Existing Handling Equipment
- Time to Market
- Cost Cost Cost Cost

Next Generation IC Package Requirements



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Future Trends in IC Packages

- I/O count to increase
- Lead/ball pitches will decrease
- Packages will get thinner and lighter
- IC pad pitches will get smaller
- Area array pkgs. will grow in demand
- Higher performance, multilayer packages will be in demand
- Stacked die or modules such as system-in-package (SiP)
- Demand for ICs without packages will grow
- Package costs will decline
- Faster time to market requirements

IC Package Environments

- **Severe Environment**
- **Long Lifetime – Telecommunication**
- **High Power Dissipation – Microprocessor**
- **High Performance – High End Computer Systems**
- **Automotive**

Temperature	Driver Interior	-40° C to +85° C
	Under Hood	-40° C to +125° C
	On Engine	-40° C to +150° C
	Exhaust & Combustion	-40° C to +200-600° C
Mech. Shock	During Ass'y (drop test)	3000 G's
	On the vehicle	50 – 5000 G's
Mech. Vibration		15G, 100Hz to 2KHz
EM Impulses		100 to 200 V/m
Exposure to	Common	Humidity, salt spray
	In some applications	Fuel, oil, brake fluid

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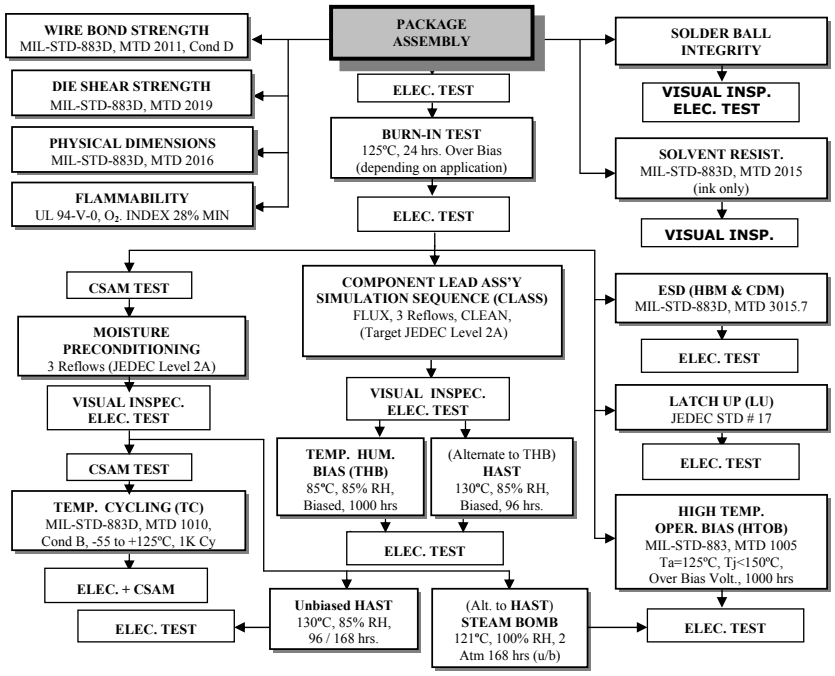
PBGA Qualification Tests for High Performance



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BGAs

- BGA Types (by construction)
  - PBGA
  - TBGA
  - CBGA/CCGA
- BGA Applications
  - Personal Computers (largest volume)
  - Game Machines
  - Workstation/Servers
  - Network Systems
  - Telecommunications
  - Military
  - Automotive

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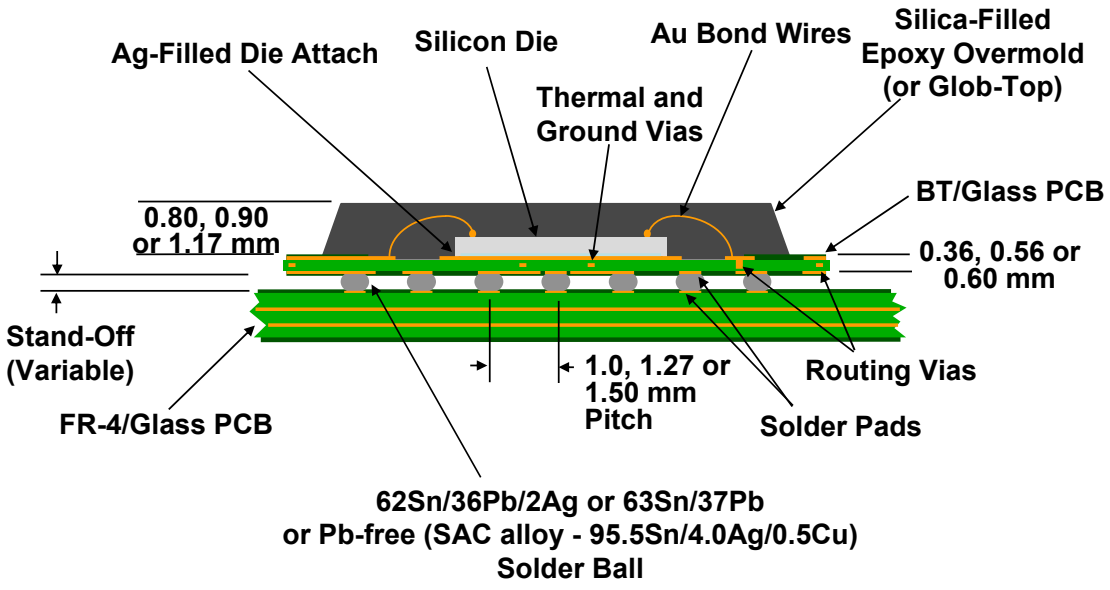
PBGA Construction



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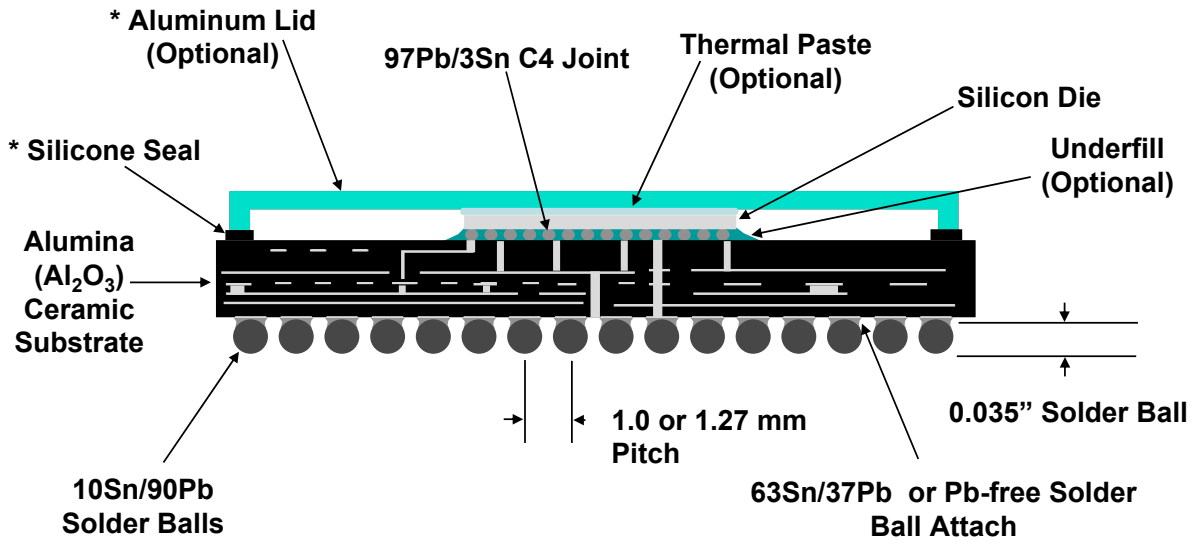
CBGA Construction



* Hermetic Lid and Seal Available

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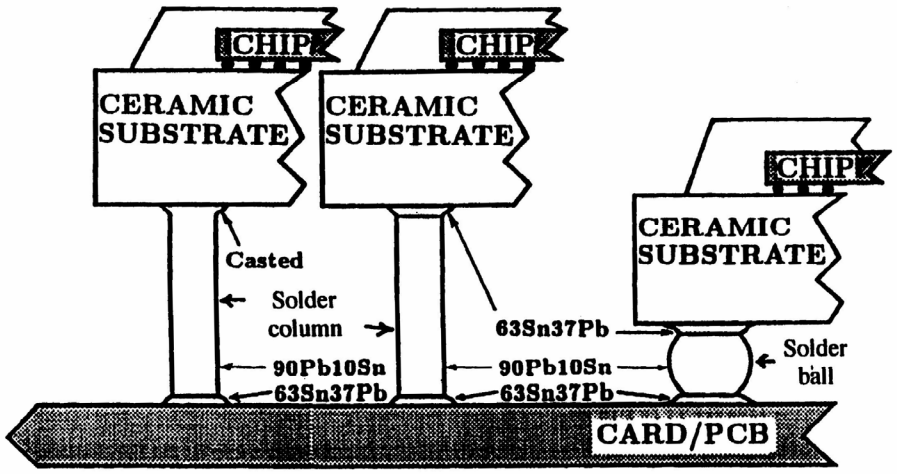
CBGA Solder Interconnects and Attachments



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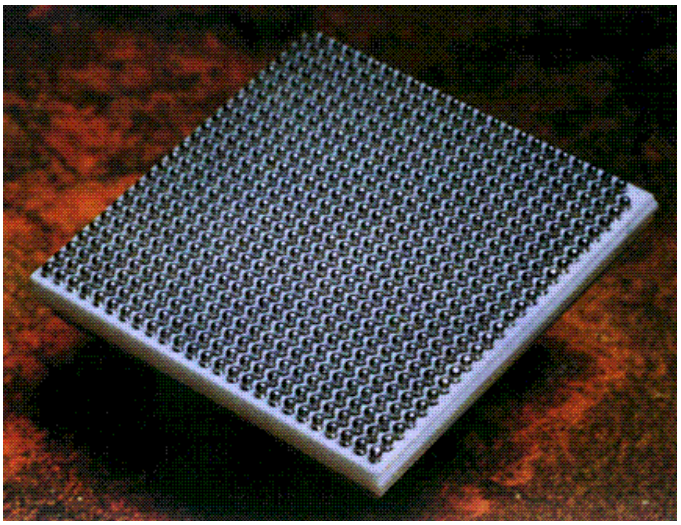
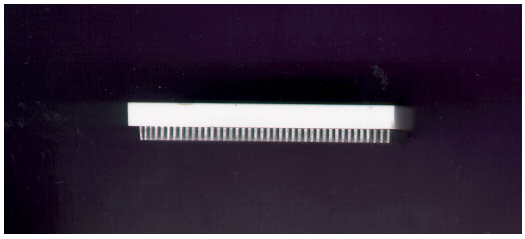
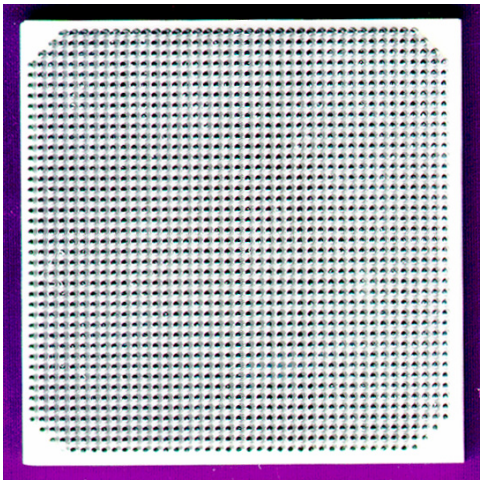
CBGA Construction

Typical Ceramic Ball Grid Array
(624 Pin, 32 mm Body, 1.27 mm Pitch, 25x25 Array Shown)



IBM's High Pin Count CCGA





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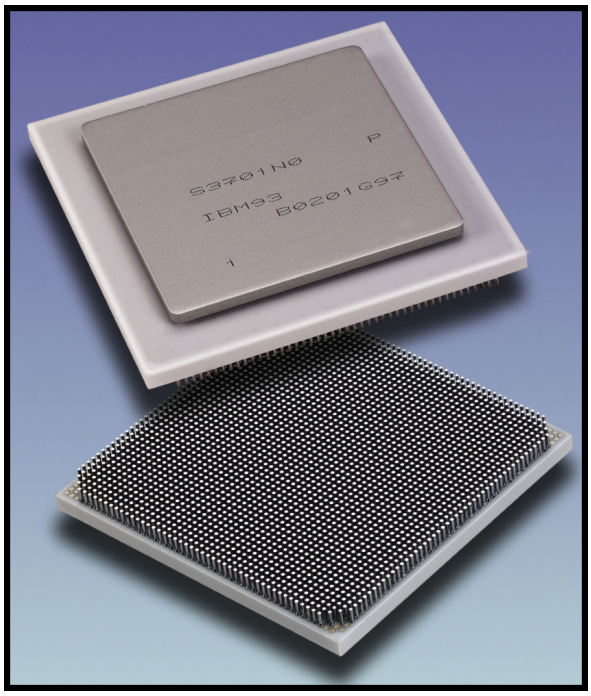
IBM's 2,577 CCGA with 1.0mm pitch



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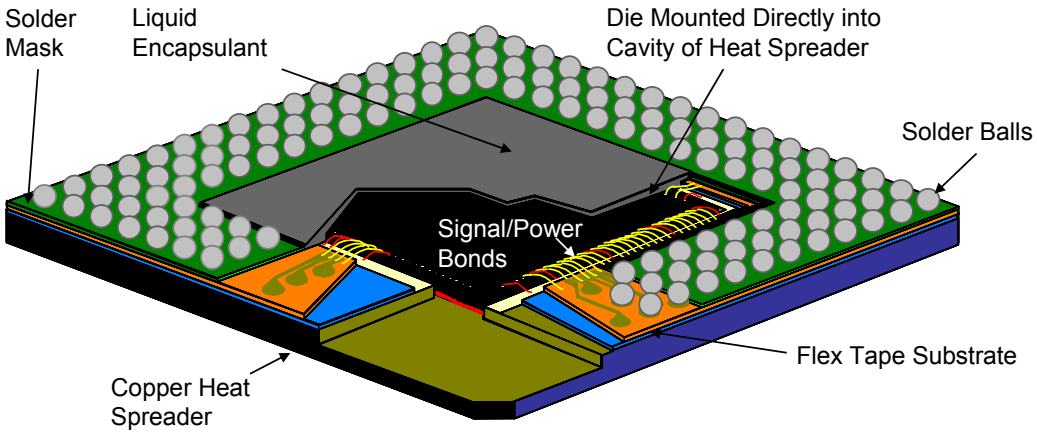
TBGA with Wire Bond

1 Metal Version



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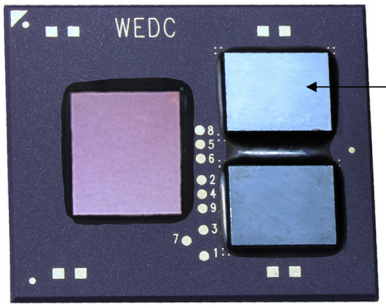
PC High Performance Packaging Trends

- PCs represent increased performance, lower prices
- Personal computers were volume driver for IC packages in 1990s, still driver for BGAs
  - Ball grid arrays (i.e., chip sets)
  - Flip chip (all CPUs for PCs now flip chip)
  - Movement from ceramic to laminate technology
- Major thermal issues for high-performance CPU packaging
  - TIM1 materials currently include indium solder
  - Critical need for development of improved thermal interface materials (TIM)
- Integrated circuit I/O counts continue to grow

Workstation/Servers, Network Systems, Telecom

- Sun Microsystems
  - Highest pin count flip chip packages (728, 784, 1,012, 1,089, 1,155, 1,280, 1,677, 1,848 balls)
  - 1,848-ball package with 42.5mm x 42.5mm body and 1.0mm ball pitch in production
  - SPARC processors still packaged in a ceramic LGA
- Cisco Systems
  - Ceramic CCGAs up to 1,657 I/O CCGA with flip chip inside
  - Increasing use of laminate substrate (2,577-ball HyperBGA with a 52.5mm x 52.5mm body size in production)
- Motorola Network Processor
  - Packaged in a 480-ball TBGA with 37.5x37.5mm body size, 1.27mm ball pitch

PowerPC for Military Applications from White Electronic Design



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What's a CSP

- Chip Scale Package or Chip Size Package?
- Chip size – packages that have the same area as the chip
- Chip scale package is defined as: $\frac{Package\ \ Area}{Die\ \ Area} \leq 1.2$
- EIAJ/JEDEC defines CSP as a package with an edge dimension no more than 1.2 times that of the die inside

EIAJ = Electronics Industries Alliance Japan

JEDEC = Joint Electron Device Engineering Council

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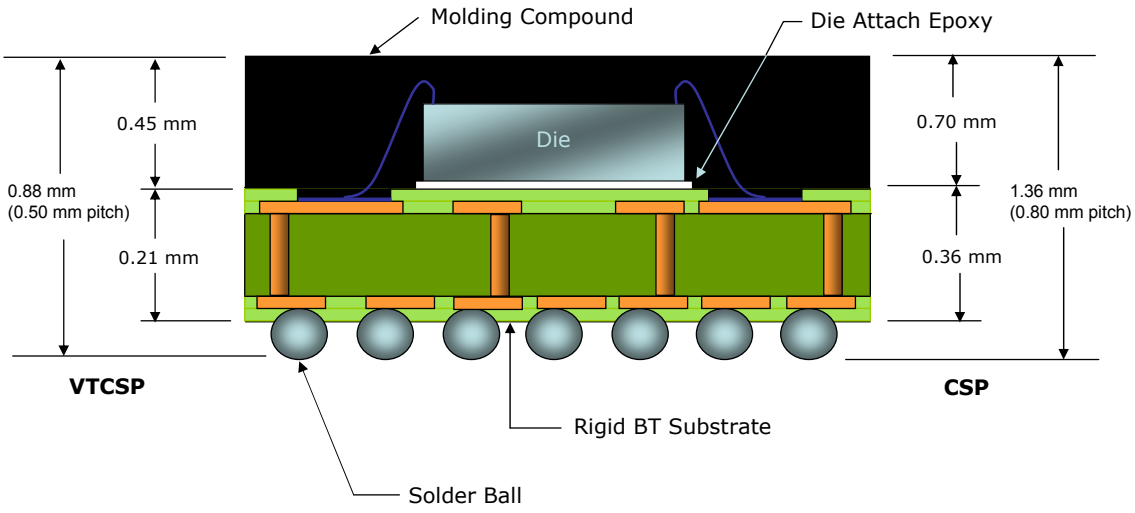
Typical Cross Section of a Plastic CSP Pkg.



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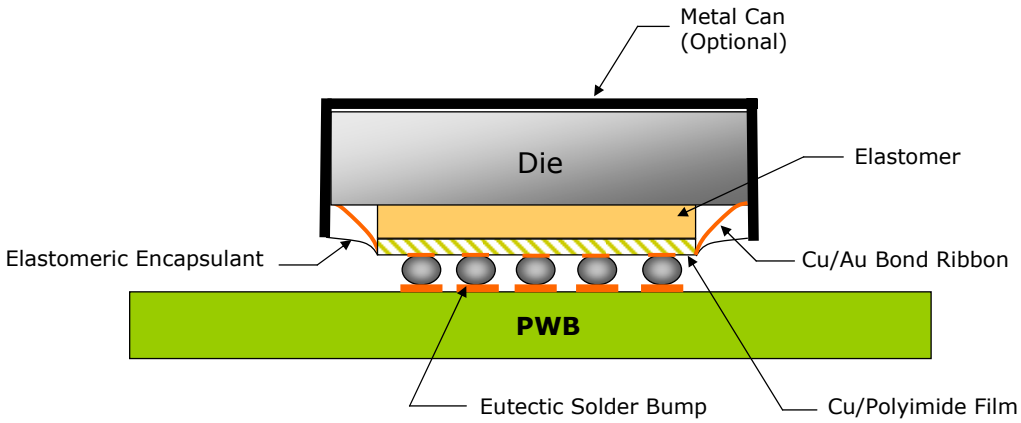
Typical Cross Section of a μBGA™



Source: Tessera

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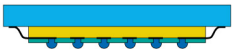
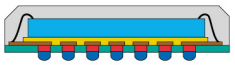
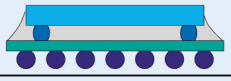
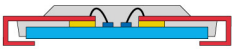
CSPs Worldwide

Category	Type	Example	Devices / Applications
Flex Interposer	TAB/flip chip		Devices: Flash, SRAM, ASIC, Microcontroller, DSP Applications: Camcorder, cell phone, memory card, computer
	Wire bonding		
Rigid Substrate	Flip chip		Devices: Processor, Controller, DSP, SRAM, ASIC Applications: Cell phone, camcorder, PDA
	Wire bonding		
Lead Frame	Wire bonding		Devices: Flash, DRAM, analog IC Applications: Cell phone, memory card, notebook
Wafer-Level Assembly	Redistribution		Devices: Memory, controllers, ASICs, sensors, op-amp, power devices Applications: Computers, communications
	Substrate		

csp dev/apps.rev3

Source: TechSearch International, Inc.

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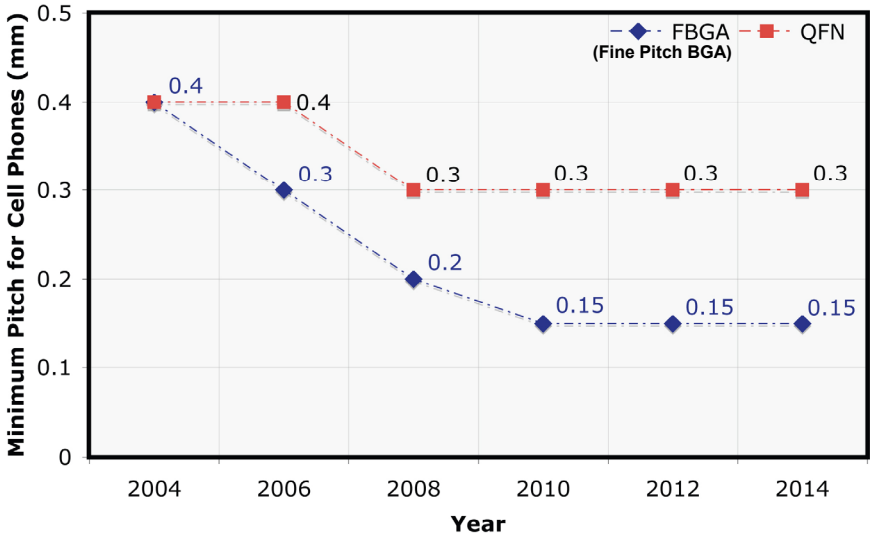
Pitch Trends for Mobile Phone IC Packages

- Jisso Japan Council roadmap shows fine pitch trends for cell phone packages
- Requires fine pitch test sockets



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Green Packaging Adoption Rates

Almost all mobile phones have IC packages with lead free solder balls

Estimated Adoption Rates by Packaging Subcontractors

"Green" Packaging Technology	Estimated Percent of Units Shipped in 2005	Percent of Units Forecasted in 2006
Pb-free	20%–50%	50%–80%
Halogen-free Mold Compound	5%–40%	30%–60%
Halogen-free Laminate Substrates	15%–40%	50%–75%

Source: SEMI and TechSearch International, 2005 Global Semiconductor Packaging Materials Outlook (January 2006)

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Driver for CSP Growth

- Mobile phones as volume driver
  - More than a billion handsets expected to ship in 2007
  - Mobile phones contain an average 15 CSPs, including wafer level packages, stacked die packages, and SiP
  - Mobile phones drive volumes for stacked die packages and system-in-package (SiP)
- Wafer level packaging demand driven by memory, IPDs, analog devices, power devices, and others
  - Applications range from diodes to DRAMs
  - Mobile phones main application
  - Potential for DRAM package in mobile phones

Trends in Mobile Phones: Increased Integration

- New features are being incorporated in the phone
  - WLAN
  - Bluetooth
  - FM Radio
  - MP3 Player
  - Camera
- Driven by market forces
  - Technology convergence
  - New form factors
  - Smaller, thinner, lighter
  - Cheaper
  - Reduced time to market
  - Environmental
- Challenges
  - Cost
  - Density
  - Reliability
  - Technology selection
  - Co-design

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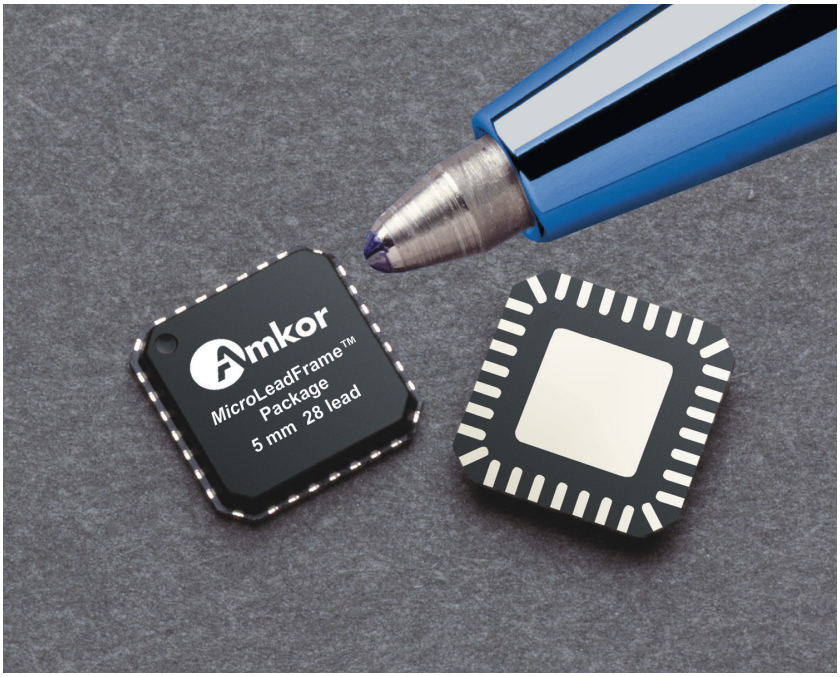
High Volume Production of CSPs

- **Lead frame-based packages:**
  - **Bumped Chip Carrier (BCC™), *Micro*Leadframe MLF®, MLP, QFNs, and Small Outline Non-lead Pkgs. (SONs)**
- **Flex-based packages:**
  - **µBGA® from Tessera's licensees, TI's µStar BGA™ and other wire bond on tape packages**
- **Laminate-based packages:**
  - **ChipArray™(CABGA), Intel's Very Thin Profile Fine Pitch BGA (VFBGA) and Easy BGA, and other wire bond on laminates**
- **Stacked CSPs, Package-on-package (PoP), Package-in-package (PiP)**

Amkor's MicroLead Frame™ Package



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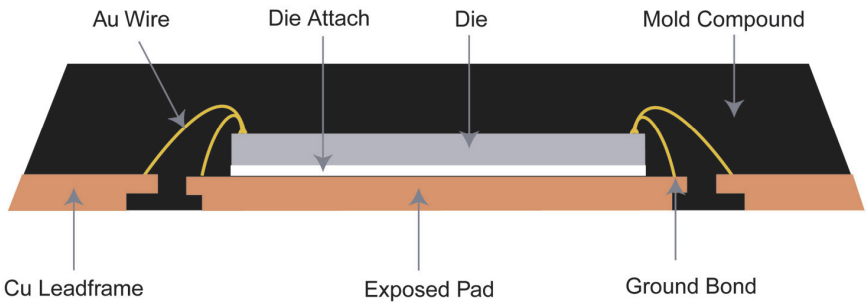
Amkor's MicroLead Frame™ Package Cross-section



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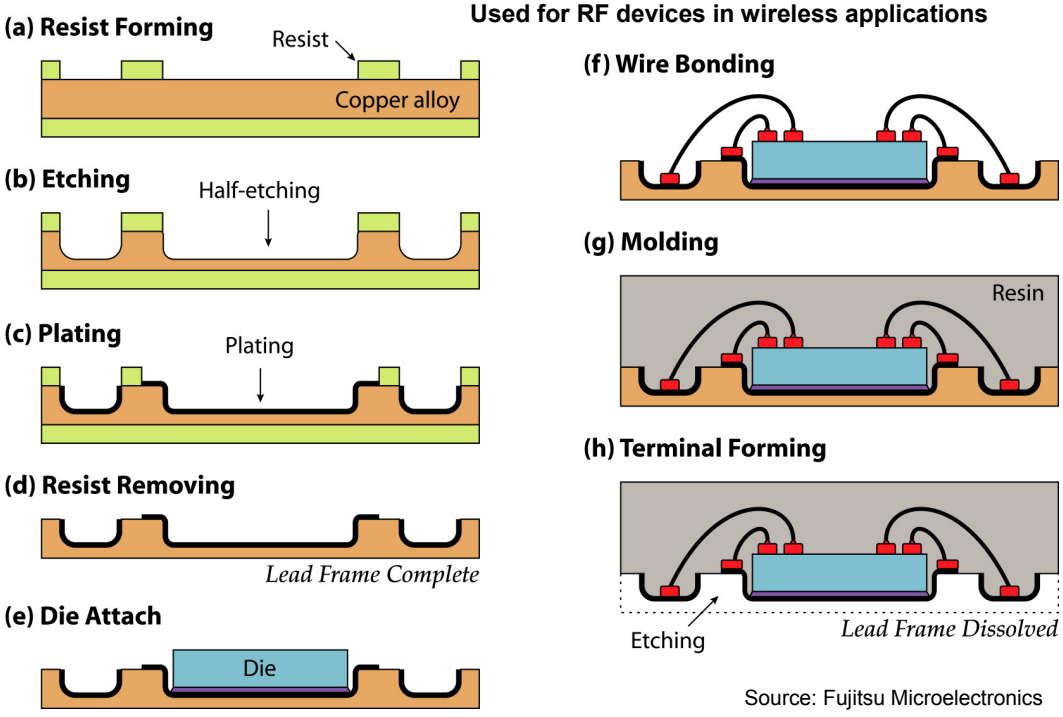
Fujitsu's Bump Chip Carrier (BCC++) Process Flow

Used for RF devices in wireless applications



Source: Fujitsu Microelectronics

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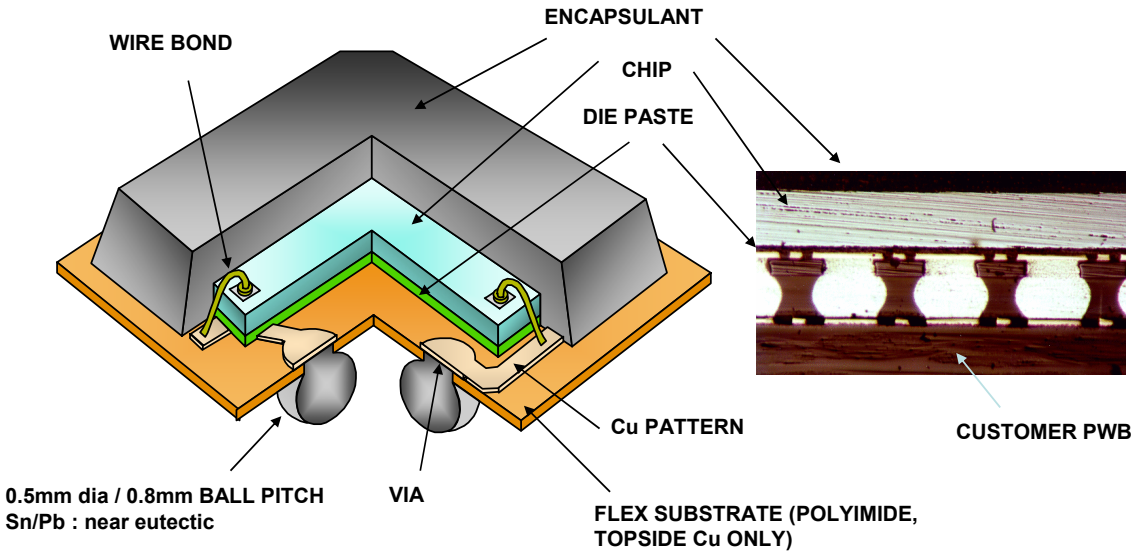
MicroStar BGA™ Package Structure



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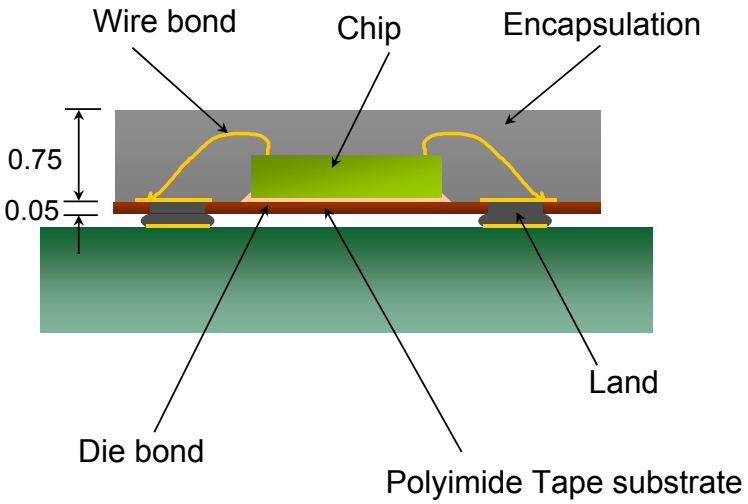
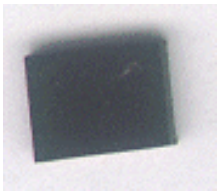
VFLGA package - MicroStar Junior ™





Land Grid Array
0.50mm pitch

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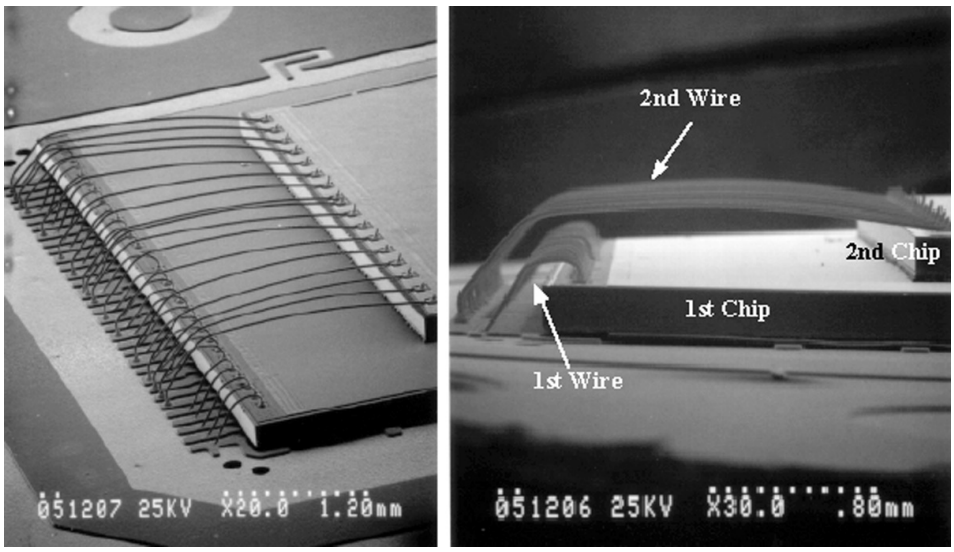
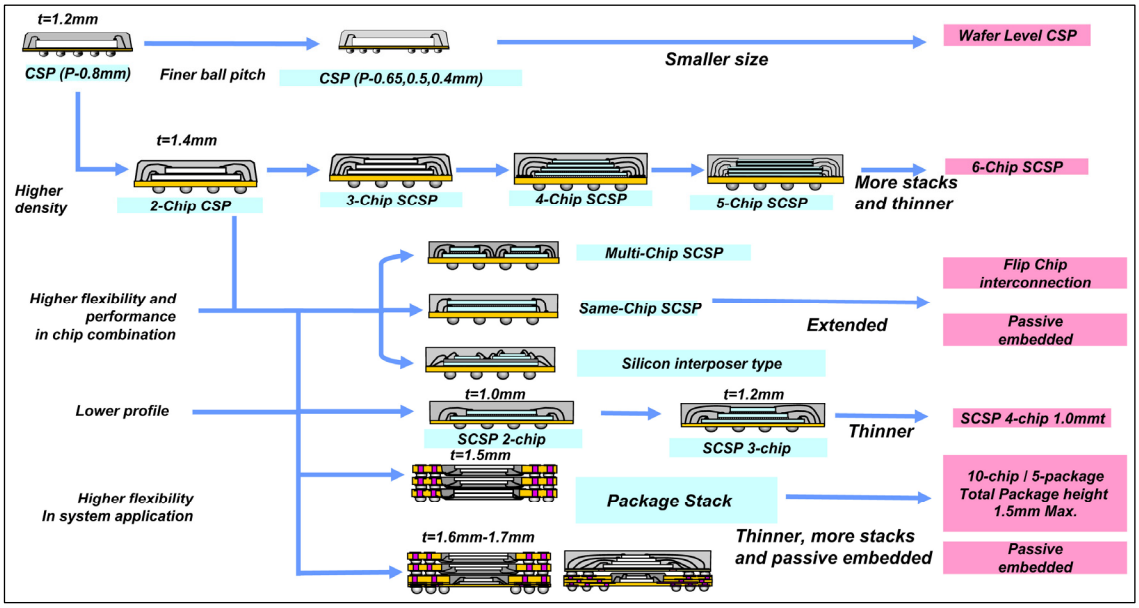
Sharp's Dual Stage Wire Bonding



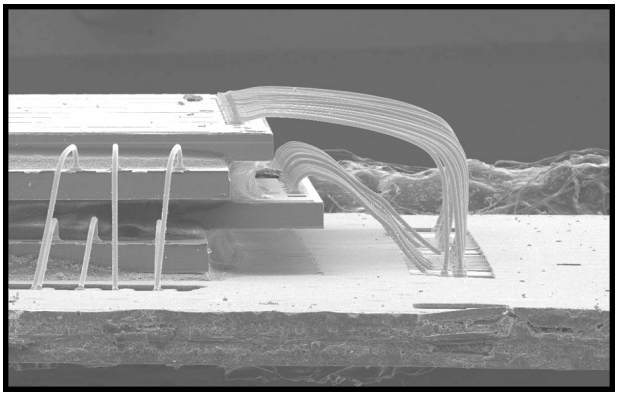
Source: Sharp.

Sharp Development History and Packaging Roadmap



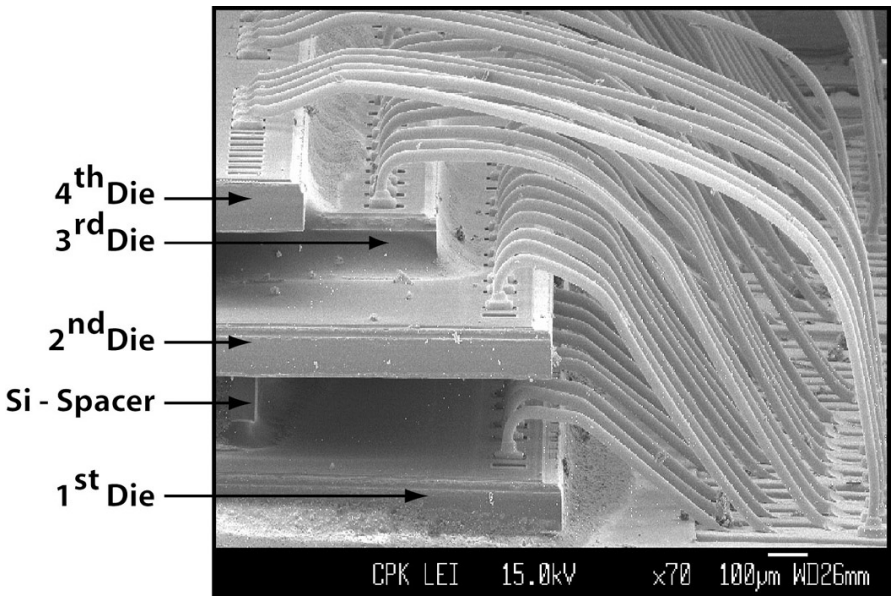
Source: Sharp.

Intel's Four-die Stacked Package



Source: Intel

STATSChipPAC's 4+1 Stacked Die Package



Source: STATSChipPAC

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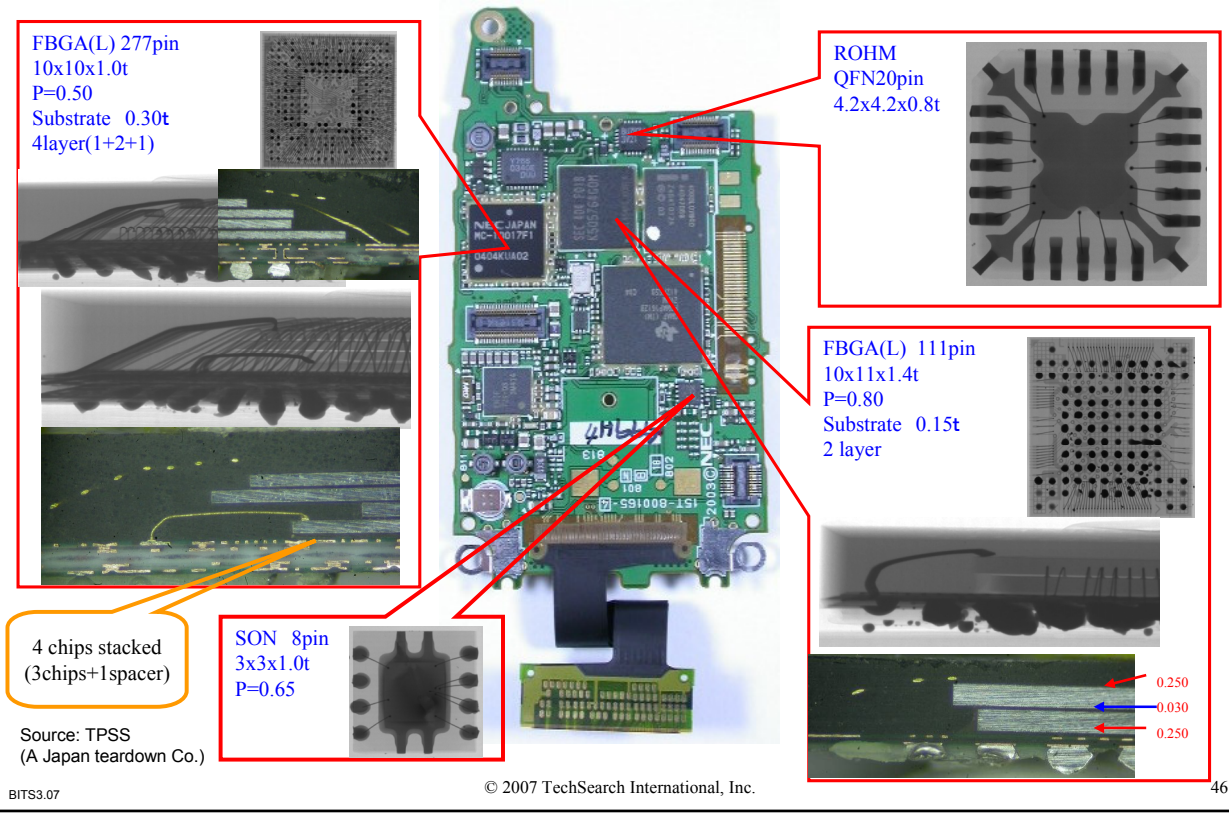
Camera Module & LCD Board

FOMA N900i



Source: TPSS
(A Japan teardown Co.)

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Wafer Thinning Issues for Stacked Die

- Typical wafer thinned by mechanical back grinding
  - Thickness of 75 µm in production today
  - New methods for wafer thinning in development
  - Development work with thickness of 50 to 25 µm
- Flip chip die must be thicker than wire bond die
- Most wafers are 200 mm, some 300 mm in diameter
- New developments in wafer tape
- Challenges in dicing are mechanical, including:
  - Handling
  - Chipping
  - Flaking

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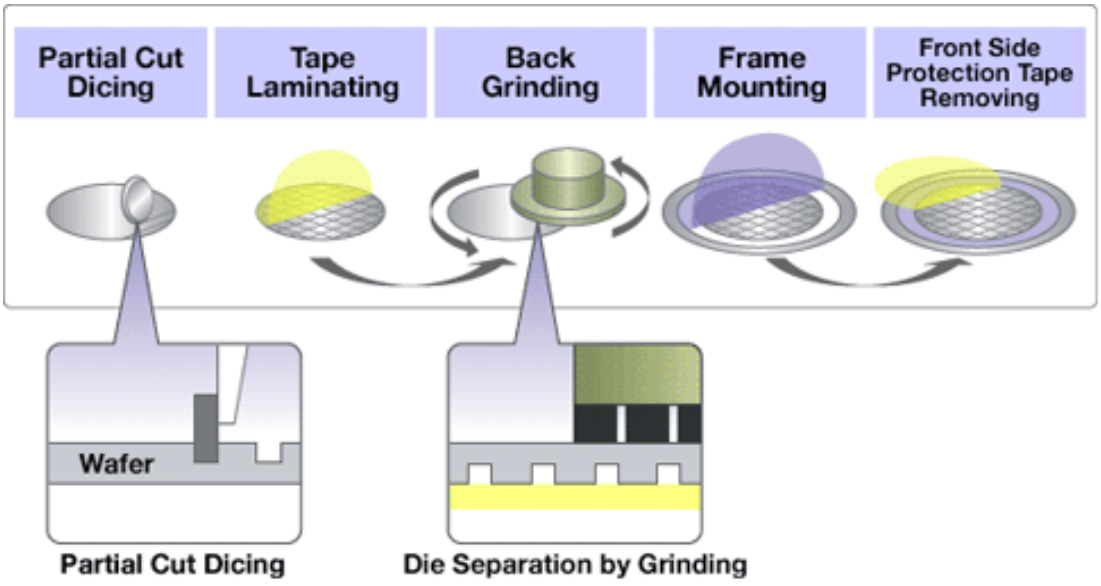
Dicing Before Grinding Process



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New Dicing Technology

- Laser cutting
  - Synova (water jet guided laser)
  - XSiL
  - Disco
  - Shibuya Kogyo
  - ALSI
  - ESI
  - EO Technics
  - NewWave
  - Panasonic
  - Singulase
- Laser scribing followed by dicing blade (for low-K silicon technology)
  - Advanced Dicing Technologies (ADT)
  - Disco
- Laser control break
  - Hamamatsu Photonics
- Plasma
  - Panasonic

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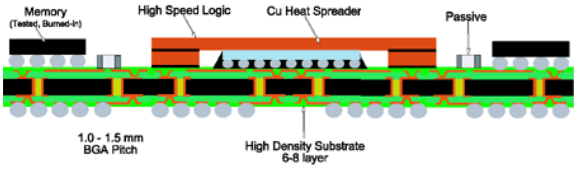
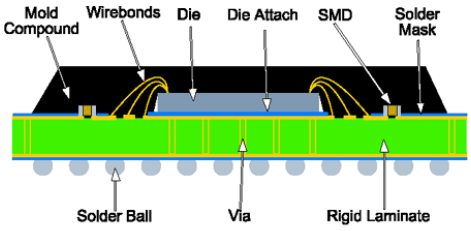
System-in-Package

- SiP is a functional system or subsystem assembled into a single package
  - Contains one or more die
  - More than just memory die, contains logic
  - Typically combined with other components such as passives, filters, antennas, and/or mechanical parts
  - Components are mounted together on a substrate to create a customized, highly integrated product for a specific application
  - Die may be stacked, but stacking is not required





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System-in-Package

- SiPs may utilize a combination of advanced packaging including
  - Bare die (wire bond or flip chip)
  - Wafer level packages
  - Pre-packaged die such as CSP
  - Stacked packages
  - Stacked die
- Drivers for SiP
  - Greater functionality in a smaller area is the driver for consumer and portable products
  - High performance is the main driver for computers, telecommunications, and military/aerospace
  - Some applications such as medical driven by both
  - Applications, such as network systems, driven by the need to decrease motherboard layer counts and complexity
- Examples of SiP
  - Mobile phones
  - Consumer product such as camcorders and cameras
  - Military
  - High performance SiP applications such as computers and network systems

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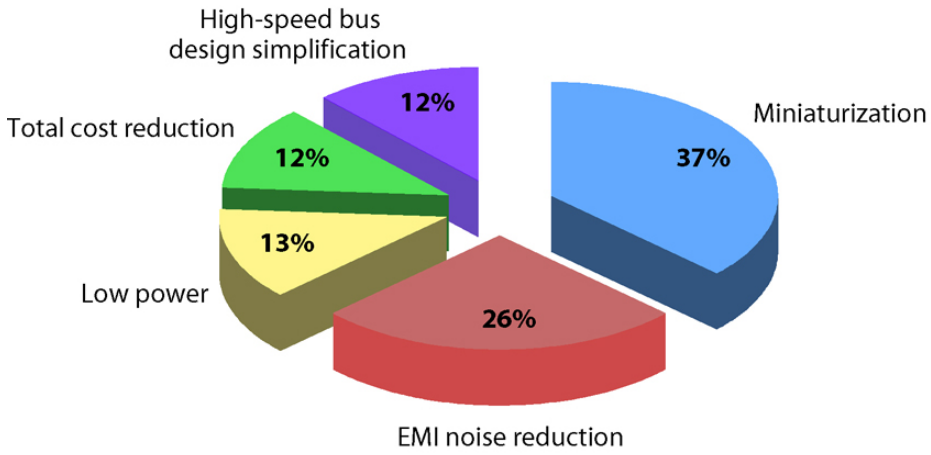
System-in-Package Applications

- Mobile phones
- MP3 players
- Digital still cameras
- Digital camcorders
- Personal digital assistants
- Laptop computers
- Mid-range consumer products
- Automotive electronics
- Medical electronics
- Industrial applications
- Defense electronics

Why SiPs?

According to Renesas (A Mitsubishi/Hitachi Co.) Customer Survey



Source: Renesas Technology

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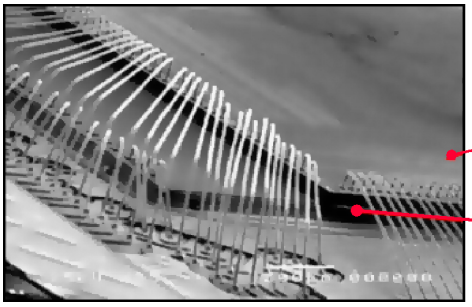
TI's SiP



- TI's processor and SDRAM stacked in package
- TI's digital baseband and SRAM stacked die package found in Nokia's 6225 CDMA phone
- Package also found in Nokia's N-Gage GSM platform

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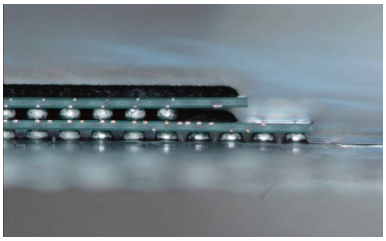
Package-on-Package (PoP)

- Individual packages are stacked on top of each other
  - Separate package for logic
  - Separate package for memory
- At least 10 major OEMs in handset and digital still camera market adopting PoP
- Infrastructure developments were required
  - Standardization of pin-out footprints for the top stacked package
  - Required development of package stacking equipment (now 5 equipment suppliers offer PoP mounter)
  - IC package subcontractor (some early examples)
  - Board level assembly service provider does stacking of packages (most cases) and 5 major EMS providers in production or development



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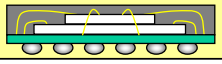
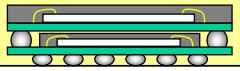
Stacked Die vs. PoP – Trade-offs

Stacked Die 	PoP 
Prospects • IDM (Independent Device Mfg.) ownership • Smaller body size and lower package profile	***Prospects*** • OEM (Original Equipment Mfg.) ownership • Flexible memory sources, facilitate memory capacity increases • Tested at individual package level for Known Good Device
Concerns • KGD required for high product yield • Single-sourced product • New development needed to change a device or handle die shrink • Compound yield and multi test	***Concerns*** • Slightly larger / thicker Package stack • Co-design for bottom and top packages • Infrastructure for package stacking

Source: Amkor

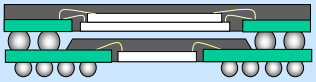
PoP Board Mounting Height

Now

1.6mm (no cavity substrate)

1.4mm (cavity substrate for either package)

1.2mm (cavity substrate for both packages)



Thinner substrate
Thinner molding
Lower ball height

Source: Amkor

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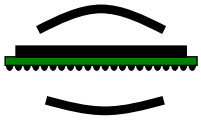
PoP Warpage Control

- Varied by material set and size, thickness
- Need to see the warpage of both top and bottom package
- Warpage at reflow temperature is more important

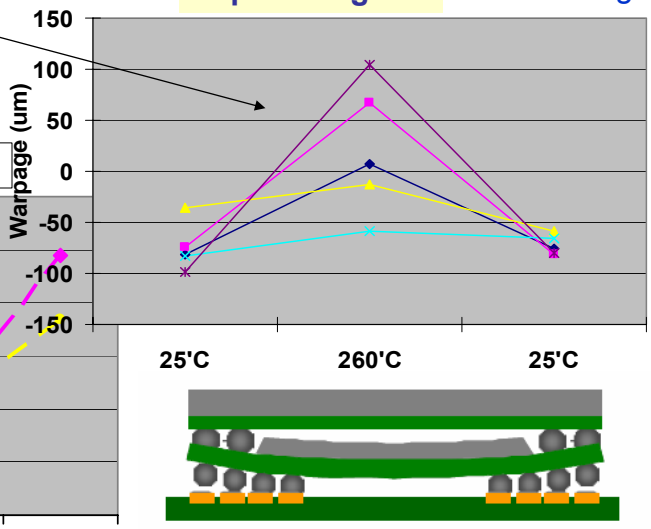
+: Crying



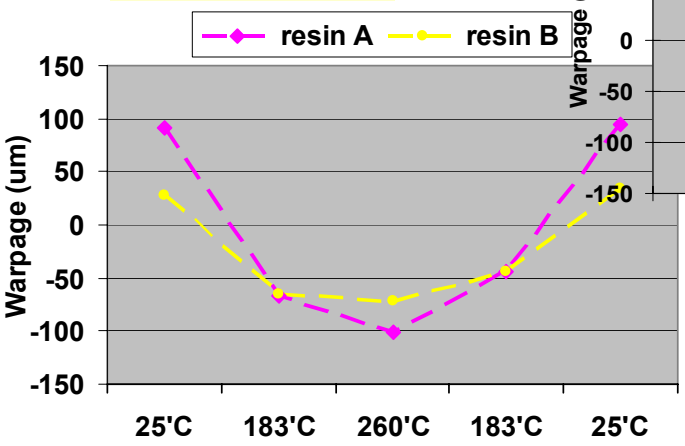
-: Smiling

Mold compound and die attach material differences

Top Package

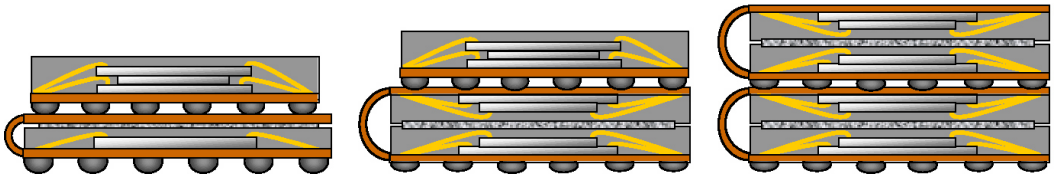


Bottom Package



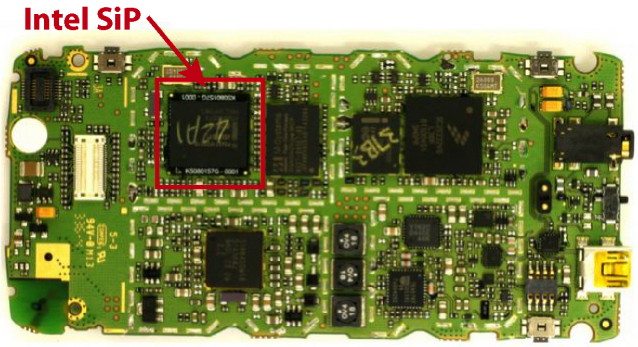
Source: Amkor

Intel's Folded Stacked Configurations



Source: Intel

Intel's SiP in Motorola's E680 Tri-band phone



- Folded flex technology has been adopted in Motorola's E680 Tri-band phone
- Folded flex uses two-metal layer tape

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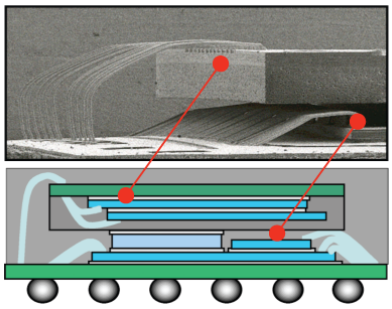
Package-in-Package (PiP)

PiP (before final overmold)



- Two or more packages assembled together and overmolded so end result is a single package that interconnects to the product board
- Also called a stacked module package by Qualcomm
- Typically more expensive than stacked die package, but allows for flexibility in configuration of the memory
- Allows memory to be fully tested before assembly
- Done by IC package subcontractor such as STATSChipPAC or Amkor

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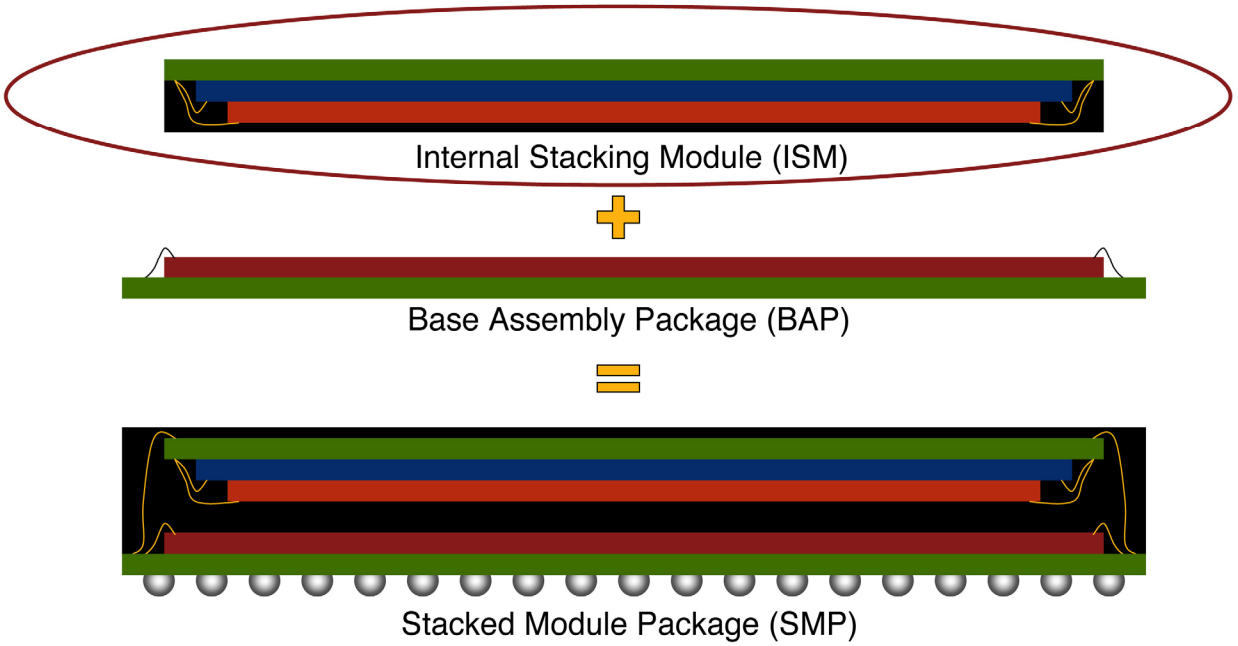
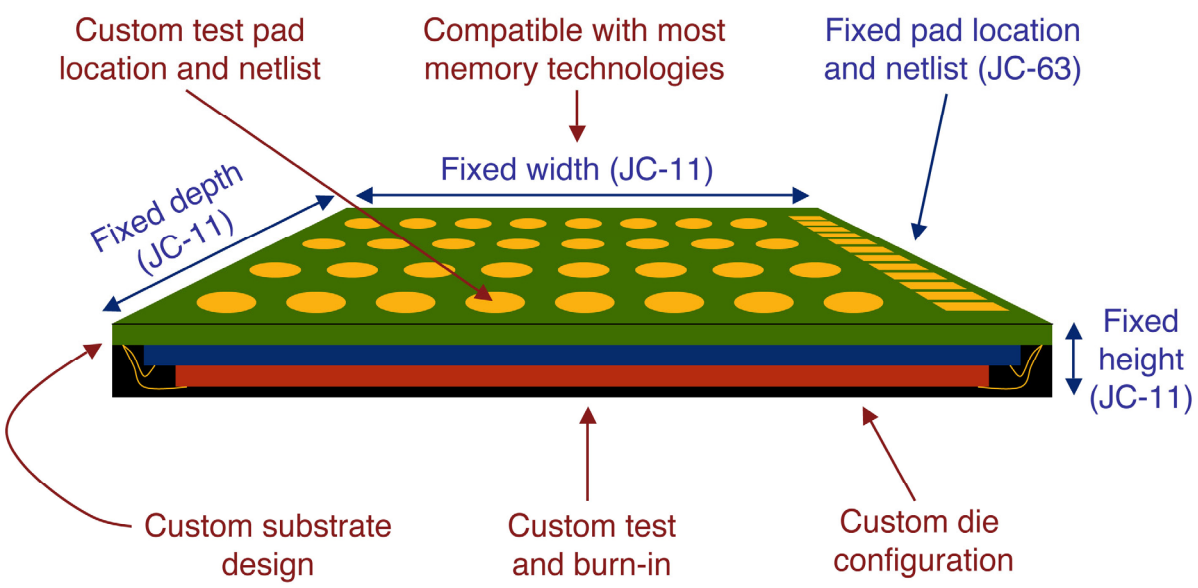
Stacked Module Package (SMP)



Source: Qualcomm.

Internal Stacking Module (ISM)



Source: Qualcomm

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SIP Engine Package Comparison

Key:
Best - ● OK - △
Good - ◎ NG - X

	Stacked CSP	Stacked Module Pkg	Package On Package
Package / System Cost	● X	◎ ◎	△ △
Package Reliability	●	◎	△
Package Mounting Height	●	△	△
Package Availability	●	△	△
Needs Memory Sub-Package	●	X	X
PCB Footprint	●	●	△
Customer SMT Assembly	●	●	◎
Electrical Performance	●	◎	△
Thermal Performance	◎	◎	◎
Requires Memory KGD	△	◎	◎
QCT Development Resources	△	◎	△
Memory Test, Repair & Burn-in	X	●	●
Flexible Memory Configuration	X	●	●
Future Memory Standardization	X	◎	△

Note: QCT = Qualcomm CDMA Technologies, where CDMA = Code Division Multiple Access

Source: Qualcomm

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Medical Applications for SiP

- Applications
  - Pacemakers, defibrillators, and other implantable devices
  - Portable defibrillators
  - Wireless communications inside the implantable (Zarlink has RF transceiver designed to link implantable to base station)
  - X-ray detectors for nuclear medicine and ultrasound equipment (Philips expected to use SiP, thin film with integrated passives)
  - Smart pills (capsule endoscopy)
  - Hearing aids
- MSE System's example
  - MSE test module 11mm x 11mm x 1.5mm with 169 solder balls on a 0.8mm pitch
  - Includes stacked die (ASIC processor/controller and SRAM)
  - Substrate is a BT-resin, 4-layer
- Zarlink Semiconductor's example
  - Based on technology developed from Telecom SiP
  - Mixed IC technology (SiGe, CMOS)
  - Provides better performance (shorter interconnect lengths)
  - Small size 1-inch x 1-inch SMT package

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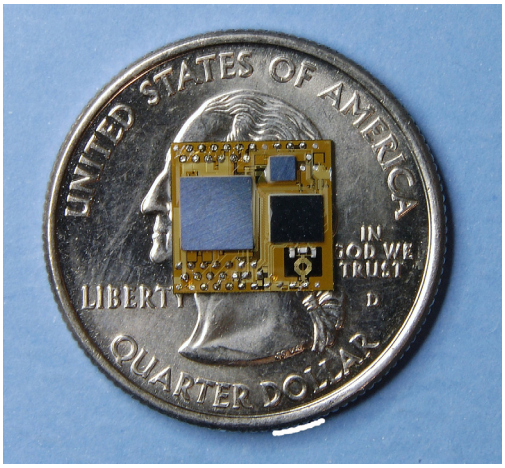
SyChip's SiP CSM

- SyChip's Module is A WLAN IEEE 802.11g Embedded Module
- True Plug-and-Play
  - Incorporates WiFi, VoIP, Bluetooth
  - All software included so user does not need RF design capability
- Thin-Film-on-Silicon Targeted for Mobile Phones
  - Small footprint 11 x 9 x 0.9 mm
  - Includes all components and software
  - Flip chip devices mounted on substrate with integrated passives
  - Packaged in a chip scale module



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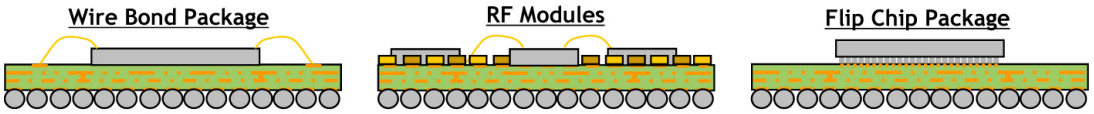
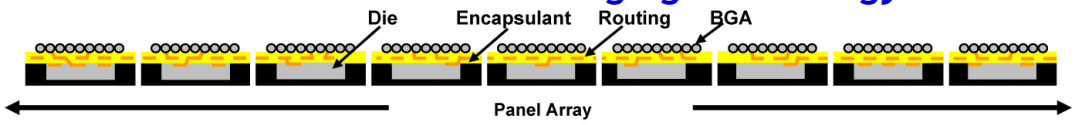
Freescale's New RCP SiP Technology

Existing Packaging Technology



Freescale's *RCP Packaging Technology*

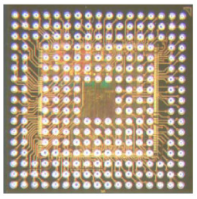


RCP Benefits:

- Freescale low-cost, batch process package invention
  - Ultra Low k Compatible
  - Pb-free
  - Cost effective packaging solution
    - > No package substrate
    - > No wirebond / bumps
  - 3 patents granted, 10 filed
  - Good Thermal Management
  - Single or Multi Chip or component
- Technology not available outside Freescale

Freescale Produced *RCP*

(BGA Bottom View)



9 x 9-mm
280-I/O

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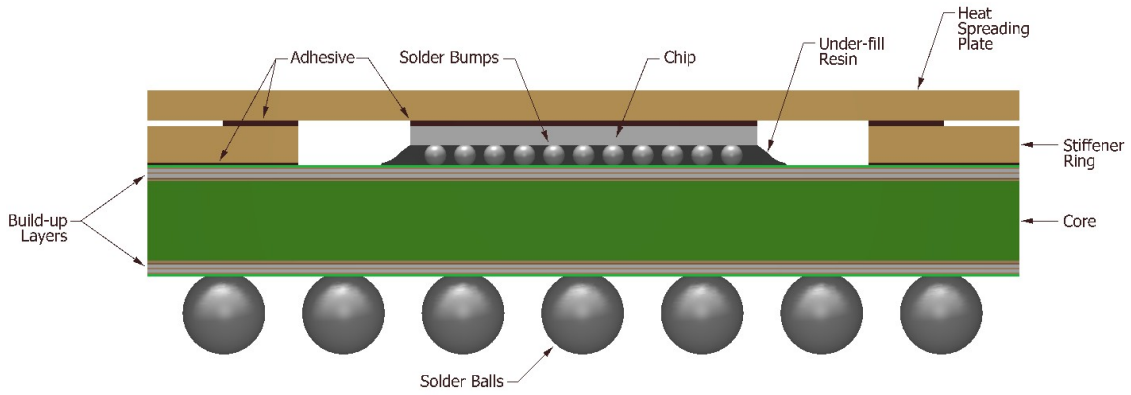
Flip Chip Packaging Trends

Typical Ring & Plate FCBGA Cross Section



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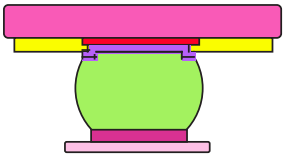
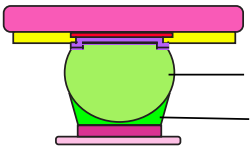
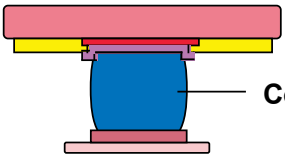
Flip Chip Bump Family



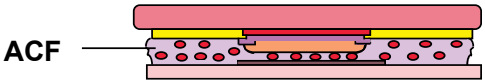
C4 (high T), eutectic (low T)



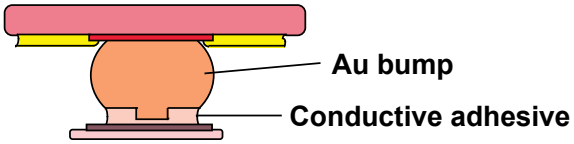
High T Solder to Laminate



Polymer Flip Chip



Au Bump with ACF



Au Bump with ICA

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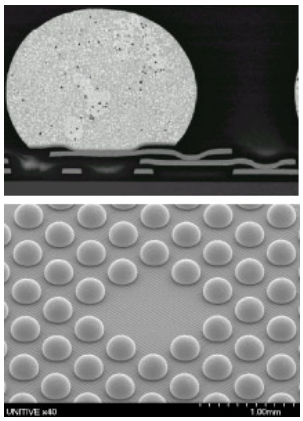
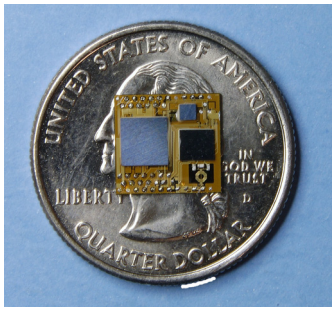
Solder Bump Flip Chip

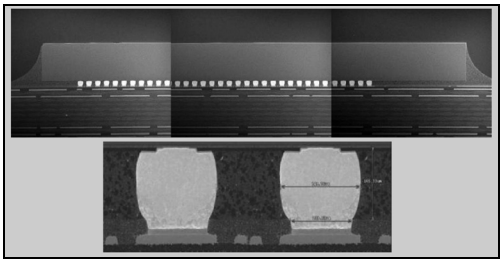
- Die size — up to 24 mm
- I/O count — 1,000s
- Minimum I/O pitch — 150 microns
- Bump diameter — <150 microns typical
- Bump height — 100 microns typical
- Package height — 0.4 to 0.75 mm



Source: Amkor



Source: SyChip



Source: ASE

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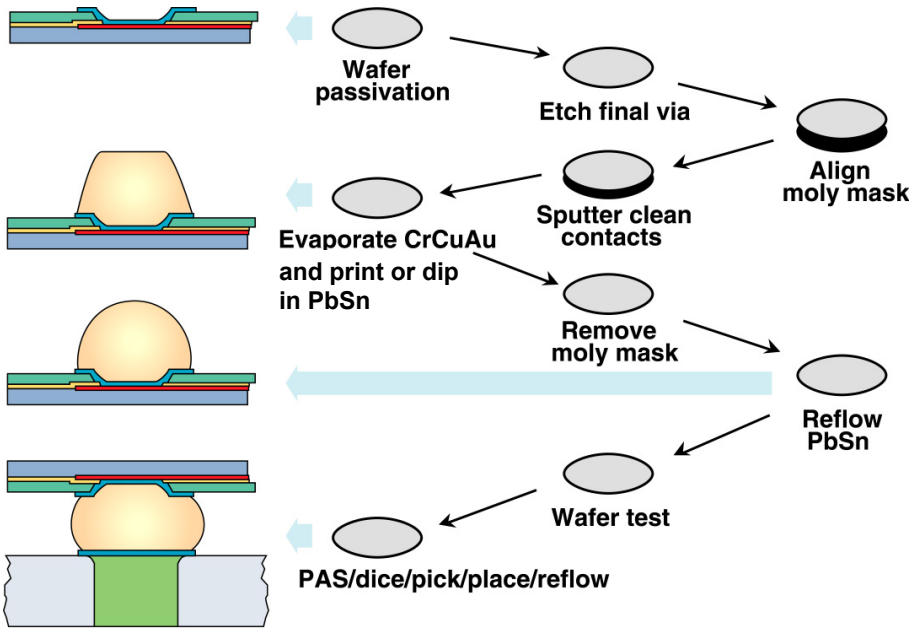
IBM's C4 (Controlled Collapse Chip Connection) Evaporation Process



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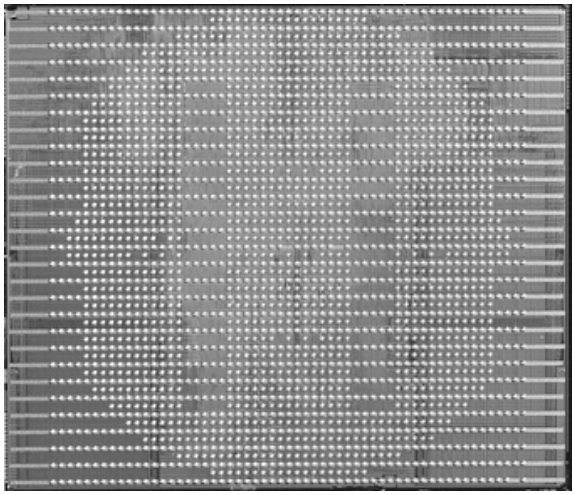
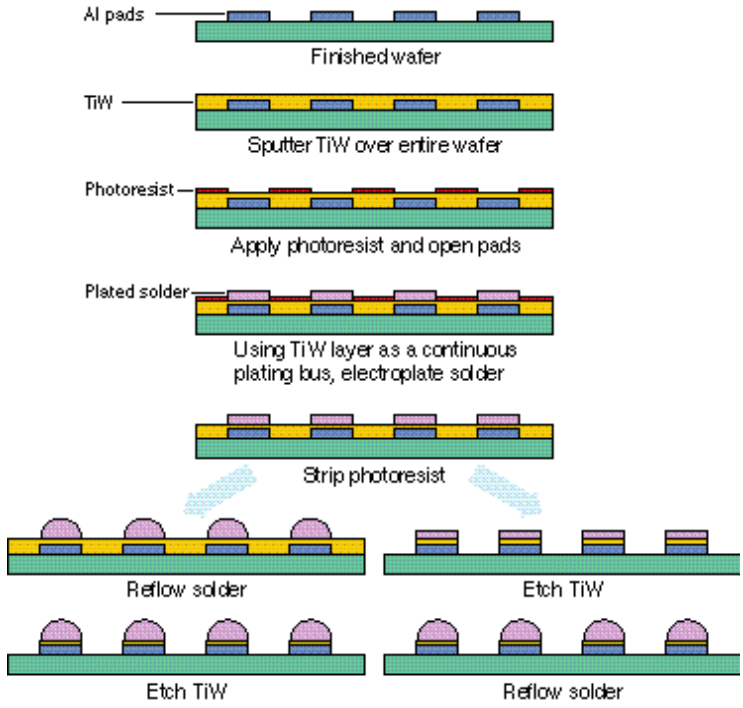
IBM BiCMOS Chip with 2,648 C4 Bumps



Source: IBM.

Electroplated Solder Bump Process



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Bumping Trends: Back to the Future

- Early IBM bump was copper ball
- Early bumps were copper posts with solder
  - Citizen Watch
  - Automotive electronics
- Widespread adoption of the high-Pb bump using evaporation process (C4 bump)
  - Licensed and put into production by Motorola, AMD
  - Cross licensing agreement with Intel, but plating process used in production
- Industry moved to electroplated bumps for flip chip
  - Intel
  - TI
  - IBM, Motorola/Freescale Semiconductor, AMD, TSMC
- Some companies use printing, but plating favored for fine pitch
- Copper pillar process being adopted by some companies

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Advanpack Solutions Pte Ltd.

- Copper Pillar bump process
  - Incoming wafer/preclean
  - Sputter Ti, Cu
  - Photoresist (2 passes 35µm each for 70µm thickness)
  - Expose/develop photoresist
  - Plate copper, solder
  - Resist strip to form column
  - Etch and reflow
- Pillar bump
  - Copper post is 100µm pillar (Cu post <65µm ±10 µm, Solder cap 30-35µm ±15 µm)
  - Less than 100µm pitch on pillar tip, eutectic solder or other on top
  - Bump pitch 150 µm, 46µm min. space
  - Promises better coplanarity, higher standoff, consistent flow under die for underfill

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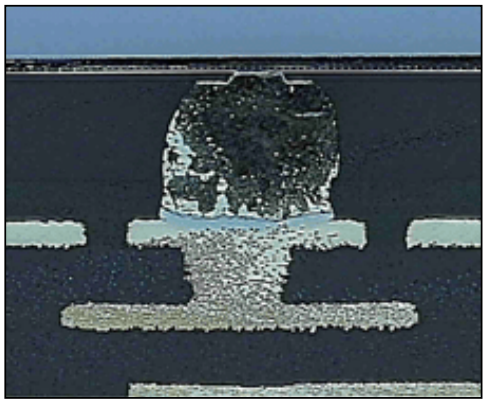
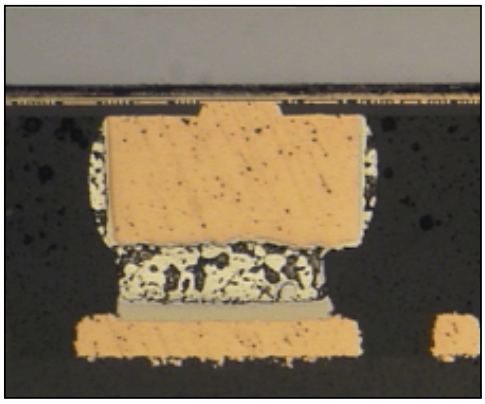
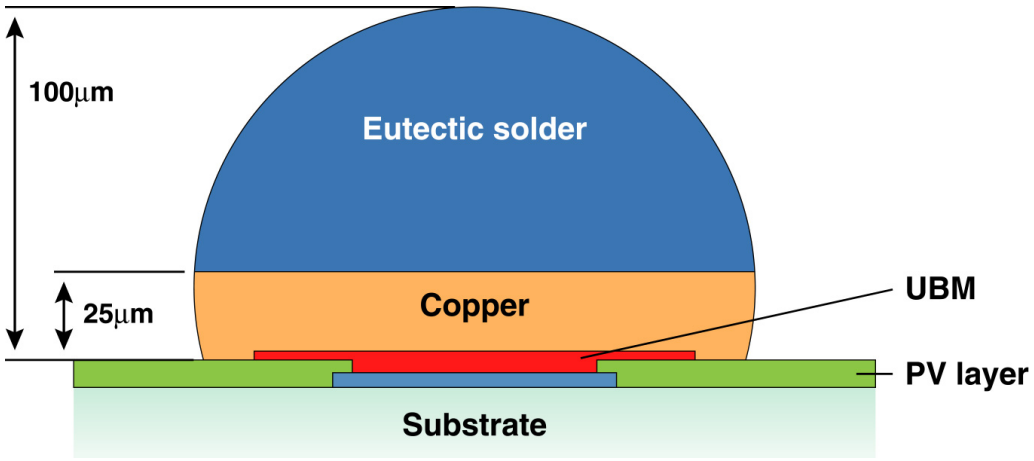
Chipworks Finds Intel's Copper Pillar in Presler Processor
(Internal Code Processor)





Source: Chipworks.

Citizen's Watch Bump Structure



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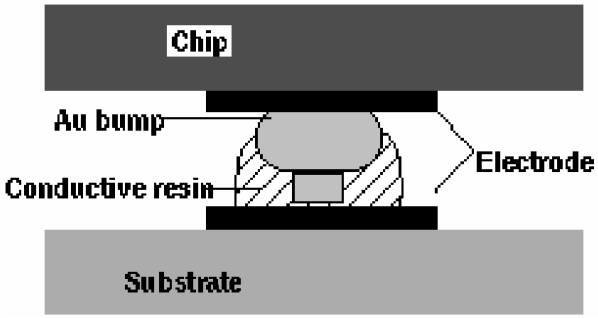
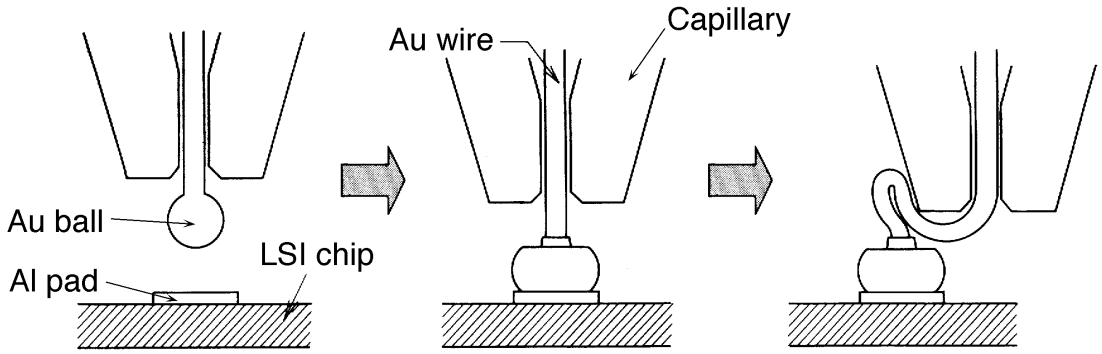
Stud Bump Bonding (SBB)





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Source: Matsushita.

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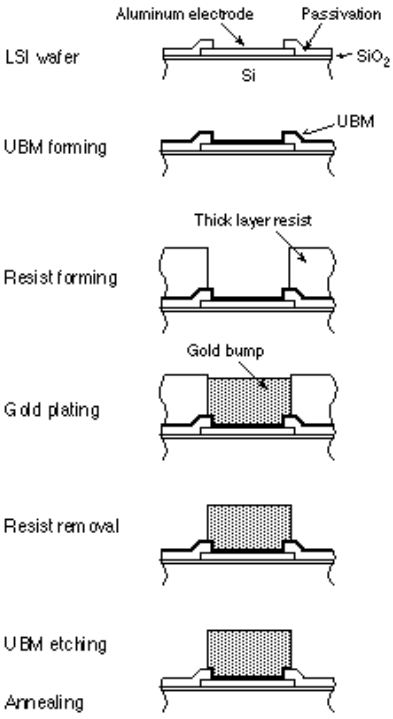
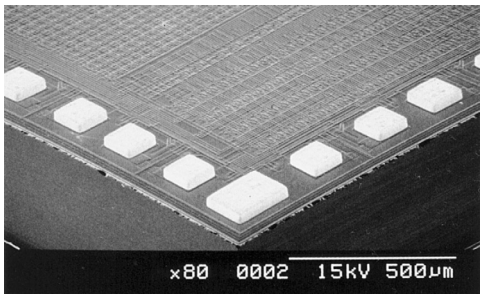
Gold Wafer Bumping (Process)





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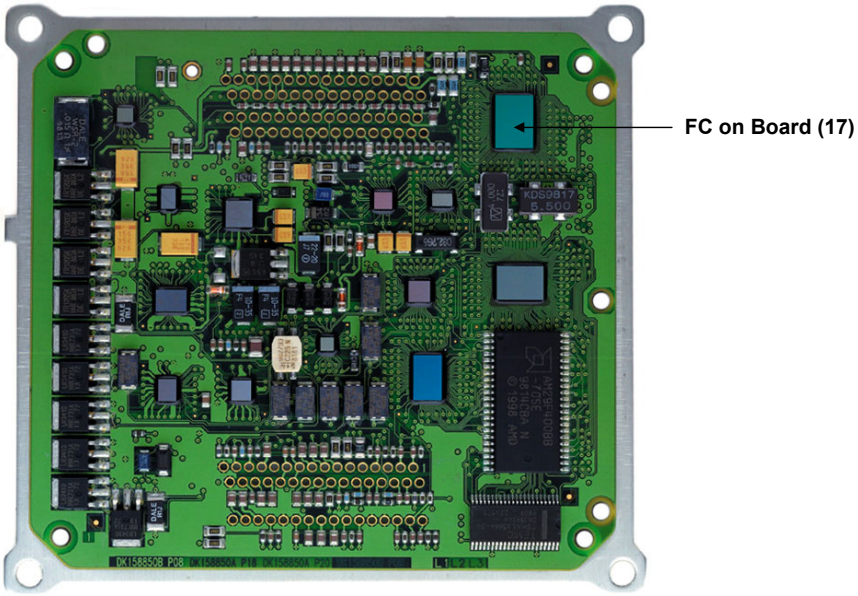
Gold Bumped Devices

- LCD drivers (main application)
  - Chip on glass (COG)
  - Chip on film (COF)
  - Tape automated bonding (TAB)
- Medical devices
- RFID tags

Delphi's on-engine module



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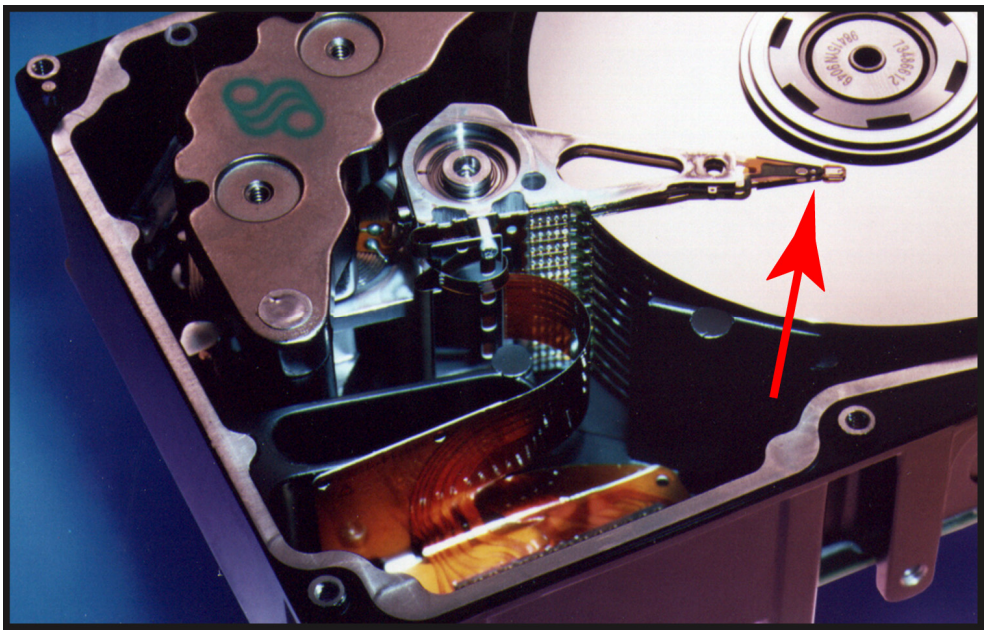
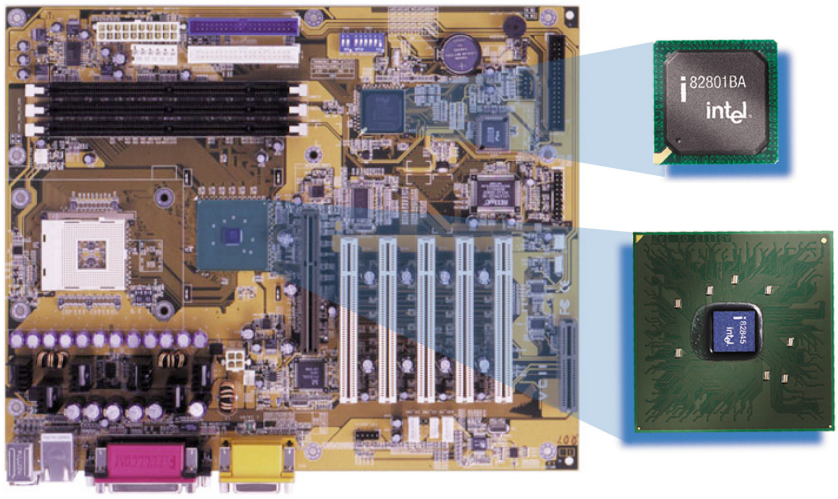
Seagate HDD with Flip Chip



Source: Seagate

Intel's Pentium IV Motherboard w/ PBGA Chipset



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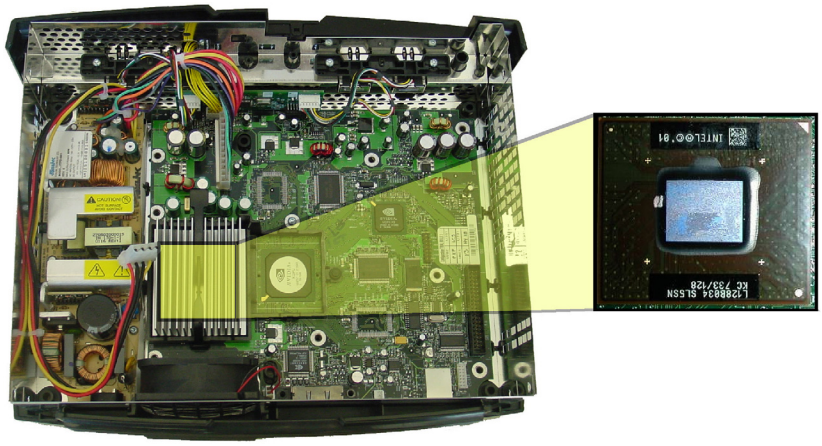
Intel's CPU for XBox Game Machine



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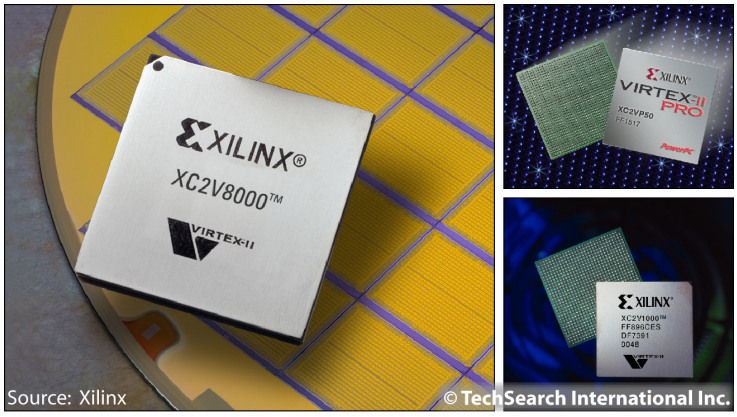
Xilinx VIRTEX-II
Field Programmable Gate Array – FCBGA Pkg.



PMC-Sierra Flip Chip

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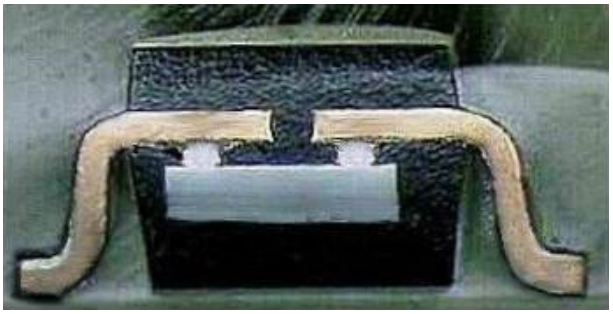
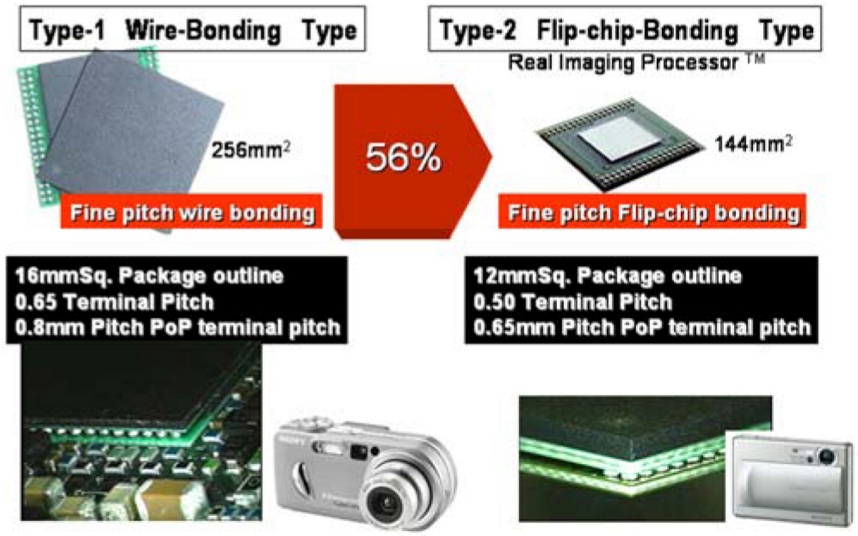
Carsem's FC on Leadframe (FCOL)



Sony's PoP



Source: Sony

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Solder Bump Pitch Trends

- DSP
  - TI was in production with 160µm bump pitch for three years
  - Found not to need tight bump pitch, current designs 180 µm
  - Finer pitch in future
- ASICs
  - Bump pitch of 200-180 µm in production today, moving to 150 µm in the future
- Network server processors
  - Bump pitch of 180 µm moving to 150 µm

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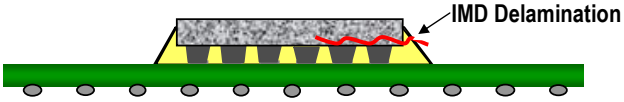
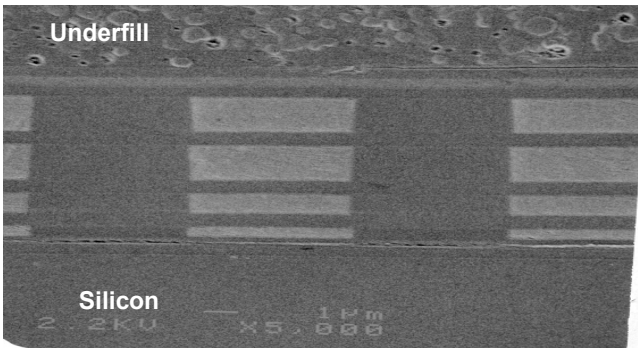
Cu/Low-k Integration Issues

(Replacing the SiO_2 with low-k dielectric and Cu metallization)

- **Industry issues with copper/low-k silicon technology**
  - **Low-k is susceptible to mechanical stress**
  - **CTE mismatch between low- k IMD (Inter-Metal Dielectric) and metal stack**
  - **Industry forgot about the package**
- **New package material sets characterized for low-k silicon assembly**
  - **Mold compounds for QFP and BGA**
  - **New formulations of underfill materials**
  - **Improved substrate designs**





Source: LSI Logic

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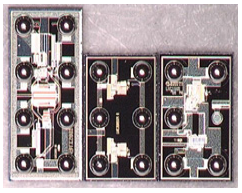
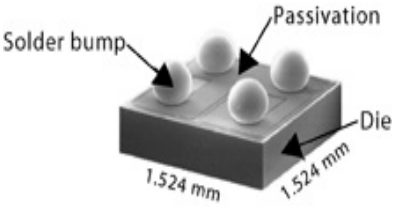
Wafer Level Packaging

Wafer Level Packages

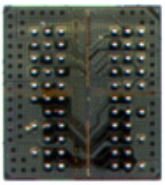
- Die size <5 mm
- I/O count 4 to 100
- Minimum I/O pitch 400 microns
- Bump diameter 250 to 500 microns
- Bump height 180 to 400 microns
- Package height 0.5 to 1.2 mm



Source: Texas Instruments



Source: International Rectifier



60 I/O Wafer Level Fabricated Package (WFP)
Source: Samsung

Wafer Level CSP Categories

Package Construction	Companies
Redistribution/Bump	ASE, Amkor/Unitive, Dallas Semiconductor (Maxim), Hitachi, FlipChip International, National Semiconductor, PacTech, Renesas, Seiko Epson, SPIL, STMicroelectronics, STATSChipPAC
Metal post/bump with epoxy resin	Casio, Fujitsu/Shinko Electric, Oki Electric, Fujikura
Encapsulated bond	FormFactor, Tessera
Encapsulated beam lead	ShellCase (Xintec, Sanyo)

Source: TechSearch International, Inc.

Expansion of Wafer Level Packaging

- Wafer level packaging of all types expanding
  - Form factor driven
  - Performance driven
- Increased use in portable electronics applications
  - Watch modules
  - Personal digital assistants
  - Mobile phones
  - Consumer products such as digital cameras/camcorders
  - MiniDisk
  - Laptop computers
- New service providers expanding capacity
  - Almost two dozen companies (merchant and captive)
  - Increasing number of devices

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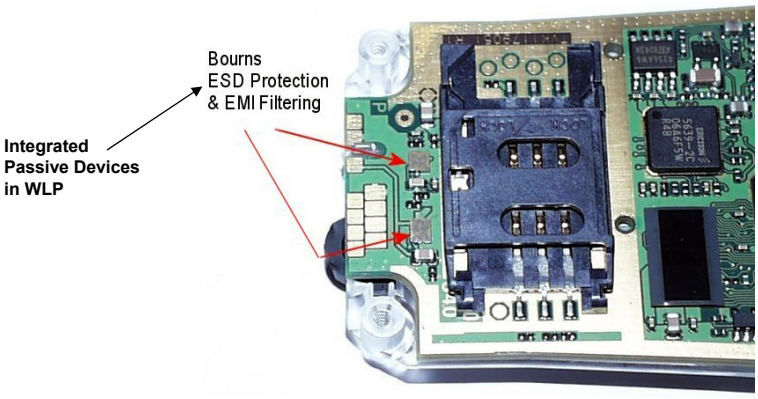
Bourns' Products in Sony Ericsson Phone



Source: Bourns

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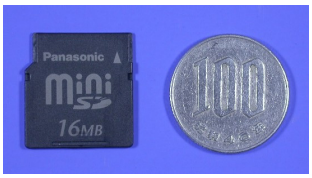
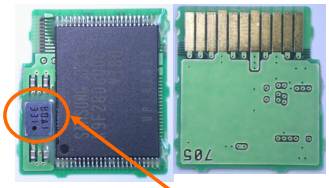
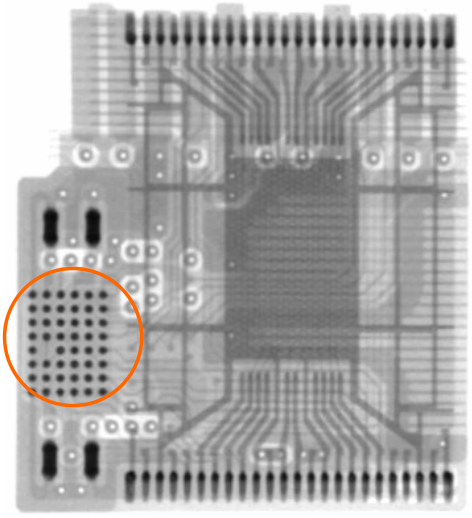
Panasonic's Mini SD Drive

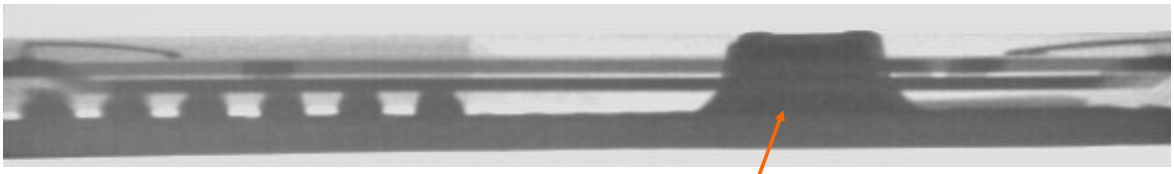




WL-CSP(OKI)
47 pins



Top view



Passive

Side view

Source: TPSS

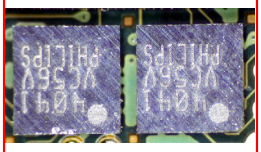
Nokia 702 Main Board

Main Board:56.3 × 104.15 × 0.90mmt

Terminal to Receiver

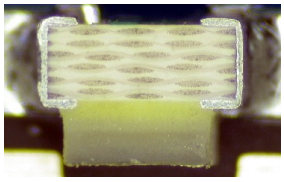
4 Grand Terminal For LCD

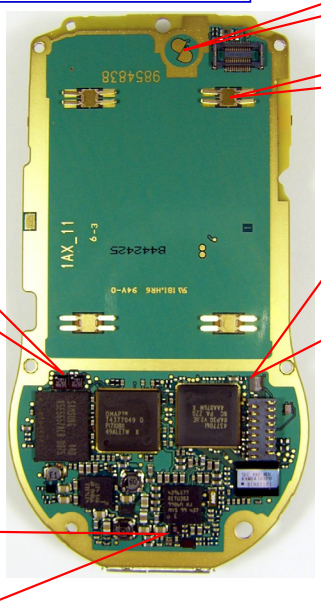
WLP
PHILIPS



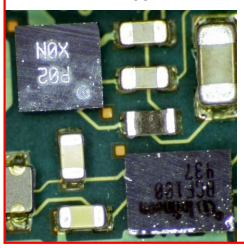
WLP
PHILIPS

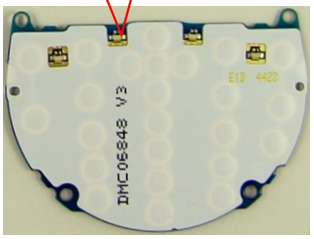
Backlight for Key Board
LED 4pcs





WLP
Infineon





《Key Board》

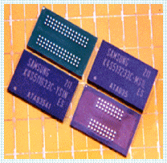
Sub Board:36.8 × 53.3 × 0.70mmt

Source: TPSS

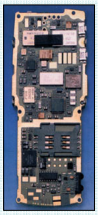
Advantages of WLP

❑ Conventional Packaging

Fab. Process



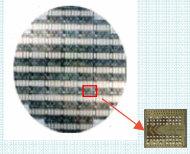
Die Level Packaging



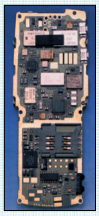
Board Level Packaging

System

❑ WFP



Wafer Level Packaging (Fab. + WFP)



Board Level Packaging

System

Source: Samsung

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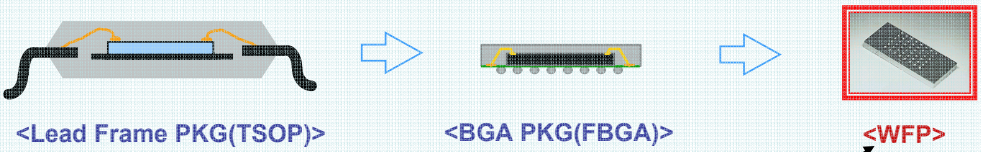
Advantages of WLP

❑ Comparison of Typical Package Type

For the same size die, package size is quite different!!



<Lead Frame PKG(TSOP)> <BGA PKG(FBGA)> <WFP>

Samsung's Wafer Level Fabricated PKG.

❑ Advantages

- ✓ Small form factor : Die size = Package size
- ✓ Improvement of electrical performance :
  - • Shorter RDL length than Au wire
- ✓ Process simplicity/Low cost :
  - • Simple assembly process
  - • Short TAT
  - • No substrate : Wiring/BGA on the die

Source: Samsung

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Disadvantages of WLP

- Disadvantages

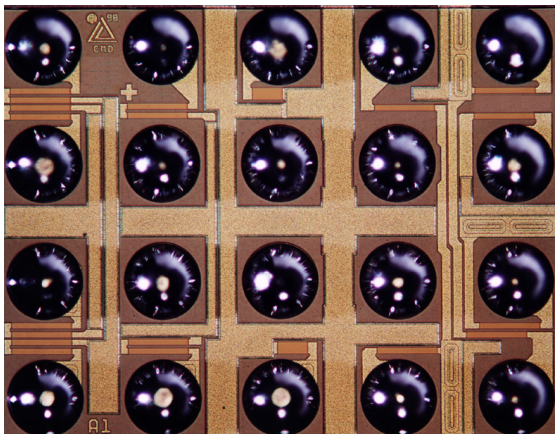
✓ Large Die Difficulties
- Solder Joint Reliability
- Chip Crack during Die Handling
- Difficulties in Component Biz.

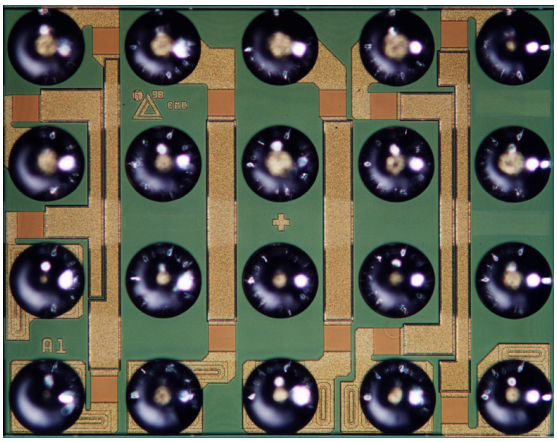
→ The larger the worse.

✓ System Manufacturer (Customer) Friendliness/Preference:
- Customers should be more careful in handling WFP dies.
- Customers may invest new SMT equipments.

Source: Samsung

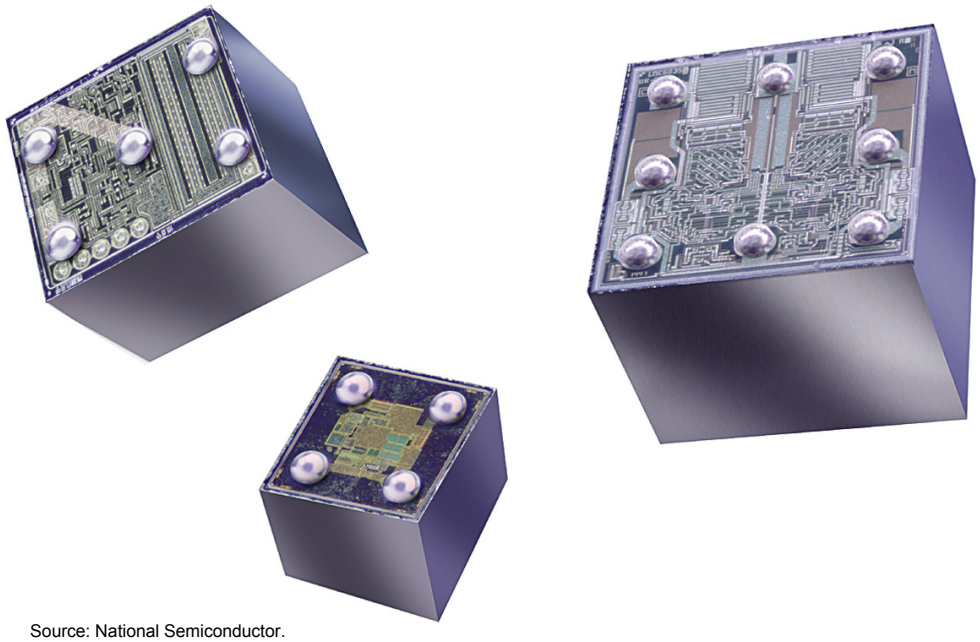
P/Active™ Device Packaged in a CSP
from California Micro Devices (CAMD)





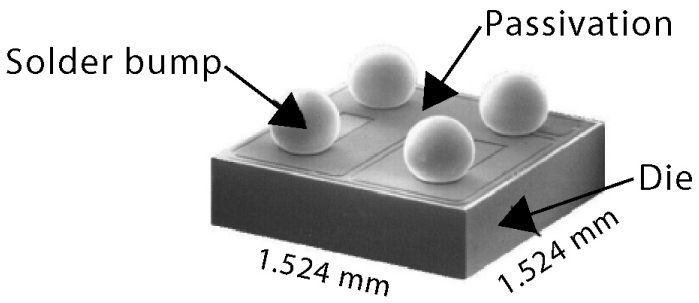
Source: CAMD.

Micro SMD (Surface Mount Device) Wafer Level Chip Scale Packages



Source: National Semiconductor.

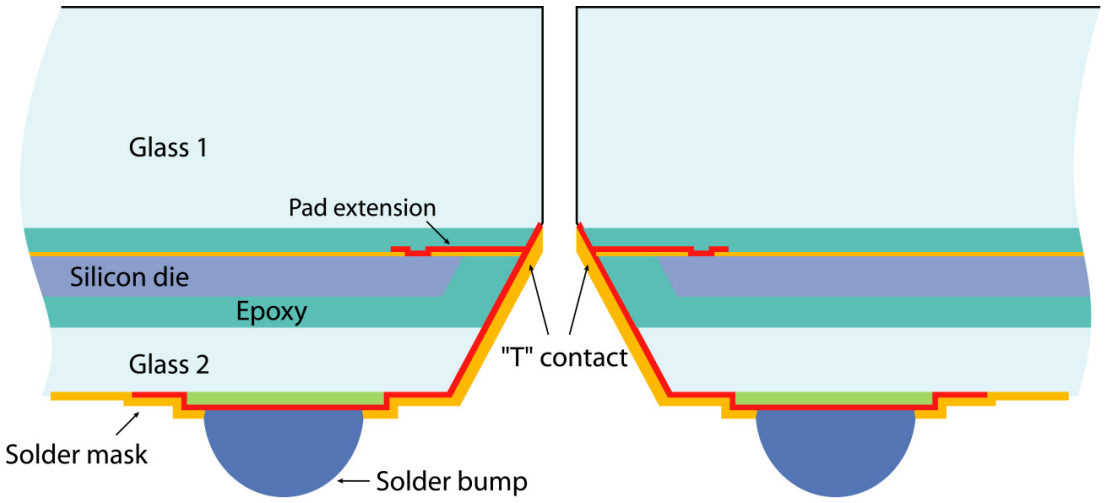
International Rectifier's FlipFET (Power MOSFET) WLP



Source: International Rectifier

Tessera's ShellOP Wafer Level Chip Size Package

(Glass-silicon-glass sandwich structure)



Source: ShellCase.

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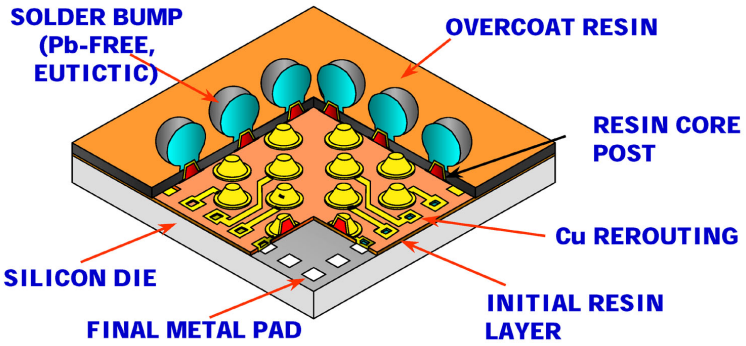
Fujikura's WLP

Resin Core Post Structure



Source: Fujikura

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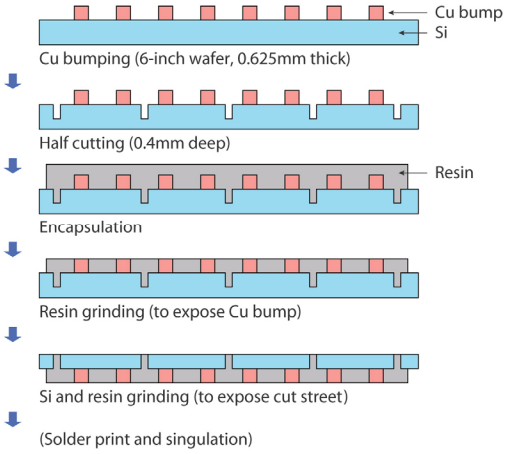
Casio Micronics WLP Process



Source: Casio Micronics

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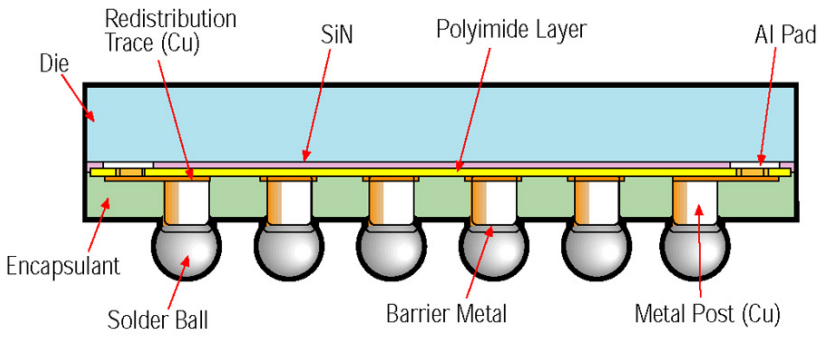
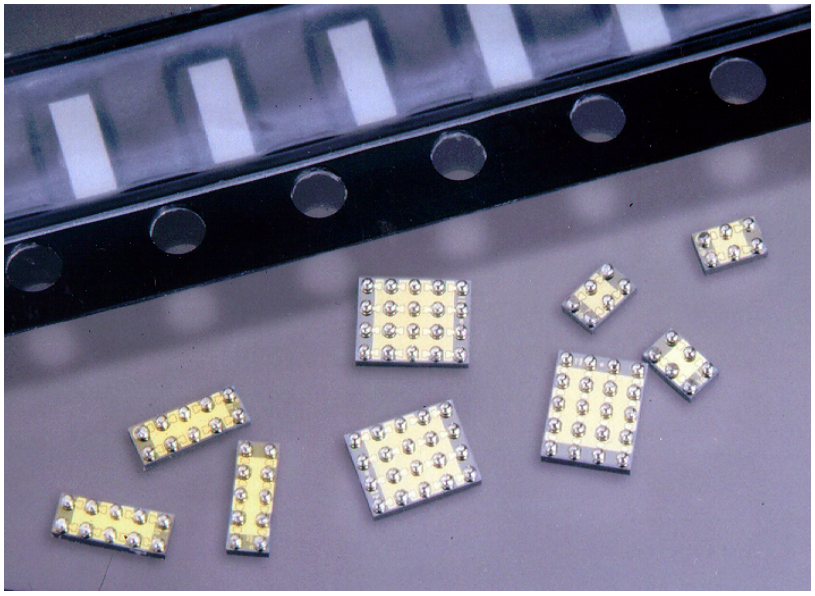
Fujitsu's Super CSP Structure



Source: TechSearch International, Inc.

Littelfuse Diode Arrays for ESD Protection



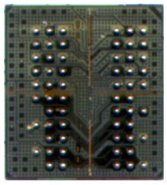
Source: Littelfuse

DRAM Package Trends

- Higher speed DRAM or modules that require higher density are increasingly using FBGA
- Graphics applications (higher speed) use FBGA package
  - Better electrical performance
  - Smaller size package so more memory on the module (number of slots limited, so want more density per module)
- Some DDR2 (Dynamic Data Rate) makers are using wafer level packages
  - Micron shipped a limited number of DDR2 SDRAM in wafer level package (uses bumps instead of wires)
  - Samsung announced DDR2 SDRAM in 60 I/O wafer level package
  - TwinMOS ships Twister module (SO-DIMM) with WLP
- DDR3 expected to use WLP or flip chip on laminate substrate, not wire bond

WLP for DRAM

Future production of DDR3 is expected to use WLP. WLP provides better electrical performance and higher density on the module. Footprint changes with die shrinks and test are concerns.



60 I/O Wafer Level Fabricated Package (WFP)

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TechSearch International, Inc.
(www.techsearchinc.com)

- Founded in 1987 by E. Jan Vardaman and based in Austin, Texas offering consulting services including:
  - Semiconductor packaging and assembly trends
  - Semiconductor packaging materials
  - Market forecasts and technology licensing
- Research topics include flip chip, BGAs, CSPs (inc. stacked die and WLP), SiP, 3D Integration with through silicon vias (TSV)
- Analysts with mixture of materials science, chemistry, assembly and process development, reliability, marketing, economic, strategy, competitive analysis, and modeling backgrounds
- Extensive contacts (>15,000) throughout North America, Europe, Japan, China, Hong Kong, Taiwan, Korea, Singapore, Malaysia, Thailand, and The Philippines

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