PCB ADVANCEMENTS AND OPPORTUNITIES

“Socket Signal Integrity – Impact From IC & Board”
James Zhou, Jiachun (Frank) Zhou
Antares Advanced Test Technologies

“Minimizing Socket & Board Inductance Using a Novel De-Coupling Interposer”
Nicholas Langston, Sr., James Zhou, Hongjun Yao
Antares Advanced Test Technologies

“Benchmarking Printed Circuit Board Fabrication Suppliers Using IPC PCQR^2 Database”
Bill Mack
Texas Instruments Inc.

COPYRIGHT NOTICE

The papers in this publication comprise the proceedings of the 2007 BiTS Workshop. They reflect the authors’ opinions and are reproduced as presented, without change. Their inclusion in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.

There is NO copyright protection claimed by this publication or the authors. However, each presentation is the work of the authors and their respective companies: as such, it is strongly suggested that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.

All photographs in this archive are copyrighted by BiTS Workshop LLC. The BiTS logo and ‘Burn-in & Test Socket Workshop’ are trademarks of BiTS Workshop LLC.
Socket Signal Integrity – Impact from IC & Board

James Zhou, presenter
Jiachun Zhou (Frank)

Antares Advanced Test Technologies

March 11-14, 2007
Hilton Phoenix East, Mesa Arizona

Outline

- Introduction
- QFN package + spring pin socket
- BGA package + spring pin socket
- LGA pad size vs. bandwidth
- Summary
**Introduction**

- Package test system:
  - IC package + Contactor/socket + Load board
- Common practice to simulate SI performance separately
  - attempt to derive the system performance from individual sub-systems of loadboard, socket and package.
- In reality these components have EM coupling between each other. SI performance of each component is affected by other components.
- Analysis on system level coupling effects between components are presented.

---

**Spring pin socket for QFN package**
A Simple QFN Package Model

- Two signal paths formed by:
  - PCB pads
  - QFN pads
  - Bondwires
  - Signal pads on silicon

- Ground loop formed by:
  - PCB ground plane
  - 2x4 via array
  - QFN ground pad
  - Bondwires
  - Ground pads on silicon

QFN Package Performance

Insertion loss (IL): IL = 1dB @4.9GHz
Return loss (RL): RL = 13dB@2.4GHz
Crosstalk (XT): XT = 30dB@1GHz
A High-speed Pin Array

- 3x4 pin array
- 2 signal pins + 10 ground pins
- Multi-conductor transmission line
- Bandwidth determined by characteristic impedance $Z_0$
  - $Z_0$ is function of pitch-to-diameter ratio and dielectric constant
- Pin array parameters:
  - length: 2.5mm
  - diameter: 0.3mm
  - pitch: 0.5mm

Pin Array Performance

- Max insertion loss 0~40GHz is 0.6dB
- 1dB bandwidth is greater than 40GHz
Cascaded Networks

- By cascading the QFN package and pin array networks, the overall system 1dB bandwidth is 5.6GHz.
- It is higher than the bandwidth of QFN package
  - How could the bandwidth increase after inserting a pin array?

Matching Network

- pin array forms matching network
- two additional mismatch factors are introduced at input and output
  - In a near-lossless network, IL is mostly caused by reflection; as a result, reducing RL will yield better IL performance
  - Overall system bandwidth cannot in general be derived from arithmetic of sub-system bandwidth numbers
3D Full-wave EM Analysis

- 3D full-wave EM analysis (HFSS) of entire system
- 1dB bandwidth is 2.3GHz, less than half of QFN package bandwidth of 4.9GHz
- Bandwidth significantly lower than cascading network bandwidth of 5.6GHz.
- What has gone wrong?

A Low-speed Pin Array

- 1dB bandwidth = 7.3GHz, significantly lower than the high speed pin array
  - Pin array parameters: length=2.5mm; diameter=0.4mm; pitch=0.5mm
Cascading S Parameters

• By cascading QFN package and pin array sub-networks, overall system 1dB bandwidth is 4.9GHz
• It’s the same as the bandwidth of the QFN package itself

3D Fullwave EM Analysis

• 3D fullwave EM analysis of low-speed pin array plus the QFN package system
  - 1dB bandwidth = 2.5GHz
  - It is higher than the high-speed pin array bandwidth of 2.3GHz
  - It is about half of the cascading network bandwidth
• How could a low-speed pin array has higher bandwidth than the high-speed pin array? (same QFN package)
**Observations**

- QFN package itself has a 1dB bandwidth of 4.9GHz
- Cascading S-parameter networks: the overall system bandwidth is equal to or higher than the bandwidth of the QFN package
- 3D fullwave EM analysis: the overall system bandwidth is significantly lower than the QFN package
- Low-speed pin has slightly better performance than the high-speed pin in the overall system (WHY?)
- 3D fullwave analysis reveals additional source of insertion loss from radiation
  - Pins surrounded by all ground pins has much less radiation

**Discussion – Cascaded Networks**

- Cascaded network technique is often used in the calculation of overall system performance from individual sub-systems of PCB, socket and package
- In network analysis, the input/output ports are assumed to be terminated by infinitely long transmission lines
Cascaded Networks (cont.)

- When two networks of disparate interface geometries are cascaded, this important termination condition is violated.
- An extra “invisible transitional network” has been created in the system, which characteristics are totally unaccounted for:
  - Higher order modes exist in the vicinity of the transition.

![Diagram showing cascaded networks and invisible transitions.]

Discontinuity and Mismatch

- By separating a system at its discontinuity points, potentially large errors can be introduced due to impedance mismatch and higher order mode.
- Discontinuities cause impedance mismatch; higher order modes EM fields exist in its vicinity.
- When a reference plane is set up at these locations, the field patterns are greatly disturbed by the reference planes and port structure, resulting in potentially large errors.

![Diagram showing discontinuity and mismatch.]

When system boundary is setup at discontinuity transitional locations, large errors can occur.
The Golden Rule

- When using “reference planes” to break a system into sub-systems, the planes must be located at uniform transmission lines with fair distance on both sides of the plane away from any discontinuity.
- The interface between socket and package is NOT in the middle of a uniform transmission line; in fact it is one of the most significant discontinuity points in the system.

![Image of Golden Rule Diagram]

Socket Discontinuities

- Two biggest discontinuities in a socket system:
  - PCB to socket transition
  - Socket to package transition
- Spring pins also have discontinuities:
  - Change of diameter
  - From plunger to shell
  - From shell/plunger to pin tips
- By setting up input/output ports at these discontinuity locations, large errors usually occur.

![Image of Socket Discontinuities Diagram]
Port Setup

• To satisfy the fundamental requirements of port (reference plane) setup:
  - use microstrip or coplanar waveguide (CPW) transmission lines
  - setup the ports at fair distance away from any discontinuities of pad, via, dielectric boundary

Port Setup – long pins

• For longer pins, reference planes can be setup at mid-section of pins
  - Satisfy uniform transmission line requirement
  - Electrical boundaries do not necessarily follow natural mechanical boundaries
  - Think out of the “box” and beyond the normal “boundaries”
Board + Socket + Package

- In order to obtain accurate results on overall system bandwidth, it is highly desirable to analyze the entire system of load board + socket + package.
- The input/output ports can be set up at locations of loadboard/package PCB traces, which are good uniform transmission lines.
- This approach will guarantee the proper set up of the problem.

Spring pin socket for BGA package
BGA Package Model

- 1dB bandwidth = 3.7GHz
- Usable frequency up to 10GHz

BGA Package + High-speed Pins

- Using 40GHz high-speed pins with BGA package:
  - 1dB bandwidth = 1.7GHz
  - Less than half of BGA package bandwidth
**BGA Package + Low-speed Pins**

- Using 7GHz low-speed pins with package:
  - 1dB bandwidth = 1.8GHz
  - Less than half of BGA package bandwidth
  - Higher than high-speed pin bandwidth

**Discussions**

- Overall system performance of low-speed pins is better than high-speed pins
- BGA package bandwidth of 3.7GHz is reduced to 1.7GHz after inserting a 40GHz pin array; it is reduced to 1.8GHz after inserting a 7.3GHz pin array
- **Why does the 7GHz low-speed pin array result in better performance than the 40GHz high-speed pin array?**
Discussions

- Bandwidth of “package+socket” system is not directly related to the individual subsystem bandwidth
- 3D EM effects must be simulated in one system
- Discontinuities between socket and package can only be accurately modeled in 3D full-wave analysis
- Radiation effects
- Changing pitch will completely change socket characteristic

LGA Pad Size vs. Bandwidth
LGA Pad sizes vs. IL

- Pin array: 2 signals, 10 grounds
- Pad size sweep values: 0.3/0.5/0.7/0.9mm
- 1dB bandwidth: 4.35/4.25/3.85/3.35 GHz

Discussion

- Very large pads are often used in LGA package for mechanical alignment tolerances
- These large pads have adverse effects on system bandwidth
- Large discontinuities and impedance mismatch exist at socket-to-package transition
- Degradation of IL cannot be easily overcome by spring pin design
Summary

- The discontinuities at PCB-to-socket and socket-to-package transitions must be evaluated as an integrated part of the system.
- Cascaded network approach may result in large errors if these discontinuities are not modeled properly.
- Socket SI performance is NOT just determined by the socket itself; it is dependent on the package and PCB design.
- To ensure best accuracy, model the PCB+socket+package as an integrated system using 3D full-wave EM tools.

About Authors

James Zhou, Senior Technical Staff
Antares ATT
1150 North Fiesta Blvd., Gilbert, AZ 85233
Ph: (480)682-6200

Jiachun Zhou (Frank), PhD
PD Eng Manager, Antares ATT
1150 North Fiesta Blvd., Gilbert, AZ 85233
Ph: (480)682-6225
Minimizing Socket & Board Inductance using a Novel Decoupling Interposer

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Nick Langston
James Zhou, Hongjun Yao

• It is better to uncover a little than to cover a lot.
  • *Eric Bogatin*, SI Artisan
  » www.bethesignal.com
Performance Limiting Noise

- Power ground voltage droop (Rail Collapse)
- Simultaneous Switching Noise (SSN – Ground Bounce)
- PDS Components
- Board – Socket – DUT package – decoupling components

PDS has to distribute the power to the chip
Has to keep the ripple (noise) to spec ~ 5%
Can not droop all the way to the BW of DUT
**Schematic of PDS with simple lumped models**

- **Via-pogo**
- **Electrolytic Bulk Capacitors**
- **Inter-plane Capacitance**
- **Voltage Regulator Module/Pwr Supplies**
- **On-die Capacitor**
- **Package Caps**
- **High Frequency Ceramic Decoupling Capacitors**
- **Bypass Capacitors**
- **Low Freq Lo Z Mid Frequency Lo Z Hi Frequency Lo Z**

**Are Bypass and Decoupling the same?**

- **Power supply**
- **Cbypass**
- **L dec**
- **Cdec**
- **Load**
Basic PDS Design Strategy

Determine required PDS impedance

\[ Z = \frac{\Delta V}{\Delta I} \]

Determine the frequency for the PDS alone

\[ F_{pds} = \frac{Z}{2\pi L_{pds}} \]

Bypass \( C = \frac{1}{2\pi F_{pds}Z} \)

Determine how much \( L \) we can handle at \( F_{max} \)

\[ L = \frac{Z T_r}{\pi} \]

---

Reviewing SSO/SSN/Ground Bounce

Test Cell Schematic
\[ V_{gb} = n \times L_{net} \quad 3 \text{ nets, } 5nH, 0.5ns \text{ Tr, } 50 \text{ ohms} \]
\[ V_s \quad T_{r} \times Z_0 \quad 60\% \text{ V}_{gb}! \]

**Inductance is like Kryptonite!**

- For Digital Designers of high speed test cells,
- Inductance is the bane of good designs

**Capacitance is like Free Beer!**
Simulation of the impact of Bypassing

• 8 layer FR4 board; 0.635mm dielectric
• 5 .01uF caps on bottom of the board
• 1 power via; .25mm dia.; 0.5mm antipad
• Chip mounted directly to the board
• Chip in a socket mounted to the board
• Chip in a socket with the .01uF caps

Load Configuration

• 10 ohm resistive load to draw 100ma
  • from 1v supply
• 0.1nF on chip bypass on each power pin
• Load is turned on at 5ns,
  • the Tr is 200ps
Spring Pin and Load Model

- Spring Pin is modeled as a CLC pi network
- There is a 10nF bypass in the interposer

Case 1. Chip mounted to the PCB

- Test socket not in power loop
- Voltage drop is 22%
- Ringing period is about 5ns
- No long term ringing on power net
Case II: Using Socket with no bypass

- Test socket in power loop without any bypass capacitor
  - Voltage drop is 31%
  - Ringing period is 7ns
  - No long term ringing

Case III: Contactor with bypass interposer

- Test socket in power loop
  - 10nF interposer in skt
  - Voltage drop is 18%
  - Ringing period is ~7ns
  - Ringing is longer term
**Observations**

- 1nH test contactor increases the power drop from 22% to 31%
- 10nF bypass cap reduces the power drop to 18%
- The built-in bypass cap and the spring pin inductance causes some long term ringing on the power net.

**Interposer Position**

[Diagram showing interposer position with labels for device, socket, contacts, decoupling caps, power, backside caps, and PCB board.]

FIGURE B
### Decoupling Interposer

**Drawing of Interposer**

**Photo of Interposer – 1mm pitch**

---

### Socket without Built-in Decap

**WELLS LOW INDUCTANCE SOCKET**

Data=Address: 1CYC=4hrs; Ref=70VCC=1.50V; "K/K# CLOCK SKEW TEST"

K/K Skew vs VCCCY7C14V18 QDRI-5x36 36M=512x2x36

<table>
<thead>
<tr>
<th>VCC (V)</th>
<th>-0.75</th>
<th>-0.5</th>
<th>-0.25</th>
<th>0</th>
<th>0.25</th>
<th>0.5</th>
<th>0.75ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.100V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>2.075V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>2.050V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>2.025V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>2.000V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.975V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.950V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.925V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.900V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.875V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.850V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.825V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.800V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.775V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.750V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.725V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.700V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.675V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.650V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1.625V</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
</tbody>
</table>

K/K# Skew (ns)

---

**Bits 2007**
Summary

- Inductance is the number one cause of noise and the primary cause of rail collapse.
- A well designed cap network will counteract the Inductance.
- The closer the caps to the noise source; the more effective they are.

- Thanks to Cary Stubbles of Cypress for his support.
Benchmarking Printed Circuit Board Fabrication Suppliers Using IPC’s PCQR² Database

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Bill Mack
Texas Instruments Incorporated

Agenda

• Problem Statement

• What is PCQR²

• Test Panel Design & Attributes

• Supplier Results

• Observations

• Actions Taken & Plans
Problem Statement
A Critical Need for Printed Circuit Boards (PCBs) that are Challenging for Suppliers to Fabricate Resulting In:

Manufacturing Issues, Late Deliveries, and Field Failures

In 2006 it became evident to further evaluate & engage our PCB supplier base:

IPC’s PCQR² Database

What is PCQR²?
PCQR² is an IPC Benchmarking Test Standard & Information Database
IPC-9151

PCQR² stands for: Process Capability, Quality & Relative Reliability

Standardized Test Panels Provide:
• A level field for comparing impartial results
• Statistical and manufacturing significance
• A design for manufacturability basis
• Analysis reports and an information database
Test Panel Design & Attributes

16 Standardized IPC Test Panel Designs Available

The study was conducted primarily for Automated Test Equipment (ATE) platform boards:

- Many Layers, 20+
- Thick – High Aspect Ratios
- Sequential Lamination
- Microvias, 1 & 2 Layers Deep
- Include Back Drill

IPC-24VB-D Test Panel Chosen

IPC-24VB-D 18” x 24” Panel Size
“R” Modules Test Registration
“V” Modules for Via Daisy Chain Testing
Test Panel Design & Attributes

“Cross-section”

- 24 Layers
- 6 Via Types:
  - Through Via
  - 1-Deep Microvia
  - 2-Deep Microvia
  - 10 Layer Blind
  - 4 Layer Buried
  - Back Drill

Test Panel Design & Attributes

Process Capability
- Via Formation
- Via Registration

Quality
- Via Daisy Chain Resistance & Variation

Relative Reliability
- 6 Reflow Passes, Change in Resistance
- Highly Accelerated Thermal Shock (HATS) Cycles to 10% Change in Resistance
- Cycles to Open Circuit
Test Panel Design & Attributes

Example of a partial test panel including trace & space, controlled impedance, & soldermask registration modules

Via Daisy Chain Module

Registration Test Module

Test Panel Design & Attributes

Panel Submission Requirements

15 Total Test Panels Fabricated

3 lots of 5 panels

Approval required for any subcontracted step...

...Including supplier-owned facilities off site

Internally Specified Requirements

0.187” thick

Material Tg minimum 170° C

Surface plating 200 µIN Ni / 50 µIN Au

6 of Our Suppliers Participated in 2006
Supplier Results
Via Formation: Defect Density

Defects Per Million Vias

<table>
<thead>
<tr>
<th>Via Type</th>
<th>Drill Size (mils)</th>
<th>Aspect Ratio</th>
<th>Supplier A</th>
<th>Supplier B</th>
<th>Supplier C</th>
<th>Supplier D</th>
<th>Supplier E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Through</td>
<td>10</td>
<td>18:1</td>
<td>2680</td>
<td>1921</td>
<td>1501</td>
<td>1205</td>
<td>6275</td>
</tr>
<tr>
<td>Through</td>
<td>12</td>
<td>15:1</td>
<td>67</td>
<td>696</td>
<td>205</td>
<td>255</td>
<td>1266</td>
</tr>
<tr>
<td>Through</td>
<td>13.5</td>
<td>13:1</td>
<td>34</td>
<td>136</td>
<td>145</td>
<td>42</td>
<td>439</td>
</tr>
<tr>
<td>Through</td>
<td>14.5</td>
<td>12:1</td>
<td>17</td>
<td>146</td>
<td>102</td>
<td>67</td>
<td>378</td>
</tr>
<tr>
<td>Blind</td>
<td>8</td>
<td>6:1</td>
<td>12</td>
<td>66</td>
<td>37</td>
<td>1201</td>
<td>1154</td>
</tr>
<tr>
<td>Blind</td>
<td>10</td>
<td>5:1</td>
<td>12</td>
<td>20</td>
<td>0</td>
<td>18</td>
<td>1106</td>
</tr>
<tr>
<td>Blind</td>
<td>12</td>
<td>4.5:1</td>
<td>12</td>
<td>33</td>
<td>6</td>
<td>24</td>
<td>867</td>
</tr>
<tr>
<td>Blind</td>
<td>13.5</td>
<td>4:1</td>
<td>6</td>
<td>46</td>
<td>6</td>
<td>12</td>
<td>666</td>
</tr>
<tr>
<td>Buried</td>
<td>6</td>
<td>3:1</td>
<td>1433</td>
<td>138</td>
<td>128</td>
<td>780</td>
<td></td>
</tr>
<tr>
<td>Buried</td>
<td>8</td>
<td>2.5:1</td>
<td>15</td>
<td>171</td>
<td>30</td>
<td>53</td>
<td>3037</td>
</tr>
<tr>
<td>Buried</td>
<td>10</td>
<td>2:1</td>
<td>0</td>
<td>24</td>
<td>45</td>
<td>23</td>
<td>2896</td>
</tr>
<tr>
<td>Buried</td>
<td>12</td>
<td>1.5:1</td>
<td>15</td>
<td>65</td>
<td>113</td>
<td>7</td>
<td>2351</td>
</tr>
<tr>
<td>Back Drill</td>
<td>10</td>
<td>18:1</td>
<td>3181</td>
<td>3946</td>
<td>Not Built</td>
<td>1214</td>
<td>8029</td>
</tr>
<tr>
<td>Back Drill</td>
<td>12</td>
<td>15:1</td>
<td>633</td>
<td>2068</td>
<td>Not Built</td>
<td>256</td>
<td>846</td>
</tr>
<tr>
<td>Back Drill</td>
<td>13.5</td>
<td>13:1</td>
<td>463</td>
<td>1272</td>
<td>Not Built</td>
<td>41</td>
<td>341</td>
</tr>
<tr>
<td>Back Drill</td>
<td>14.5</td>
<td>12:1</td>
<td>594</td>
<td>1150</td>
<td>Not Built</td>
<td>82</td>
<td>386</td>
</tr>
</tbody>
</table>

Poor 10 mil Through and Back Drill Yields

Defects: Through Via Predicted Yields

10 mil Drill
Poor performance by all suppliers
18:1 Aspect Ratio

12 mil Drill
Significantly better, Varied results
15:1 Aspect Ratio

13.5 mil Drill
13:1 Aspect Ratio

Paper #3

March 11 - 14, 2007
Defects: Laser vs. Mech. Drill Microvias

2-Deep Microvias: Defects Per Million Vias

![Bar graph comparing laser and mechanical drill microvias defects per million vias.]

Mechanically Drilled Microvias: Poor Yield

Registration: Inner vs. Outer Panel

![Diagram showing registration tests on outer and inner panels.]

Best Registration Results - Inner Panel

Paper #3
Drill Misregistration & Breakout

Ideal, uniform annular ring size is determined by:
(Copper Pad Diameter – Drill Diameter) ÷ 2

### Registration: Drill to Copper Clearance

**Through Hole Via to Cu Feature Spacing Chart**

0.5 Oz Inner Layer Cu, 12:1 Aspect Ratio, Sequential Lam Build: 10 Layer Outers & 4 Layer Inner

<table>
<thead>
<tr>
<th>Board Layers:</th>
<th>Supplier A</th>
<th>Supplier B</th>
<th>Supplier C</th>
<th>Supplier D</th>
<th>Supplier E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top Lam. L2, 4, 6, 8</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Middle Lam. L11 &amp; 14</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Top to Bot Lams. L10 &amp; 15</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>Bottom Lam. L17, 19, 21, 23</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
</tbody>
</table>

**Drill to Cu Clearance (mils):**

Within 12” Center Panel Area

<table>
<thead>
<tr>
<th>Within 12” Center Panel Area</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>Supplier B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>Supplier C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td>Supplier D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>Supplier E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Outer Corners of 18” x 24” Panel</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>Supplier B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>Supplier C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td>Supplier D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>Supplier E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

**Percent Yield:**

<table>
<thead>
<tr>
<th>100 - 90</th>
<th>99 - 80</th>
<th>98 - 70</th>
<th>97 - 60</th>
<th>96 - 50</th>
<th>95 - 40</th>
<th>&lt;= 90</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>Supplier B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
<tr>
<td>Supplier C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
<td>C</td>
</tr>
<tr>
<td>Supplier D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>Supplier E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
<td>E</td>
</tr>
</tbody>
</table>

Relative Supplier Registration Performance
Quality: Resistance Measurements

Through Hole Via Resistance

Supplier C: Significantly High

Quality: Resistance Variation

Through Hole Via Resistance Variation

Supplier D: Consistently Lowest
Quality: Daisy Chain Resistance Plot

14.5 mil Drill Through Hole Structure

Supplier E: Spike in CoV Value – Panel 12

Reliability: Through Hole Via Reflow

Resistance Change After 6 Reflow Passes @ 245 C Through Hole Via Structures

Supplier C: Decrease in Resistance
Reliability: Through Hole Via HATS

Highly Accelerated Thermal Shock (HATS), -40 to 145 C
Through Hole Via Structures

Supplier C: Survived 500 Thermal Cycles

Reliability: Laser Drilled Microvias

Resistance Change After 6 Reflow Passes, 245 C
Laser Drill Microvia Structures, All Applicable Suppliers

Few Cycles Between 10% Change and Open
Reliability: Blind & Buried Via Reflow

Resistance Change After 6 Reflow Passes, @ 245 C
Blind & Buried Via Structures

<table>
<thead>
<tr>
<th>Drill Diameter (mils) / Aspect Ratio</th>
<th>Average Resistance Change (Ohms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 Layer Blind Via</td>
<td>Supplier A: Consistent Smallest Change</td>
</tr>
<tr>
<td>4 Layer Buried Via</td>
<td>Supplier B: Earliest Thermal Shock Failure</td>
</tr>
</tbody>
</table>

Reliability: Blind Via HATS

Highly Accelerated Thermal Shock (HATS), -40 to 145 C
10 Layer Blind Via Structures

Supplier A: Consistent Smallest Change
Supplier B: Earliest Thermal Shock Failure
**Reliability: Buried Via HATS**

Highly Accelerated Thermal Shock (HATS), -40 to 145°C
4 Layer Buried Via Structures

<table>
<thead>
<tr>
<th>Drill Diameter (mils) / Aspect Ratio</th>
<th>6 / 3:1</th>
<th>8 / 2.5:1</th>
<th>10 / 2:1</th>
<th>12 / 1.5:1</th>
<th>6 / 3:1</th>
<th>8 / 2.5:1</th>
<th>10 / 2:1</th>
<th>12 / 1.5:1</th>
</tr>
</thead>
<tbody>
<tr>
<td>10% Change in Resistance Open Circuit</td>
<td>Supplier A</td>
<td>Supplier B</td>
<td>Supplier C</td>
<td>Supplier D</td>
<td>Supplier A</td>
<td>Supplier B</td>
<td>Supplier C</td>
<td>Supplier D</td>
</tr>
<tr>
<td>Supplier Relative Results Through Hole Structure Dashboard</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Defect Density</td>
<td>Registration</td>
<td>Resistance Values</td>
<td>Resistance Variation</td>
<td>Reflow Reliability</td>
<td>Thermal Shock</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPP A</td>
<td>BEST</td>
<td>BEST</td>
<td>OK</td>
<td>MIDDLE</td>
<td>MIDDLE</td>
<td>MIDDLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPP B</td>
<td>MIDDLE</td>
<td>MIDDLE</td>
<td>OK</td>
<td>MIDDLE</td>
<td>WORST</td>
<td>WORST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPP C</td>
<td>MIDDLE</td>
<td>MIDDLE</td>
<td>HIGH</td>
<td>WORST</td>
<td>BEST</td>
<td>BEST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPP D</td>
<td>BEST</td>
<td>BEST</td>
<td>OK</td>
<td>BEST</td>
<td>WORST</td>
<td>WORST</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPP E</td>
<td>WORST</td>
<td>WORST</td>
<td>OK</td>
<td>MIDDLE</td>
<td>WORST</td>
<td>WORST</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

No supplier excelled in all test aspects
Observations

Aspect Ratios
• High defect densities at 18:1, some supp. at 15:1

Laser vs. Mech. Microvias
• Mechanically drilled microvias yielded poorly

Back Drill
• Larger defect rate than anticipated

Thermal Stress
• Supplier through hole reliability did not correlate to pre-reflow resistance & variation measurements

Actions Taken & Plans

Suppliers:
• Analysis report assessments
• Corrective actions
• New equipment purchases
• Process alignments
Actions Taken & Plans
Supplier Equipment Implementations

• On-site Laser Drill
• In-line Develop / Etch / Strip
• Reverse Pulse Plating
• Laser Direct Imaging
• Additional Drills & Presses
• Vision Drilling
• Post-Etch Punch

Actions Taken & Plans
Internal:

• Design Rules & Protocol
• 2\textsuperscript{nd} Test Submissions in 2007
• Overseas Supplier Evaluations
• Burn-in Board Supplier Study

In Conclusion:
The PCQR\textsuperscript{2} Database Provides an Effective, Quantified, & Impartial Base to Compare PCB Fabrication Suppliers
Acknowledgements

Mike Korson
TI Make PCB Development
David Reed
TI Make Infrastructure
David Wolf
Conductor Analysis Technologies
Timothy Estes
Conductor Analysis Technologies
IPC PCQR² Database
Participating TI PCB Supplier Partners

Additional Information & Contacts

PCQR²: www.pcbquality.com
CAT Inc: www.cat-test.info
IPC: www.ipc.org
HATS: www.hats-tester.com

David Wolf, Conductor Analysis Technologies Inc.
dave.wolf@cat-test.info

Bill Mack, Texas Instruments Inc.
bigm@ti.com