BiTS Burn-in & Test Socket Workshop

2007 Session 5

ARCHIVE 2007

PCB ADVANCEMENTS AND OPPORTUNITIES

"Socket Signal Integrity – Impact From IC & Board"

James Zhou, Jiachun (Frank) Zhou
Antares Advanced Test Technologies

"Minimizing Socket & Board Inductance Using a Novel De-Coupling Interposer"

Nicholas Langston, Sr., James Zhou, Hongjun Yao
Antares Advanced Test Technologies

"Benchmarking Printed Circuit Board Fabrication Suppliers Using IPC PCQR^2 Database"

Bill Mack
Texas Instruments Inc.

antares Advanced Test Technologies

Socket Signal Integrity – Impact from IC & Board

James Zhou, presenter
Jiachun Zhou (Frank)

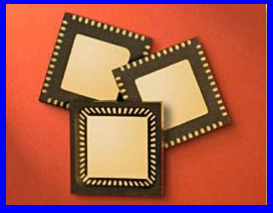
Antares Advanced Test Technologies

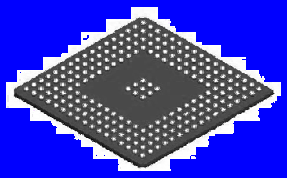
March 11-14, 2007
Hilton Phoenix East, Mesa Arizona

BiTS Burn-in & Test Socket Workshop

Outline

- ✓ Introduction
- ✓ QFN package + spring pin socket
- ✓ BGA package + spring pin socket
- ✓ LGA pad size vs. bandwidth
- ✓ Summary





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Introduction

- Package test system:

IC package + Contactor/socket + Load board

- Common practice to simulate SI performance separately
  - attempt to derive the system performance from individual sub-systems of loadboard, socket and package.
- In reality these components have EM coupling between each other. SI performance of each component is affected by other components.
- Analysis on system level coupling effects between components are presented.

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Spring pin socket for QFN package

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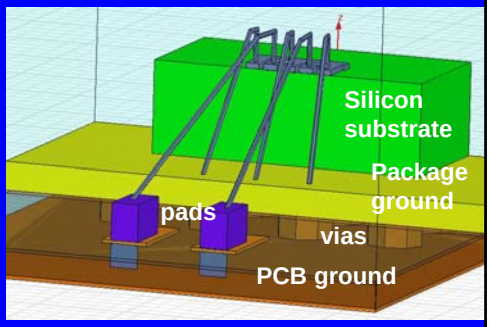
A Simple QFN Package Model

- Two signal paths formed by:
  - PCB pads
  - QFN pads
  - Bondwires
  - Signal pads on silicon
- Ground loop formed by:
  - PCB ground plane
  - 2x4 via array
  - QFN ground pad
  - Bondwires
  - Ground pads on silicon



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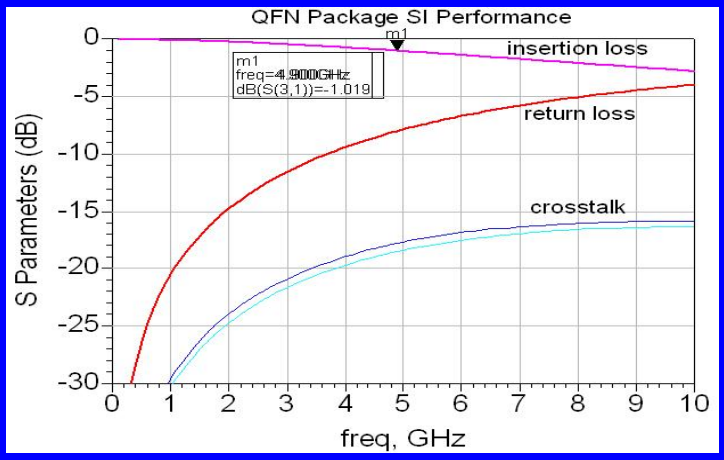
QFN Package Performance



Insertion loss (IL): IL = 1dB @4.9GHz
Return loss (RL): RL = 13dB@2.4GHz
Crosstalk (XT): XT = 30dB@1GHz

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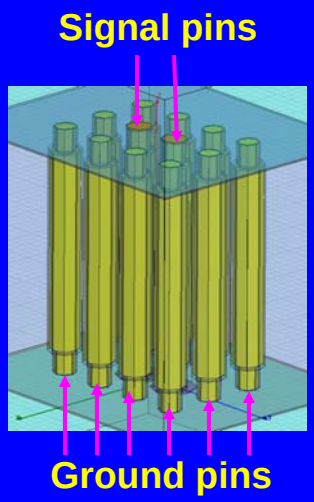
A High-speed Pin Array

- 3x4 pin array
- 2 signal pins + 10 ground pins
- Multi-conductor transmission line
- Bandwidth determined by characteristic impedance Z_0
  - Z_0 is function of pitch-to-diameter ratio and dielectric constant
- Pin array parameters:
  - length: 2.5mm
  - diameter: 0.3mm
  - pitch: 0.5mm



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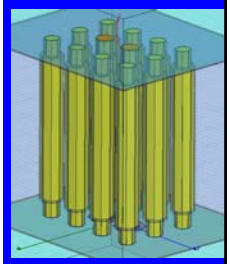
Pin Array Performance



- Max insertion loss 0~40GHz is 0.6dB
- 1dB bandwidth is greater than 40GHz

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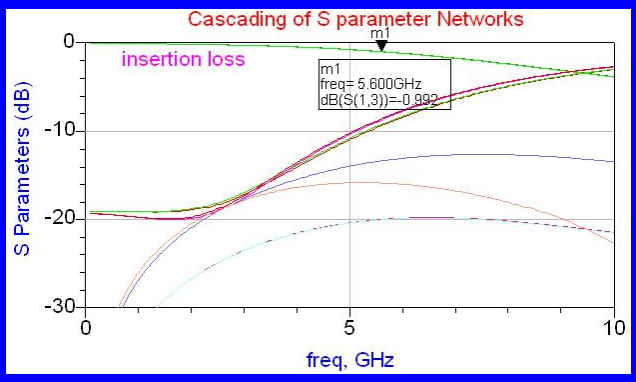
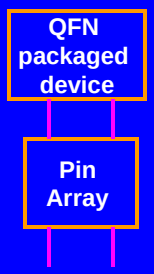
Cascaded Networks





- By cascading the QFN package and pin array networks, the overall system 1dB bandwidth is 5.6GHz
- It is higher than the bandwidth of QFN package
  - How could the bandwidth increase after inserting a pin array?

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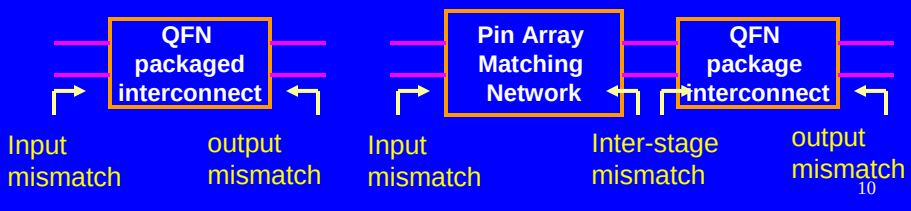
Matching Network

- pin array forms matching network
- two additional mismatch factors are introduced at input and output
  - In a near-lossless network, IL is mostly caused by reflection; as a result, reducing RL will yield better IL performance
  - Overall system bandwidth cannot in general be derived from arithmetic of sub-system bandwidth numbers



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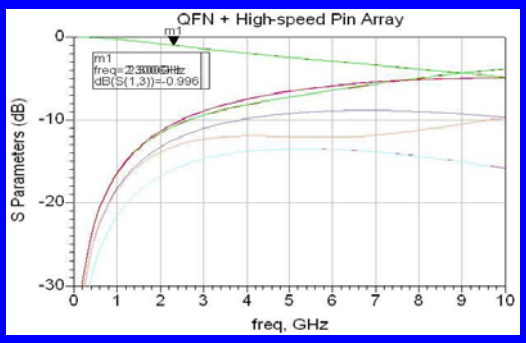
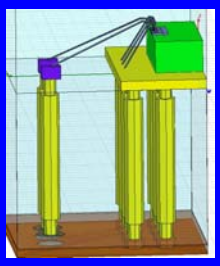
3D Full-wave EM Analysis





- 3D full-wave EM analysis (HFSS) of entire system
- 1dB bandwidth is 2.3GHz, less than half of QFN package bandwidth of 4.9GHz
- Bandwidth significantly lower than cascading network bandwidth of 5.6GHz.
- What has gone wrong?

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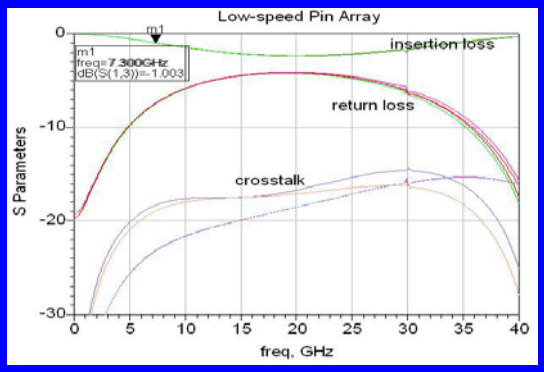
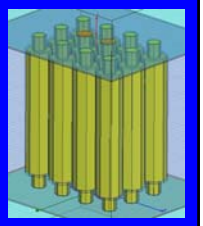
A Low-speed Pin Array





- 1dB bandwidth = 7.3GHz, significantly lower than the high speed pin array
  - Pin array parameters: length=2.5mm; diameter=0.4mm; pitch=0.5mm

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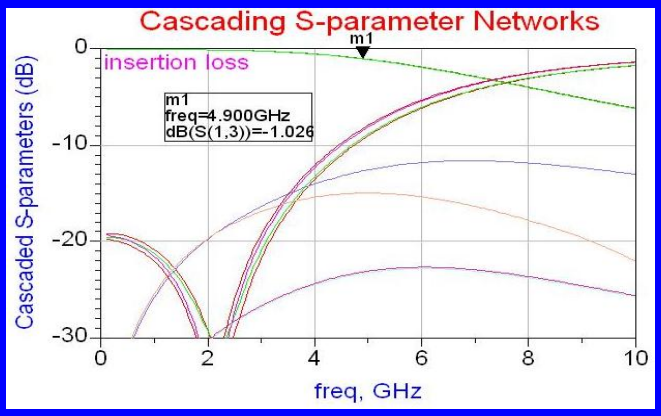
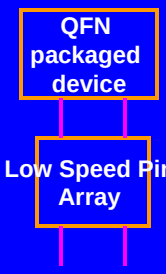
Cascading S Parameters





- By cascading QFN package and pin array sub-networks, overall system 1dB bandwidth is 4.9GHz
- It's the same as the bandwidth of the QFN package itself

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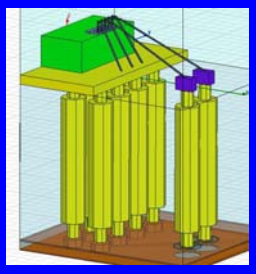
3D Fullwave EM Analysis



- 3D fullwave EM analysis of low-speed pin array plus the QFN package system
  - 1dB bandwidth = 2.5GHz
  - It is **higher** than the high-speed pin array bandwidth of 2.3GHz
  - It is about half of the cascading network bandwidth
- **How could a low-speed pin array has higher bandwidth than the high-speed pin array? (same QFN package)** 14

Observations

- QFN package itself has a 1dB bandwidth of 4.9GHz
- cascading S-parameter networks: the overall system bandwidth is equal to or higher than the bandwidth of the QFN package
- 3D fullwave EM analysis: the overall system bandwidth is significantly lower than the QFN package
- Low-speed pin has slightly better performance than the high-speed pin in the overall system (WHY?)
- 3D fullwave analysis reveals additional source of insertion loss from radiation
  - Pins surrounded by all ground pins has much less radiation

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Discussion – Cascaded Networks

- Cascaded network technique is often used in the calculation of overall system performance from individual sub-systems of PCB, socket and package
- In network analysis, the input/output ports are assumed to be terminated by infinitely long transmission lines

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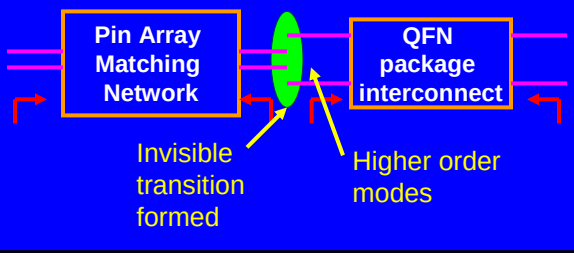
Cascaded Networks (cont.)

- when two networks of disparate interface geometries are cascaded, this important termination condition is violated
- An extra "invisible transitional network" has been created in the system, which characteristics are totally unaccounted for
  - Higher order modes exist in the vicinity of the transition



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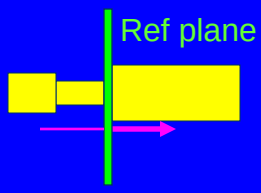
Discontinuity and Mismatch

- By separating a system at its discontinuity points, potentially large errors can be introduced due to impedance mismatch and higher order mode
- Discontinuities causes impedance mismatch; higher order modes EM fields exist in its vicinity
- when a reference plane is set up at these locations, the field patterns are greatly disturbed by the reference planes and port structure, resulting in potentially large errors



When system boundary is setup at discontinuity transitional locations, large errors can occur

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The Golden Rule

- When using "reference planes" to break a system into sub-systems, the planes must be located at **uniform transmission lines** with fair distance on both sides of the plane away from any discontinuity.
- The interface between socket and package is NOT in the middle of a uniform transmission line; in fact it is one of the most significant discontinuity points in the system

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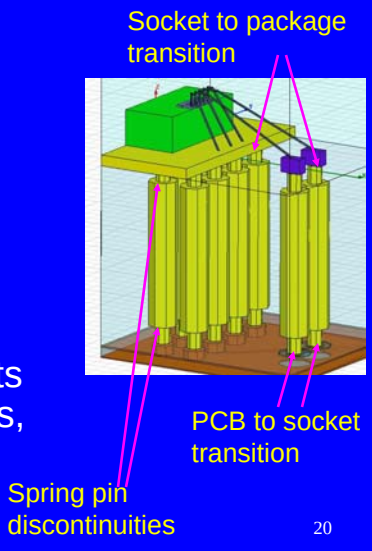
Socket Discontinuities

- Two biggest discontinuities in a socket system:
  - PCB to socket transition
  - Socket to package transition
- Spring pins also have discontinuities :
  - Change of diameter
  - From plunger to shell
  - From shell/plunger to pin tips
- By setting up input/output ports at these discontinuity locations, large errors usually occur



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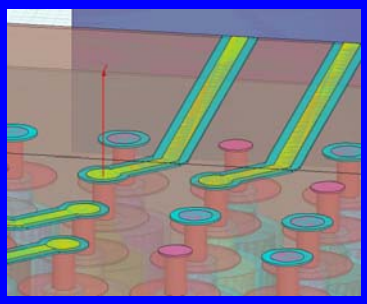
Port Setup

- To satisfy the fundamental requirements of port (reference plane) setup:
  - use microstrip or coplanar waveguide (CPW) transmission lines
  - setup the ports at fair distance away from any discontinuities of pad, via, dielectric boundary



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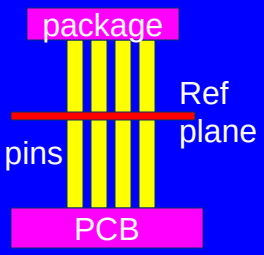
Port Setup – long pins

- For longer pins, reference planes can be setup at mid-section of pins
  - Satisfy uniform transmission line requirement
  - Electrical boundaries do not necessarily follow natural mechanical boundaries
  - Think out of the "box" and beyond the normal "boundaries"



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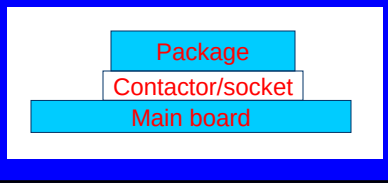
Board + Socket + Package

- In order to obtain accurate results on overall system bandwidth, it is highly desirable to **analyze the entire system** of load board + socket + package
- The input/output ports can be set up at locations of loadboard/package PCB traces, which are good uniform transmission lines
- This approach will guarantee the proper set up of the problem



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Spring pin socket for BGA package

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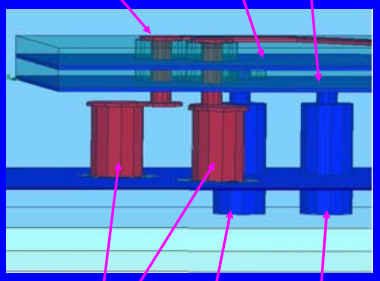
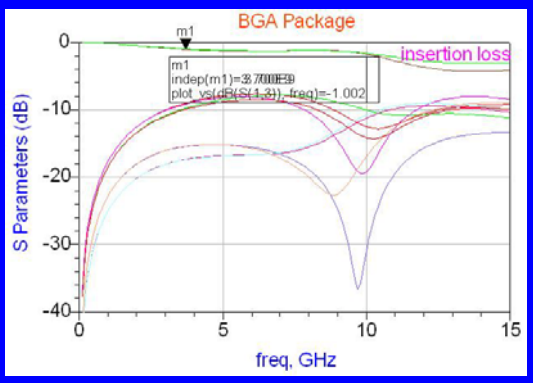
BGA Package Model





- 1dB bandwidth = 3.7GHz
- Usable frequency up to 10GHz

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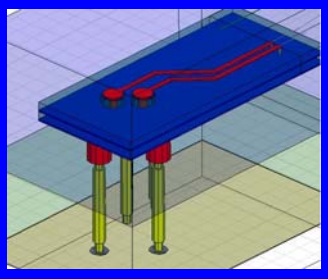
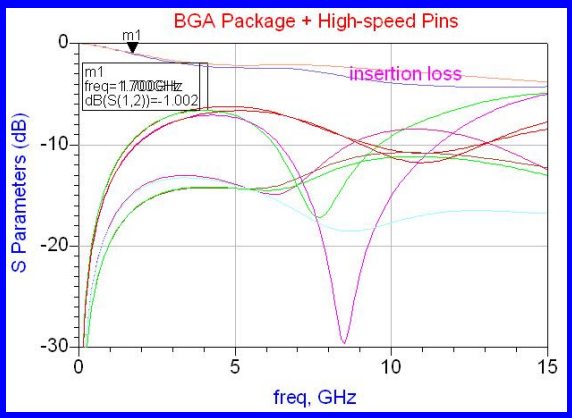
BGA Package + High-speed Pins





- **Using 40GHz high-speed pins with BGA package:**
  - **1dB bandwidth = 1.7GHz**
  - **Less than half of BGA package bandwidth**

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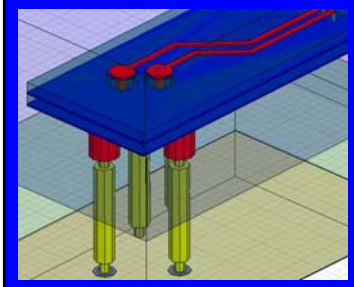
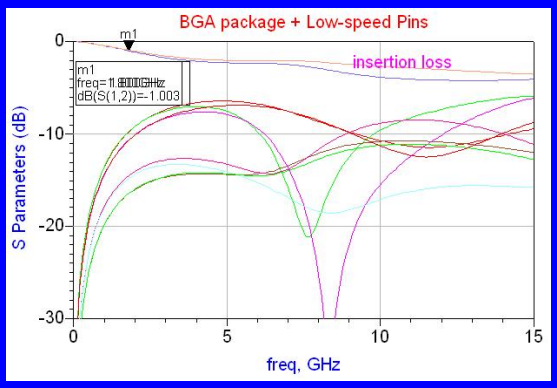
BGA Package + Low-speed Pins





- Using 7GHz low-speed pins with package:
  - 1dB bandwidth = 1.8GHz
  - Less than half of BGA package bandwidth
  - Higher than high-speed pin bandwidth

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Discussions

- Overall system performance of low-speed pins is better than high-speed pins
- BGA package bandwidth of 3.7GHz is reduced to 1.7GHz after inserting a 40GHz pin array; it is reduced to 1.8GHz after inserting a 7.3GHz pin array
- Why does the 7GHz low-speed pin array result in better performance than the 40GHz high-speed pin array?

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Discussions

- Bandwidth of "package+socket" system is not directly related to the individual sub-system bandwidth
- 3D EM effects must be simulated in one system
- Discontinuities between socket and package can only be accurately modeled in 3D full-wave analysis
- Radiation effects
- Changing pitch will completely change socket characteristic

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LGA Pad Size vs. Bandwidth

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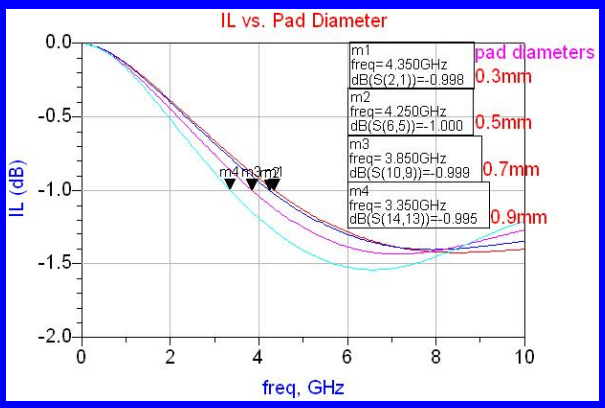
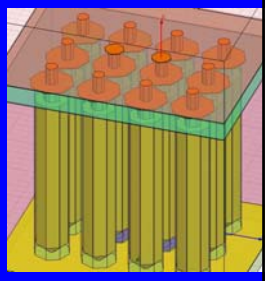
LGA Pad sizes vs. IL





- Pin array: 2 signals, 10 grounds
- Pad size sweep values: 0.3/0.5/0.7/0.9mm
- 1dB bandwidth: 4.35/4.25/3.85/3.35 GHz

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Discussion

- Very large pads are often used in LGA package for mechanical alignment tolerances
- These large pads have adverse effects on system bandwidth
- Large discontinuities and impedance mismatch exist at socket-to-package transition
- Degradation of IL cannot be easily overcome by spring pin design

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Summary

- The discontinuities at PCB-to-socket and socket-to-package transitions must be evaluated as an integrated part of the system
- Cascaded network approach may result in large errors if these discontinuities are not modeled properly
- Socket SI performance is NOT just determined by the socket itself; it is dependent on the package and PCB design
- To ensure best accuracy, model the PCB+socket+package as an integrated system using 3D full-wave EM tools

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About Authors

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Advanced Test Technologies
Minimizing Socket & Board Inductance using a Novel decoupling Interposer
2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007
BiTS
Nick Langston
James Zhou, Hongjun Yao


• It is better to uncover a little than to cover a lot.
• Eric Bogatin , SI Artisan
» www.bethesignal.com
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2

Performance Limiting Noise

- Power ground voltage droop (Rail Collapse)
- Simultaneous Switching Noise (SSN – Ground Bounce)

- PDS Components
- Board – Socket – DUT package – decoupling components

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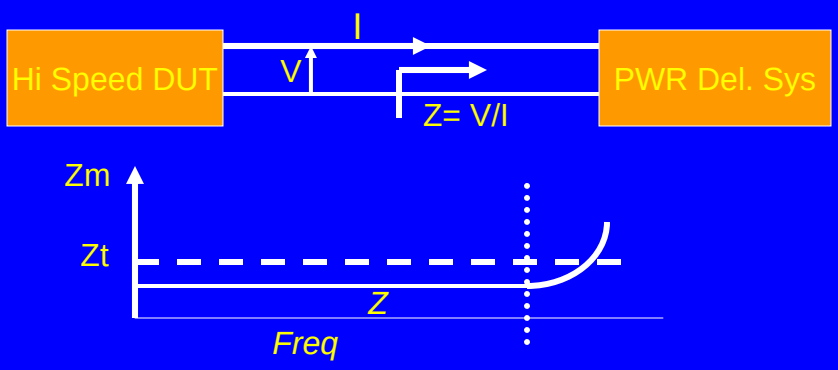

PDS has to distribute the power to the chip
Has to keep the ripple (noise) to spec ~ 5%
Can not droop all the way to the BW of DUT

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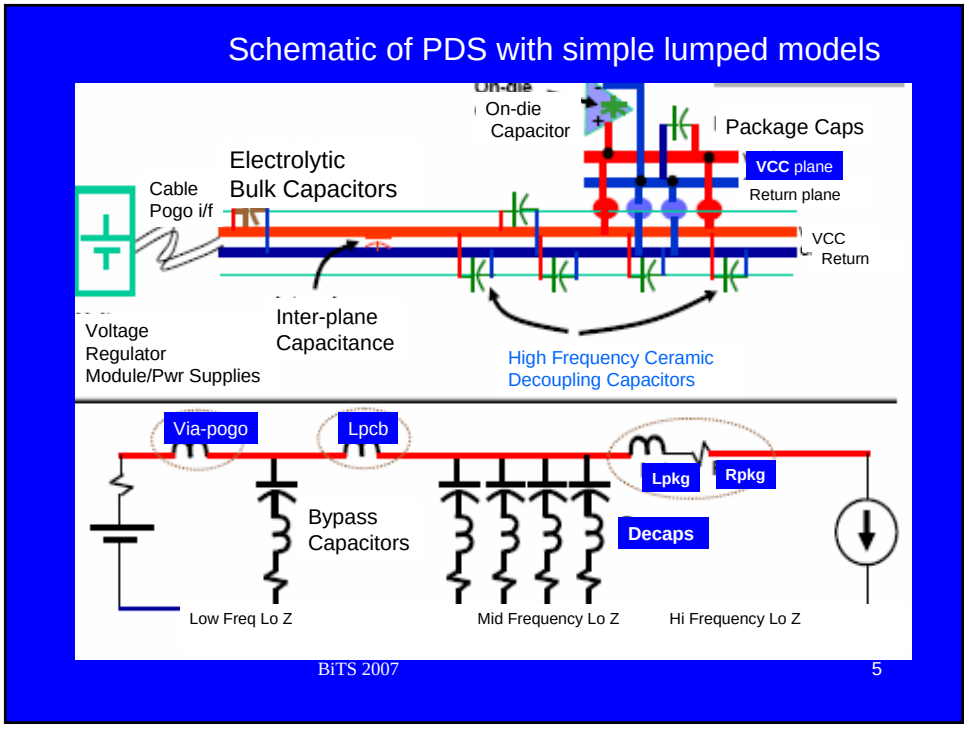
Schematic of PDS with simple lumped models
On-die Capacitor
Package Caps
Electrolytic Bulk Capacitors
Cable Pogo i/f
VCC plane
Return plane
VCC Return
Voltage Regulator Module/Pwr Supplies
Inter-plane Capacitance
High Frequency Ceramic Decoupling Capacitors
Via-pogo
Lpcb
Lpkg
Rpkg
Bypass Capacitors
Decaps
Low Freq Lo Z
Mid Frequency Lo Z
Hi Frequency Lo Z
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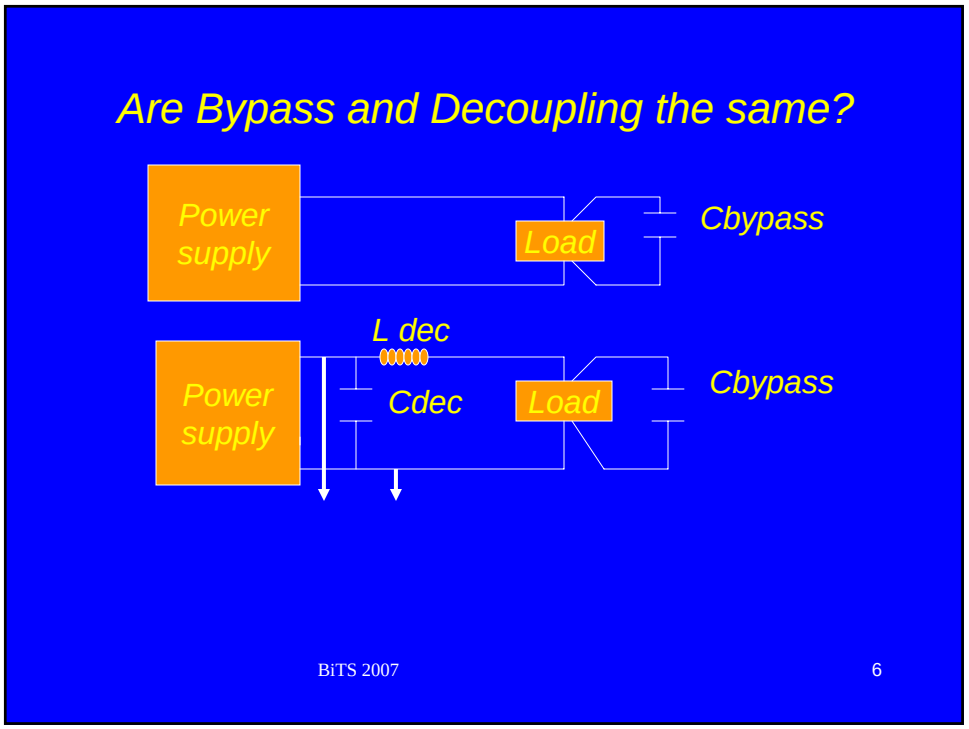
5


Are Bypass and Decoupling the same?
Power supply
Load
Cbypass
L dec
Power supply
Cdec
Load
Cbypass
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6

Basic PDS Design Strategy

Determine required PDS impedance

$Z = \Delta V / \Delta I$

Determine the frequency for the PDS alone

$Fpds = Z / 2\pi L\ pds$

Bypass $C = 1 / 2\pi FpdsZ$

Determine how much L we can handle at Fmax

$L = Z\ Tr/\pi$

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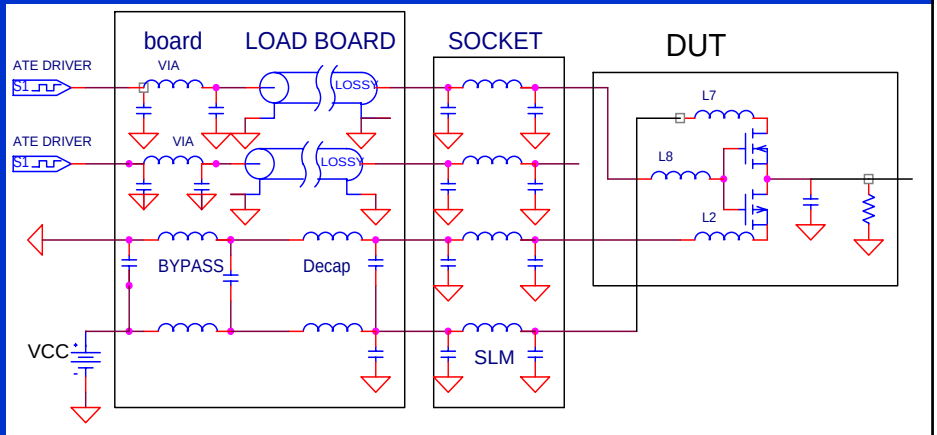
Reviewing SSO/SSN/Ground Bounce



Test Cell Schematic

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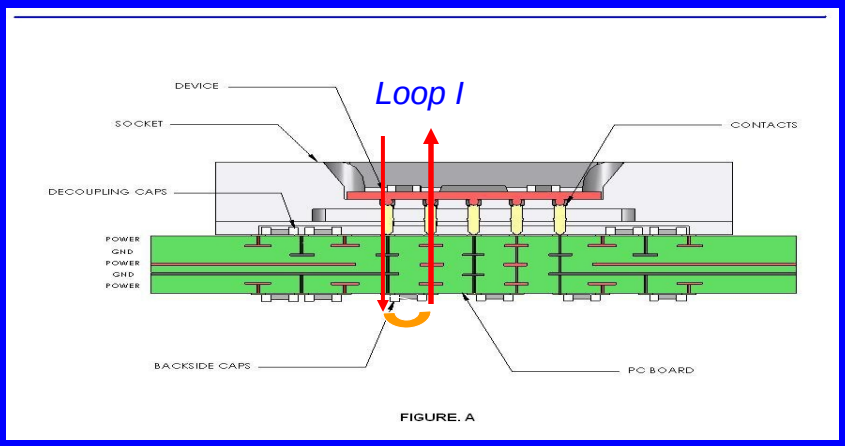

FIGURE. A

$\frac{Vgb}{Vs} = n \times \frac{Lnet}{Tr \times Zo}$

3 nets, 5nH, 0.5ns Tr, 50 ohms
60% Vgb!

Inductance is like Kryptonite!

- For Digital Designers of high speed test cells,
- Inductance is the bane of good designs

Capacitance is like Free Beer!

Simulation of the impact of Bypassing

- 8 layer FR4 board; 0.635mm dielectric
- 5 .01uF caps on bottom of the board
- 1 power via; .25mm dia.; 0.5mm antipad
- Chip mounted directly to the board
- Chip in a socket mounted to the board
- Chip in a socket with the .01uF caps

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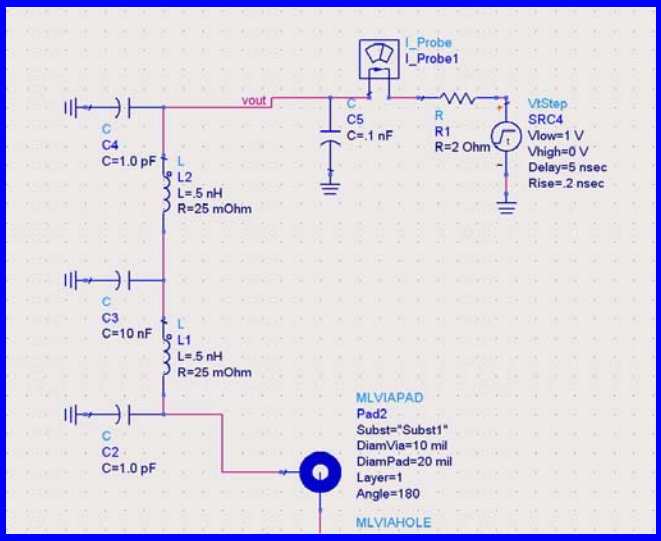
Load Configuration

- 10 ohm resitive load to draw 100ma
  - from 1v supply
- 0.1nF on chip bypass on each power pin
- Load is turned on at 5ns,
  - the Tr is 200ps

BiTS 2007 12

Spring Pin and Load Model

- *Spring Pin is modeled as a CLC pi network*
- *There is a 10nF bypass in the interposer*



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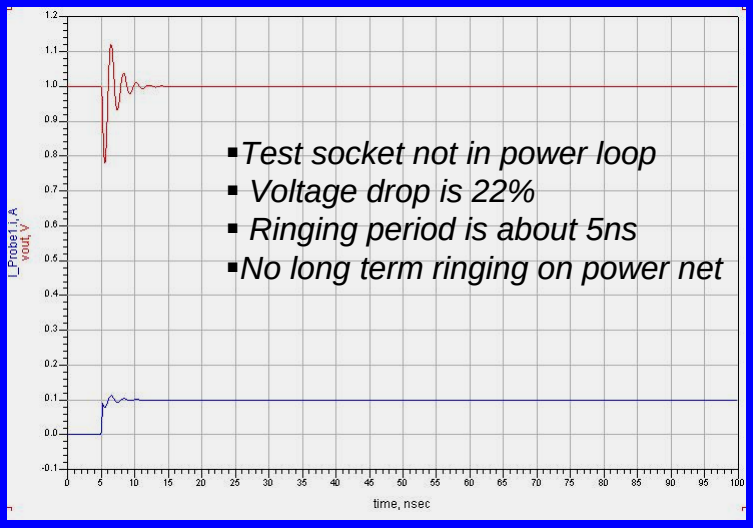
Case 1. Chip mounted to the PCB



- *Test socket not in power loop*
- *Voltage drop is 22%*
- *Ringing period is about 5ns*
- *No long term ringing on power net*

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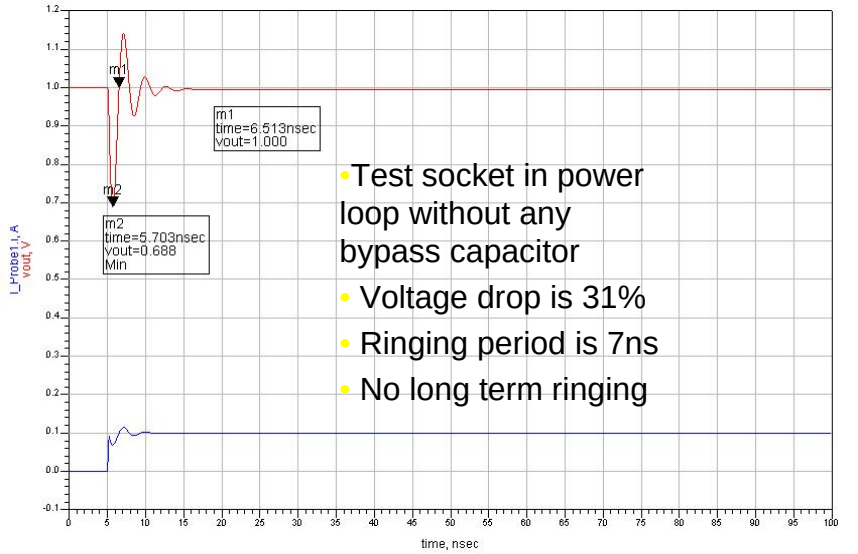
Case II: Using Socket with no bypass



- Test socket in power loop without any bypass capacitor
- Voltage drop is 31%
- Ringing period is 7ns
- No long term ringing

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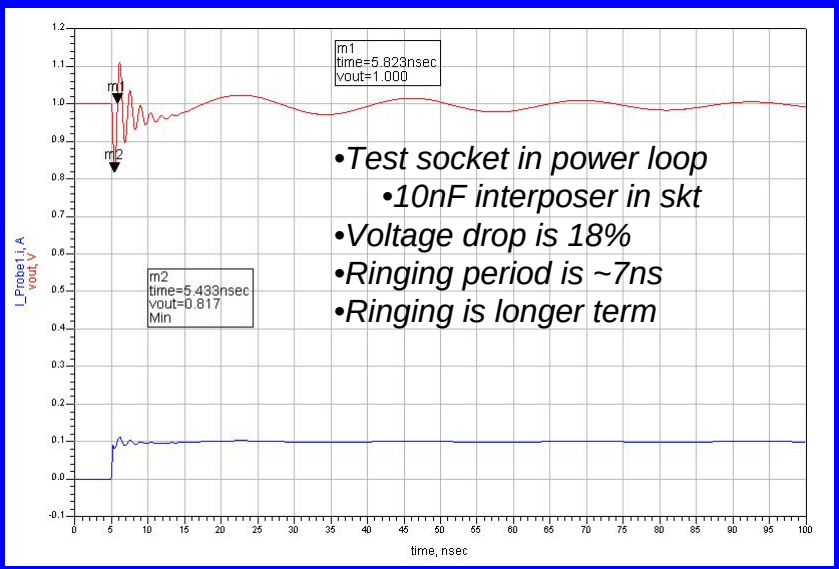
Case III: Contactor with bypass interposer



- *Test socket in power loop*
  - *10nF interposer in skt*
- *Voltage drop is 18%*
- *Ringing period is ~7ns*
- *Ringing is longer term*

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Observations

- 1nH test contactor increases the power drop from 22% to 31%
- 10nF bypass cap reduces the power drop to 18%
- The built-in bypass cap and the spring pin inductance causes some long term ringing on the power net..

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Interposer Position

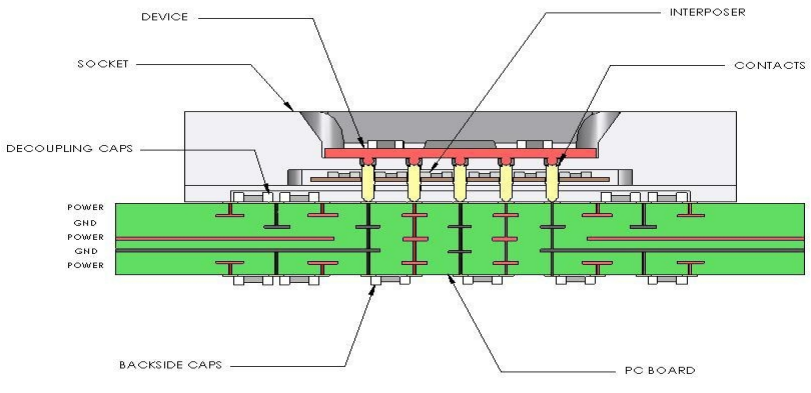

FIGURE. B

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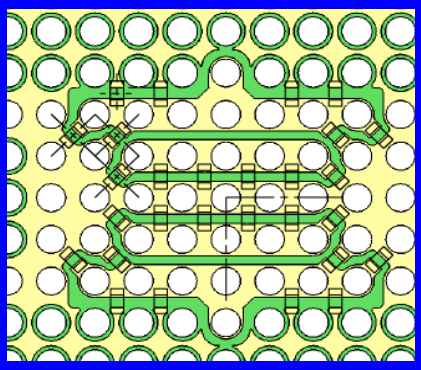
Decoupling Interposer



Drawing of Interposer

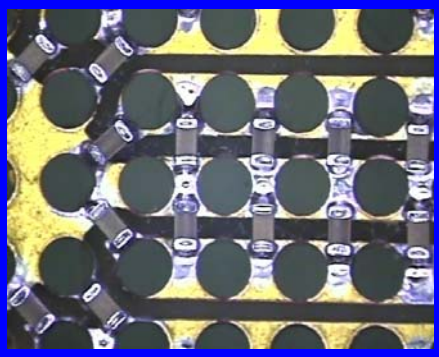


Photo of Interposer – 1mm pitch

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Socket **without** Built-in Decap

WELLS LOW INDUCTANCE SOCKET
Data=Address tCYC=4.0ns Vref=.75 VCCQ=1.50V "K/K# CLOCK SKEW TEST"
K/K# Skew vs VCCCY7C1414V18 QDR2-2bx36 36M=512Kx2x36

```
                -.75    -.5     -.25     0      0.25     0.5     0.75ns
          VCC(V)  +--------+--------+--------+--------+--------+--------+-
2.100V    |.............PPPPPPPPPPPPPP.PP.PPPPPPPPP.P.P.P.P.PPPPP.PPPP|
2.075V    |.............PPPPPPPPPP.PPPPPPPPPP.PPPPP.P.P..PPPP.PPPP.PP.|
2.050V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PPP..P.PPPPPPPPPP..PP|
2.025V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP..P.PPP.P.PPPPPPPPPP
2.000V    |.............PPPPPPPPPPPP.PPPPPPPP.PPPPPP.PPPP..P..PPPPP.P.|
1.975V    |.............PPPPPPPPPPPP.PPPPPPPPPPPPPP..PPP.P.P.PPPPPP.PP|
1.950V    |.............PPPPPPPPPPPPPPPPPP.PPPPPPPPP.P.P.P.P..PPP.PPP.|
1.925V    |.............PPPPPPPPPPPPPPPPP.PPPP.PP.PPP..PP.PP.PPPPP.P.P|
1.900V    |.............PPPPPPPPPPPPPPPPPPPPPPPPPP.PPP.PPP.PP..PPPPPP|
1.875V    |.............PPPPPPPPPP.PPPPP.PPPPP.PPPPP.P.PPP.P.PPPPPP.PP|
1.850V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PPP.PPP.P.P..PPPPPPP|
1.825V    |.............PPPPPPPPPPPPPPPP.P.P.PPP.PP..P.PPPP.PP.PPPPPPP|
1.800V    |.............PPPPPPPPPPPPPPPPPPPPPPP.P.PPP..PPP.P..PP.PPPP.|
1.775V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.P.PPPPPP.PPPP.PPPPPP|
1.750V    |.............PPPPPPPPPPPPPPP.PPPPPPPPP.P.PPP.PPP.P..PPP.P.|
1.725V    |.............PPPPPPPPPPPP.PP.PPPPPP.P.PP.PP.P.P.PP.P..P.P.|
1.700V    |.............PPPPPPPPPPPPPPPPPPP.PPPPPP.PP.PP.P.PP.PPPP.PP|
1.675V    |.............PPPPPPPPPP.PPPPPPPPPPPP.PP.PP.PPPP.PPPP.PPPPPP|
1.650V    |.............PPPPPPPPPPPPPPPPPPPPPPPPPP.P.PP.PPP.PPPPPPPPP|
1.625V    |.............PPPPPPPPPPPPPPPPPPPPPPPPP.PP.PP.P.PP.PPPPPPP.|
                +--------+--------+--------+--------+--------+--------+-
                -.75    -.5     -.25     0      0.25     0.5     0.75ns
                                  K/K# Skew (ns)
```

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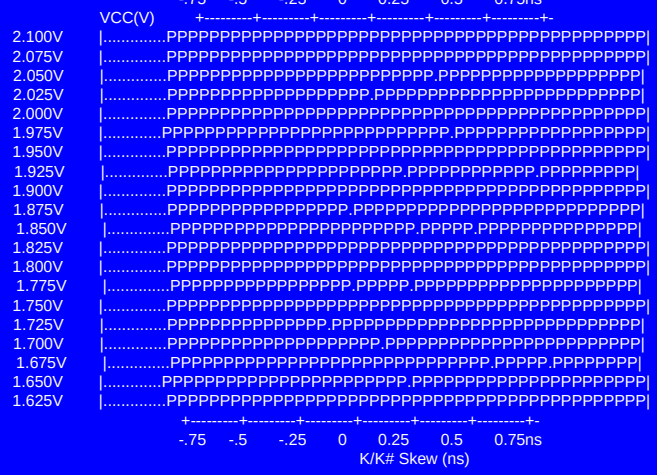
Paper #2

Socket with Built in Decoupling

SOCKET WITH BUILT IN DECOUPLING
Data=Address tCYC=4.0ns Vref=.75 VCCQ=1.50V "K/K# CLOCK SKEW TEST"
K/K# Skew vs VCCCY7C1414V18 QDR2-2bx36 36M=512Kx2x36



Summary

- Inductance is the number one cause of noise and the primary cause of rail collapse
- A well designed cap network will counteract the Inductance
- The closer the caps to the noise source; the more effective they are

- **Thanks to Cary Stubbles of Cypress for his support.**

Benchmarking Printed Circuit Board Fabrication Suppliers Using IPC's PCQR² Database

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Bill Mack
Texas Instruments Incorporated

Agenda

- Problem Statement
- What is PCQR²
- Test Panel Design & Attributes
- Supplier Results
- Observations
- Actions Taken & Plans

2

Problem Statement

A Critical Need for Printed Circuit Boards (PCBs) that are Challenging for Suppliers to Fabricate Resulting In:

Manufacturing Issues, Late Deliveries, and Field Failures

In 2006 it became evident to further evaluate & engage our PCB supplier base:

IPC's PCQR^2 Database

3

What is PCQR^2 ?

PCQR^2 is an IPC Benchmarking Test Standard & Information Database
IPC-9151

PCQR^2 stands for:
Process Capability, Quality & Relative Reliability

Standardized Test Panels Provide:

- A level field for comparing impartial results
- Statistical and manufacturing significance
- A design for manufacturability basis
- Analysis reports and an information database

4

Test Panel Design & Attributes

16 Standardized IPC Test Panel Designs Available

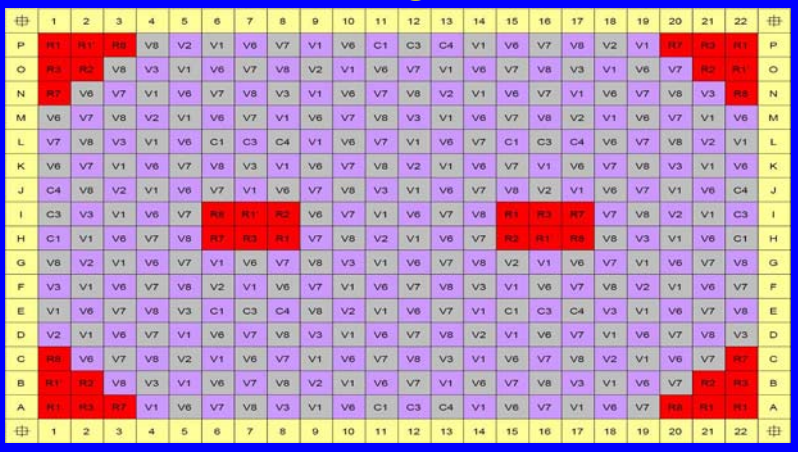
The study was conducted primarily for Automated Test Equipment (ATE) platform boards:

- Many Layers, 20+
- Thick – High Aspect Ratios
- Sequential Lamination
- Microvias, 1 & 2 Layers Deep
- Include Back Drill

→ **IPC-24VB-D Test Panel Chosen**

5

Test Panel Design & Attributes



IPC-24VB-D **18” x 24” Panel Size**

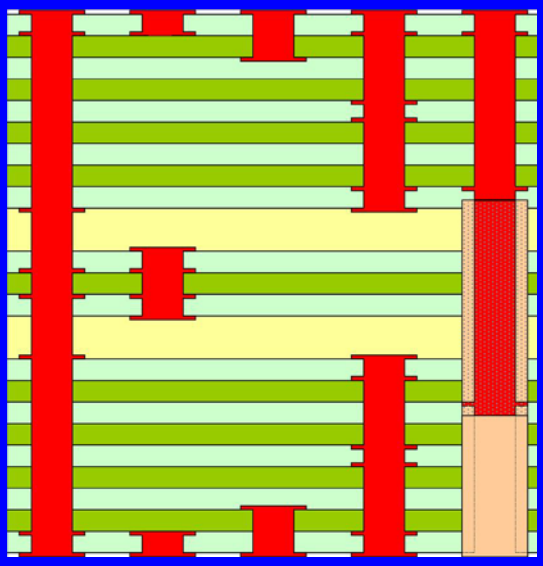
“R” Modules Test Registration

“V” Modules for Via Daisy Chain Testing 6

Test Panel Design & Attributes

"Cross-section"

- 24 Layers
- 6 Via Types:
  - Through Via
  - 1-Deep Microvia
  - 2-Deep Microvia
  - 10 Layer Blind
  - 4 Layer Buried
  - Back Drill



7

Test Panel Design & Attributes

Process Capability

- Via Formation
- Via Registration

Quality

- Via Daisy Chain Resistance & Variation

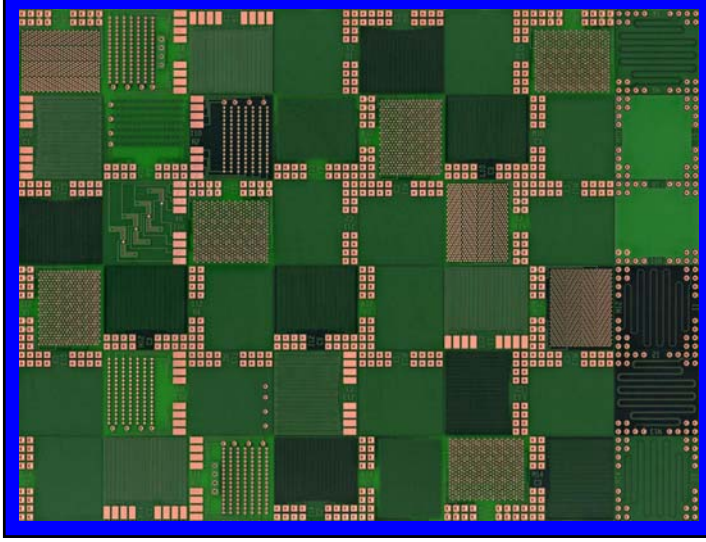
Relative Reliability

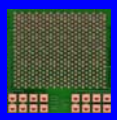
- 6 Reflow Passes, Change in Resistance
- Highly Accelerated Thermal Shock (HATS)
  - Cycles to 10% Change in Resistance
  - Cycles to Open Circuit

8

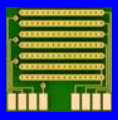
Test Panel Design & Attributes

Example of a partial test panel including trace & space, controlled impedance, & soldermask registration modules





Via Daisy Chain Module



Registration Test Module

9

Test Panel Design & Attributes

Panel Submission Requirements

15 Total Test Panels Fabricated

- 3 lots of 5 panels

Approval required for any subcontracted step...

- ...Including supplier-owned facilities off site

Internally Specified Requirements

- 0.187” thick
- Material Tg minimum 170° C
- Surface plating 200 µIN Ni / 50 µIN Au

6 of Our Suppliers Participated in 2006

10

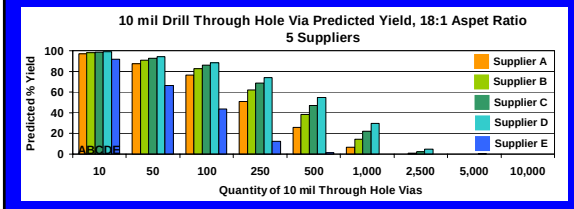
Supplier Results
Via Formation: Defect Density

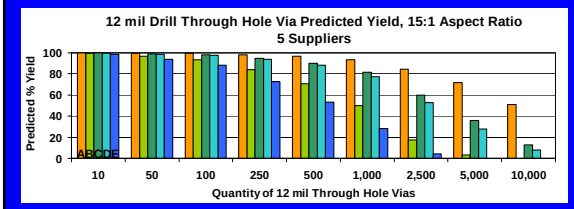
Defects Per Million Vias

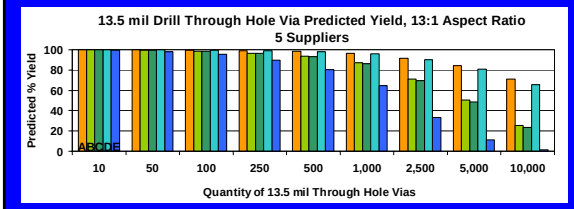
Via Type	Drill Size (mils)	Aspect Ratio	Supplier A	Supplier B	Supplier C	Supplier D	Supplier E
Through	10	18:1	2680	1921	1501	1205	8275
Through	12	15:1	67	696	205	255	1266
Through	13.5	13:1	34	136	145	42	439
Through	14.5	12:1	17	146	102	67	378
Blind	8	6:1	12	66	37	1201	1154
Blind	10	5:1	12	20	0	18	1106
Blind	12	4.5:1	12	33	6	24	867
Blind	13.5	4:1	6	46	6	12	666
Buried	6	3:1	7	1433	38	128	780
Buried	8	2.5:1	15	171	30	53	3037
Buried	10	2:1	0	24	45	23	2896
Buried	12	1.5:1	15	65	113	7	2351
Back Drill	10	18:1	3181	3946	Not Built	1214	8029
Back Drill	12	15:1	633	2068	Not Built	256	846
Back Drill	13.5	13:1	463	1272	Not Built	41	341
Back Drill	14.5	12:1	594	1150	Not Built	82	386

Poor 10 mil Through and Back Drill Yields [11]

Defects: Through Via Predicted Yields







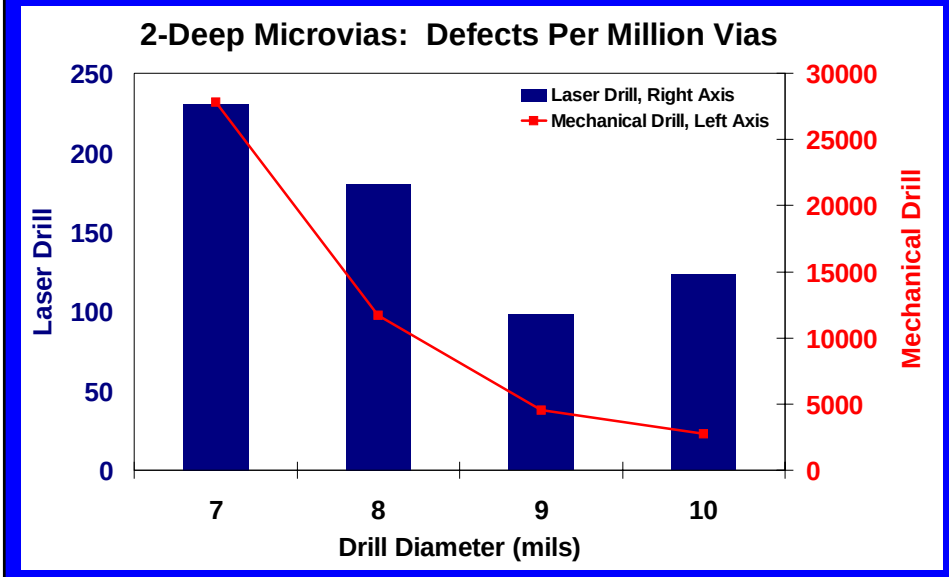
10 mil Drill
Poor performance by all suppliers
18:1 Aspect Ratio

12 mil Drill
Significantly better, Varied results
15:1 Aspect Ratio

13.5 mil Drill
13:1 Aspect Ratio

12

Defects: Laser vs. Mech. Drill Microvias



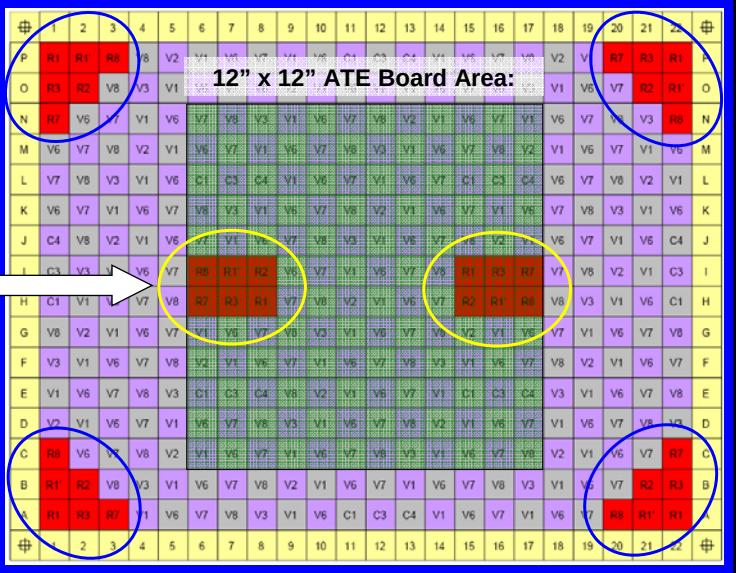
Mechanically Drilled Microvias: Poor Yield [13]

Registration: Inner vs. Outer Panel

Outer Corner Registration Test Modules

Inner Panel Registration Test Modules

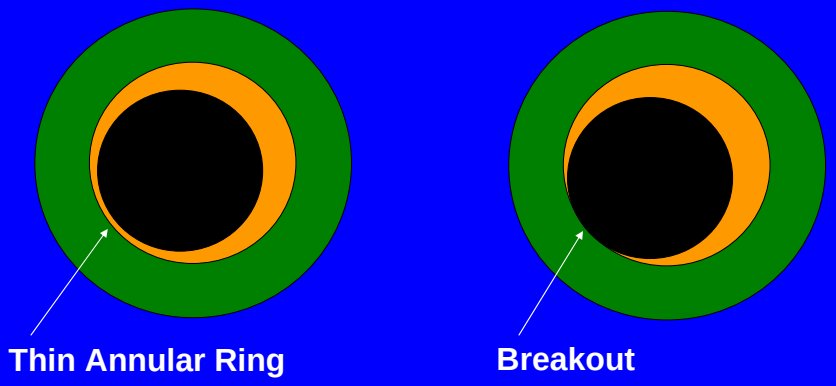
Outer Corner Registration Test Modules



Best Registration Results - Inner Panel [14]

Paper #3

Drill Misregistration & Breakout



Ideal, uniform annular ring size is determined by:
(Copper Pad Diameter – Drill Diameter) ÷ 2

15

Registration: Drill to Copper Clearance

Through Hole Via to Cu Feature Spacing Chart

0.5 Oz Inner Layer Cu, 12:1 Aspect Ratio, Sequential Lam Build: 10 Layer Outers & 4 Layer Inner

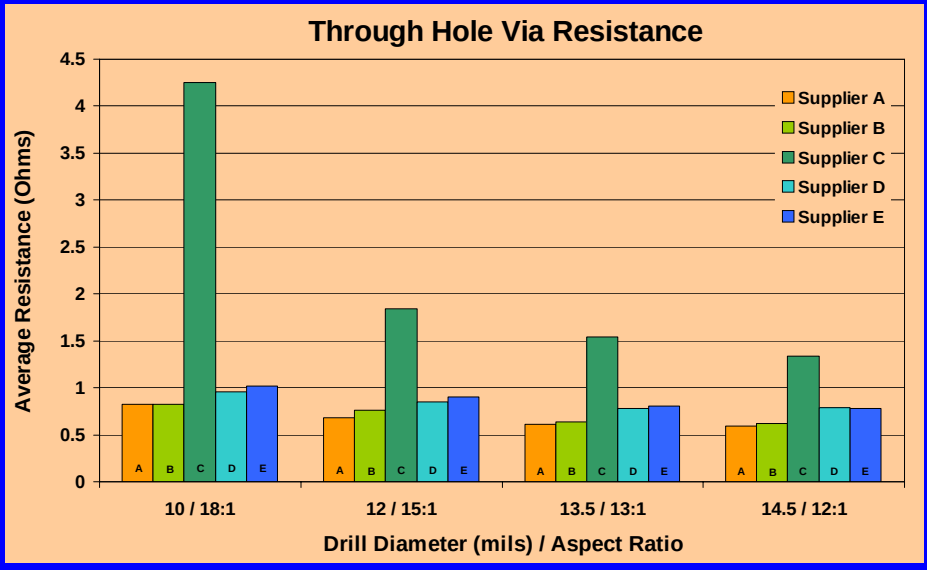
Drill to Cu Clearance (mils):	Within 12" Center Panel Area							Outer Corners of 18" x 24" Panel						
Board Layers:	8	7	6	5	4	3		8	7	6	5	4	3	
Top Lam L2, 4, 6, 8	100-90	100-90	100-90	89-80	59-50	39 or <	Supplier A	100-90	100-90	89-80	59-50	39 or <	39 or <	
Middle Lam L11 & 14	100-90	100-90	100-90	100-90	89-80	69-60		100-90	100-90	100-90	89-80	79-70	49-40	
Top to Bot Lams L10 & 15	100-90	100-90	100-90	100-90	89-80	39 or <		100-90	100-90	89-80	59-50	39 or <	39 or <	
Bottom Lam L17,19, 21, 23	100-90	100-90	79-70	49-40	39 or <	39 or <		100-90	89-80	69-60	49-40	39 or <	39 or <	
Top Lam L2, 4, 6, 8	100-90	100-90	69-60	49-40	39 or <	39 or <	Supplier B	79-70	49-40	39 or <	39 or <	39 or <	39 or <	
Middle Lam L11 & 14	100-90	89-80	89-80	79-70	49-40	39 or <		100-90	89-80	69-60	49-40	39 or <	39 or <	
Top to Bot Lams L10 & 15	100-90	89-80	69-60	49-40	39 or <	39 or <		79-70	69-60	59-50	39 or <	39 or <	39 or <	
Bottom Lam L17,19, 21, 23	100-90	100-90	89-80	59-50	39 or <	39 or <		89-80	79-70	49-40	49-40	39 or <	39 or <	
Top Lam L2, 4, 6, 8	100-90	100-90	100-90	79-70	49-40	39 or <	Supplier C	89-80	69-60	49-40	39 or <	39 or <	39 or <	
Middle Lam L11 & 14	100-90	100-90	100-90	79-70	49-40	39 or <		100-90	89-80	69-60	49-40	39 or <	39 or <	
Top to Bot Lams L10 & 15	100-90	100-90	79-70	69-60	49-40	39 or <		100-90	79-70	69-60	49-40	39 or <	39 or <	
Bottom Lam L17,19, 21, 23	100-90	100-90	89-80	69-60	39 or <	39 or <		69-60	49-40	39 or <	39 or <	39 or <	39 or <	
Top Lam L2, 4, 6, 8	100-90	100-90	100-90	100-90	89-80	59-50	Supplier D	100-90	89-80	69-60	49-40	39 or <	39 or <	
Middle Lam L11 & 14	100-90	100-90	100-90	100-90	79-70	49-40		100-90	89-80	69-60	49-40	39 or <	39 or <	
Top to Bot Lams L10 & 15	100-90	100-90	100-90	89-80	79-70	49-40		79-70	69-60	49-40	39 or <	39 or <	39 or <	
Bottom Lam L17,19, 21, 23	100-90	100-90	100-90	79-70	59-50	39 or <		79-70	59-50	39 or <	39 or <	39 or <	39 or <	
Top Lam L2, 4, 6, 8	79-70	39 or <	39 or <	39 or <	39 or <	39 or <	Supplier E	39 or <	39 or <	39 or <	39 or <	39 or <	39 or <	
Middle Lam L11 & 14	89-80	79-70	69-60	49-40	39 or <	39 or <		79-70	59-50	49-40	39 or <	39 or <	39 or <	
Top to Bot Lams L10 & 15	79-70	59-50	39 or <	39 or <	39 or <	39 or <		59-50	39 or <	39 or <	39 or <	39 or <	39 or <	
Bottom Lam L17,19, 21, 23	79-70	59-50	39 or <	39 or <	39 or <	39 or <		39 or <	39 or <	39 or <	39 or <	39 or <	39 or <	
Percent Yield:	100 - 90		89 - 80		79 - 70		69 - 60	59 - 50		49 - 40		<= 39		

16

Relative Supplier Registration Performance

Paper #3

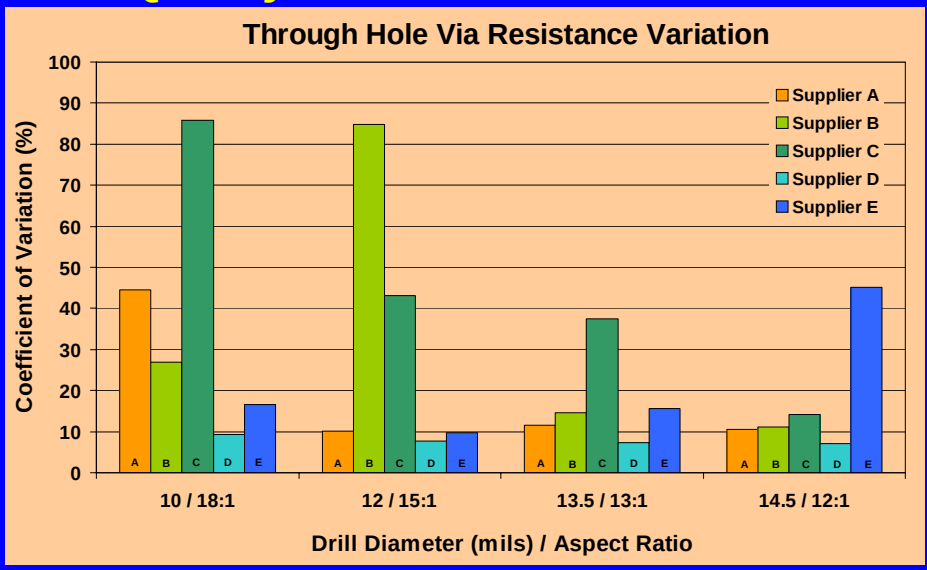
Quality: Resistance Measurements



Supplier C: Significantly High

17

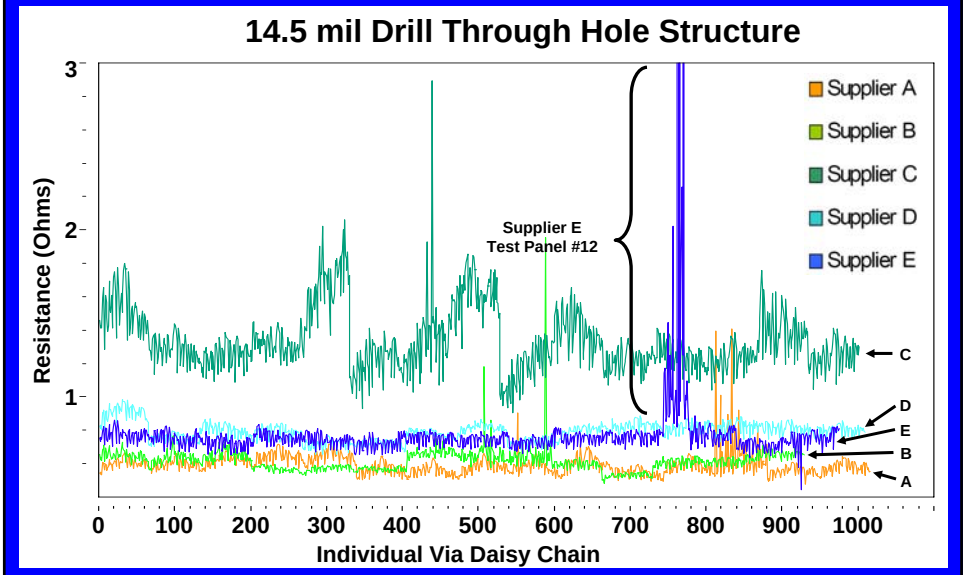
Quality: Resistance Variation



Supplier D: Consistently Lowest

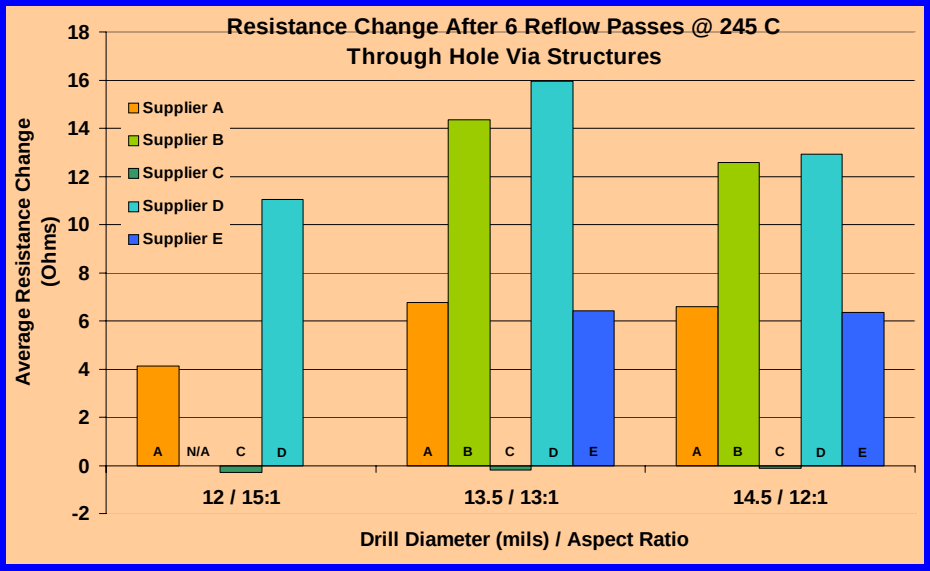
18

Quality: Daisy Chain Resistance Plot



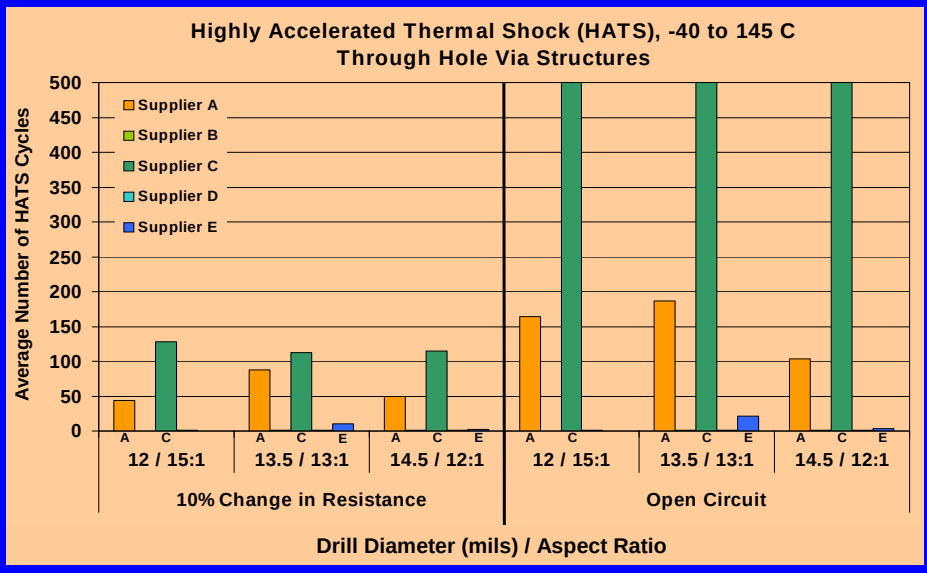
Supplier E: Spike in CoV Value – Panel 12 [19]

Reliability: Through Hole Via Reflow



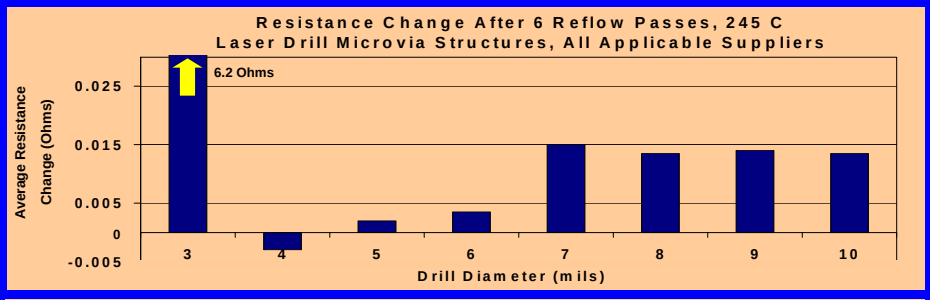
Supplier C: Decrease in Resistance [20]

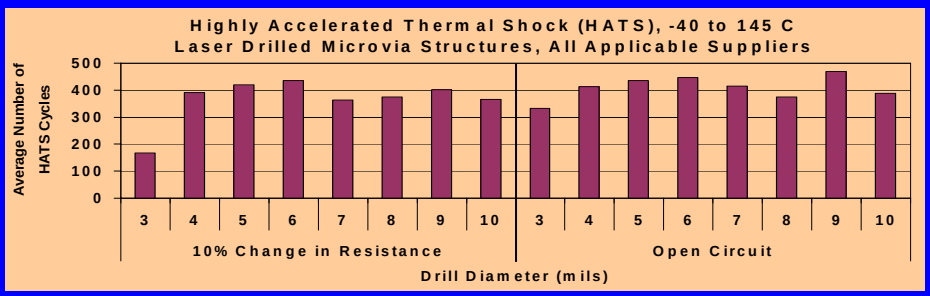
Reliability: Through Hole Via HATS



Supplier C: Survived 500 Thermal Cycles [21]

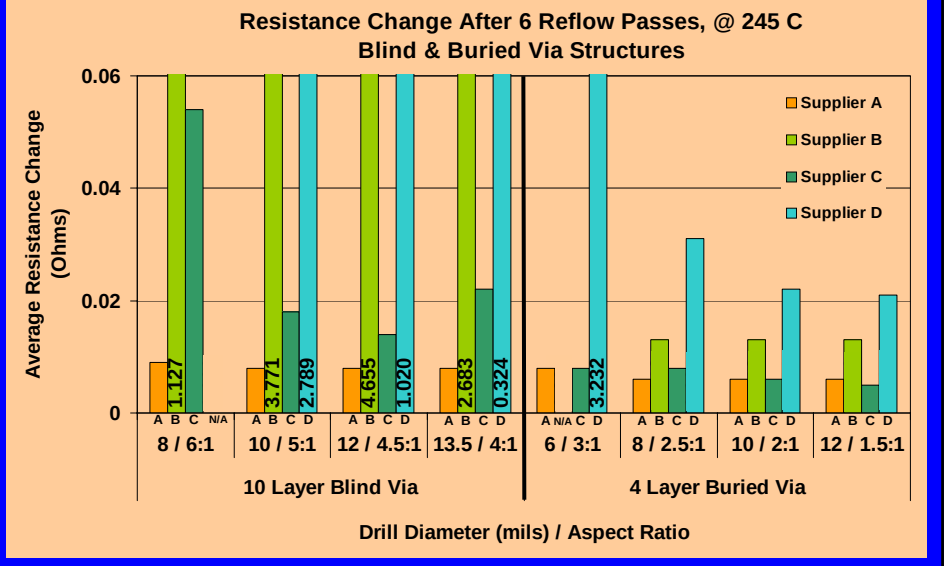
Reliability: Laser Drilled Microvias





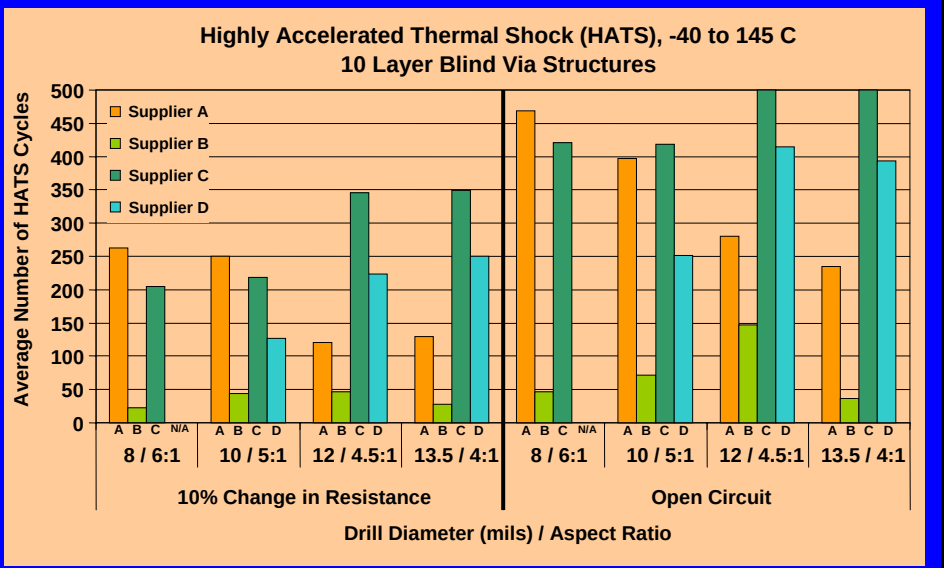
Few Cycles Between 10% Change and Open [22]

Reliability: Blind & Buried Via Reflow



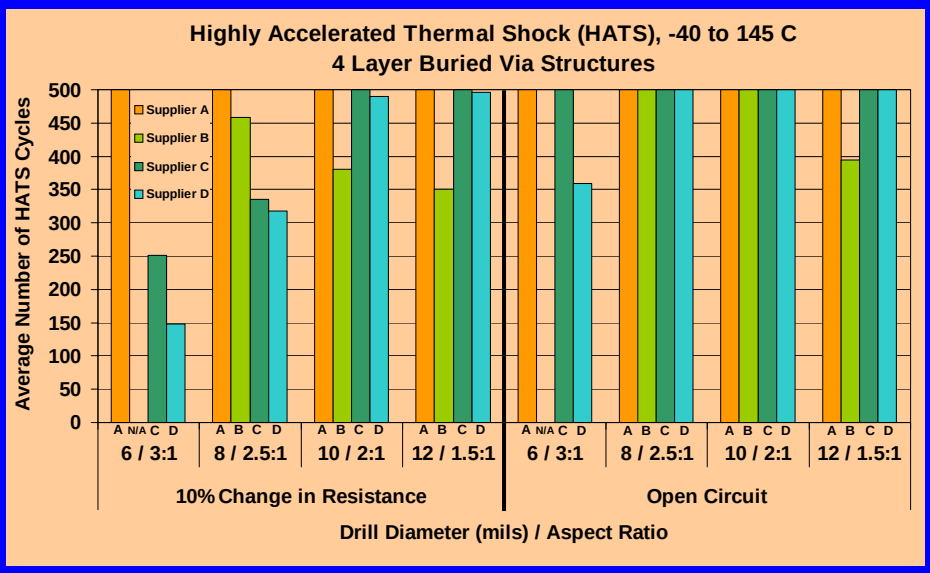
Supplier A: Consistent Smallest Change 23

Reliability: Blind Via HATS



Supplier B: Earliest Thermal Shock Failure 24

Reliability: Buried Via HATS



Supplier A: Max 500 Shock Cycles on All

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Supplier Relative Results

Through Hole Structure Dashboard

	Defect Density	Registration	Resistance Values	Resistance Variation	Reflow Reliability	Thermal Shock
SUPP A	BEST	BEST	OK	MIDDLE	MIDDLE	MIDDLE
SUPP B	MIDDLE	MIDDLE	OK	MIDDLE	WORST	WORST
SUPP C	MIDDLE	MIDDLE	HIGH	WORST	BEST	BEST
SUPP D	BEST	BEST	OK	BEST	WORST	WORST
SUPP E	WORST	WORST	OK	MIDDLE	WORST	WORST

No supplier excelled in all test aspects

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Observations

Aspect Ratios

- High defect densities at 18:1, some supp. at 15:1

Laser vs. Mech. Microvias

- Mechanically drilled microvias yielded poorly

Back Drill

- Larger defect rate than anticipated

Thermal Stress

- Supplier through hole reliability did not correlate to pre-reflow resistance & variation measurements

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Actions Taken & Plans

Suppliers:

- Analysis report assessments
- Corrective actions
- New equipment purchases
- Process alignments

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Actions Taken & Plans

Supplier Equipment Implementations

- On-site Laser Drill
- In-line Develop / Etch / Strip
- Reverse Pulse Plating
- Laser Direct Imaging
- Additional Drills & Presses
- Vision Drilling
- Post-Etch Punch

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Actions Taken & Plans

Internal:

- Design Rules & Protocol
- 2nd Test Submissions in 2007
- Overseas Supplier Evaluations
- Burn-in Board Supplier Study

In Conclusion:

The PCQR² Database Provides an Effective, Quantified, & Impartial Base to Compare PCB Fabrication Suppliers

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Mike Korson
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David Wolf
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Conductor Analysis Technologies
IPC PCQR² Database
Participating TI PCB Supplier Partners

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Additional Information & Contacts

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