BiTS Burn-in & Test Socket Workshop

2007 Session 3

ARCHIVE 2007

PUSHING THE POWER/THERMAL ENVELOPE

"Comparison of Methods for Measuring Residual Stresses in Connector Alloy Strip for BiTS Applications"

John Harkness, FASM
Brush Wellman, Inc.

"Socket and Heat Sink Considerations in High Power Burn-in"

John McElreath
Micro Control Company

"Determining Thermal Resistance Characteristics Without a Power Sensor"

Trent Johnson
AMD
Jerry Tustaniwskyj
Delta Design

COMPARISON OF METHODS FOR MEASURING RESIDUAL STRESSES IN CONNECTOR ALLOY STRIP FOR BiTS APPLICATIONS

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2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

OUTLINE

- Background of BiTS-grade strip
- Introduction to residual stresses in strip
- Questions
- Comparison of residual stress tests
  - **X-Ray Diffraction**
  - **Wire-EDM Finger Test**
  - **Etch-to-1/2 Thickness Test**
- Example results – Cu-Be strip
- Cu-Be results vs. literature
- Conclusions
- Future work

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BACKGROUND

- **BiTS contact requirements**
  - Co-planar & dimensionally uniform STAMPED parts
  - Low/uniform/predictable AGING distortion
    - Reason: consistent spring performance in large grid arrays
- **One *widely perceived* cause** of problem = variable distortion from high/non-uniform residual stresses in strip
- **Opportunity** … provide the industry with "BiTS-grade", **dimensionally stable** strip via processing for low/uniform residual stress

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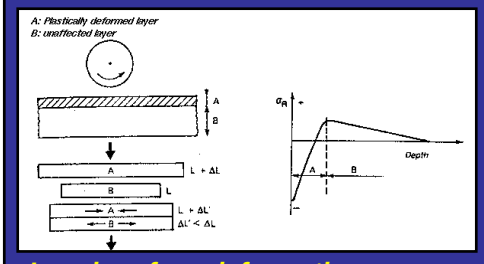
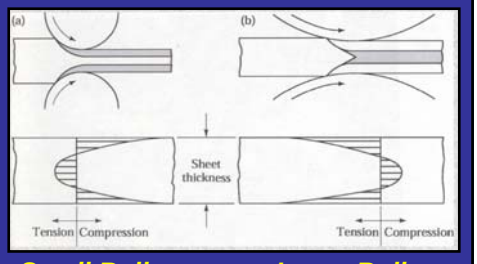
Residual Stress (I)

Definition & Origin in Cold Rolled Strip

RESIDUAL STRESS = The stress (Compressive or Tensile) which exists in an elastic solid body in the absence of, or in addition to, the stresses caused by an external load. Such stresses can arise in strip from NON-UNIFORM or localized deformation during rolling or stamping … even brushing.



Local surface deformation: COMPRESSIVE surface & underlying TENSILE residual stress



Small Rolls Heavy Passes

Large Rolls Light Passes

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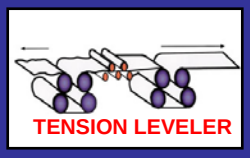
Residual Stress (II)

Basic "Tool Kit" for Management & Control

- *References: text books, literature, patents*
- Deliberate "management"
  - **Cold rolling practice**
  - **Surface treatment** to impart desirable COMPRESSIVE stress (e.g., shot peening)
- Residual stress "reduction"
  - **Thermal stress relief** ... Render YS < residual stress (enable distortion for residual stress relief)
  - **Mechanical stress relief** (e.g., Tension or Stretch Bend Leveling) … PLASTICALLY DEFORM strip to override original stress distribution
- *Combined* "management" + "reduction"



[STRETCH BEND LEVELER has more "robust" Roller Leveling (BENDING)]

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Questions (I)

- **What stress distribution in strip is "best" for BiTS?**
  - **COMPRESSIVE surface stress enhances fatigue & corrosion resistance in engineering applications**
  - **TENSILE surface stress degrades Spring Bend Limit**
  - **Is ZERO stress "good" or "bad" in connectors?**
    - **NO references in literature**
- **How does stress vary over a large coil & does that alter part distortion between slit cuts/down length?**
- **Does slitting "release" as-shipped stress?**

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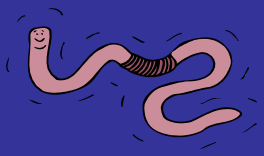
Questions (II)

- What is "best" practice for MECHANICAL STRESS RELIEF vs. shape correction (flattening/decambering) of a coil?
- Do **parts-forming strains** override as-shipped stresses?
- Do ELASTIC residual stresses affect precipitation & shrinkage during age hardening, ***increasing*** distortion?
- Does age hardening "thermally relieve" residual stress?



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Residual Stress Tests for Strip

- **QUANTITATIVE measure**
  - **X-Ray Diffraction**
    - Stress-induced change in a diffraction pattern peak
- **QUALITATIVE measures**
  - **Wire-EDM Finger Test**
    - Deflection of cut fingers = relative indicator of base metal residual stress DISTRIBUTION over an area
  - **Etch-to-1/2 Thickness Test**
    - Distortion of a specimen after etching away of ½ thickness = relative indicator of through-t residual stress PROFILE
      - **QUANTITATIVE** OPTION: Step-wise etch & measure incremental change in curvature, compute residual stress vs. depth [NOT employed in this work]

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X-Ray Diffraction (XRD) Test

- **Determine X-Ray Elastic Constant (XEC)**
  - Change in XRD peak vs. stress in 4-point bend test
  - **Alloy 25 unaged < Brush 60 aged < Alloy 25 aged**
- **Cu-Be settings = {311} peak, Mn target, no filter**
  - 10-12 exposures (10-13 minutes)/data point
- **Data types**
  - **Surface** residual stress
    - **Line scan L, T or "contour map"**
  - **Through-thickness** stress **PROFILE**
    - **Surface to mid-plane -- serial etch**
- **Stress = DIRECTIONAL (L, T, 45 deg)**
- **Specimen size**
  - Sheared sheets, slit cuts & stamped parts
- **Typical cost (2006)**
  - VENDOR = **$100/data point, $40/etch step, $1500/XEC test**

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Wire-EDM Finger Test

- **Specimen Geometry**
  - 8 in. square sheared panel of strip
    - Wire-EDM 32 fingers, ¼ in. X 6 in. (L & T)
    - Can stack sheets in fixture for gang cutting
- **Measurement**
  - Hang panel & observe finger displacement(s)
    - Distortion pattern = **relative indicator** of stress distribution over area of panel
- **Cost (2006)**
  - VENDOR = **$200-$400/single panel**

Bizarre example – NOT "BiTS grade" material!!

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Etch-to-1/2 Thickness Test (Etch Test)

- **Specimen Geometry**
  - Shear 0.4 in. X 6.5 in. specimens
    - Use steel backer sheet to prevent burr in thin strip
  - Shear in PAIRS
    - L, T & 45 deg
    - Mill Edge vs. Center of MW (L)
- **Procedure**
  - Mask one surface & etch to ½ thickness from opposite side
    - Cu-Be = **hot ferric chloride**, spray etched
  - Etched distortion = **relative indicator** of stress PROFILE in remaining ½ of strip thickness
- **Cost (2006)**
  - **$35.00/single etched specimen**

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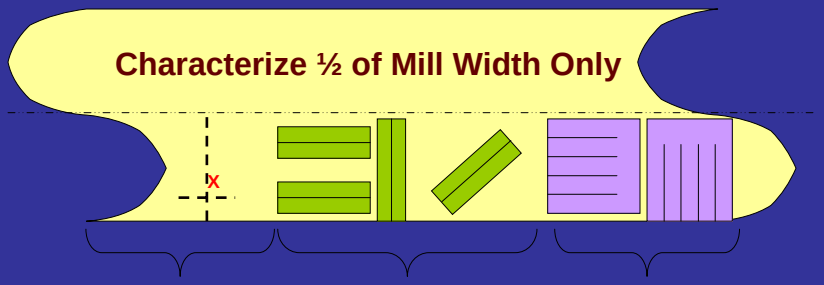
Residual Stress Test Comparison

6 ft. long coil end X 16 in. MW



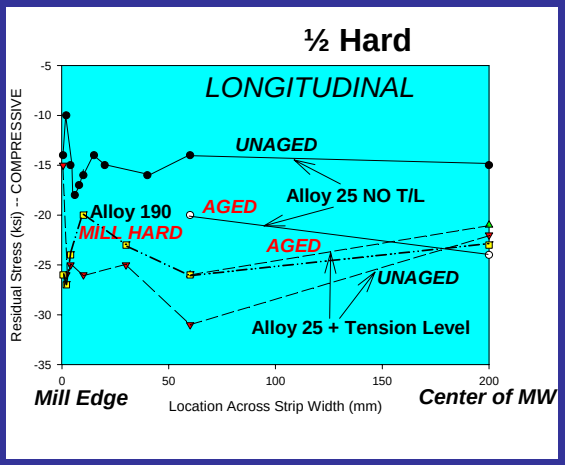
GOAL: "Baseline" Cu-Be stress distributions & understand effects of coil processing on them. Link to connector performance.

Unaged

Aged AFTER EDM
Age distortion??

XRD Results (I)

***SURFACE* Residual Stress in Alloy 25/190 Strip**



- All surface stress = COMPRESSIVE
- NOT T/L = UNIFORM stress across MW
- T/L = center MORE COMPRESSIVE [LESS UNIFORM over width]
- Aging increases NOT T/L surface stress = MORE COMPRESSIVE
- Aging relieves T/L surface stress = LESS COMPRESSIVE

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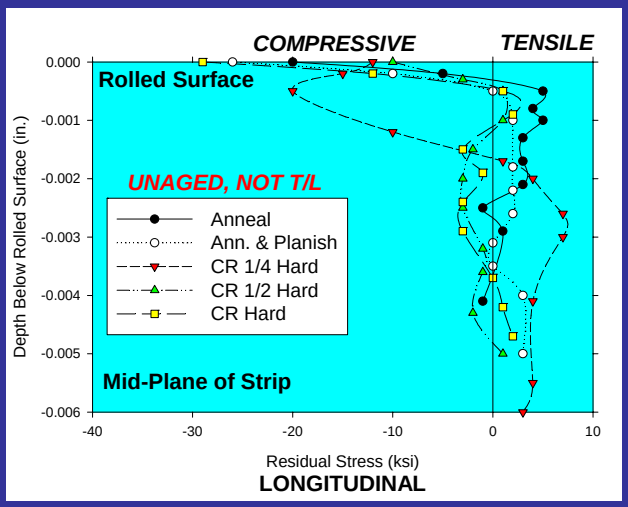
XRD Results (II)

***THROUGH-THICKNESS* Residual Stress Profiles of Alloy 25**



- All surface stress = COMPRESSIVE
- Surface stress not proportional to rolled temper
- Interior stress fast approaches ZERO or low TENSILE
- Stress profiles = symmetrical about the strip mid-plane

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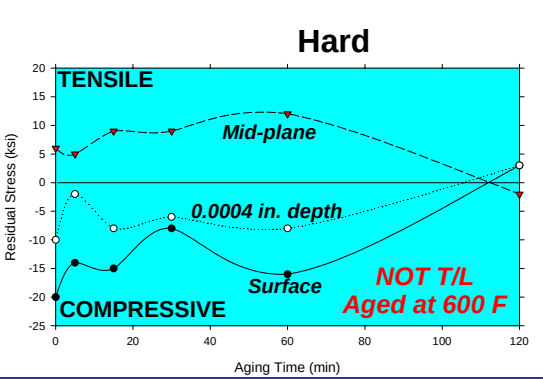
XRD Results (III)

THROUGH-THICKNESS Residual Stress Profile
Changes in Alloy 25 During AGE HARDENING

- Aged 0 to 30+ min
  - **Rapid HARDENING**
  - **Surface = LESS COMPRESSIVE**
  - **MID-PLANE = MORE TENSILE**
- Aged 2 hr
  - **Hardness plateau**
  - **Stress PROFILE approaches ZERO**



Aging → "Thermal Stress Relief"?
[Aged ½ H did NOT go to ZERO]

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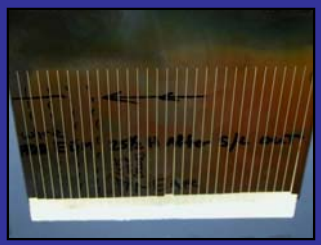
Wire-EDM Finger Test Results (I)

UNAGED Alloy 25 (1/2 Hard)

NOT T/L ***Tension Leveled***



- Minimal L distortion, NOT T/L
- **Large** EDGE L deflection +T/L
- NO T distortion, +/- T/L
- **FLAT fingers = Symmetrical thru-t profile, NOT "ZERO stress"**

Thermal stress relief before EDM = INCONCLUSIVE

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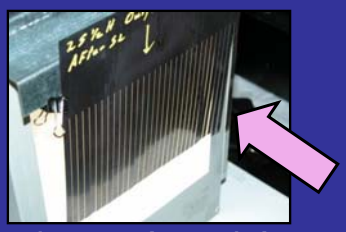
Wire-EDM Finger Test Results (II)

FAILED Attempt to Predict Aging Distortion in Alloy 25

L



T/L + Aged 600 F/2 hr AFTER Wire-EDM

T

- **NO T/L strip** = NO new L distortion after aging
- **T/L strip** REVERSED direction & lower L Edge finger distortion; NO other distortion
- T = NO distortion after aging

Wire-EDM Test

- **Detects only large & asymmetrical stress profiles**
- **Does NOT predict aging distortion**

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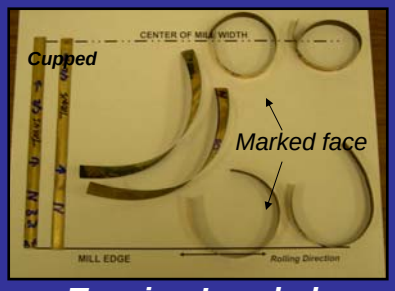
Etch-to-1/2 Thickness Test Results (I)

UNAGED Alloy 25 ½ Hard Strip

NOT T/L



Tension Leveled

- **NOT T/L** – negligible distortion
- **T/L --** HIGH/VARIABLE distortion = through-t gradient (L)
- NO (T) stress gradient in UNAGED strip

Regions of TENSILE residual stress contract on etching – ends curl toward the original TENSILE location

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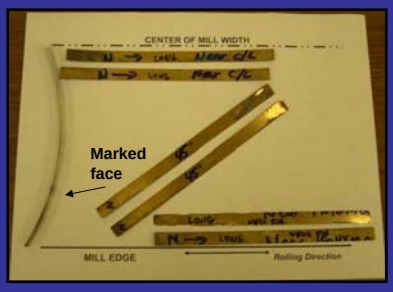
Etch Test Results (II)

MILL HARDENED Alloy 190 & Brush 60 Strip

C17200: Alloy 190 XHM



C17460: Brush 60 HT

- Similar distortion in both Alloy 190 & Brush 60
  - Minor to moderate COIL SET, CROSS BOW & Twist
  - *Opposite curvatures* L vs. T
- Cross Bow → TRANSVERSE stress gradient in MILL HARDENED strip [NOT PRESENT IN UNAGED STRIP]

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Residual Stress -- Distortion *Correlation*?

Stamping & Aging Distortion in Connector Alloy Strip

- **NO REFERENCES** on stamped/aged part distortion vs. stress in strip
- Single ref. to **Etch Test** distortion vs. various stress profiles
- INCONCLUSIVE **BiTS customer trial** with stamped & aged Alloy 25 parts
  - Stress profile UNCHANGED by **Stretch Bend Leveling (SBL)**
  - NO EFFECT of **SBL** on **parts** dimension variation
  - **AGE HARDENING** (+/- SBL) REDUCED parts variation
- *More BiTS customer trials planned*

NO "smoking gun"

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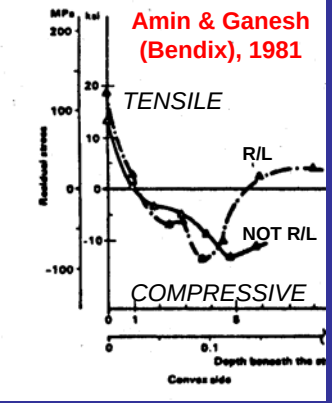
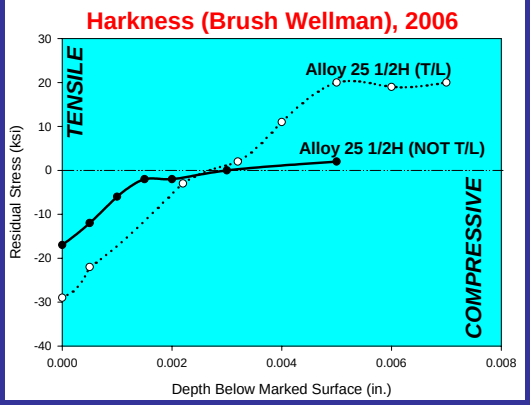
Cu-Be Test Results vs. Literature (I)

UNAGED Alloy 25 ½ H, "XRD -- Then & Now"





- 1981: **TENSILE** surface stress [Supplier unknown]
- 2006: **COMPRESSIVE** surface stress [BW mat'l]
- Rolling practice change or supplier difference?

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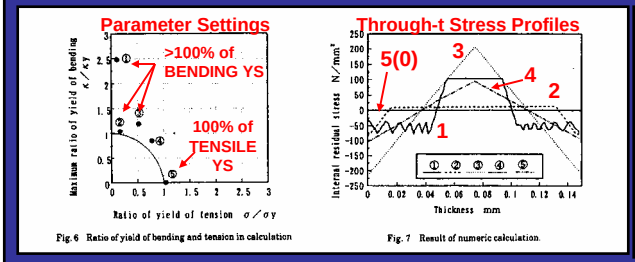
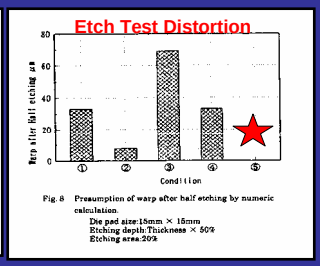
Cu-Be Test Results vs. Literature (II)

XRD Stress Profile & ETCH TEST DISTORTION vs. Tension Leveling Practice in Copper Alloy Strip

Ref.: Mitani, *et al*. (Furukawa Electric), 1999





T/L Parameters:

(1) Mostly BENDING

(2-4) Bend + Stretch

(5) Pure STRETCH

- Settings (#2-4) = consistent with 2006 T/L Cu-Be profiles
- NO T/L = not reported

- All STRETCH (#5) = NO distortion → **ZERO stress**
- (#3) ~ 2006 T/L Cu-Be

YIELDING IN *PURE STRETCHING* GIVES "STRESS-FREE" STRIP

Cu-Be Test Results vs. Literature (III)

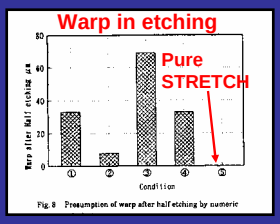
ETCH TEST vs. Stretch Bend Leveling in C7025 Strip

2006 Alloy 25 (T/L)

Falls between Ungerer SBL extremes

Ref.: Ungerer, 1995 [maker of SBL equipment]

Cu alloy (T/L or SBL)
Ref.: Mitani, 1999



CONFLICTING CONCLUSIONS ON "BEST" MECHANICAL STRESS RELIEF?

OR IS YIELDING IN EITHER STRAIN MODE THE ANSWER?

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Conclusions (I)

- Residual stresses: non-uniform deformation
- Residual stress control
  - Cold rolling practice
  - Mechanical stress relief (Tension Level or SBL)
  - Thermal stress relief
- Residual stress tests
  - **XRD** = quantitative surface stress distribution & through-t stress profile
  - **Wire-EDM** = insensitive & does not predict age distortion
  - **Etch-to-1/2 Thickness** = relative indication of through-t stress distribution

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Conclusions (II)

- **"Baseline" stresses in today's Cu-Be strip**
  - Surface **COMPRESSIVE** stresses in ALL Cu-Be (good)
  - Through-t stress profiles in **unaged** strip change to ZERO, then slightly TENSILE with depth
  - **Tension Leveling** → surface residual stress MORE COMPRESSIVE; mid-plane MORE TENSILE
    - **T/L = LESS UNIFORM surface stress**
  - **Stretch Bend Leveling** → apparently have not yet achieved **EFFECTIVE** mechanical stress relief
  - **Aging of Alloy 25 (600 F/2 hr)**
    - Surface stress = MORE COMPRESSIVE (NOT T/L), LESS COMPRESSIVE (T/L) … ½ Hard
    - Stress profile approaches ZERO (NOT T/L) … Hard
      - **Aging imparts some "thermal stress relief"**

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Conclusions (III)

- **Cu-Be XRD & Etch Test results vs. literature**
  - Alloy 25 stress profile = OPPOSITE "sign" of 1981 data
  - T/L Alloy 25 stress profile = consistent with literature on strip T/L with bend + stretch < YS of both strain modes
  - T/L Alloy 25 strip = Etch Test distortion consistent with literature
  - **Apparently conflicting conclusions on "best" MECHANICAL STRESS RELIEF practice**
- **NO correlation (yet) of BiTS connector distortion with a known stress distribution**
  - **No literature references**
  - **Initial Alloy 25 BiTS customer trial INCONCLUSIVE**
- **"Best" residual stress distribution for BiTS strip performance remains undefined**

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Future Work

- **IMPLEMENT cost-effective residual stress test**
  - **Etch Test** = Process development & inspection
  - **XRD** = R & D tool
- **CONFIRM residual stress -- distortion correlation in stamped & aged BiTS parts**
  - More “discriminating” BiTS customer trial(s)
- **DEVELOP a proprietary process to make BiTS strip with a preferred residual stress distribution for dimension stability as-stamped & after age hardening**
  - Guide development by residual stress testing

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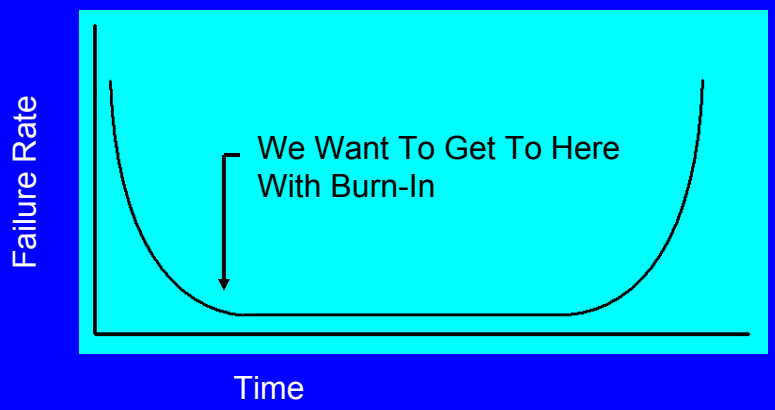
Socket and Heat Sink Considerations in High Power Burn-In

John McElreath

MICRO CONTROL COMPANY

2007 Burn-in and Test Socket Workshop

Overview – Bath Tub Curve



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Burn-In Example

Desired Burn-In Temp =150 Degrees C
No Individual Temperature Control
Device Power Plus or Minus 40%
Oven Airflow Plus or Minus 30%
Low Temperature Device = 135.8
High Temperature Device = 167.2

Low Temperature Device Will Take 4.14 Times As Long to Burn-In

Using Acceleration Factor as defined in A.T.& T. Reliability Manual: Klinger, Nakada, Menendez

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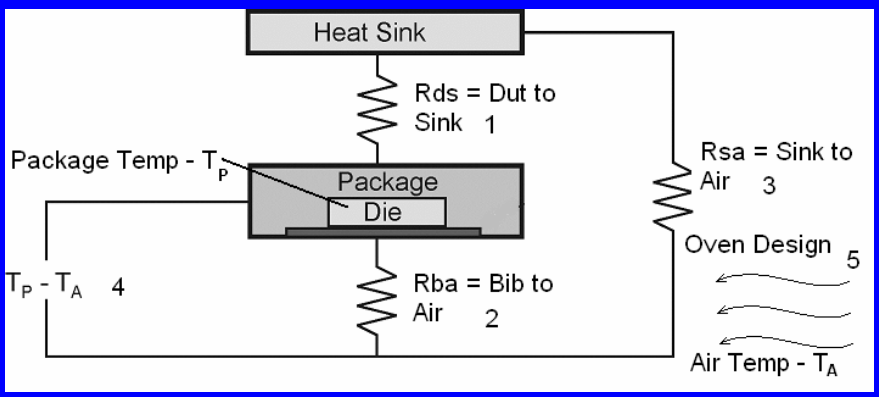
What Affects the Burn-In Temperature ?

Thermal Schematic Representation of Factors to be Addressed



While a major factor - Resistance From Die to Package is not part of this discussion.

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Interface Factors Affecting Burn-In

1. Interface Selection and Issues - Rds
2. Heat Flow Through BIB
3. HeatSink Considerations
4. Temperature Measurement
5. Burn-In Chamber Layout Considerations

- Conclusion

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Interface Resistance Dependant On Both the Heat Sink and DUT:

- Interface Materials
- Flatness
- Force Applied
- Force Centrality
- Size
- Foreign Particles

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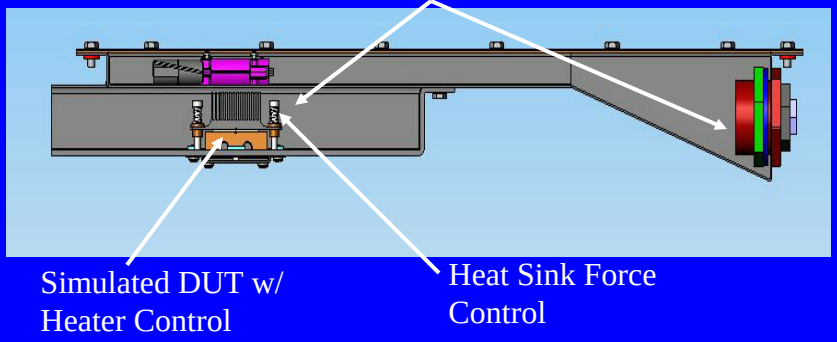
Interface Material Testing



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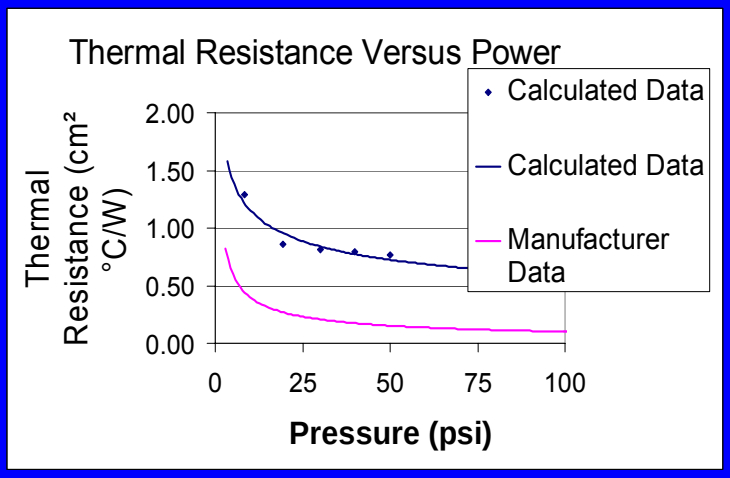
Interface Materials



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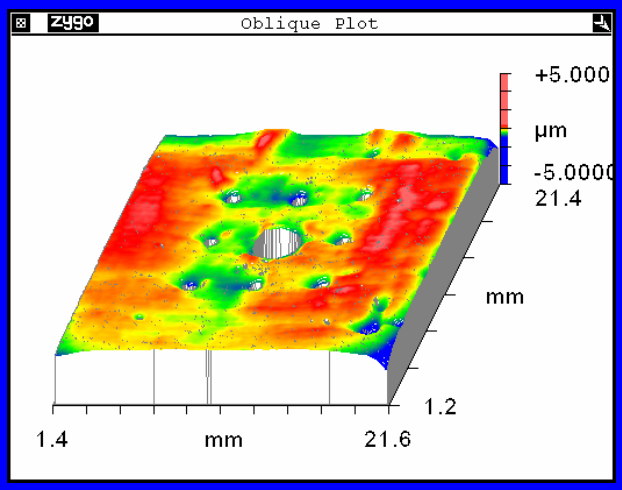
Flatness and Flatness Measurement



Lap Thermal Heads to:

0.5 Microns

Use Bearing Analysis Statistics to Pass Thermal Heads.

Sink to DUT Resistances =

0.1 ºC / W on 22x22 mm head at 10psi interface pressure

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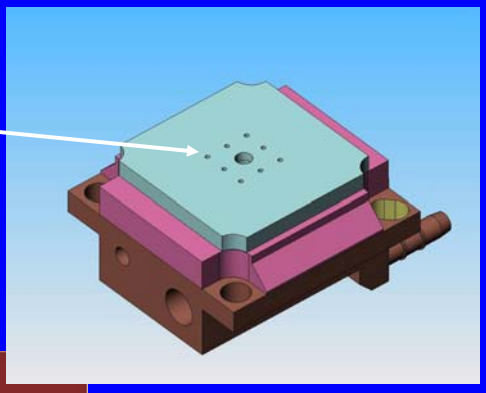
Injected Interface Material

- Can introduce a interface material via injection holes
- e.g. – Helium's Thermal Conductivity is 6x Air



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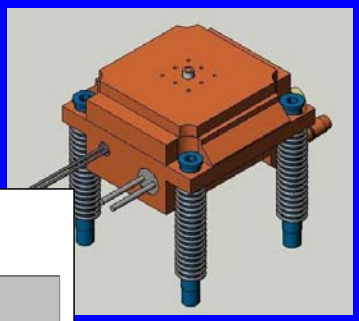
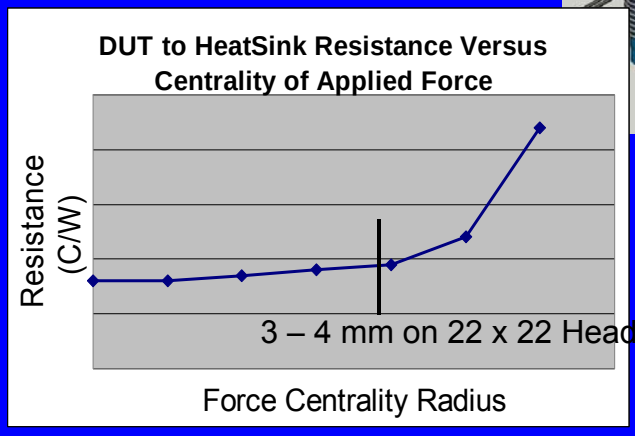
Force Centrality





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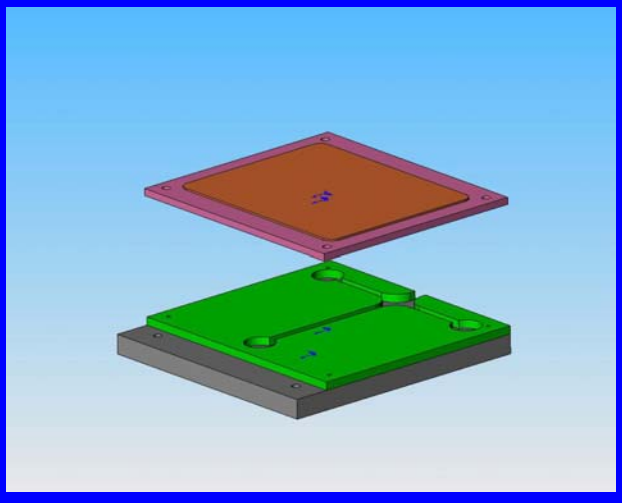
Force Centrality Measurement



Make a Simulated DUT with Strain Gauges to be able to measure the Force Centrality

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BIB Design Factors Affecting Burn-In

1. Interface Selection and Issues
2. Heat Flow Through BIB - Rba
3. HeatSink Considerations
4. Temperature Measurement
5. Burn-In Chamber Layout Considerations

- Conclusion

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Typical BIB to Air Resistance Values for Various Pin Count Devices

- 208 Pins ~ 11 ºC/W
- 1000 Pins ~ 6 ºC/W
- 1500 Pins ~ 3 ºC/W
- 2000 Pins ~ 1.5 - 2 ºC/W
- With Tdut – Tair = 140ºC on a 2000 pin Device, Approx. 80 Watts may go into BIB

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BIB Backer Treatments

Install temperature sensors on the BIB to monitor BIB Temperature

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HeatSink Factors Affecting Burn-In

1. Interface Selection and Issues
2. Heat Flow Through BIB
3. HeatSink Considerations - Rsa
4. Temperature Measurement
5. Burn-In Chamber Layout Considerations

- Conclusion

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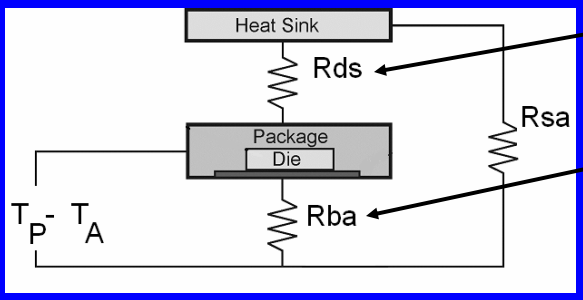
Steps to design a HeatSink

- Determine Device Minimum and Maximum Power
- Using Max Power - Determine DUT to Air Resistance Required for Air Temp and Burn-in Temp ($R_T=\Delta T/Q$)



Rds from testing or data sheets

Rba from experience or testing

- Rt = (Rds+Rsa)*Rba / (Rds + Rsa + Rba)

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Design Steps Cont'd

- Determine Rsa required
- Using chamber or Socket air flow data, Design a HeatSink to meet this requirement. **Don't Over-design**. Undertemps the Biggest Problem.
- Check DUT at low end of power tolerance with HeatSink performance.
- Is a heater req'd?
  - Verify Chamber can source the required power.
  - Heater placement critical to ensure heat goes into the DUT, not up into the air.
  - Cartridge heater easier to get heat down near the DUT than a foil heater.

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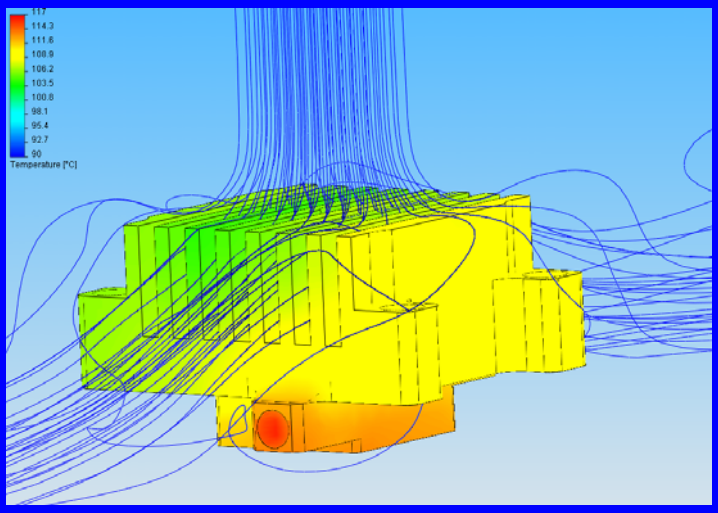
CFD of the Proposed Design



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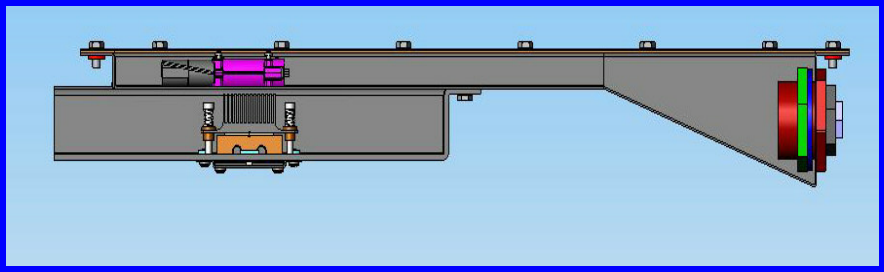
Bench Top Analysis of HeatSink Performance



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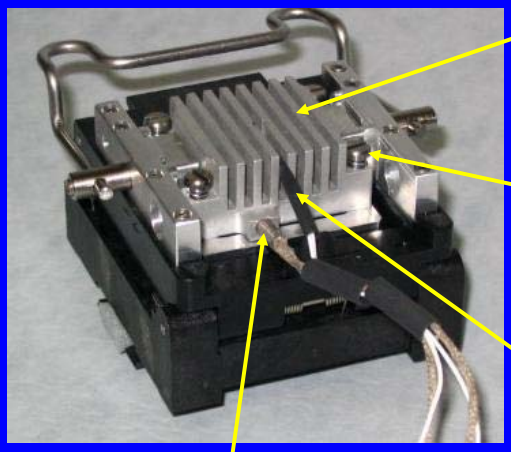
Final HeatSink Design



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Temperature Measurement Factors Affecting Burn-In

1. Interface Selection and Issues
2. Heat Flow Through BIB
3. HeatSink Considerations
4. Temperature Measurement (T1-T2)
5. Burn-In Chamber Layout Considerations

- Conclusion

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Temperature Sensing

Need to consider:

- External Sensor or Internal Diode
- Accuracy
- Size of Sensor
- Flatness of Sensor
- Cost of Sensor

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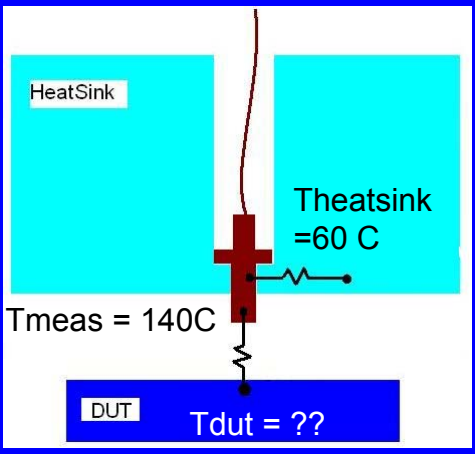
Temperature Measurement Correction



The larger the temperature difference (Theatsink – Tdut) the greater the error.

Using a calibration fixture – determine correction factor such that :

Tdut = Tmeas +

CF * (Tmeas – Tsink)

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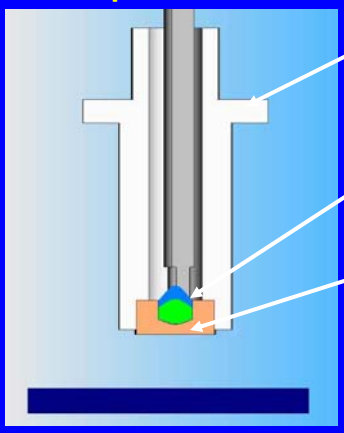
Temperature Sensor Issues



Insulating Sleeve – Need to measure the DUT, not the Heatsink

How Big is the Blob – Solder or Glue?

How Flat is the Sensor?

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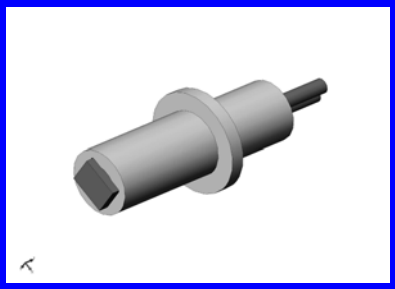
RTD DUT Temperature Sensor

Advantages:

1. Can read a voltage for direct temperature measurement. (No cold junction compensation).
2. Can use stranded wires. No strain relief.

Disadvantages:

1. Repeatability issue. Non-Repeatable contact Resistance.
2. Fragile. (Very thin ceramic.)
3. Fairly high chip to ceramic thermal resistance.
4. Higher cost.



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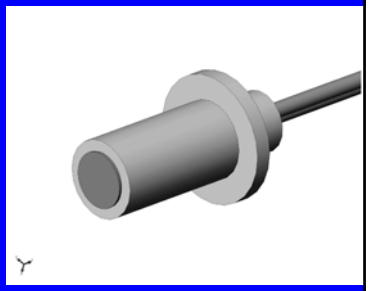
Thermocouple DUT Temperature Sensor

Advantages:

1. Low cost.
2. Durable. (Nickel plated copper.)
3. Low chip to copper thermal resistance.
4. Repeatable. (Machined compliant copper surface and low thermal resistance.)
5. Fairly accurate.

Disadvantages:

1. Need cold junction compensation
2. Solid wires, need strain relief.



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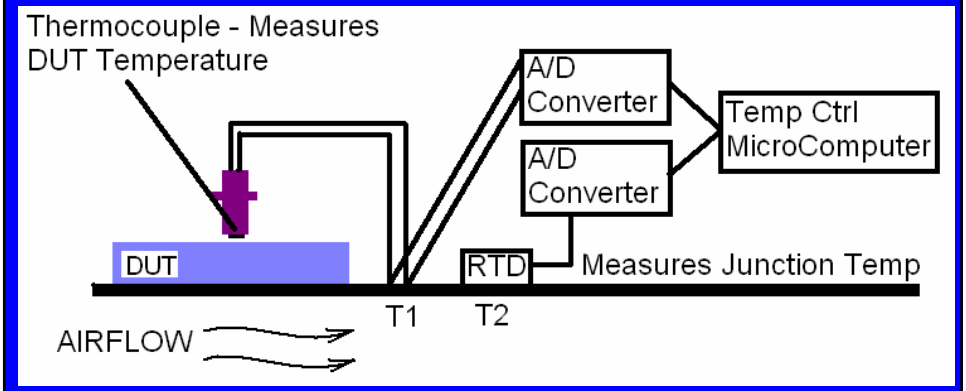
Cold Junction Compensation



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Chamber Layout Factors Affecting Burn-In

1. Interface Selection and Issues
2. Heat Flow Through BIB
3. HeatSink Considerations
4. Temperature Measurement
5. Burn-In Chamber Layout Considerations
- Conclusion

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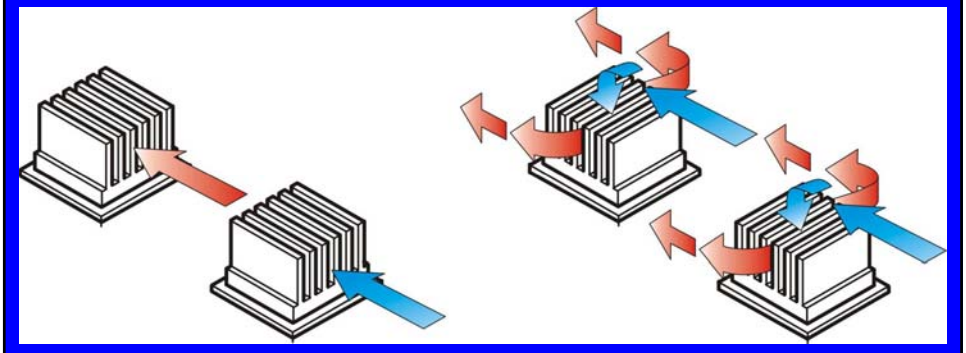
HeatSink Orientation



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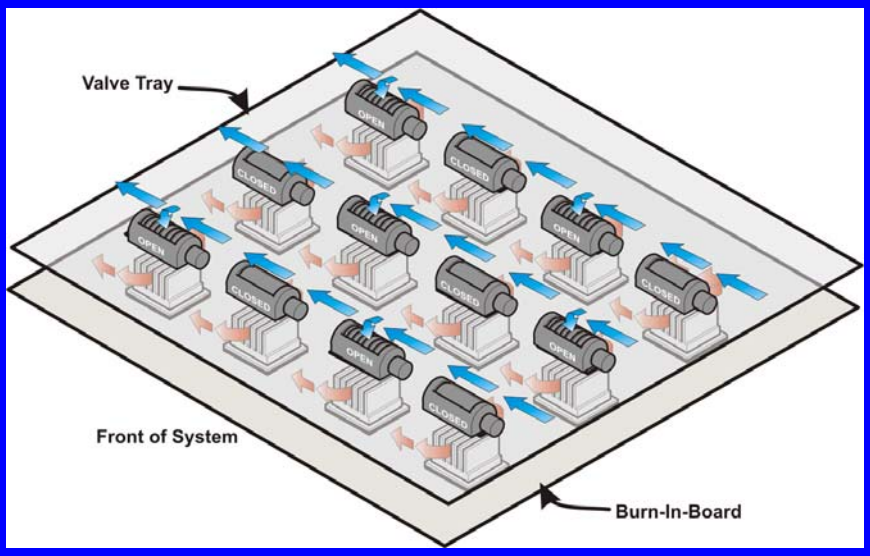
Per Device Air Flow Control



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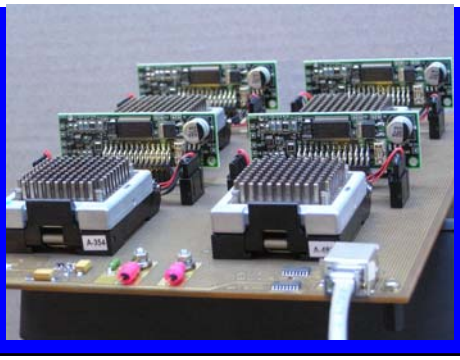
Burn-In Temperature Variation Versus Power and Air Flow Fluctuation

	-30% Air Flow	Nominal Air Flow	+30% Air Flow
+40% Power	159.3	152.9	148.9
Nominal Power	148.1	143.5 Deg. C	140.6
-40% Power	136.9	134.1	132.4



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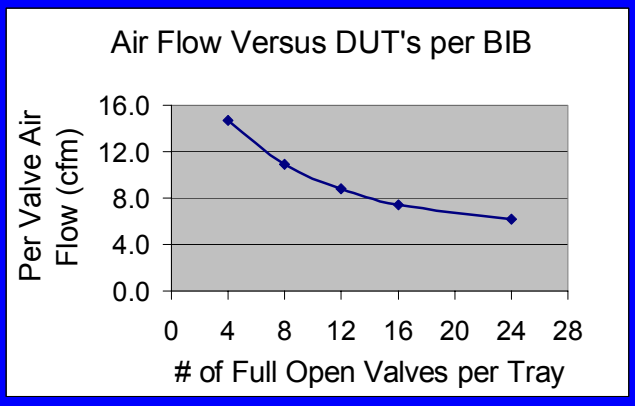
Chamber Specific Airflow Considerations



Chamber Airflow Characteristics Needed Whether Air Flow is Controlled via a Socket Level Fan or Chamber Tray

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Conclusion

- Determining how to burn-in a Device during the design phases, may create an easier to test component.
- Fully understanding the chamber specific characteristics will yield the most effective burn-in solution. What does the Thermal Circuit look like?
- Developing tools for evaluating properties of materials, verifying designs, and calibrating measurement tools will get all the Devices to the bottom of the Bathtub.

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Determining Thermal Resistance Characteristics Without a Power Sensor

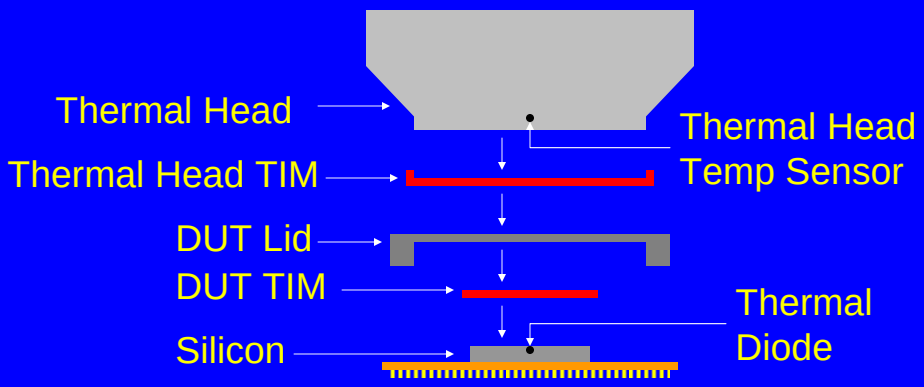
2007 Burn-in and Test Socket Workshop
March 12, 2007

Trent Johnson, AMD
Jerry Tustaniwskyj, Delta Design

Agenda

- Thermal Resistance Overview
- Problem Statement
- Two Methodologies Tried by AMD
- One Methodology Tried by Delta Design
- Results
- Summary

Thermal Stack-Up



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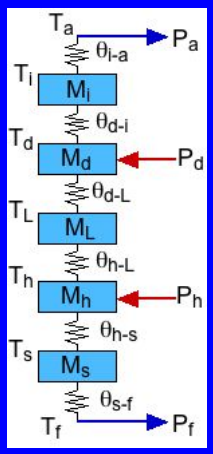
Thermal Stack-Up - Lumped Mass Approximation



- T_a - ambient temperature
- T_i - "lumped" intermediate temp. (substrate, socket, etc)
- T_d - DUT (chip) temperature
- T_L - DUT lid temperature
- T_h - heater temperature
- T_s - heat sink temperature
- T_f - cooling fluid temperature
- P_d - DUT power
- P_h - heater power
- P_f - power removed by cooling fluid
- M_x - thermal mass at T_x
- θ_{x-y} - thermal resistance between T_x and T_y

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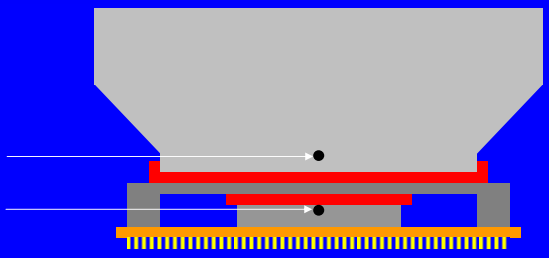
Traditional Thermal Resistance Measurement

$$T_{resist} = \frac{\Delta Temperature}{\Delta Power}$$

Measure:
- Power Output
- Temperature



$$T_{resist_{total}} = T_{resist_{TIM1}} + T_{resist_{LID}} + T_{resist_{TIM2}}$$

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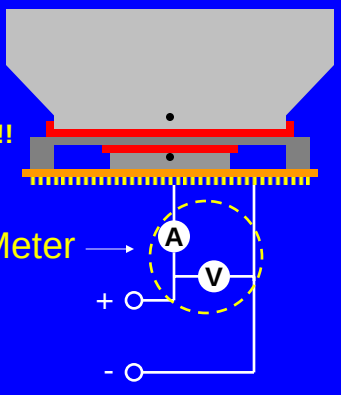
Traditional Thermal Resistance Measurement

- T_h measured by inexpensive temperature sensor
- T_d measured by on-die thermal diode
- P_d measured by DUT power meter
  - dynamic DUT power swings are hard to measure
  - Accurate power meters are expensive!!



$$T_{resist} = \frac{T_d - T_h}{p_d}$$

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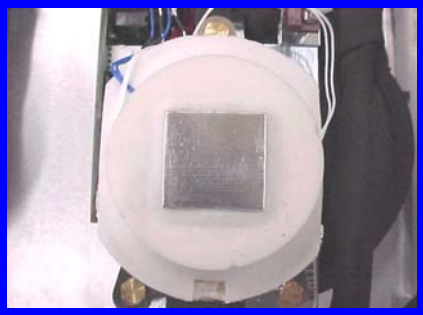
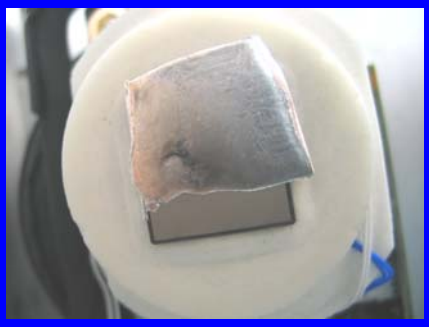
Problem Statement

Good





Bad

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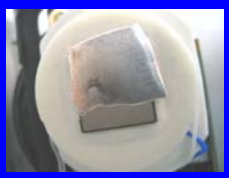
Problem Statement

- Need to detect poor thermal interfaces on a large scale of thermal heads
- Cannot afford an accurate power meter for all thermal heads

Task:

- Observe symptoms of poor T_{resist}
- Try to fit ideal behavior into a model

Good 

Bad 

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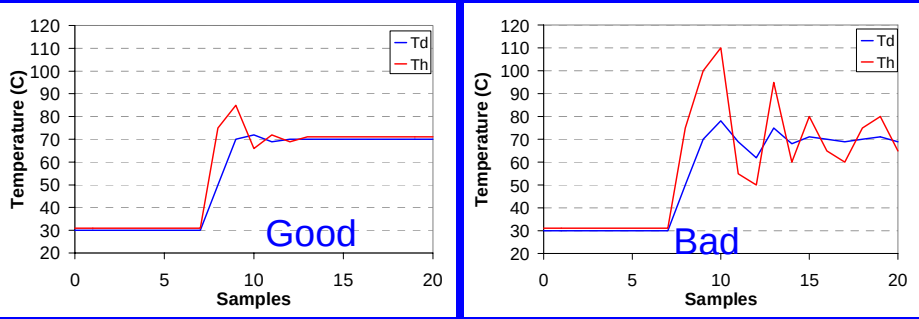
First Method

- Input a step function in diode control & observe response of Thermal head
- Theoretical Response:



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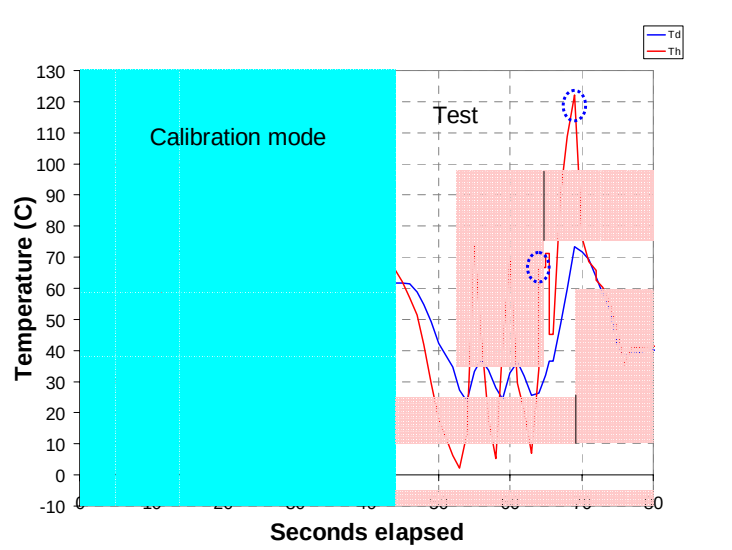
First Method: Actual response



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First Method (results)

- Slow and unpredictable sample rate
  - Sample noise may cause false passes or false fails
- Sampled ringing and overshoots do not match mathematical models very well
- Thermal control response varies between thermal heads
  - Variations in system components causes some heads to ring or overshoot naturally
  - Test depends heavily on refrigerant level
- Repeatability is terrible
  - Only the worst of the worst are caught consistently

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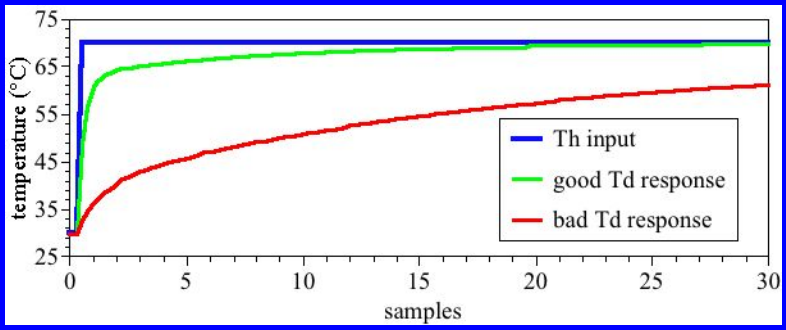
Second Method

- Input a step function in heater control & observe response of Thermal Diode
- Try to fit ideal behavior into a model
- Theoretical response:



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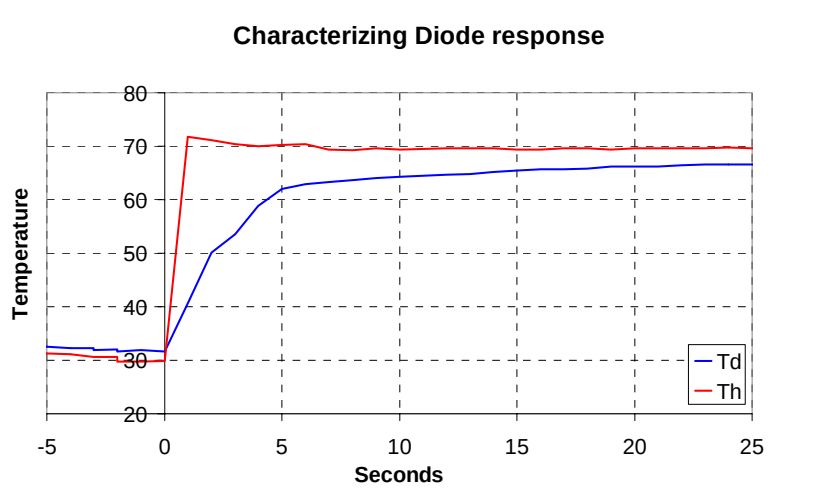
Second Method

- **Actual response:**



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Second Method (experimental results)

- Resulting curve fits the mathematical model:

$$T_d(t) \approx T_{d\infty} - C_1 e^{-t/\tau_1} - C_2 e^{-t/\tau_2}$$

- τ_1 & τ_2 are time constants that are functions of thermal resistance $\theta_{h\text{-}L}$ (TIM2)
- Limitations on correlation to $\theta_{h\text{-}L}$:
  - Slow sample rate and/or inconsistent sample period
  - τ_1 and τ_2 are also a function of TIM1 and interactions with ambient conditions
- Note that high current applications require low electrical resistance
  - $\Rightarrow$ low thermal resistance to ambient

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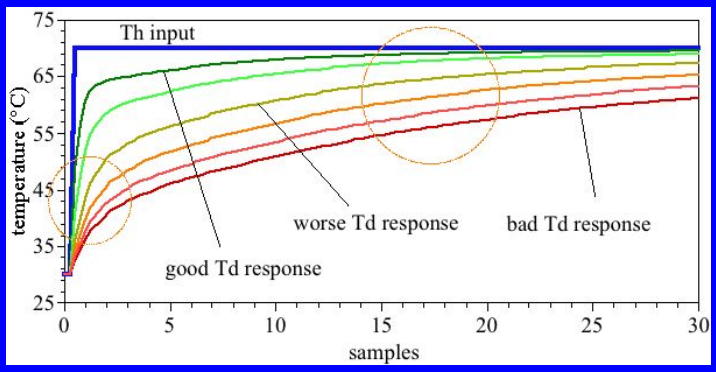
Second Method : observations

- Near the start of the ramp, good interfaces have higher slope than bad interfaces
- Near the end of the ramp, bad interfaces have higher slopes than good interfaces



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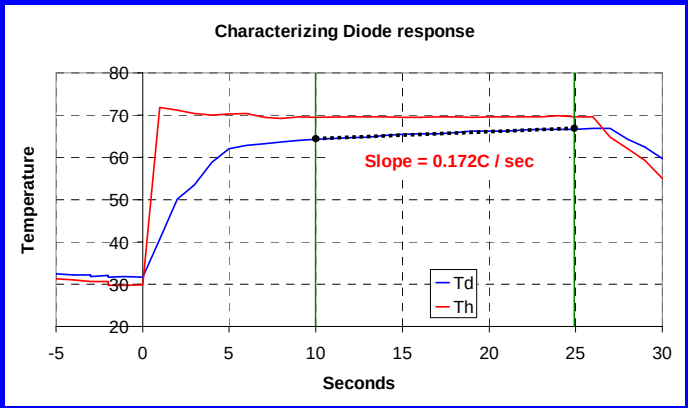
Second Method

- Set a metric as the slope between the 10 and 25 second marks



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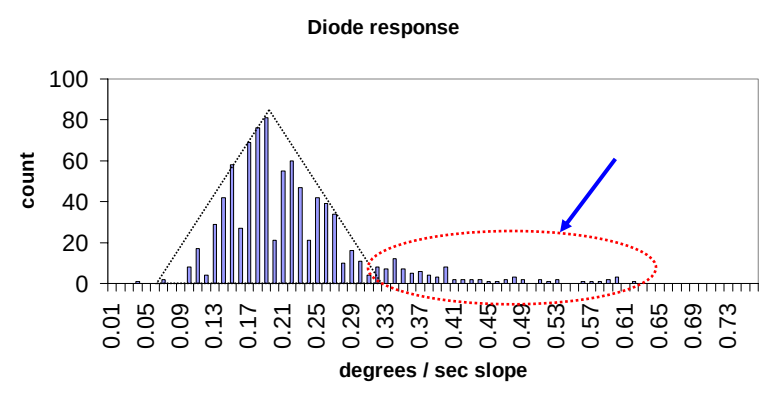
Second Method (wide deployment results)

- Histogram shows a normal distribution with a tail of abnormal results



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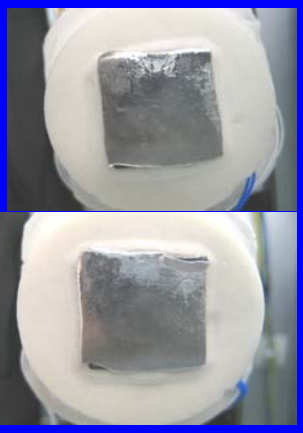
Second Method (wide deployment results)

Root Cause of Interfaces with high slope:

- Inadequate mating force
- Gimballing problems
- Deformed TIM
- Burned TIM



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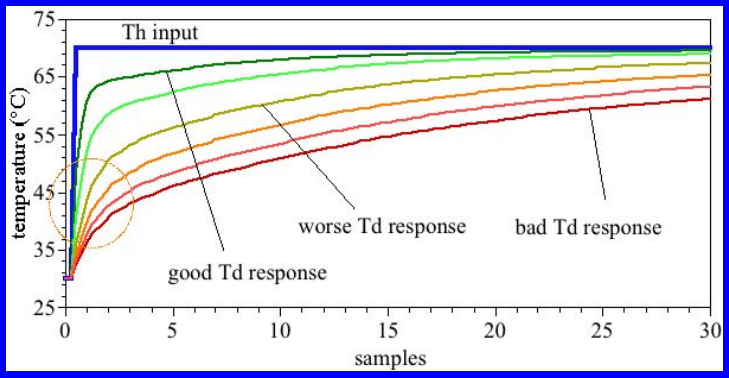
Third Method

- Near the start of the ramp, good interfaces have higher slope than bad interfaces
- DSP upgrades have enabled us to sample temperature faster



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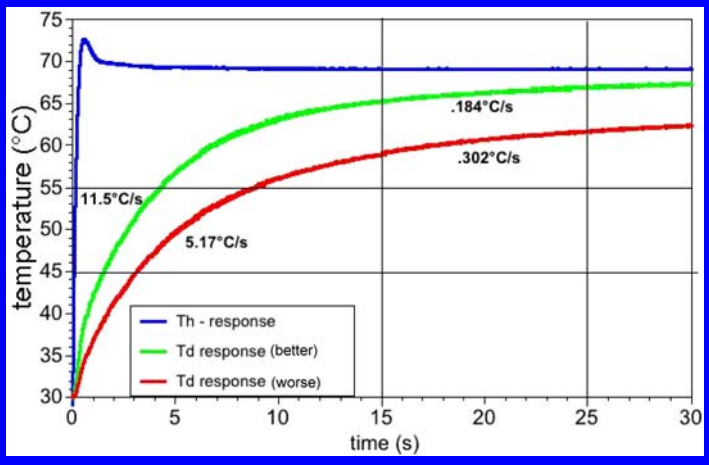
Third Method

- **Actual response:**



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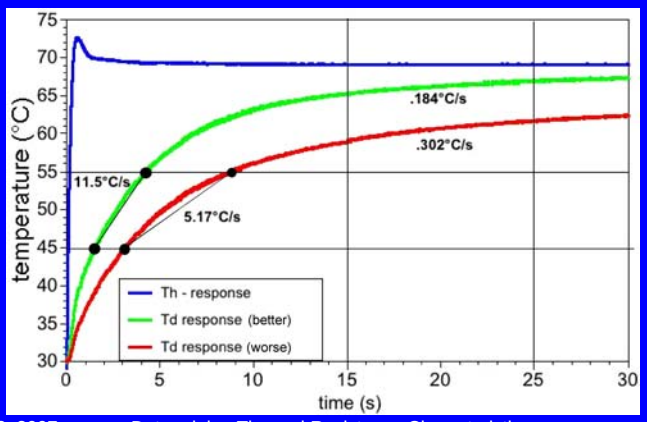
Third Method

- Set a metric to be the slope between the 45 and 55 degree marks



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Third Method

- Third method faster than second method
  - 5X or more when measuring a good interface
- Uses the same theory as the second method
- Good correlation with second method
  - Diverges somewhat for very good interfaces
- Faster sampling yields consistent results
- Less dependent on interactions with ambient
  - ⇒ better correlation with thermal resistance
  - ⇒ theoretically more accurate than second method

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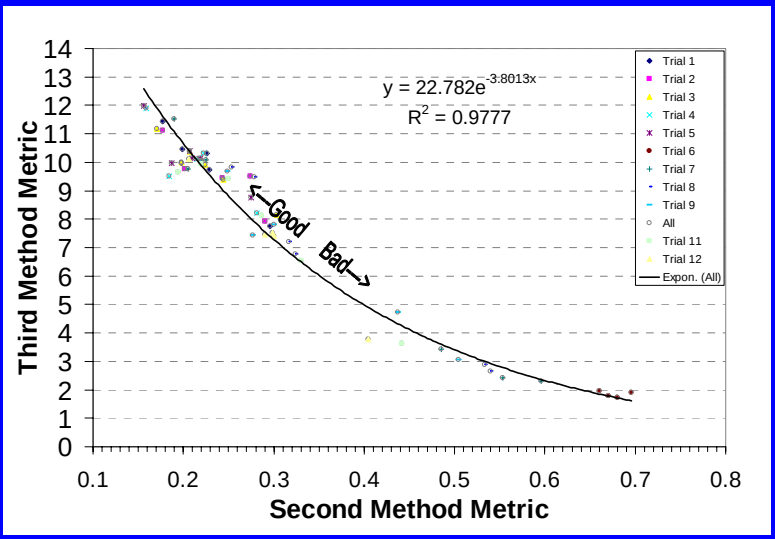
Correlation



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Comparison

	Method 1	Method 2	Method 3
Works	☒	☑	☑
Currently in use	☒	☑	☒
Most accurate	☒	?	?
Fastest	☒	☒	☑
Can work on all systems @ AMD	☒	☑	☒

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Method (2&3) Limitations

- Raw test results cannot easily differentiate between TIM1 & TIM2 outliers
  - Work in progress
- Some amount of sampling noise exists, but is minimal
- Correlation with thermal resistance possible but complicated by dependence on other factors
- Accuracy of either method not yet quantified

Summary

- We have developed two working metrics for determining thermal resistance without a power meter
- Statistical results confirm effectiveness of both tests
- Visual inspection confirms defects exist for test outliers