2007 Session 2

ARCHIVE 2007

SOCKET ANALYSIS AND CHARACTERIZATION METHODS

"Revolutionizing High-Speed Socket Test"

Michael de Bie
Exotest
Boris Coto, Rafiq Hussain
Advanced Micro Devices

"Understanding Impact of Burn-in Sockets on Fragile Semiconductor Packages Using Finite Element Analysis"

Prasanth Ambady, Keith Crowe, Hide Furukawa
Sensata Technologies

"Contact Resistance is Sexy Again"

Tim Swettlen, Morten Jensen
Intel Corporation

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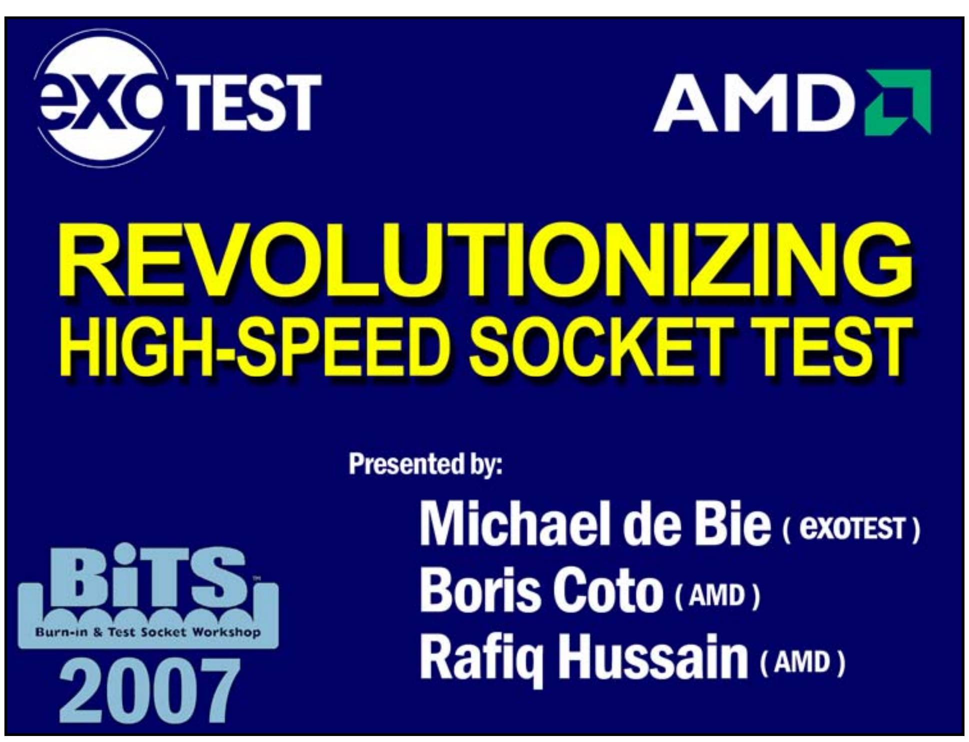
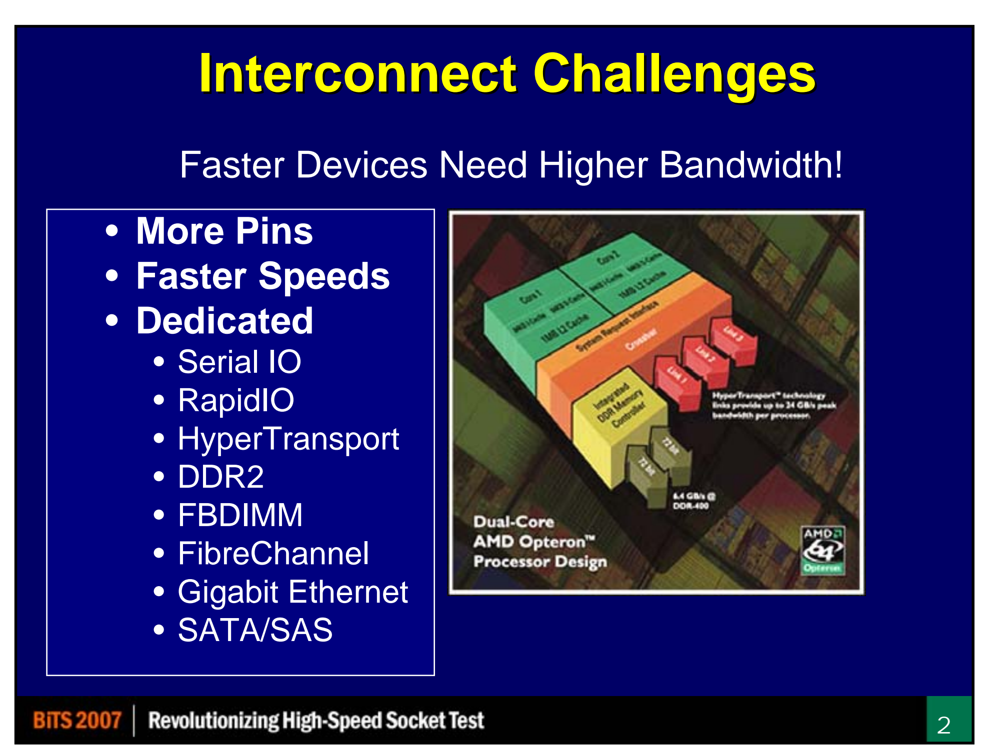

exoTEST
AMD
REVOLUTIONIZING
HIGH-SPEED SOCKET TEST
Presented by:
Michael de Bie (EXOTEST)
Boris Coto (AMD)
Rafiq Hussain (AMD)
BiTS
Burn-in & Test Socket Workshop
2007


Interconnect Challenges
Faster Devices Need Higher Bandwidth!
• More Pins
• Faster Speeds
• Dedicated
• Serial IO
• RapidIO
• HyperTransport
• DDR2
• FBDIMM
• FibreChannel
• Gigabit Ethernet
• SATA/SAS
Dual-Core
AMD Opteron™
Processor Design
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Got Enough Bandwidth?

Standard	Max Data Rate	Bandwidth Required
DDR2-533	1.066Gbps	2.132GHz
HyperTransport Consortium (1.0) & DDR2-800	1.6Gbps	3.2GHz
HyperTransport Consortium (2.0)	2.8Gbps	5.6GHz
HyperTransport Consortium (3.0)	5.2Gbps	10.4GHz
RapidIO	3.125Gbps	6.25GHz

- **Bandwidth is Important**
  - Allows sufficient headroom for 3rd and 4th harmonics
  - Reduces path impact on jitter

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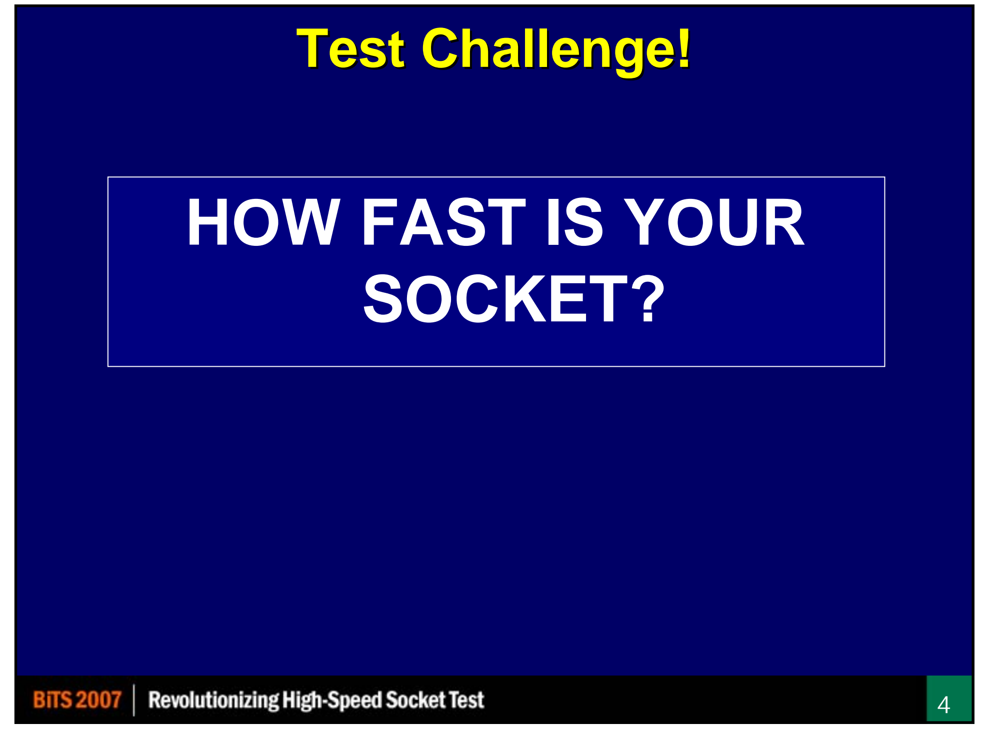

Old Way: *Opens & Shorts*

- Test for Open and Short conditions on each pin
  - Typical DC measurements of voltage and current
- Great for basic wiring and gross errors
- Will not detect Bandwidth or impedance problems

CONCLUSION:
Informative for gross errors, but won't catch other more critical errors

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Old Way: *Network Analyzer*

Shorted Die
SocketUnderTest

- Measuring Link Bandwidth Requires:
  - Network Analyzer for S21 parameters on each pin
  - Shorted die for round trip bandwidth
  - 500 measurements for 1000 pin device

CONCLUSION:
Great result, but impractical for most cases

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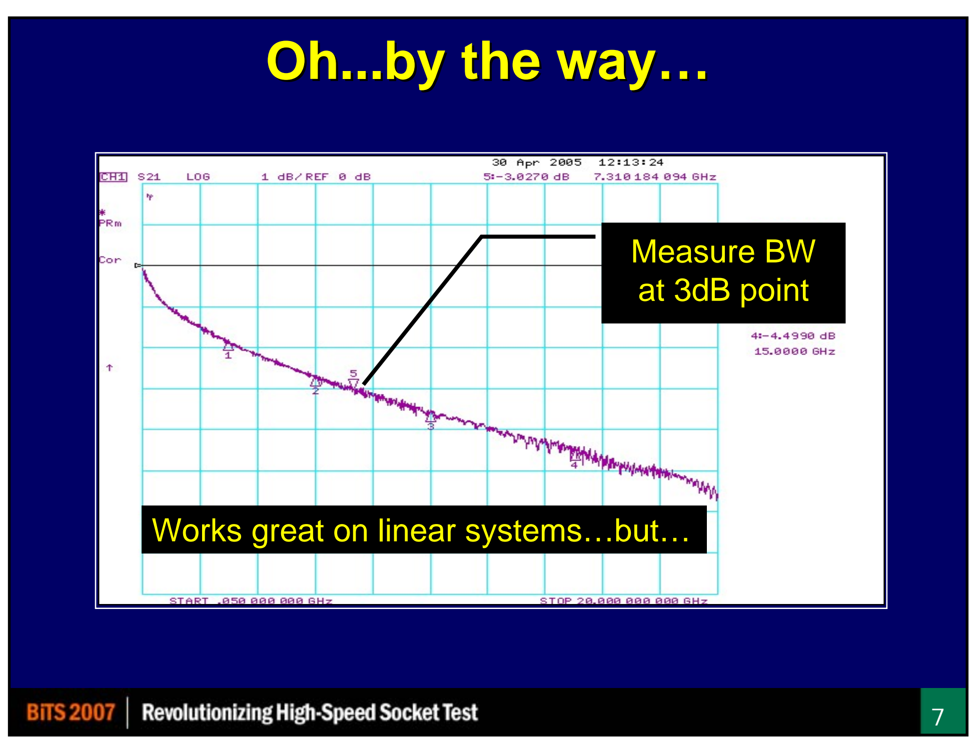
Oh...by the way…
30 Apr 2005 12:13:24
CH1 S21 LOG 1 dB/ REF 0 dB
5:-3.0270 dB 7.310 184 094 GHz
Measure BW
at 3dB point
4:-4.4990 dB
15.0000 GHz
Works great on linear systems…but…
START .050 000 000 GHz
STOP 20.000 000 000 GHz
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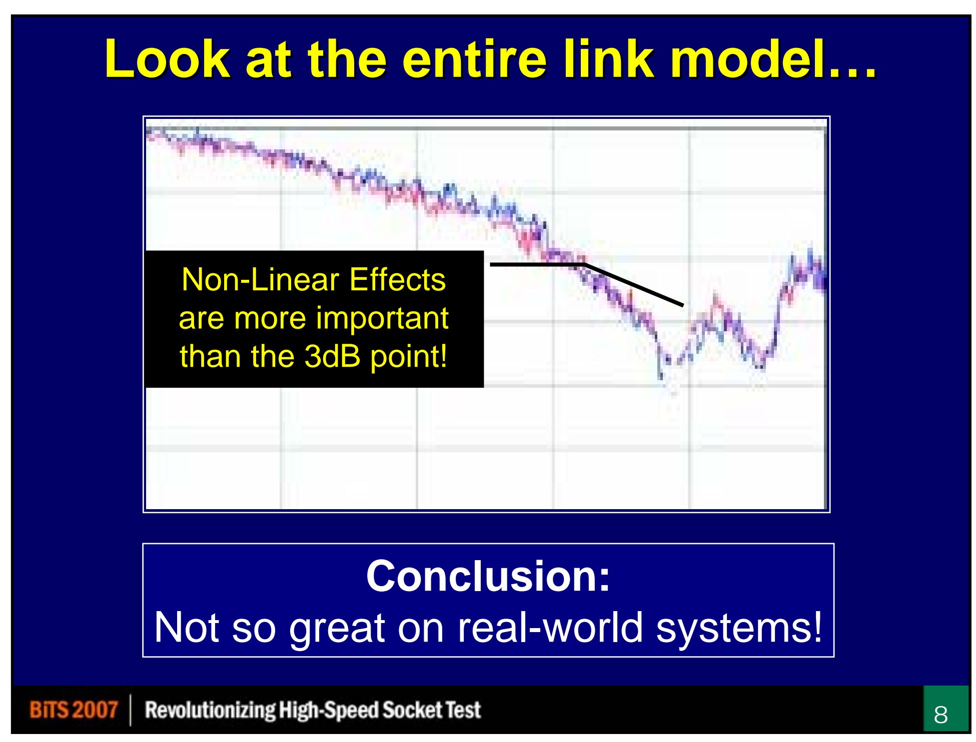
Look at the entire link model…
Non-Linear Effects
are more important
than the 3dB point!
Conclusion:
Not so great on real-world systems!
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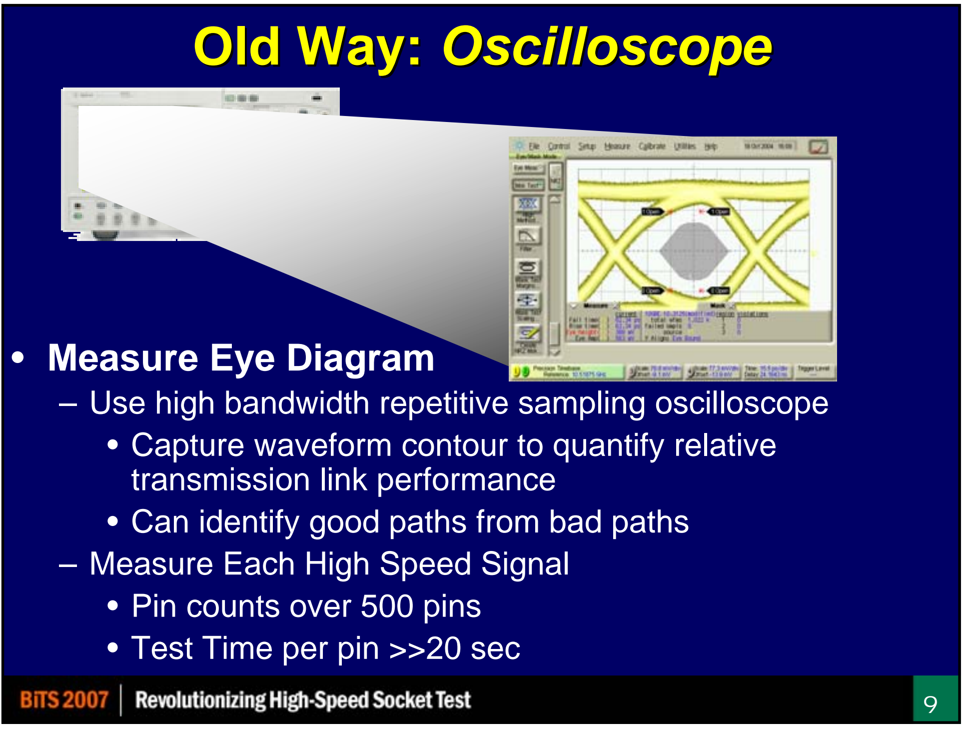
Old Way: Oscilloscope
• Measure Eye Diagram
– Use high bandwidth repetitive sampling oscilloscope
• Capture waveform contour to quantify relative transmission link performance
• Can identify good paths from bad paths
– Measure Each High Speed Signal
• Pin counts over 500 pins
• Test Time per pin >>20 sec
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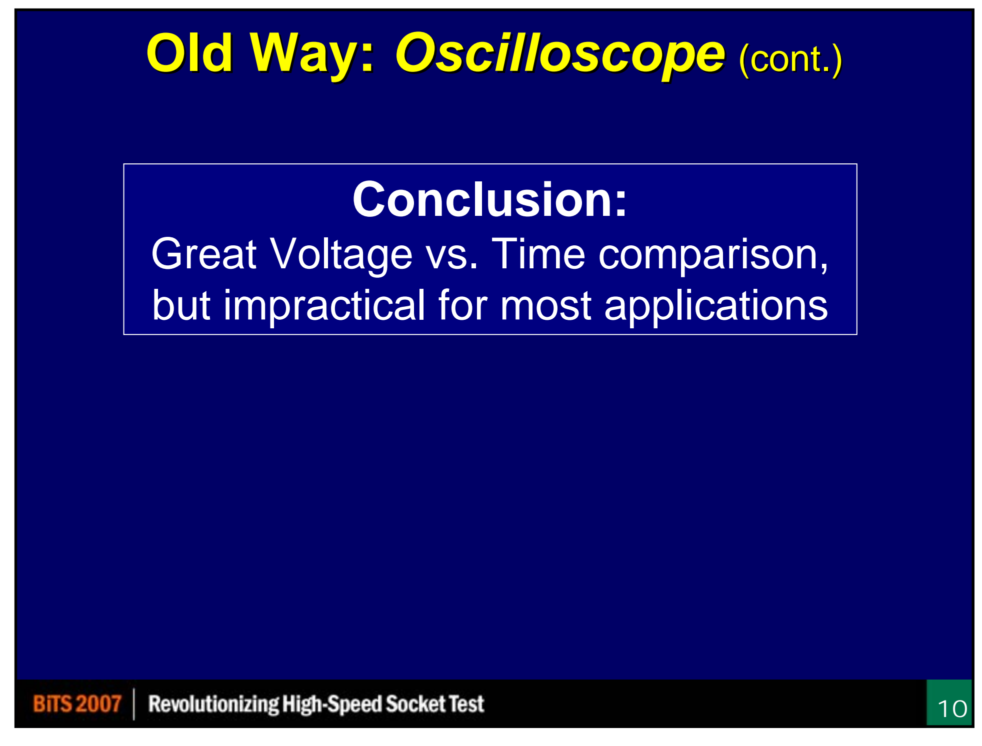
Old Way: Oscilloscope (cont.)
Conclusion:
Great Voltage vs. Time comparison,
but impractical for most applications
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Old Way: *TDR*

- Measure line length of each pin
  - Requires sampling oscilloscope and high bandwidth pulse generator
    - Determine length of each trace, including socket
    - Compare skew results to known good setup
- Measure each high speed signal

Conclusion:
TDR can find opens and shorts, but not effective for high bandwidth applications

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Old Way: *Software*

- Use bus protocol to predict pin failure by coding patterns and transmitting them onto the bus
- Can detect certain pin failures at speed
- In-system testing
- Drawbacks
  - Code intensive/Proprietary software
  - Some uncertainty determining a local or remote pin error
  - Limited signal pin coverage
  - Lack of testing capabilities defined in the protocols (ie. DDR2, HyperTransport)

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Risks of Current Methods

Open/Short Socket Tester	Not enough test coverage
Network Analyzer	Too time consuming
Oscilloscope	Too time consuming
TDR	Too time consuming
Software	Low pin coverage

Conclusion: Time to shift paradigms!

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Paradigm Shift

- What is needed:
  - Need to test as much as 500 pins for bandwidth
  - Need to test beyond 800MHz Bandwidth
  - Need to test reliability of socket in the development phase before production release
- Why?
  - Sockets begin to lose bandwidth over time from repetitive insertions and environmental breakdown
  - Lower bandwidth signal paths will reduce yield
  - Remove guess work from determining a failed socket in production
  - Reduce cost in socket development

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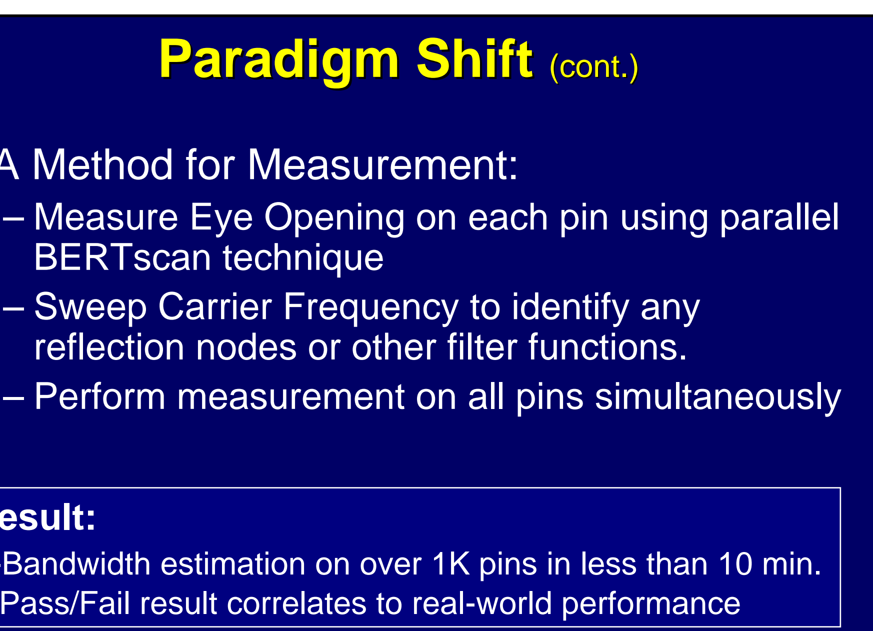
Paradigm Shift (cont.)
• A Method for Measurement:
– Measure Eye Opening on each pin using parallel BERTscan technique
– Sweep Carrier Frequency to identify any reflection nodes or other filter functions.
– Perform measurement on all pins simultaneously
Result:
-Bandwidth estimation on over 1K pins in less than 10 min.
-Pass/Fail result correlates to real-world performance
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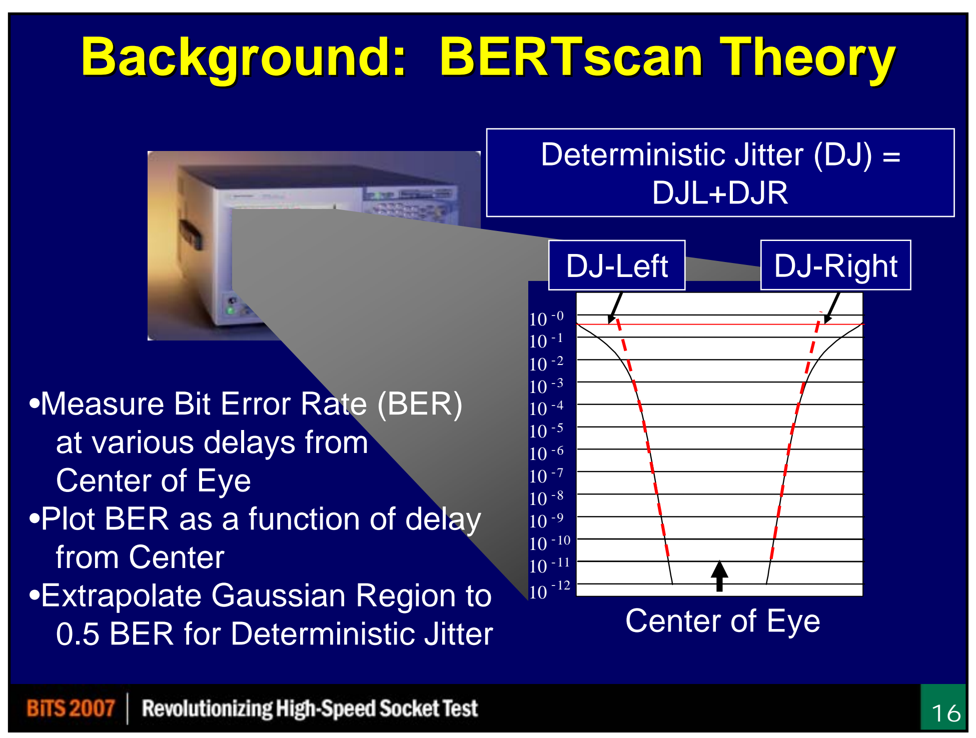
Background: BERTscan Theory
Deterministic Jitter (DJ) = DJL+DJR
DJ-Left
DJ-Right
10 -0
10 -1
10 -2
10 -3
10 -4
10 -5
10 -6
10 -7
10 -8
10 -9
10 -10
10 -11
10 -12
Center of Eye
•Measure Bit Error Rate (BER) at various delays from Center of Eye
•Plot BER as a function of delay from Center
•Extrapolate Gaussian Region to 0.5 BER for Deterministic Jitter
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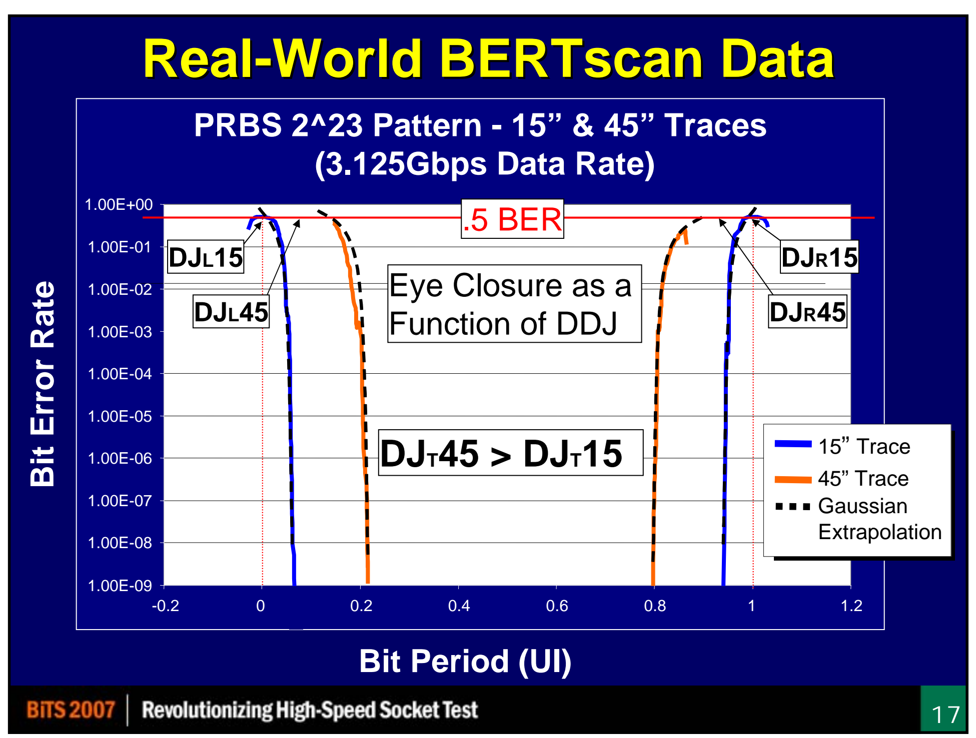
Real-World BERTscan Data



Bit Period (UI)

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BERTscan Graph Analysis

- Socket-induced DJ can be simulated by increasing the trace length
- These data show correlation between decreased bandwidth and increased DJ
- Left and Right DJ are measured at the intersection with .5BER
- Data-Dependent Jitter (DDJ) is the only component of DJ present in our system
- Random and Periodic Jitter are held constant
- Marginal socket continuity will be visible as increased DJ outside the known good range

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Conclusion

- Deterministic Jitter measured through socket quantifies Bandwidth Effect on real data patterns at data rate of target application
- No interpolation is needed
- Please contact the authors for additional data that was not available at press time.

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Understanding Impact of Burn-In Sockets on Fragile Semiconductor Packages using Finite Element Analysis

Burn-in & Test Socket Workshop
March 11-14, 2007

Prasanth Ambady
Keith Crowe
Hide Furukawa

Sensata Technologies
Attleboro, MA

REV 1.2

OVERVIEW

- Trends in semiconductor industry driving burn-in socket technology.
- Modeling complex systems- defining the environment and constraints of the package undergoing burn-in.
- Analysis using finite element computational tools.
- Interpretation of results and incorporation into design.

INTRODUCTION
•When America runs on bigger the better philosophy, our communication tools are getting ever smaller…….
1970's
1990's
TODAY
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BURN-IN CHALLENGES - SHRINKING SILICON AND PACKAGES
300~350 I/O, 1.00mm pitch BGA package
300~350 I/O, 0.50mm pitch BGA package
Packaging Trends:
•Extremely small and thin packages.
•High I/O count bumped and LGA.
• 0.65mm pitch and below.
•Bare die and POP style packages.
•Soft mold compound.
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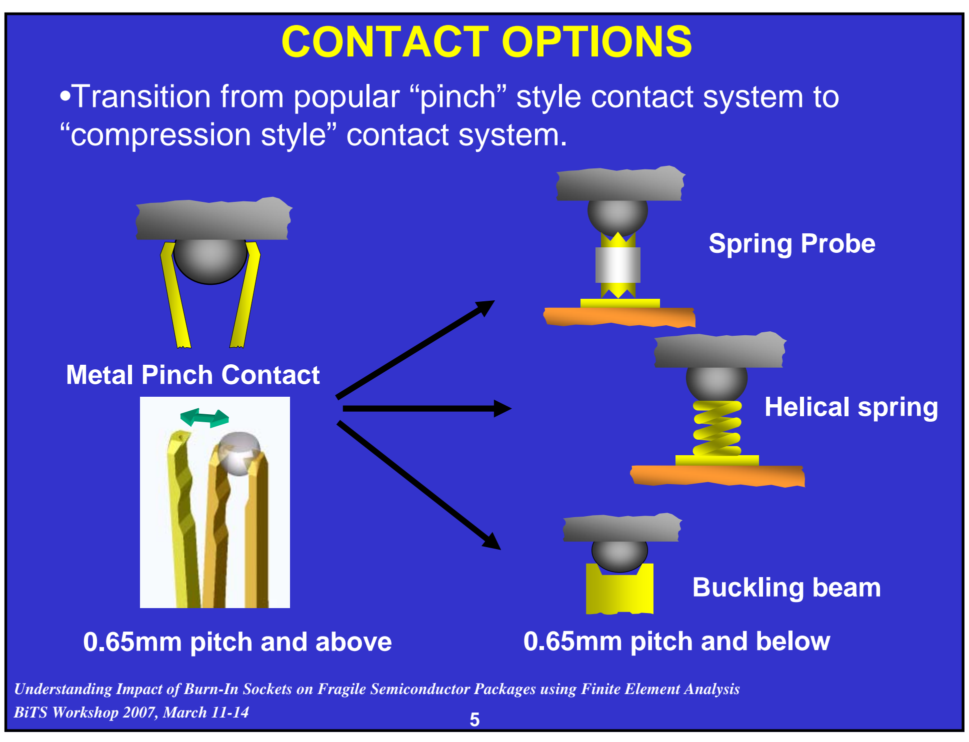
CONTACT OPTIONS
•Transition from popular "pinch" style contact system to "compression style" contact system.
Metal Pinch Contact
Spring Probe
Helical spring
Buckling beam
0.65mm pitch and above
0.65mm pitch and below
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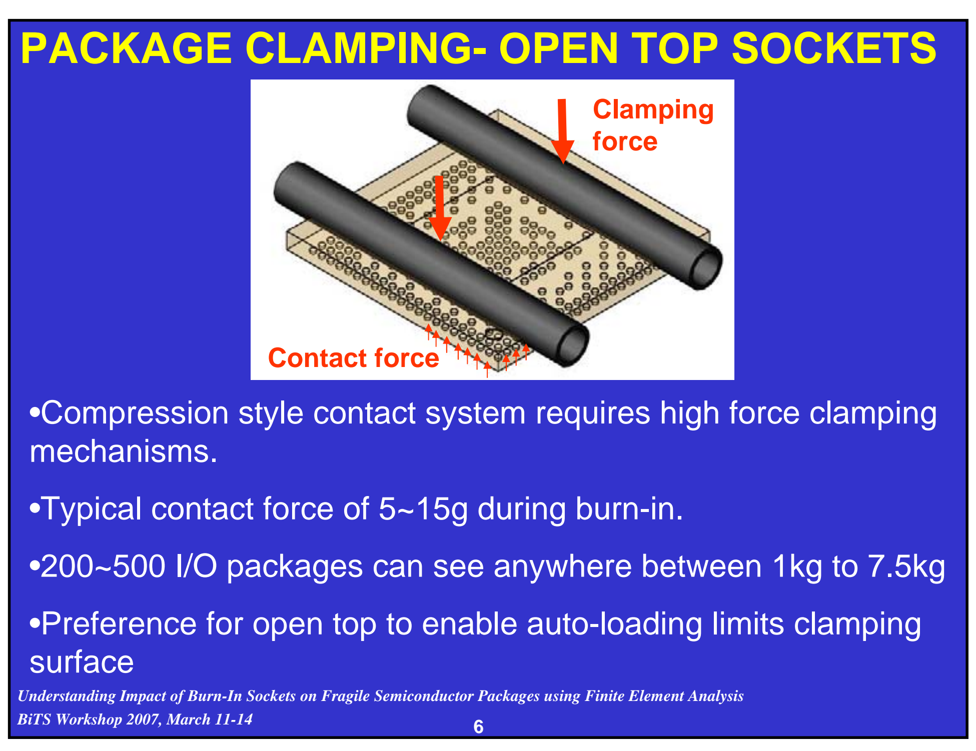
PACKAGE CLAMPING- OPEN TOP SOCKETS
Clamping force
Contact force
•Compression style contact system requires high force clamping mechanisms.
•Typical contact force of 5~15g during burn-in.
•200~500 I/O packages can see anywhere between 1kg to 7.5kg
•Preference for open top to enable auto-loading limits clamping surface
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UNDESIRABLE EFFECTS OF BURN-IN

- Burn-in is an elevated temperature, long duration process in which the package is undesirably stressed by the loadings of the clamps and large number of electrical contacts.
- These loadings can cause distortion of the package and stress the circuitry on silicon.

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UNDESIRABLE EFFECTS OF BURN-IN

- The extended duration of these conditions can cause continual deformation (creep) of the softer materials in the package like PCB, over mold compound etc., leading to possibly significant permanent change of shape of the package even when the high temperature and forces are removed.
- This condition can render the package useless.

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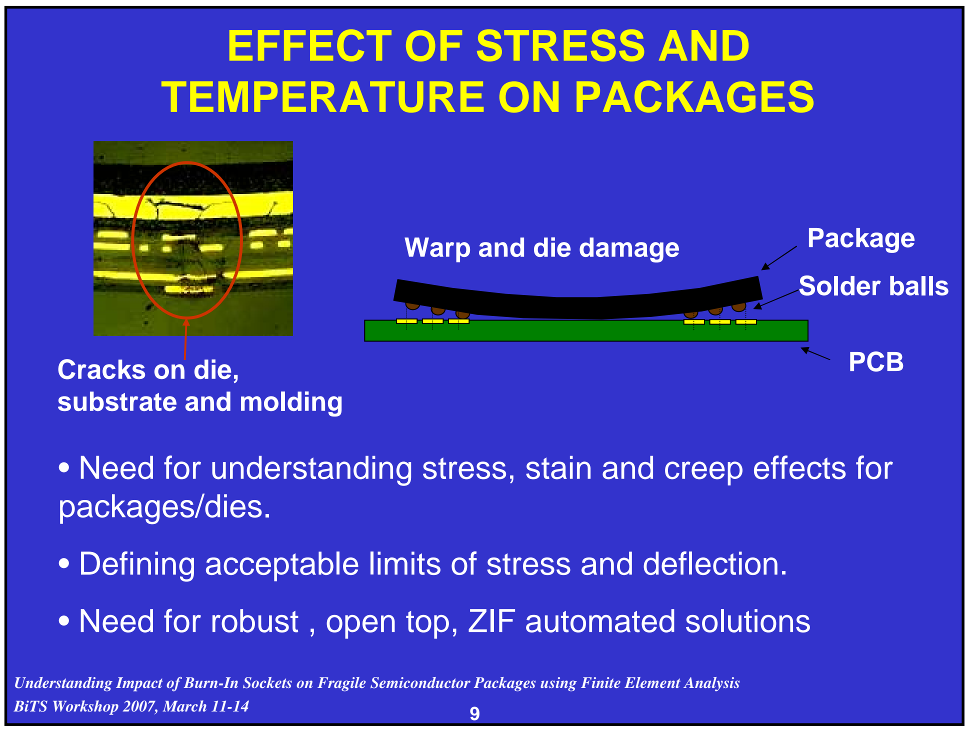

BURN-IN SOCKET REQUIREMENTS

- Temperature: Up To 150 C
- Life: Up to 10,000 Cycles
- Resistance : Less Than 1 ohm per pin
- Acceptable Capacitance & Inductance
- Auto Loading Capabilities
- Acceptable Witness Marks
- No Damage To Die Or Package During Burn-in

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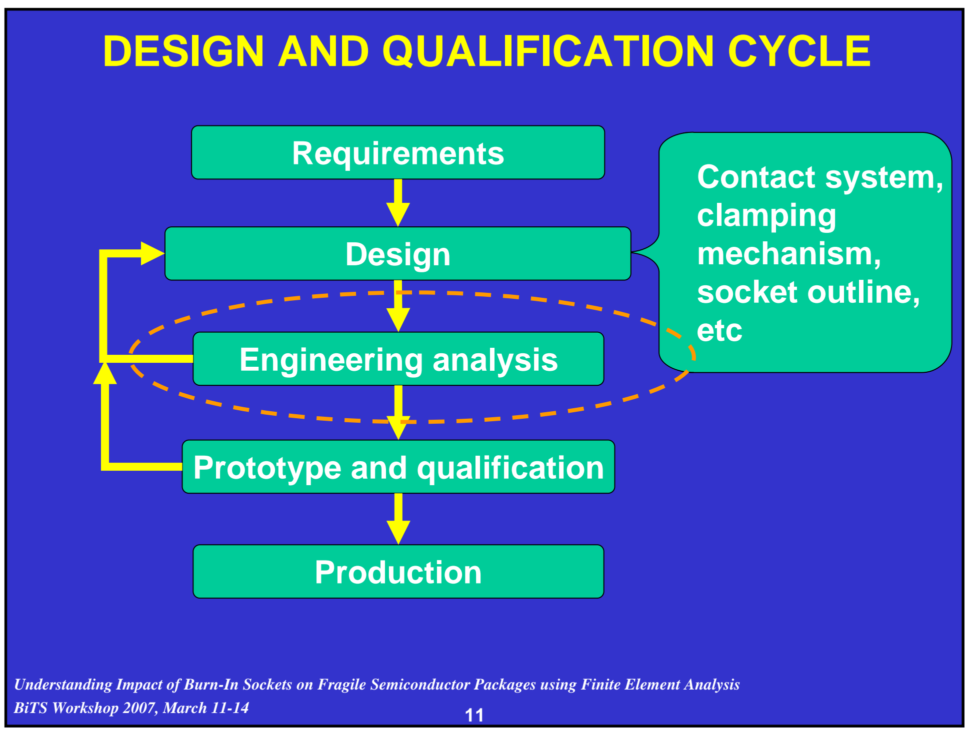
DESIGN AND QUALIFICATION CYCLE
Requirements
Design
Engineering analysis
Prototype and qualification
Production
Contact system, clamping mechanism, socket outline, etc
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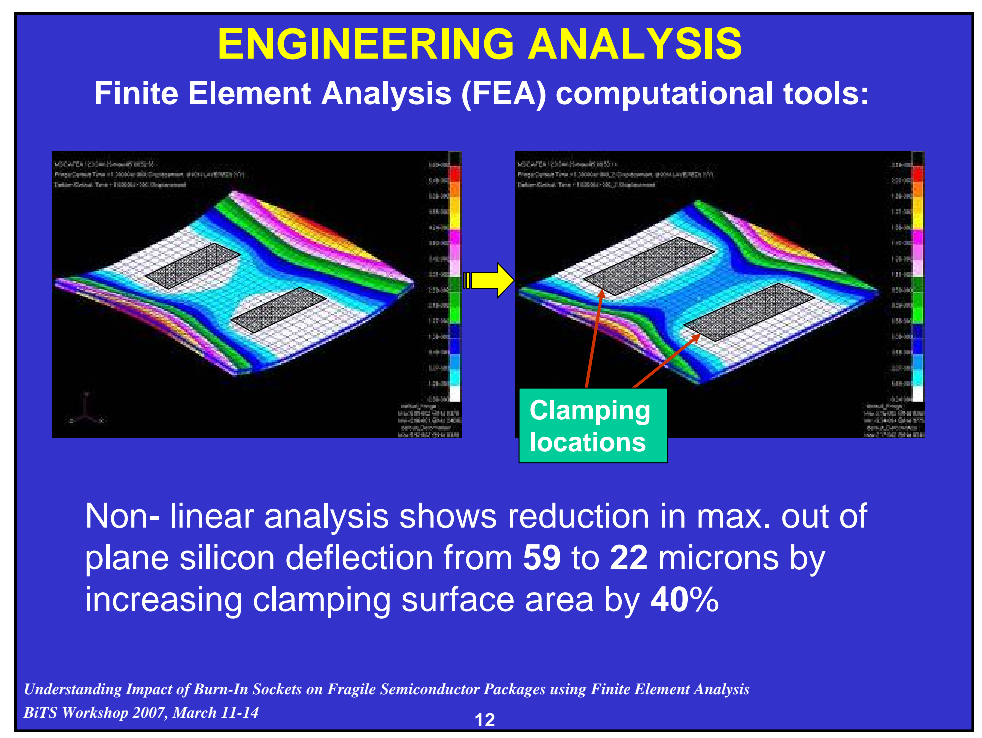
ENGINEERING ANALYSIS
Finite Element Analysis (FEA) computational tools:
Clamping locations
Non- linear analysis shows reduction in max. out of plane silicon deflection from 59 to 22 microns by increasing clamping surface area by 40%
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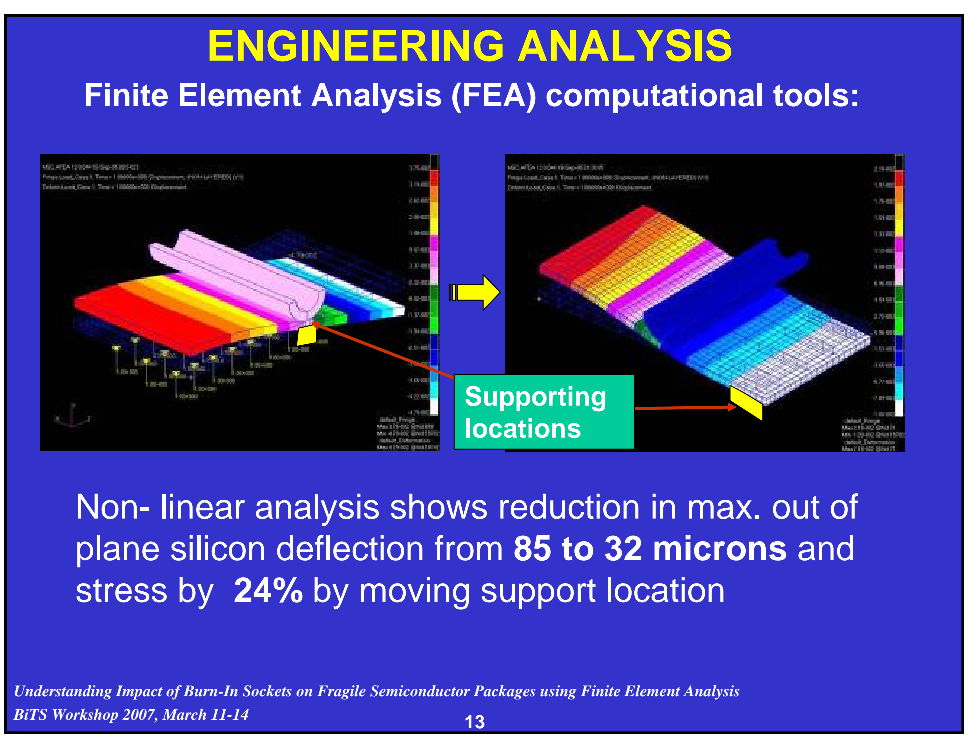
ENGINEERING ANALYSIS

Finite Element Analysis (FEA) computational tools:



Non- linear analysis shows reduction in max. out of plane silicon deflection from **85 to 32 microns** and stress by **24%** by moving support location

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ANALYZING AN IC PACKAGE

- Finite Element Analysis (FEA) is a powerful tool for accurately computing the physical response of a system when the geometry, boundary and initial conditions as well as the material properties are known.
- The material properties are often the limiting factor in the ability to perform a highly accurate analysis.

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ANALYZING AN IC PACKAGE

•For the class of problem in this presentation, the elastic properties may be known or can be measured, but the creep properties are not known and will be very difficult to measure.

• The package is a composite structure, with each material zone having it's own properties.

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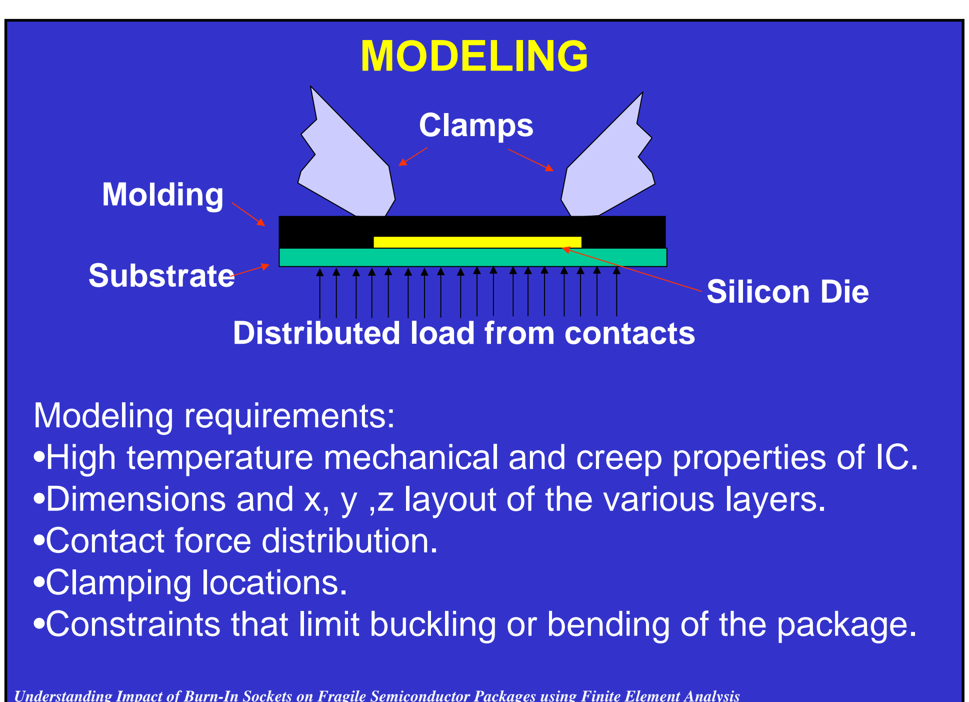

MODELING

Modeling Concerns:
- Lack of good structural data on packages.
- Availability of mechanical properties at elevated temperatures.
- Creep properties.
- Composite material behavior depends on the type of attachment between layers.

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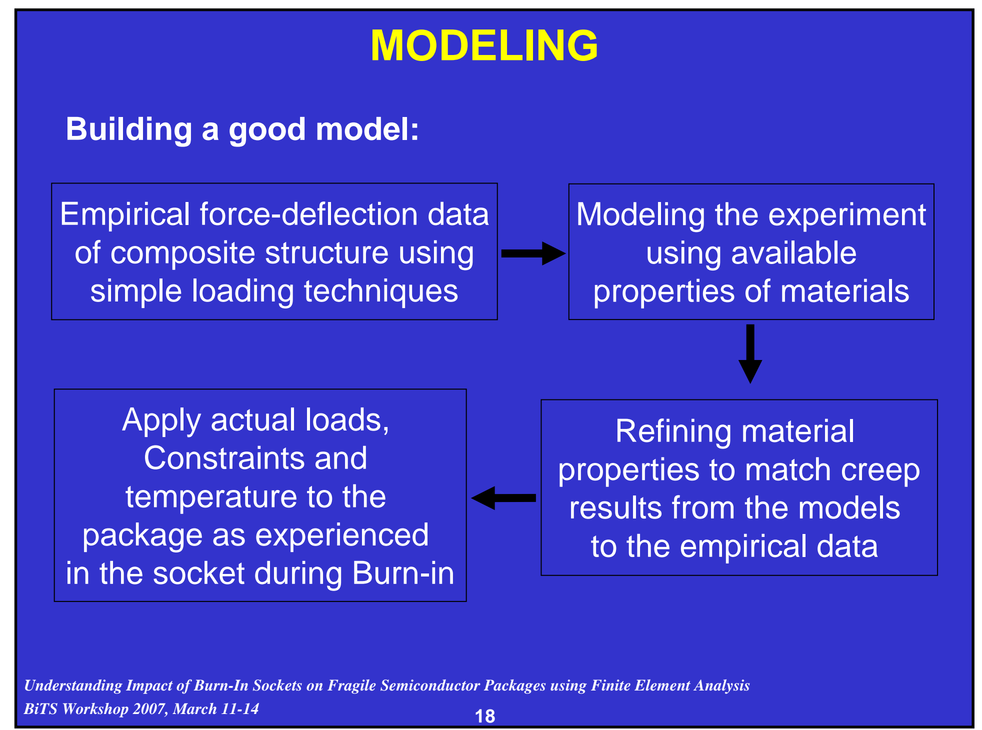

EMPIRICAL DATA EXTRACTION

Force

- Three point bend test used to measure the force displacement response→ Stiffness
- Fixed displacement extended time testing to measure the force decay → Creep properties of composite
- Image above shows FEM for quarter symmetric model. Package consists of FR4 substrate, silicon die, over mold compound.
- Contact conditions are used where package interfaces center shaft (where load is applied) and the bottom support shelf.

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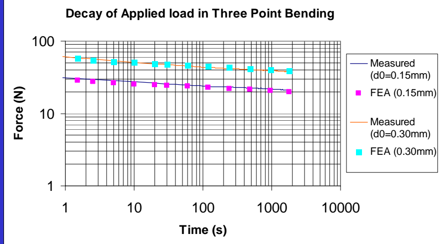
EMPIRICAL DATA EXTRACTION



- The force decay curves above follow a power law in time.
- This suggests that a simple power law representation of the creep strain can be used: $\varepsilon_C = a_0 \sigma^{a_1} t^{a_2}$
- Through iteration we arrive at the following effective creep constants for the given composite structure a0=7.0E-05, a1=1.2, a2=0.15.
- The FEA results match the experimental results well.
- Apply these creep properties to package when loaded in socket.

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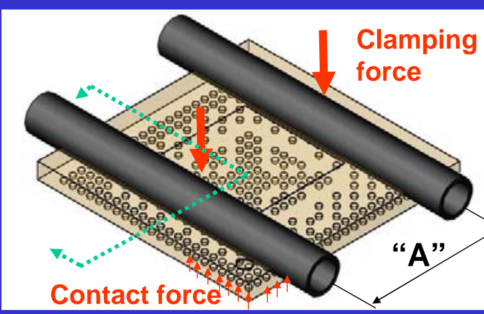
ANALYSIS- CREEP MODELS

Advanced features of our modeling and analysis :
- 3D Contacting surfaces
- Creep material model
- Non linear large displacement analysis
- Variable force contacts
- Computational and empirical properties extraction



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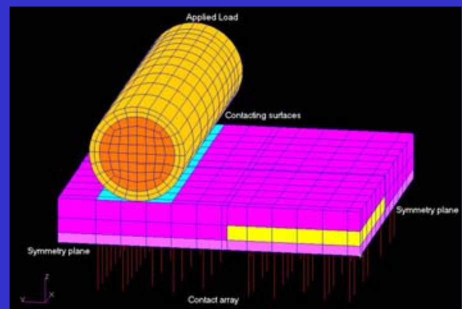
ANALYSIS- CREEP MODELS



- Model above shows the selected package with linear springs to represent contacts and cylindrical latches to apply the loading.
- Analysis uses elastic properties for Si and the derived creep constants at 125C. A 40N load is applied for 4 hrs.
- Large displacement formulation using creep material model and 3D contacting surfaces, accounts for creep decay and force reduction in the contacts.

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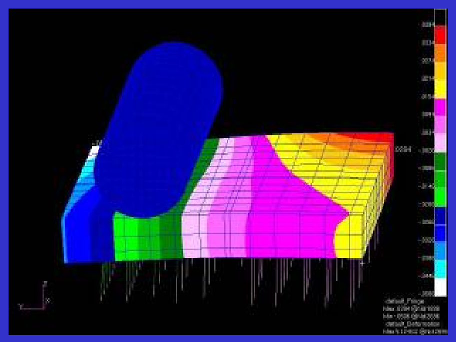
ANALYSIS- CREEP MODELS



Original design showed 90 micron out of plane permanent deflection

- Image to the left shows deformation of package over four hours of loading followed by unloading to give permanent deformation.
- FEA results of 90 um permanent deformation (creep) compared well with measured average of 96 um.

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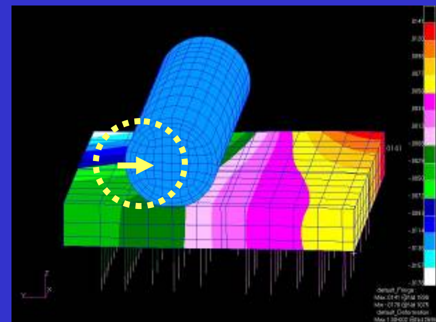
ANALYSIS- CREEP MODELS

- To reduce the deflection, the latches were moved 0.65mm inwards as shown on the image to the right.
- Moving the latches inward by only 0.65mm shows a large improvement on the permanent set. FEA results of 32um deflection compared well with measured average of 42um.
- FEA can make a useful prediction of the performance of the package in actual socket conditions.



Improved design showed only 32 micron out of plane permanent deflection

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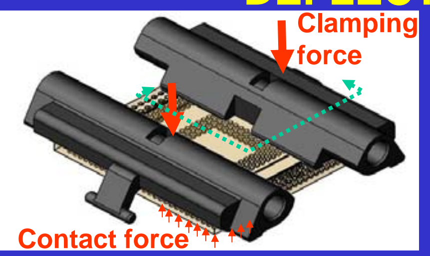
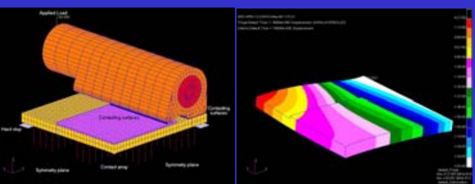
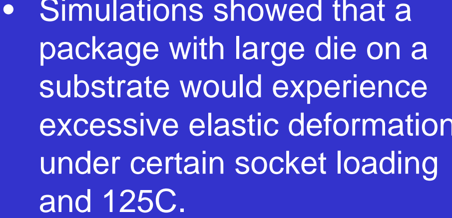
ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS







- Simulations showed that a package with large die on a substrate would experience excessive elastic deformation under certain socket loading and 125C.
- Symmetric ¼ model constructed as shown at left.
- Maximum deformation of 140 um estimated using FEA.
- Pressure plate is allowed to rotate about axis of shaft
- Therefore no resisting moment to keep package flat

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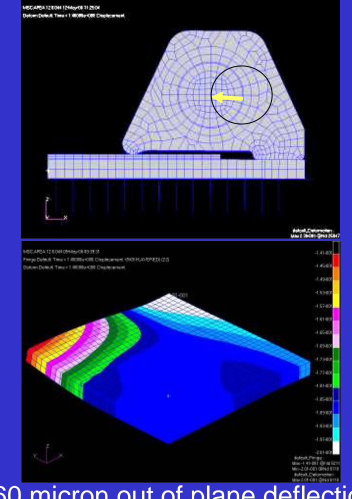
ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS



60 micron out of plane deflection concentrated towards edges

- New latch shown on left where shaft location is moved inboard with a corresponding inward contact point.
- Total package out-of-plane deformation reduced to 60 um concentrated toward edge. Die located in the center saw a 8um deflection.
- The shaft location is the key factor.

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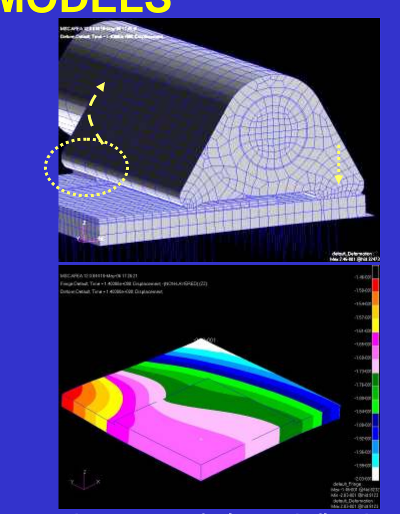
ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS

- On the right, latch was modified to add a “foot” toward the package edge.
- Out-of-plane deformation reduced to 55 um, However die region deflection increased to 16um.
- Force applied by “foot” creates moment and causes additional rotation of latch → less force on die and more bending in that zone.



55 micron out of plane deflection more distributed on package.

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Q & A

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Agenda

- Impact
- Trends and definitions
- Beyond the theory
- Measurement setup
  - System fundamentals
  - Required Support hardware
- Intel's Best Known Method
- Summary

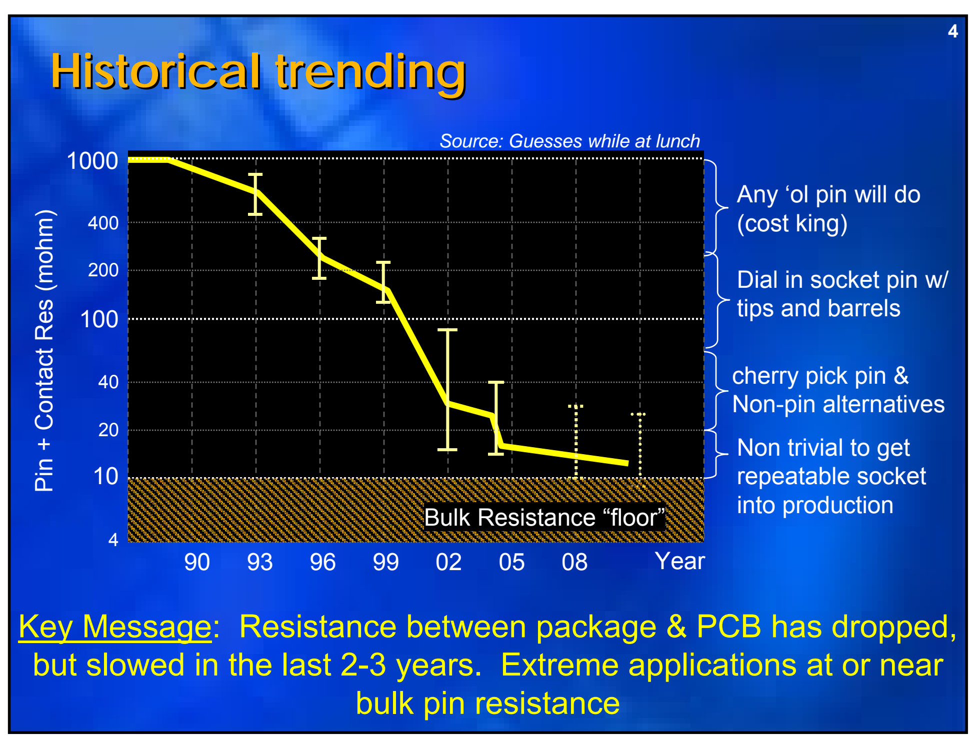
3

Impact of Contact Resistance

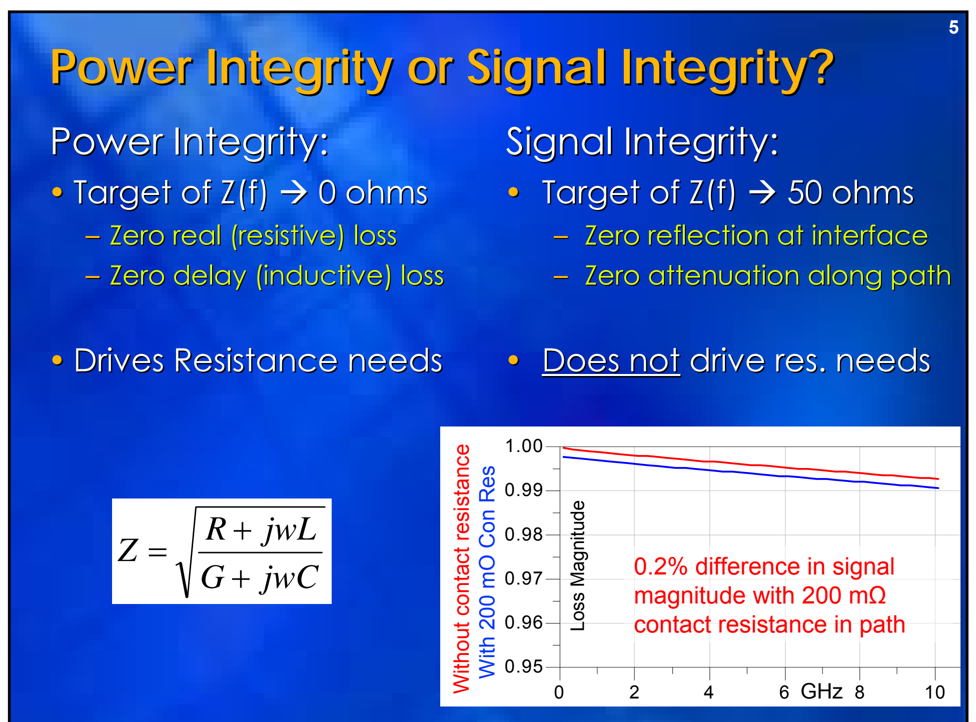
- Socket level Contact Resistance impacts Intel in three ways
  - Limits our ability to deliver power to the DUT[1]
  - Final test ≠ OEM level
    - Over- or under-kill at final test
  - Changes with cycling, forces test environment to drift with time/cycles of the socket

4

Historical trending



Key Message: Resistance between package & PCB has dropped, but slowed in the last 2-3 years. Extreme applications at or near bulk pin resistance



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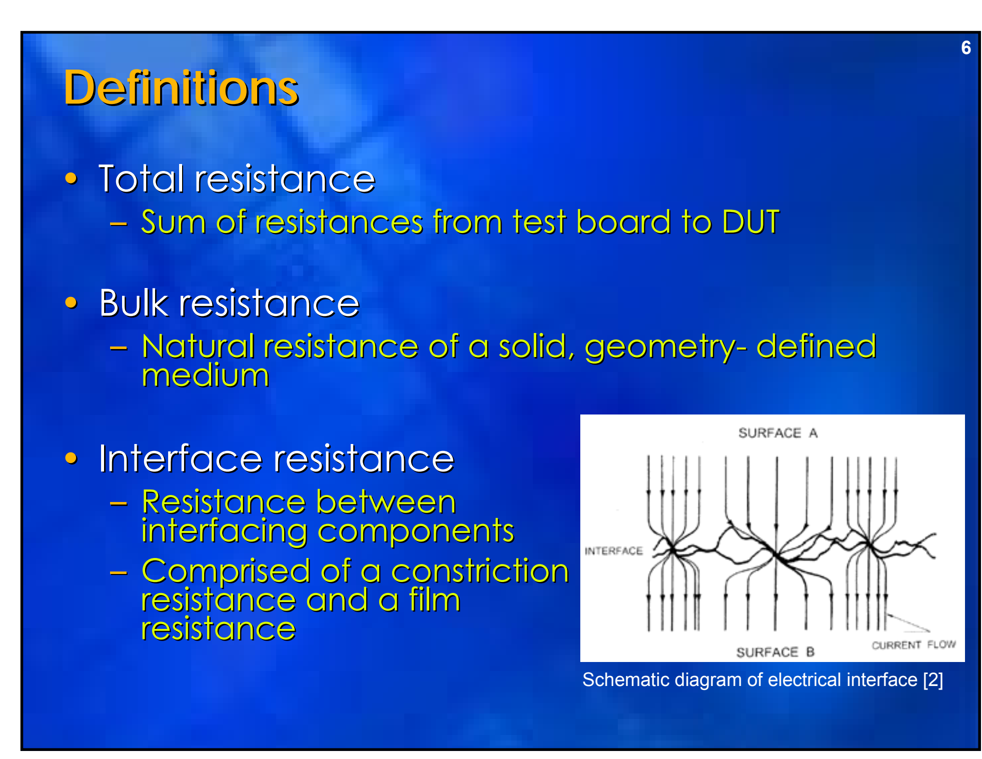
Power Integrity or Signal Integrity?
Power Integrity:
Target of Z(f) → 0 ohms
– Zero real (resistive) loss
– Zero delay (inductive) loss
Drives Resistance needs
Signal Integrity:
Target of Z(f) → 50 ohms
– Zero reflection at interface
– Zero attenuation along path
Does not drive res. needs
$Z = \sqrt{\frac{R + jwL}{G + jwC}}$
Without contact resistance
With 200 mO Con Res
Loss Magnitude
1.00
0.99
0.98
0.97
0.96
0.95
0
2
4
6
GHz
8
10
0.2% difference in signal magnitude with 200 mΩ contact resistance in path



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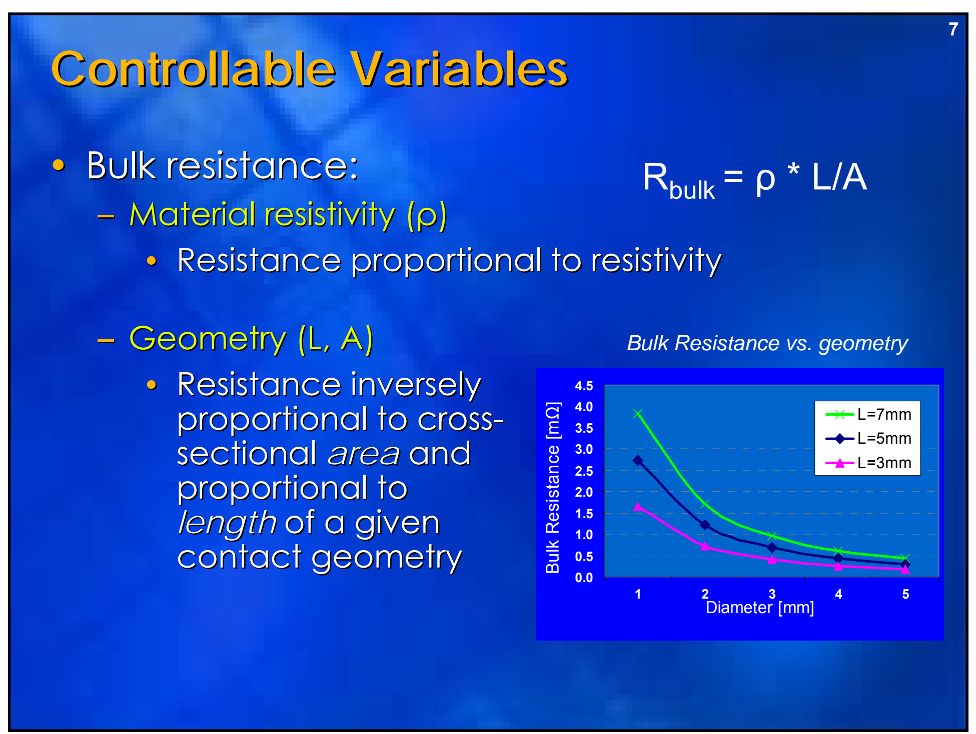
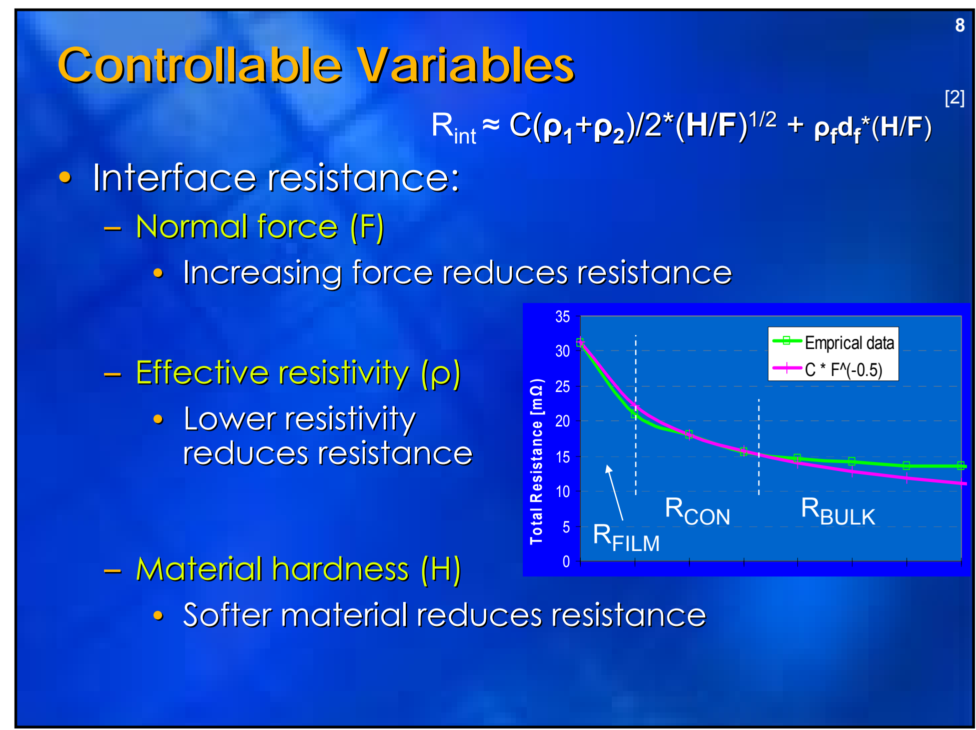
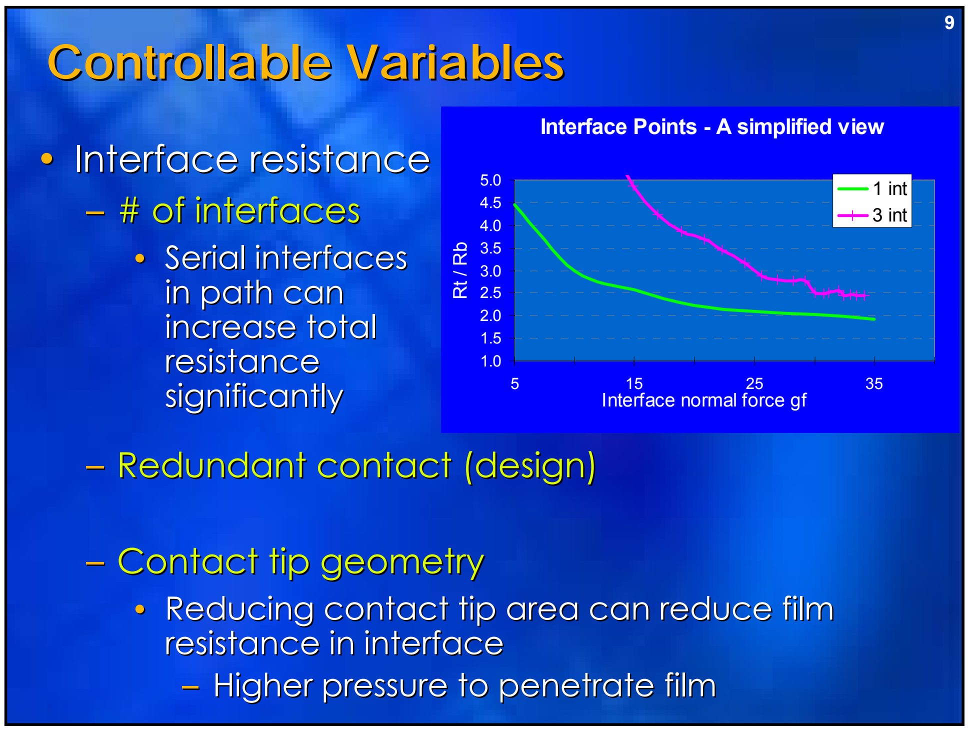
Definitions
Total resistance
– Sum of resistances from test board to DUT
Bulk resistance
– Natural resistance of a solid, geometry- defined medium
Interface resistance
– Resistance between interfacing components
– Comprised of a constriction resistance and a film resistance
SURFACE A
INTERFACE
SURFACE B
CURRENT FLOW
Schematic diagram of electrical interface [2]


7
Controllable Variables
Bulk resistance:
Material resistivity (ρ)
Resistance proportional to resistivity
Geometry (L, A)
Resistance inversely proportional to cross-sectional area and proportional to length of a given contact geometry
$R_{bulk} = \rho * L/A$
Bulk Resistance vs. geometry
Bulk Resistance [mΩ]
Diameter [mm]
L=7mm
L=5mm
L=3mm


8
Controllable Variables
[2]
$R_{int} \approx C(\rho_1+\rho_2)/2*(H/F)^{1/2} + \rho_f d_f*(H/F)$
Interface resistance:
Normal force (F)
Increasing force reduces resistance
Effective resistivity (ρ)
Lower resistivity reduces resistance
Material hardness (H)
Softer material reduces resistance
Total Resistance [mΩ]
Emprical data
C * F^(-0.5)
R_{FILM}
R_{CON}
R_{BULK}



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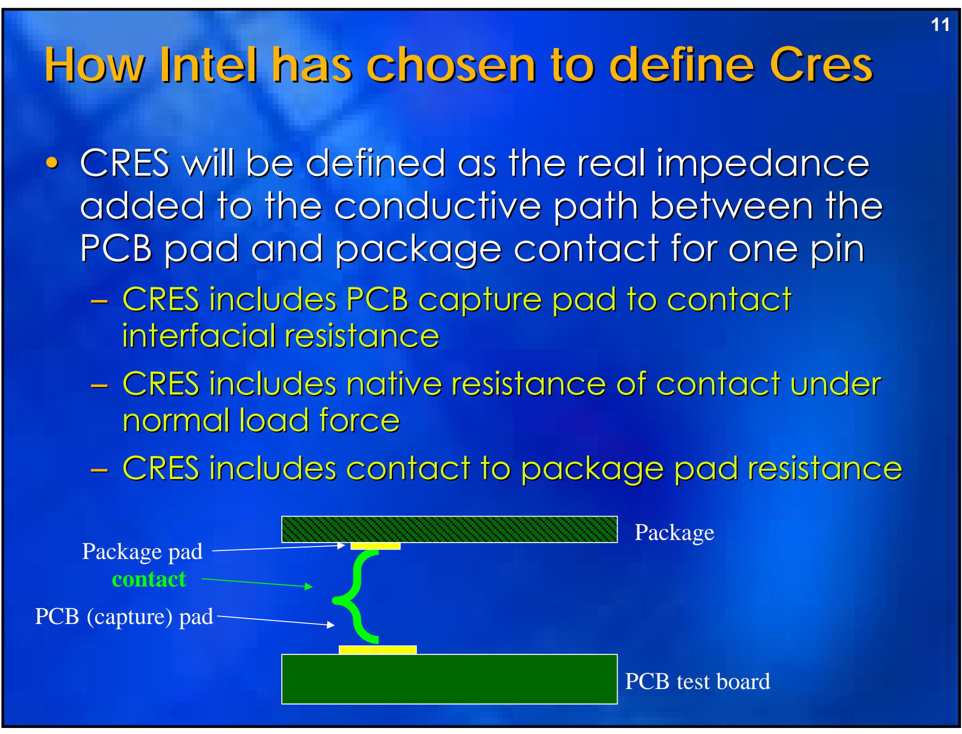
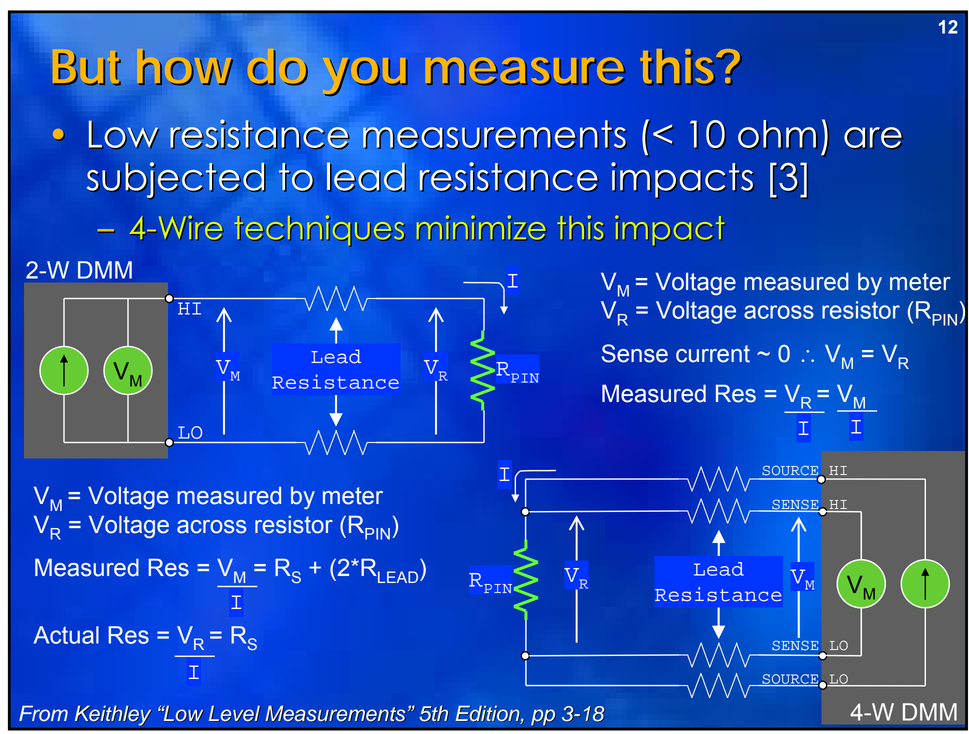
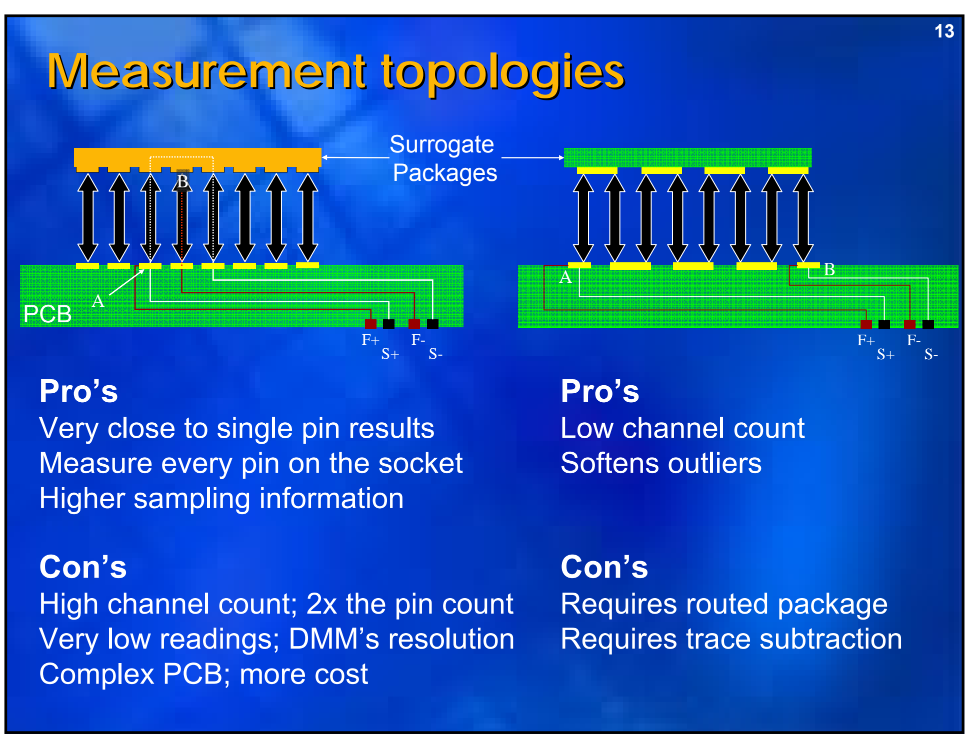
Constraints and Challenges

- Typical Design constraints
  - Force limitations (per contact)
    - Socket contacts << 100gf to avoid package stress
  - Physical size/geometry
    - Driven by device layout and electrical requirements
- Challenges
  - Interfacing test board / device properties
    - Resistivity, hardness, flatness, etc
  - Cleanliness of test board / device
    - Film resistance!
  - Corrosion and wear





Paper #3



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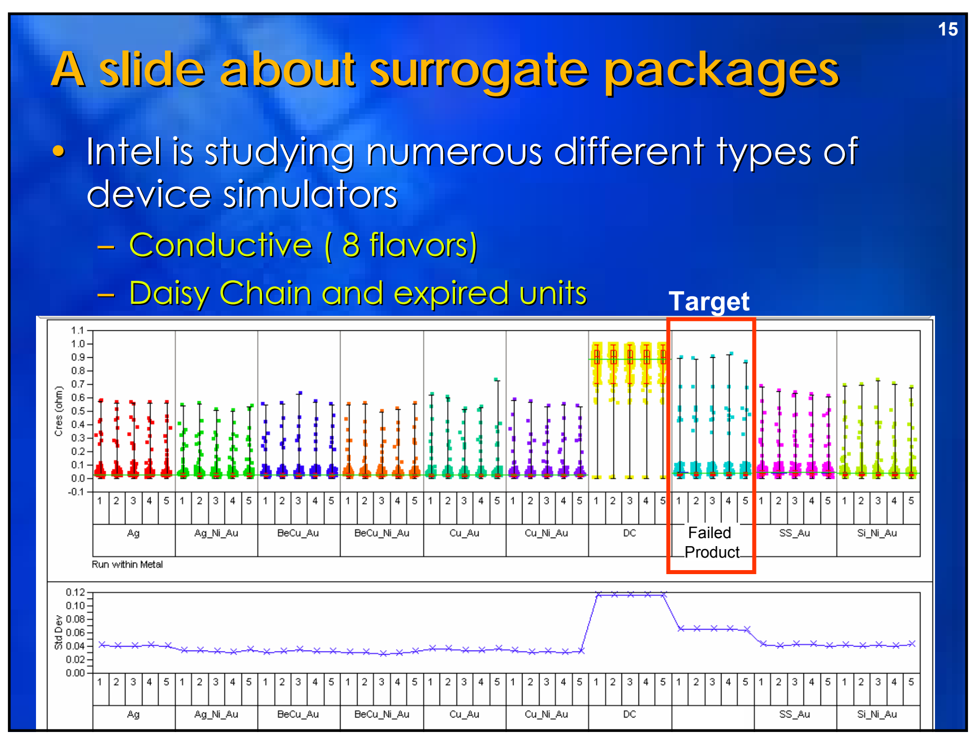
Beyond theory, practical concerns

	Life Cycling a socket	Fleet of sockets
End usage condition	Each socket "sees" 25-75k unique pristine packaged parts	Product requires 10 – 2000 sockets to support total volume
Lab validation concern	25-75k unique package simulators?	Cost & Time of measuring 10 – 2000 sockets
Simple solution	Reuse device simulators	small sample of sockets, but tight limits & every pin tested
Noise factor	Life of device simulator Topology of simulator	One outlier pin Stability of supply Pin lot-to-lot variation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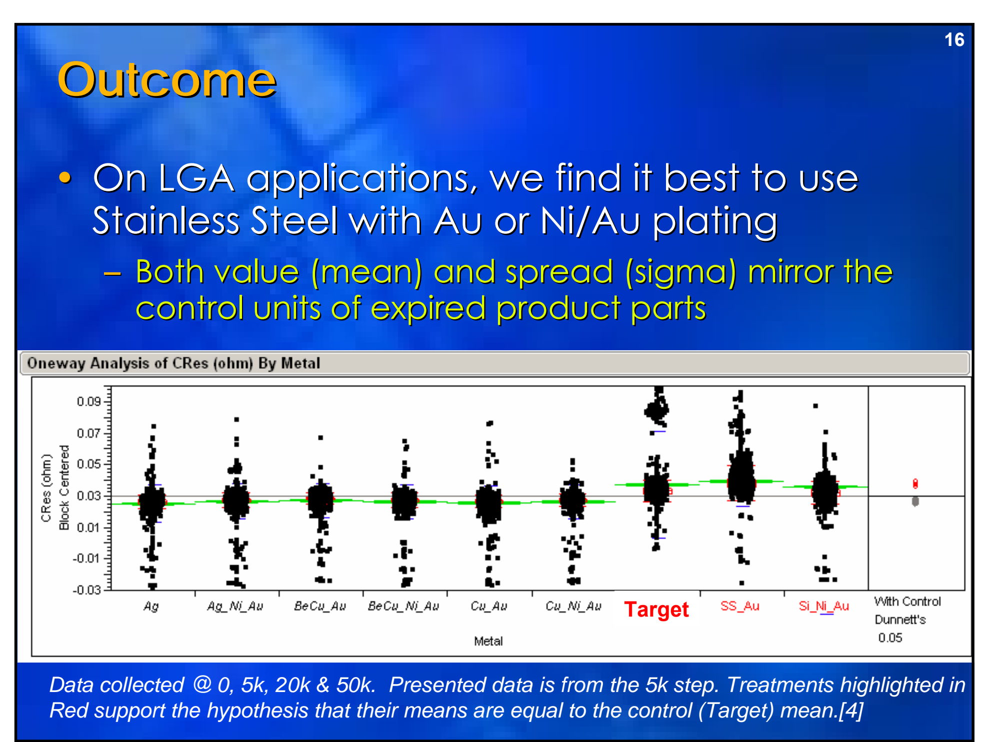
A slide about surrogate packages
• Intel is studying numerous different types of device simulators
– Conductive (8 flavors)
– Daisy Chain and expired units
Target
Failed Product
Ag
Ag_Ni_Au
BeCu_Au
BeCu_Ni_Au
Cu_Au
Cu_Ni_Au
DC
SS_Au
Si_Ni_Au
Run within Metal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Outcome
• On LGA applications, we find it best to use Stainless Steel with Au or Ni/Au plating
– Both value (mean) and spread (sigma) mirror the control units of expired product parts
Oneway Analysis of CRes (ohm) By Metal
CRes (ohm) Block Centered
Ag
Ag_Ni_Au
BeCu_Au
BeCu_Ni_Au
Cu_Au
Cu_Ni_Au
Target
SS_Au
Si_Ni_Au
With Control Dunnett's 0.05
Metal
Data collected @ 0, 5k, 20k & 50k. Presented data is from the 5k step. Treatments highlighted in Red support the hypothesis that their means are equal to the control (Target) mean.[4]

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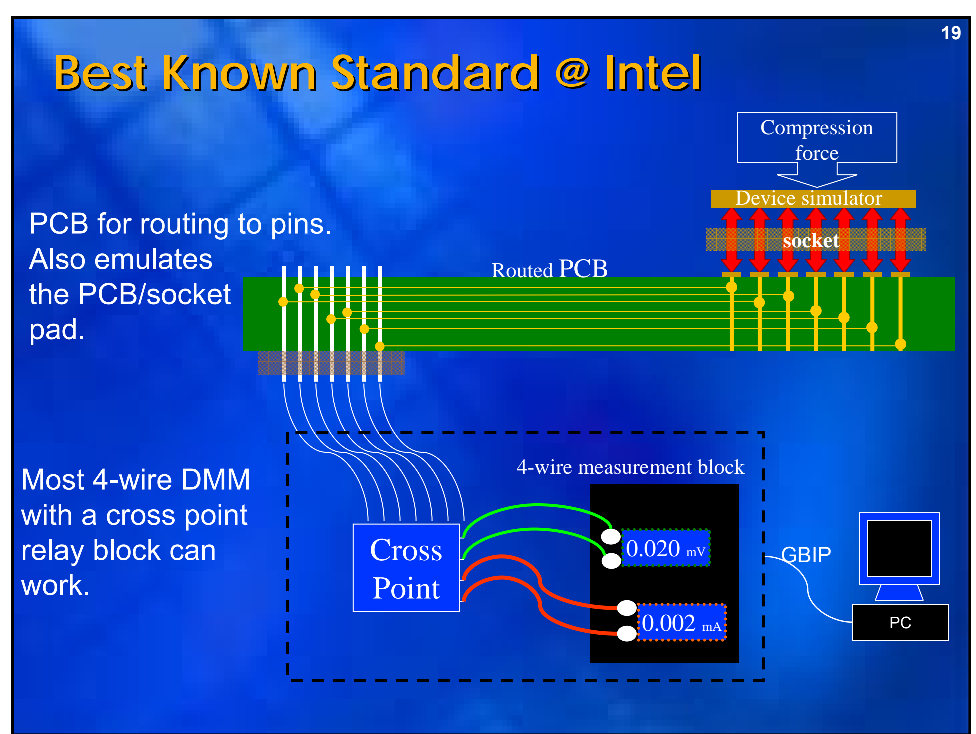
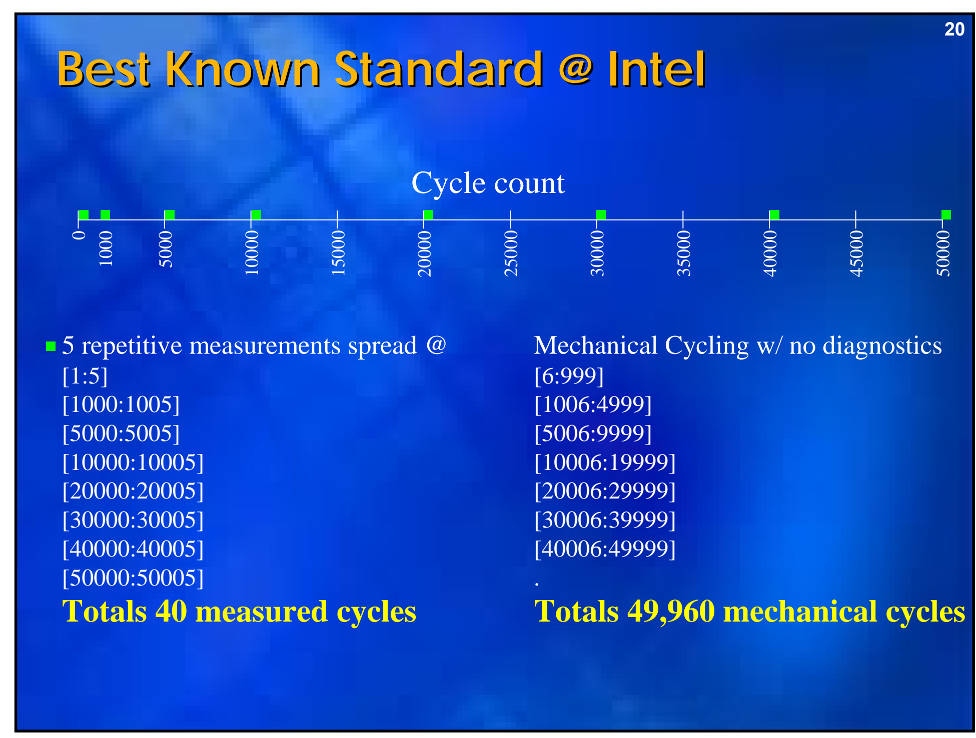
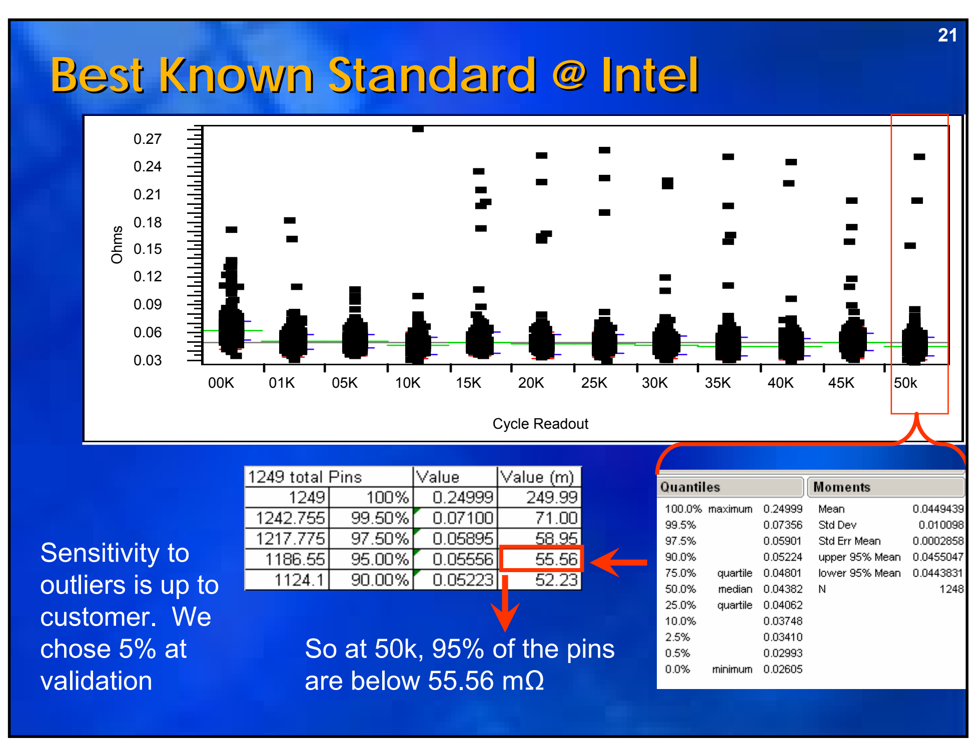
Key takeaways so far

- Dialing in Contact Resistance on a high volume platform is a multi-million dollar variable
- Today's contact resistance targets require crisp definitions between the user and supplier
- Contact Resistance is predominantly a Power Integrity impact, not a Signal Integrity one
- There are few fundamental knobs to turn in the pursuit of optimized total resistance performance.
  - Largest gain seemingly w/ interface resistance
- 4 wire techniques must be used
- Mimicking end us conditions requires care in the selection of the device simulator and cycling

Our Measurement System and How We Use It


19
Best Known Standard @ Intel
Compression force
Device simulator
socket
Routed PCB
PCB for routing to pins. Also emulates the PCB/socket pad.
Most 4-wire DMM with a cross point relay block can work.
4-wire measurement block
Cross Point
0.020 mV
0.002 mA
GBIP
PC


20
Best Known Standard @ Intel
Cycle count
0
1000
5000
10000
15000
20000
25000
30000
35000
40000
45000
50000
5 repetitive measurements spread @
[1:5]
[1000:1005]
[5000:5005]
[10000:10005]
[20000:20005]
[30000:30005]
[40000:40005]
[50000:50005]
Totals 40 measured cycles
Mechanical Cycling w/ no diagnostics
[6:999]
[1006:4999]
[5006:9999]
[10006:19999]
[20006:29999]
[30006:39999]
[40006:49999]
Totals 49,960 mechanical cycles



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Best Known Standard @ Intel

- Positives
  - Simple in theory
  - Most of the system is off the shelf hardware
  - Effort to prove it matches end use conditions
    - Still more to go
  - Open to scrutiny
- Negatives
  - Time from concept to data too long
  - requires hardware to wrap around socket to test
    - PCB, device simulator, compression force
  - Currently no automation or standardization of cycling piece of the flow

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Where do we go from here

- Intel will share the following documents
  1. Gage R&R DOE steps
     - Used to help gather a metrology system accuracy
  2. Reference design for resistance testing
     - May choose to match Intel and become qualified
  3. Reference metrology system details
  4. Reference device simulators and plating recipes
  5. Step by step validation testing

Key message, we are not contact physic experts nor do we wish to be. Our motivation is to make supplier results more meaningful so we can rapidly assess the fit of technologies to our needs

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Summary

- Contact Resistance is a widely used metric for sizing up, monitoring and validating a contact
- Today's requirements require crisp terminology and metrology between user and supplier
- We are not experts, but we have studied and will share our Best Known Methods with the goal to narrow future definitions and measurement methods

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References

[1] Swettlen, Grossman, Berube "Qualifying a supplier, what one customer does", BITS Workshop March 2005

[2] Slade, Paul G. "*Electrical Contacts : Principles and Applications*", New York: Cutler-Hammer, 1999

[3] Keithley "Low Level Measurements" 5th Edition

[4] Dunnett, C.W. (1955), "A multiple comparison procedure for comparing several treatments with a control" Journal of the American Statistical Association, 50, 1096–1121.