ADVANCEMENTS IN CONTACTING LEADING EDGE PACKAGES

“Novel Low Cost Test and Burn-in of Wafer Level Packaging”
Belgacem Haba, Ph.D., David Ovrutsky, Guilian Gao, Ph.D., Vage Oganesian
Tessera, Inc.

“A New Probe Card Approach for Wafer Level Chip Scale Package Testing”
Norman J. Armendariz, Ph.D.
Texas Instruments, Inc.

“POP Rocks: Approaches to Socketing Package-on-Package Devices”
Jon Diller, Kiley Beard, Jamie Andes
Interconnect Devices, Inc.

COPYRIGHT NOTICE
The papers in this publication comprise the proceedings of the 2007 BiTS Workshop. They reflect the authors’ opinions and are reproduced as presented, without change. Their inclusion in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.

There is NO copyright protection claimed by this publication or the authors. However, each presentation is the work of the authors and their respective companies: as such, it is strongly suggested that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.

All photographs in this archive are copyrighted by BiTS Workshop LLC. The BiTS logo and ‘Burn-in & Test Socket Workshop’ are trademarks of BiTS Workshop LLC.
Novel Low Cost Test and Burn-in Wafer Level Packaging

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Belgacem Haba, Ph.D., David Ovrutsky
Guilian Gao, Ph.D. and Vage Oganesian
Tessera, Inc.

Agenda

• Background
• Wafer Level Packaging and why?
• What needs to be done?
• Results
• Conclusion
Agenda

- Background
- Wafer Level Packaging and why?
- What needs to be done?
- Results
- Conclusion

Are Sockets Required for Test and Burn-in?

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006
Belgacem Haba, Ph.D.
Tessera, Inc.
Micro Contacts: 0.8 x 0.8 mm pitch

~80 microns tip

0.8 mm

0.8 mm

Dielectric Substrate
Etched Cu micro contact with Ni/Au

Finer Pitch (<400 µm)
Very feasible

Existing Testing and Burn-In

Package

Socket

Board

03/2007
**Micro Contacts Test and Burn-In**

- No sockets required
- Tolerance issues mitigated
- Much lower cost

**Prototype Testing**

- Simple contact direct to board
- Similar housing could be used for Test/Burn-In
Summary

- Introduction of micro contact technology
- Scalability to fine pitch and high I/O
- Cost reduction path for test & burn-in
- Versatile approach can be leveraged in many applications

Stay tuned.........

We are proposing a socket-less Wafer Level Test and Burn-in
Agenda

• Background
• Wafer Level Packaging (WLP) and why?
• What needs to be done?
• Results
• Conclusion

WLP Promise

• Low Cost
• High parallelism
• Merge front end and back end
• Minimize component handling
• Test and burn-in in a wafer form
Ensuring WLP Reliability

- Reliability deteriorates as:
  - Die size increases
  - Ball size decreases (or ball pitch)
- High reliability achieved if:
  - Die smaller than 5x5 mm
    - No need for underfill
  - Die larger than 5x5 mm
    - Need underfill or compliancy

Where does WLP fit?

The maximum number of I/O that can fit on a die at a given pitch

Area where WLP does not apply

Area where WLP may apply

Integrated Passives  Analog Std. Logic  µPROCESSORS FPGA  High Pin Count ASICs  DSPs  ASSPs  DRAM  µControllers  FLASH  SRAM

Die Size

# of I/O's

03/2007
High Volume WLP Today

- Simple redistribution layer with solder bump
- Mainly used for very small die, low I/O (analog, integrated passives, power MOSFETS)
  - Very low cost; 1000s die per wafer
- Limited because of reliability issues above 5x5 mm die size

WLP Challenges

- Assembly Infrastructure
- Reliable larger die
- Test infrastructure
- RDL, bumping capacity increasing
- 300 mm WLP more cost effective
- Compliant WLP is reliable
- Oxide-free, compliant contact enables test
- Die shrink remains an issue
Form Factor Wafer Probe

- Wafer Probe Cards
- 6” and 8” wafers
  - DRAM
  - Flash
  - Microprocessors
- Technology based on MicroSpring®

Aehr Test--Test/ BI Partner

- Aehr Systems have available test and burn-in systems
  - Based on wafer cassettes
  - Use contactors interposer between wafer and board
  - Up to 14 wafers per load

March 11 - 14, 2007
Potential Cost Reduction

WL T/BI Cost Comparison

Prev. WLBT

New WLBT

Ref: S. Steps, AEHR Test Systems, CAST, Barcelona 2005

Agenda

• Background
• Wafer Level Packaging and why?
• What needs to be done?
• Results
• Conclusion
Targeted WLP Attributes

- Low cost, HVM process
- Testable structure in wafer form (Cu posts)
- Reliable for large die such as DRAMs (Compliant bumps)
- Use available infrastructure

What’s needed to be done?

- Metal posts incorporated in the WLP
- Very good co-planarity of the WLP post tips
- Compliancy under metal posts to mitigate
  - co-planarity of the metal posts
  - test board warpage
- Manufacturable process
- Low cost
**Agenda**

- Background
- Wafer Level Packaging and why?
- What needs to be done?
- Results
- Conclusion

**Model Geometry**

- FR-4
- Solder mask
- Copper trace
- Compliant bump
- Silicon

---

*Paper #1*

March 11 - 14, 2007
Modeling and material selection

- Solder mask: WL5150
  - Compliant bump: DC6910
  - Strain ~6%
  - Solder mask: LSF-60
  - Compliant bump: DC6910
  - Strain over 5%

- Solder mask: WL5150
  - Compliant bump: JSR6224
  - Strain over 3%

- Solder mask: LSF-60
  - Compliant bump: JSR6224
  - Strain over 3%

NOTE! Analysis did NOT finish due to excessive deformation. The picture is based on 82.54% completion, i.e. T = 52 °C.

NOTE! Analysis did NOT finish due to excessive deformation. The picture is based on 77.61% completion, i.e. T = 60 °C.

Printing of bumps

- Silicon bumps
- Cost effective process
- Desired target 60 µm
- Variation too large
Protect the bumps

- Cover bumps with protective layer

Bumps covered by protective layer

Grinding of bumps

- TTV (chip) – 3.5 µm
- TTV (wafer) – 13.7 µm
Copper Post Formation

**Process Flow**

Compliant bump

- Bond pad
- DRAM wafer surface
- Compliant bump

**Compliant bump**

**Compliant bump**

- Ti deposition
- Sputtered primer metal
- Ti deposition

**EDPR I**

- Opened metal areas
- Electrophoretic photoresist

**EDPR I Strip**

**Cu lead electroplating**

**Electroplated Cu**

03/2007

Copper Post Formation Cont.

**Process Flow Cont.**

EDPR II

- Thickened electroplated copper
- Thickened electroplated copper

**EDPR II**

- Thinned electroplated copper

**Cu pins electroplating**

**Thinned electroplated copper**

**EDPR II Strip**

**Thinned electroplated copper**

**Demonstrator**

**Demonstrator**

03/2007

March 11 - 14, 2007
**Typical cross section**

- Pin height – 20-30µm
- Pin Diameter – 80µm

- Cu pin – 80µm
- Cu pin – 20-30µm
- Cu lead – 10µm
- S. Bump – 60µm
- S. Bump – 500-600µm

**Copper Posts Co-planarity**

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Pin Center, µm</th>
<th>Pin South, µm</th>
<th>Pin West, µm</th>
<th>Pin North, µm</th>
<th>Pin East, µm</th>
<th>AVG, µm</th>
<th>STDEV, µm</th>
<th>TTV, µm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>16.5</td>
<td>21.5</td>
<td>24.1</td>
<td>18.5</td>
<td>21.5</td>
<td>21.4</td>
<td>2.29</td>
<td>7.6</td>
</tr>
<tr>
<td>2</td>
<td>29.8</td>
<td>24.1</td>
<td>31</td>
<td>30.9</td>
<td>23.5</td>
<td>27.3</td>
<td>4.14</td>
<td>7.5</td>
</tr>
<tr>
<td>3</td>
<td>32.7</td>
<td>34.2</td>
<td>36.3</td>
<td>34.8</td>
<td>34.7</td>
<td>35.0</td>
<td>0.91</td>
<td>3.6</td>
</tr>
<tr>
<td>4</td>
<td>28.7</td>
<td>29.6</td>
<td>30.8</td>
<td>28.5</td>
<td>24.6</td>
<td>28.4</td>
<td>2.69</td>
<td>6.3</td>
</tr>
</tbody>
</table>

**Wafer Level Co-planarity**

<table>
<thead>
<tr>
<th>Profile Before Overcoat</th>
<th>Profile After Overcoat</th>
<th>Cross Sections</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper Pin</td>
<td>UBM</td>
<td>Co-planar Bump</td>
</tr>
</tbody>
</table>
**Metal Redistribution**

**Process Flow**

- EDPR
- EP Ni
- EP Cu
- PR Strip
- Ti Etch

![Wafer](image)

03/2007

**Reliability**

- Board level temperature cycling
  - -40°C to 125°C (1 hour cycle)
  - 1600 cycles, no failure
- MSL 1: 125°C / 24hr + 85°C/85%RH = 3 x reflow
- TH 85°C/85%RH, 1000hrs
- PCT 120°C/100%RH, 2atm/196hrs

03/2007
Parasitic RCL parameters

<table>
<thead>
<tr>
<th>Model</th>
<th>( C_r [\mu F] )</th>
<th>( L_r [\mu H] )</th>
</tr>
</thead>
<tbody>
<tr>
<td>WLP</td>
<td>0.066</td>
<td>0.065</td>
</tr>
<tr>
<td></td>
<td>166 MHz</td>
<td>1 GHz</td>
</tr>
</tbody>
</table>

Acceptable value for DRAM application

• Use silicon wafer as a probe substrate
• Achieved 100% contact
• Good contact with forces from low up to 40 g per pin
Agenda

• Background
• Wafer Level Packaging and why?
• What needs to be done?
• Results
• Conclusion

Summary

• Demonstrated a complaint wafer level packaging (WLP) for large die
• Demonstrated a WLP structure testable without socket interposer
• Demonstrated a reliable WLP structure mounted on board
• Stay tuned for more data to come
THANK YOU
A New Probe Card Approach for Wafer Level Chip Scale Package Testing

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Norman J. Armendariz, PhD

AGENDA

• The Need
• WSP-Wafer Scale Packages
• WSP- Manufacturing Test Flow
• Current WSP Probe Card Technologies
• New WSP- Probe Card Concept
• Challenges
• WSP Comparative Summary
• Discussion
THE NEED

TI has been testing packages at final test after singulation for some time. However, the increasing use of WLCSP- wafer level chip scale package formats require cost-effective RF testing at the wafer-level or before singulation to further reduce test costs and be globally competitive.

TI-WCSP Wafer Chip Scale Packages

NanoStar™
- WCSP with eutectic SnPb Solder

NanoFree™
- WCSP with Pb-Free Solder
WCSP- Redistribution Layer-RDL

SEM VIEW

OM VIEW

RDL

BUMP

UBM

Silicon

XS VIEW

Image Courtesy of the Tucson Reliability Test Lab

WLCSP w/ RDL Examples

03/2007 Wafer Level Probing of WLCSP
WSP Test Flow -Simplified

Final Test → Wafer Fab → WSP

Wafer Probe (Functional)

RDL/Bump (AOI)

Wafer Probe RF Test

Backgrind Wafer Mount/Saw Assembly RF Test (Sample Burn-in) Inspection T&R/Tray

Backgrind Laser Mark Wafer Mount/Saw Inspection T&R / WP

Current Wafer Level Probe Card Technologies

- Cantilever- (Needle Probes)
- Vertical- (Buckling Beam)
- Membrane (Beam Probes) RF
Advancements In Contacting Leading Edge Packages

Conventional Cantilever

Vertical Buckling Beam

Buckling Beam Probes

Paper #2
Membrane RF Probe Beams

Current WSP Probe Card Status

Both cantilever and VPC probe cards exhibited limited electrical properties as well as other physical & operational limitations.

Membrane probe cards have been employed for those applications that need controlled impedance for RF (radio frequency) testing, but at some cost and also with similar physical and operational limitations.
Thus, WSP Probe Card Concept

Convert or modify FT-final test boards, which already use similar sockets and RF pogo pins into a wafer level probe card for WLCSP- wafer level chip scale packages requiring RF testing and avoid an expensive probe card to skip the RF FT step!!!.

Vertical RF Pogo-Pin

RF Pogo Pins

03/2007 Wafer Level Probing of WLCSP
WSP Probe Card Integration Challenges

Initial probe cards were found to have a number of design / fabrication violations which made it difficult to mechanically and/or operationally integrate for wafer-level testing on TI probers and test floors. Major issues:

- Socket/ Pogo-Pin Design
- Prober/tester Interface
- Alignment Algorithm
- Cleaning

WSP Probe Card Design/ Fabrication

Wafer Side (L) and insulator (R) overlaid as a template showing the exposed areas that are allowed between probe card and probe card support plate (PCSP). A number of components or protruding features were found in “blue” areas or “keep-out” areas (R).
Probe Card Support Plate

PCSP typically made of ceramic. This SS version holds probe card in position (L). PCSP hole limits size of probe head and confines surface components to areas outside blue areas to a maximum component height (Z) of 0.040” for this tester interface configuration (R).

Wafer Side Component Interference

- Jumper “Blue Wires”
- Through-Hole-Mount Solder Joints
- LED Components
- PCB Barrel Vias Protruding
- Sockets and/or Pogo Pins Too Short
Components as located would interfere with interface tester features such as an “inner” ring (red circle) on PCB tester side (L) to Tester pogo-pin outer ring array on tester tower (R).

WSP Probe Card RF Pogo Pin – 4 DUT

PCB
4-DUT Probe Head

Wafer Side

Tester Side

Sockets / Pogo-Pins
1x4

Probe Head

Probe Head
In-Situ (Prober) Pogo Pin Cleaning

Leveraging FT cleaning learnings. Only the 4 tips of this 4-pt. crown pogo pin is cleaned or needs cleaning. Pogo-pin inserted into abrasive and compliant material

WSP PROBE CARD SUMMARY

<table>
<thead>
<tr>
<th>Technology</th>
<th>PROs</th>
<th>CONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cantilever Needles</td>
<td>Low price</td>
<td>Electrically Limited</td>
</tr>
<tr>
<td></td>
<td>Short Lead-time for New Designs.</td>
<td>Periphery limited</td>
</tr>
<tr>
<td></td>
<td>Repairable Contacts</td>
<td>F / D Linear</td>
</tr>
<tr>
<td></td>
<td>Many Qualified Suppliers</td>
<td>Bump-Top Damage/ Reflow</td>
</tr>
<tr>
<td>VPC Buckling Wires</td>
<td>Multi-site 4-16</td>
<td>Electrically Limited</td>
</tr>
<tr>
<td></td>
<td>F / D Profile</td>
<td>Initial Price and Lead Time</td>
</tr>
<tr>
<td>Membrane Probe Beams</td>
<td>Electrical Properties</td>
<td>Bump-Top Damage/ Reflow</td>
</tr>
<tr>
<td></td>
<td>Small scrub marks</td>
<td>Probe binding</td>
</tr>
<tr>
<td></td>
<td>Alignment</td>
<td></td>
</tr>
<tr>
<td>WSP Pogo-Pins</td>
<td>Electrical Properties</td>
<td>Production Repeatability</td>
</tr>
<tr>
<td></td>
<td>Low Price</td>
<td>Initial Price &amp; Lead Time</td>
</tr>
<tr>
<td></td>
<td>Small Marks on Sides of Bump</td>
<td>Die Size/ Routing Limits</td>
</tr>
<tr>
<td></td>
<td>Multi-site x4-x16</td>
<td>Few Qualified Suppliers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lead-Time</td>
</tr>
</tbody>
</table>

03/2007 Wafer Level Probing of WLCSP

Paper #2
WSP Probe Card Future Work

- Optimize Prober to Wafer Chuck Settings
  - Auto Vertical Chuck Adjustment
  - Alignment Method/Algorithm

- Optimize Cleaning Settings
  - Cleaning Material/ Tip Design
  - Particle Size

- Minimize Probe Card Deflection
  - Tester PCSP Design
  - Mechanical Stiffeners

- Define Probe Card Design and User Specifications
  - Multi-Site x8 to x16
  - Inspection

DISCUSSION
Acknowledgements

• Doyce Ramey
• Kelly Daughtry
• Byron Gibbs
• Dave Reed
PoP Rocks
Approaches to Socketing Package-on-Package Devices

2007 Burn-in and Test Socket Workshop
March 11 - 14, 2007

Jon Diller, Kiley Beard, Jamie Andes
Interconnect Devices, Inc.

Device Description

- Logic + Memory
- Typically BGA-on-BGA
- Enables greater density & SIP solutions
The Test Challenge

- Challenge: testing before package-to-package assembly

March 2007  Diller / Andes / Beard: PoP Rocks

The Ante

- If only tested after assembly, dollars lost on the parent (processor)
- Parent cannot be tested without memory function
- Test of unassembled devices requires contact to memory side – on the top!

March 2007  Diller / Andes / Beard: PoP Rocks
Platform Considerations

- Top-side contact integrated with handler chuck
- Must be completely free-floating
- Must mate / de-mate per cycle
- Cycle life should be ≥ socket contacts
- Should be noiseless to memory test standards

The Basis: Load Board Design

- Normal array of DUT pads
- Extra array of interface pads
Socket Construction

- Interface array surrounds normal socket construction.

The Contacts

8.64 (= DUT + 2x 2.92)

2.92
Exploded Assembly

Status of the Project

- Prototypes fielded mid-'06 in Japan, pending evaluation
- US development on hold
- To be evaluated Q1-Q2 '07

March 2007
Diller / Andes / Beard: PoP Rocks

Paper #3

March 11 - 14, 2007
Further Challenges - RF

- Coaxial contacts
- Interposer section of socket becomes conductive
- Probes isolated from interposer by washers
- BW -1dB >20 GHz

Conclusions

- Radical contact challenges solved through interfacing experience
- Any broad, solutions-focused supplier can develop
- Consider the versatility and responsiveness of your partners