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Tutorial

"Differential Impedance And Insertion Loss Applied To Sockets"

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Differential Impedance and Insertion Loss Applied to Sockets

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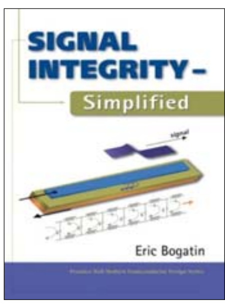
 www.BeTheSignal.com

Outline

- ✓ Who cares?
- ✓ What design features influence insertion loss?
- ✓ What is impedance
- ✓ What design features influence impedance?
- ✓ What is differential impedance
- ✓ What design features influence differential impedance
- ✓ What is differential insertion loss?

"It is better to uncover a little than to cover a lot"
- Francis Low

For More Information



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Electrical Performance of Sockets in Perspective

- Performance
  - ✓ Compliance
  - ✓ Pitch
  - ✓ Cycle lifetime
  - ✓ Time between cleaning
  - ✓ Electrical
    - – DC resistance
    - – Hi Frequency
      - – Signal Integrity
        - » Bandwidth
        - » Insertion loss
        - » Return loss
        - » SPICE models
      - – Power integrity
        - » Loop inductance

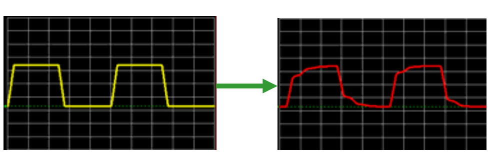
Constraints:
- **Vendors**
- **Corporate Culture**
- **Compatibility: Industry, Legacy**

Cost:
$$$, TCOO, Schedule, Risk

Partitioning:
- **Pin electronics**
- **Wiring/cabling**
- **Loadboards**
- **Sockets**

The Socket as a Component

- Purpose of an interconnect: "to transport a signal from one point to another with an acceptable level of distortion"



Simulated with HyperLynx

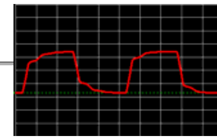
What's important to know?
1. Will the system work?
2. Is the socket "good enough?"
3. How do you know before you build it and test it?

3rd Best Alternative

- Specify values of model (circuit or behavioral) parameters
  - ✓ Z_0
  - ✓ TD
  - ✓ L
  - ✓ C
  - ✓ Insertion loss
  - ✓ Return loss
- Specifications based on ***assumptions*** of the rest of the system
- Specifications are a pre-arranged compromise- sometimes based on:
  - ✓ System level simulation balancing cost-performance-constraints- (really hard!)
  - ✓ A guess
  - ✓ Because it worked in the last design
  - ✓ Enough margin for designer to sleep at night
  - ✓ Assuming performance is free
  - ✓ Incorrect assumptions
  - ✓ Information that was passed from engineer to engineer to engineer to engineer…(only one of whom might have an idea of what they want)

Universally used metric to define "goodness" of a socket:

-1 dB insertion loss bandwidth



Is this acceptable?

Sometimes the frequency domain offers an easier path to the answer

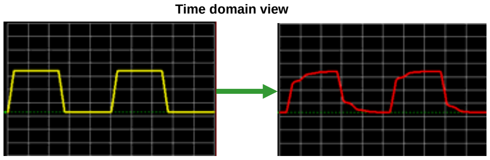
No new information in the frequency domain

The only reason we'd ever leave the time domain to go to the frequency domain:

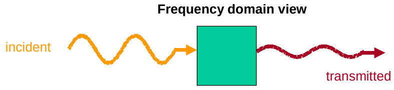
To get to the answer faster.

Two World Views

Time domain view



Frequency domain view

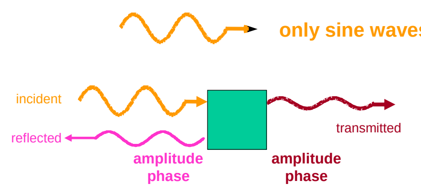


amplitude phase

Up to the highest sine wave frequency that is significant

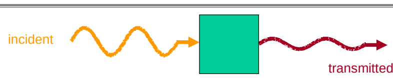
Transmitted Signals in the Frequency Domain

What are signals in the frequency domain?



Everything you ever wanted to know about the performance of a socket is contained in the reflected and transmitted signals

Terminology

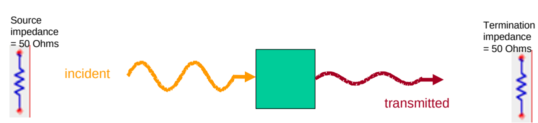


What's important: $\frac{V_{transmitted}}{V_{incident}}$ **at each frequency**

- Also called:
  - ✓ Insertion loss
  - ✓ S21
  - ✓ Transfer function

There is a magnitude and a phase at each frequency

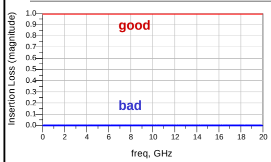
Most Important Caveat



- The source impedance and the load impedance when defining S21 is always 50 Ohms.
- Insertion loss has significance if the end use environment is 50 Ohms

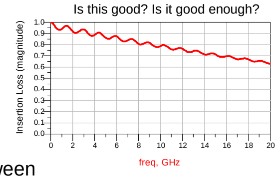
S21 is dominated by how the impedance of the socket matches the impedance of the test environment!

Good and Bad Insertion Loss



Simulated with Agilent ADS

Is this good? Is it good enough?



- Is there a difference between
  - ✓ good
  - ✓ good enough
  - ✓ better ?

-1 dB = 90% transmitted signal amplitude
-2 dB = 80% transmitted signal amplitude
-3 dB = 70% transmitted signal amplitude

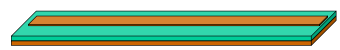
The Value of "-1 dB Insertion Loss Bandwidth" as a Metric

- Relative comparison
- First pass screening
- Rough, rule of thumb for usable operating frequency
- Should not be used to sign off on a design
  - ✓ too approximate
  - ✓ too much margin? Too little?
  - ✓ Too many assumptions
- Multiple approximations:
  - ✓ Bandwidth of the signal
  - ✓ Is the system a 50 Ohm system?
  - ✓ Total system budget
  - ✓ Allocation to the socket
- A better approach (and much more expensive):
  - ✓ Model and simulate

What Affects Insertion Loss of a Socket?

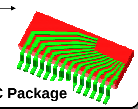
1. Matched Impedance
2. Controlled impedance
3. Discontinuities of load board
4. Length
5. Dielectric loss
6. Conductor loss
7. DC contact resistance

The Simplest Model of a Transmission Line



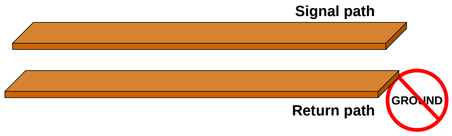
Microstrip

A "-1" order model:
Any two conductors with length

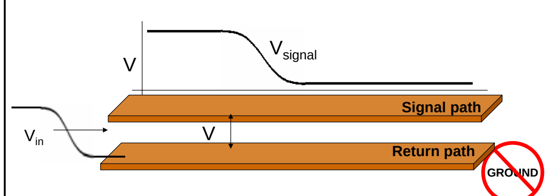


Lead frame of an IC Package

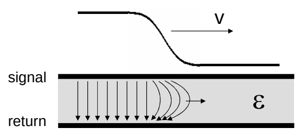
Labeling the Conductors



The Signal



How fast does a signal move down a line?

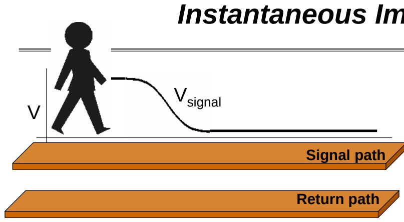


in air: v = 186,000 miles per sec

v = 12 inches/nsec

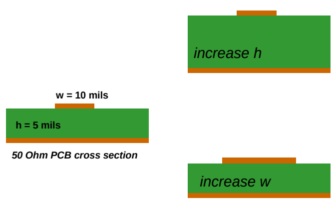
$$v = \frac{12\,\frac{inches}{n\sec}}{\sqrt{4}} = \frac{12\,\frac{inches}{n\sec}}{2} = 6\,\frac{inches}{n\sec}$$

Instantaneous Impedance



- Signal sees an “instantaneous impedance” each step along the path
- Instantaneous impedance depends on the geometry of signal and return path
- A controlled impedance when instantaneous impedance is constant
- One impedance that characterizes the interconnect:
- Characteristic impedance

Characteristic Impedance and Capacitance per Length



capacitance per length decreases, the characteristic impedance increases

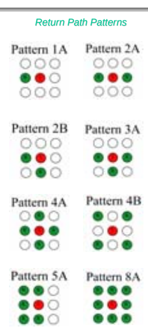
the capacitance per length increases, characteristic impedance decreases

$$Z_0 \sim \frac{1}{C_L}$$

Most Important Features of Characteristic Impedance

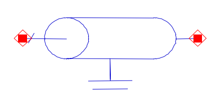
- Characteristic impedance is not about the signal path
- Characteristic impedance is not about the return path
- Characteristic impedance will depend both signal and return path, inseparably
- There is no such thing as the characteristic impedance of a single pin
- Change the return path configuration, you change the characteristic impedance
- *(Obviously, the same goes for insertion loss!)*

Return Path Selection Strongly Influences Single Ended Impedance

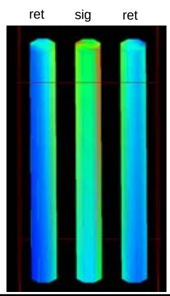


Ideal, Lossless transmission lines have just Two Parameters:

- Characteristic Impedance: Z0
- Time delay: TD

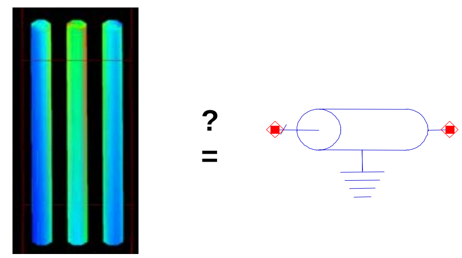


Pattern 2a: current flow at 20 GHz



Agilent ADS Momentum

How well do these pins look like an ideal transmission line?

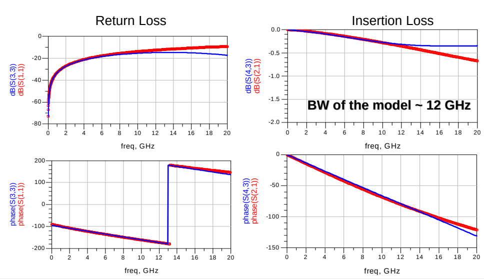


All Transmission Lines with the Same Characteristic Impedance and Time Delay Behave Exactly the Same

Agilent ADS

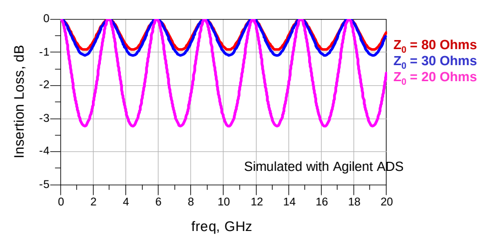
3D EM sim of the pin field

Simulated ideal transmission line (Z0 = 42 ohms)

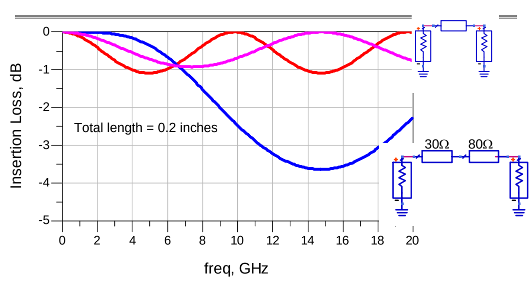


Minimizing Insertion Loss Principle #1: Match Impedance to 50 Ohms

1. Uniform impedance interconnect
2. Match socket to 50 Ohms
3. Keep: 30 Ohms < Z_0 < 80 Ohms and insertion loss will never be greater than -1 dB

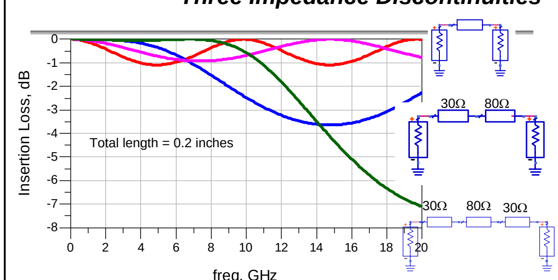


What if the Impedance is not Controlled?



- Low frequency behavior is related to ~ average impedance- can be better than either one
- Highest insertion loss can be much worse than either discontinuity (> 3x)

Three Impedance Discontinuities



- Low frequency behavior is related to ~ average impedance- can be better than either one
- Highest insertion loss can be much worse than either discontinuity (> 7x)

Minimizing Insertion Loss Principle #2: Use a controlled impedance interconnect

- Match average impedance to 50 Ohms
- Design for controlled impedance- uniform cross section

7 Principles of Socket Design for Optimized Insertion Loss

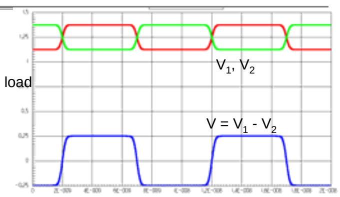
1. match characteristic impedance of socket to 50 Ohms
2. Keep the impedance constant through socket
3. Optimize (minimize) pad stack up capacitance
4. Keep socket short (shorter is better, but long may be good enough)
5. Dielectric loss of socket not critical
6. Conductor loss of socket not critical
7. Contact resistance of socket not critical

The Highest Speed Signals Are All Differential

Serial Data Interface (SDI):	0.27	→ 1.488		Gbps/pin
HyperTransport:	0.4	→ 1.2		Gbps/pin
Fibre Channel:	1.062	→ 2.125	→ 4.25	Gbps/pin
Serial RapidIO™:	1.25	→ 2.5	→ 3.125	Gbps/pin
PCI Express:	2.5	→ 5		Gbps/pin
XAUI	3.125	→ 6.25		Gbps/pin
Proprietary (Basic)	x	→ 2x	→ 3x	Gbps/pin

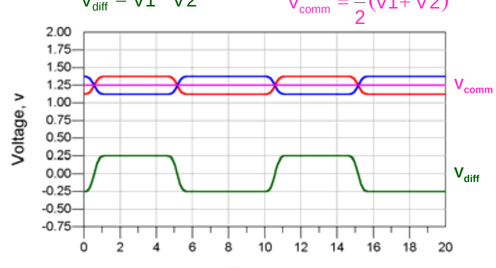
What is a differential signal?

Example:
National Semi DS92LV010A
Output swing:
1.125v to 1.375 v into 27 Ohm load



Differential and Common Signals

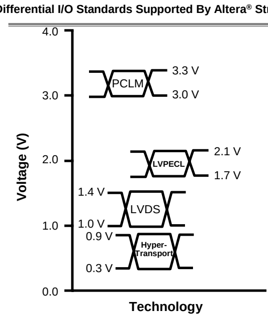
$V_{diff} = V1 - V2$ $V_{comm} = \frac{1}{2}(V1 + V2)$



There is a large common voltage component!

Differential Signals

Differential I/O Standards Supported By Altera® Stratix® Devices



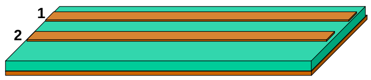
Diff Signal	Comm Signal
0.3 V	3.15 V
0.4 V	1.9 V
0.4 V	1.2 V
0.6 V	0.6 V

Note: There Is a Very Large Common Component

Courtesy of ALTERA Corp.

What's a Differential Pair Transmission Line?

Answer: .....*any* two, coupled transmission lines (with their return paths).



Optimized high speed performance for the special case: a symmetric pair, with matched time delay of both paths

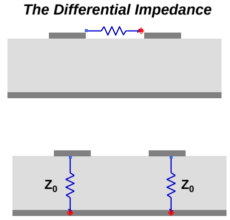
What's differential impedance?

! *Very Important Principle*

Differential impedance is the instantaneous impedance the difference signal sees

What is the Impedance the Differential Signal Sees?

The Differential Impedance



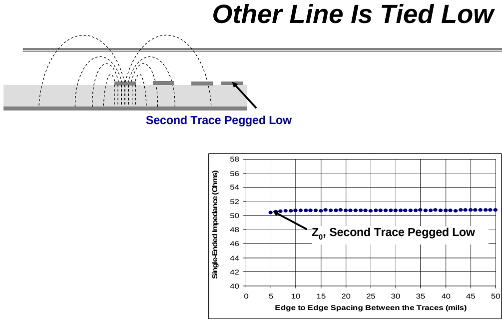
$Z_{diff} = Z_0 + Z_0$

What is the impedance of each line?

"…It Depends"

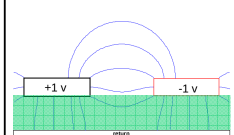
- No coupling: Z0 = single-ended characteristic impedance
- With coupling: depends on how the other line is driven
  - ✓ Other line is tied low
  - ✓ Other line is driven opposite (differential signal)
  - ✓ Other line is driven the same (common signal)

Other Line Is Tied Low

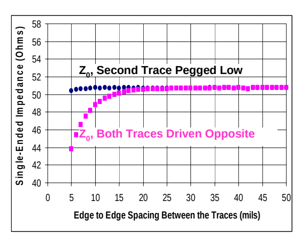


Polar Instruments SI8000

Other Line Driven Opposite

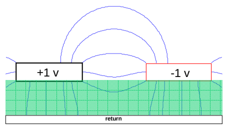


Differential Signal Odd Mode State



$Z_{diff} = 2 \times Z_{odd}$

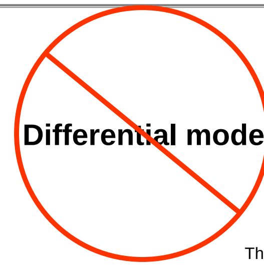
Pop Quiz



- If there is no coupling between the lines
  - ✓ How would we implement this?
- If each line had a single ended impedance of 50 ohms
  - ✓ What would be the differential impedance of the pair?

Ans: 100 ohms

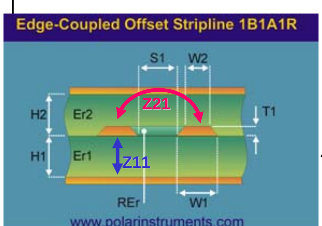
If 50 ohms is the universally used single ended impedance,
100 ohms is the universally used differential impedance



There is:
- Odd mode impedance
- Differential signals

What geometry terms influence differential impedance?

Re-train your intuition



Z11 ~ single ended impedance to the return path

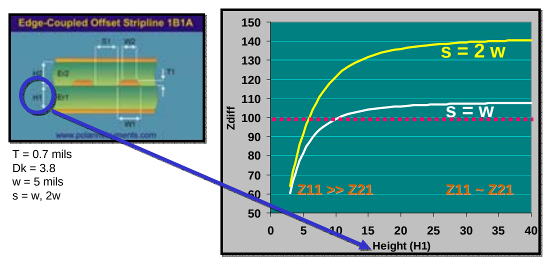
Z21 ~ the relative coupling between the two signal lines

$Z_{21} \sim Z_{11}\frac{V_2}{V_1}$ ~ induced noise on second signal line compared to the first signal line

$Z_{diff} = 2 \times (Z11 - Z21)$

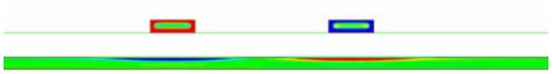
Easy: when Z11 >> Z21: no coupling, single ended case

As coupling dominates- different intuition is needed



Another way of thinking about coupling: the return current distribution

Current distribution in 2, 50 Ohm microstrips, @100 MHz
s = 3 x w



s = w

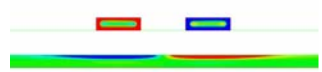
How much return current overlaps in the return plane?

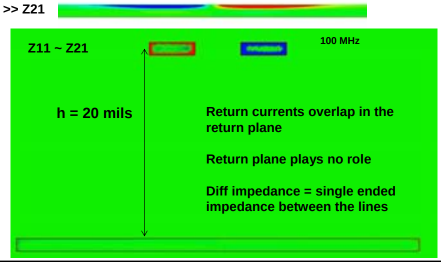
Ansoft 2D field solver

What is Z11 ?? Z21

Return Current in Closely Coupled Differential pair: plane close and far

Z11 >> Z21

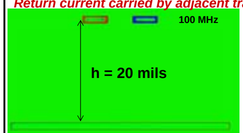




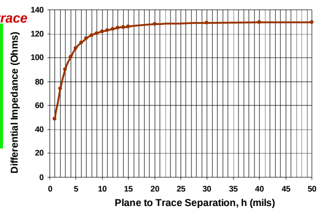
If Signal To Signal Coupling Is Much Tighter Than Signal To Return

Return current is carried by adjacent trace when the signal lines in the differential pair look like two isolated traces as part of a single ended transmission line.

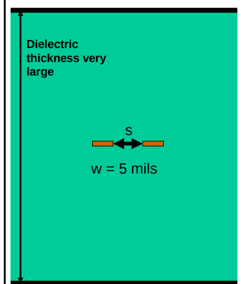
Return current carried by adjacent trace

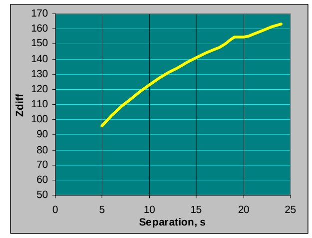


Current density scale expanded by 10x



When signal to signal coupling dominates- all return currents in planes overlap and cancel out. Planes play no role in diff impedance

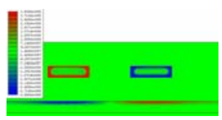




Return Currents in Differential Pairs

Most return current is carried by the plane when signal to return coupling >> signal to signal coupling

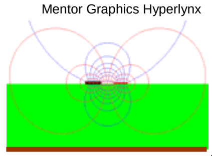
Ex: most board level interconnects



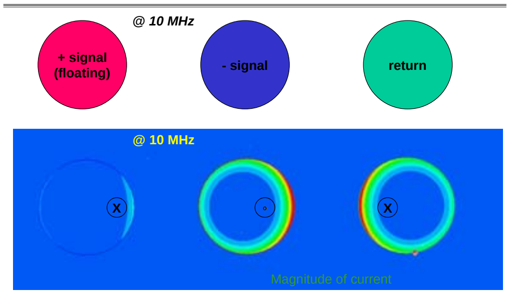
Mentor Graphics Hyperlynx

Most return current is carried by the other signal when signal to plane coupling << signal to signal coupling

Ex: most connectors, shielded twisted pair, twisted pair, sockets

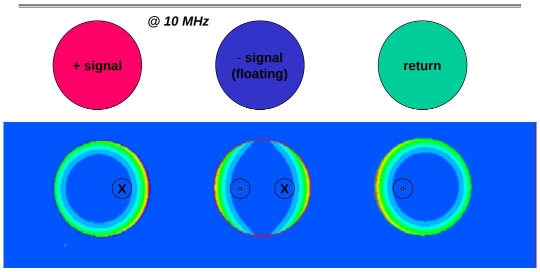


Single ended current in (-) pin

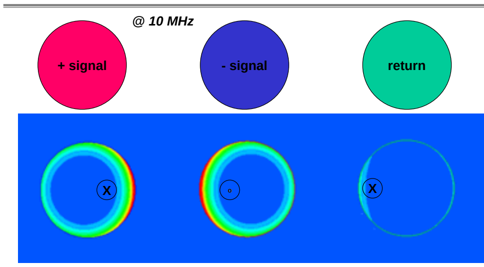


What would 1 GHz look like?

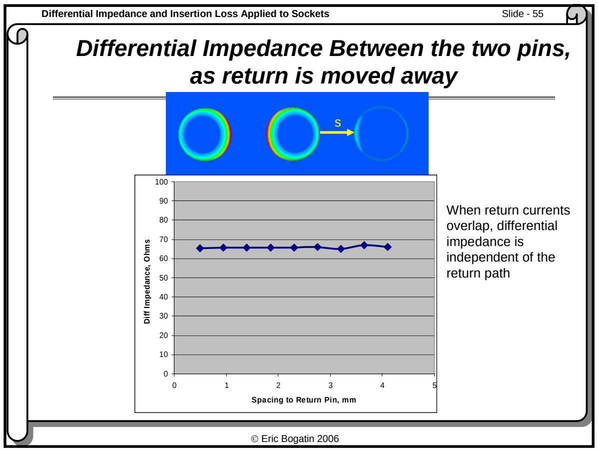
Single ended signal in (+) pin



Return Current for Differential Signal: Pattern 1a



Small amount of residual return current- mostly cancelled out


Differential Impedance and Insertion Loss Applied to Sockets
Slide - 55
Differential Impedance Between the two pins, as return is moved away
s
Diff Impedance, Ohms
Spacing to Return Pin, mm
When return currents overlap, differential impedance is independent of the return path
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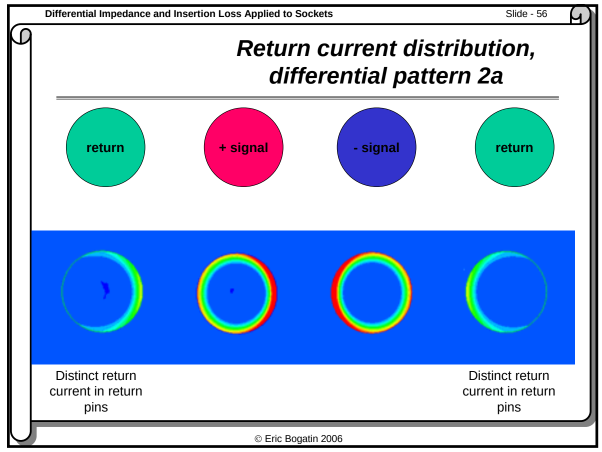
Differential Impedance and Insertion Loss Applied to Sockets
Slide - 56
Return current distribution, differential pattern 2a
return
+ signal
- signal
return
Distinct return current in return pins
Distinct return current in return pins
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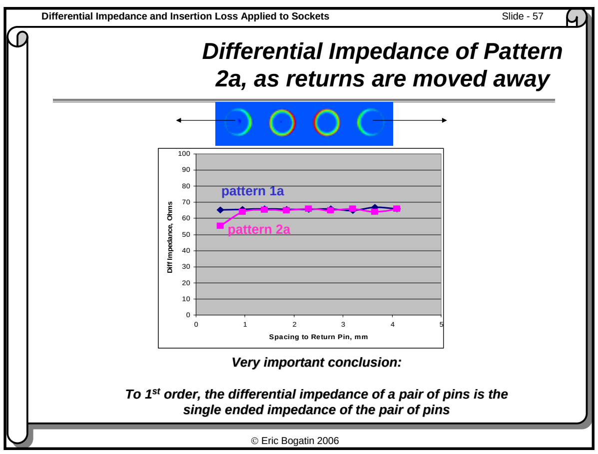
Differential Impedance and Insertion Loss Applied to Sockets
Slide - 57
Differential Impedance of Pattern 2a, as returns are moved away
pattern 1a
pattern 2a
Diff Impedance, Ohms
Spacing to Return Pin, mm
Very important conclusion:
To 1st order, the differential impedance of a pair of pins is the single ended impedance of the pair of pins
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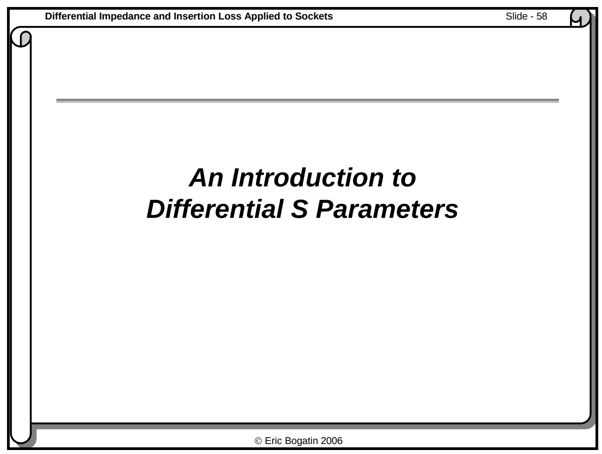
Differential Impedance and Insertion Loss Applied to Sockets
Slide - 58
An Introduction to Differential S Parameters
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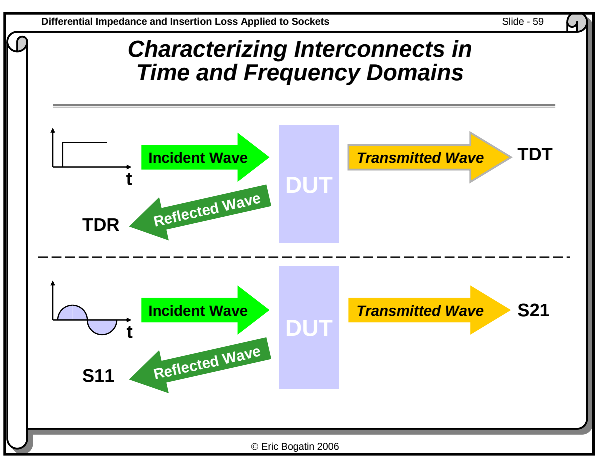
Differential Impedance and Insertion Loss Applied to Sockets
Slide - 59
Characterizing Interconnects in Time and Frequency Domains
t
Incident Wave
DUT
Transmitted Wave
TDT
Reflected Wave
TDR
t
Incident Wave
DUT
Transmitted Wave
S21
Reflected Wave
S11
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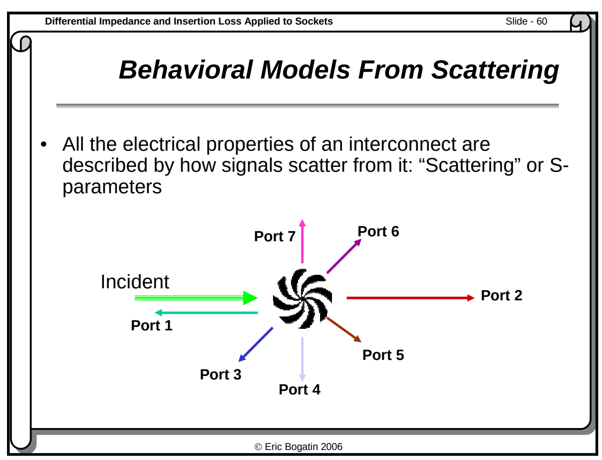
Differential Impedance and Insertion Loss Applied to Sockets
Slide - 60
Behavioral Models From Scattering
• All the electrical properties of an interconnect are described by how signals scatter from it: "Scattering" or S-parameters
Port 7
Port 6
Incident
Port 2
Port 1
Port 5
Port 3
Port 4
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4-Port Single-Ended S-Parameters Matrix for Differential Channel Characterization

1 ―― 2

3 ―― 4 (and their return paths!)

$$S_{out,in} = \frac{V_{out}}{V_{in}}$$

Stimulus

Response				
	S_{11}	S_{12}	S_{13}	S_{14}
	S_{21}	S_{22}	S_{23}	S_{24}
	S_{31}	S_{32}	S_{33}	S_{34}
	S_{41}	S_{42}	S_{43}	S_{44}

Interpreting Single-Ended Measurements:

S_{11}: return loss, single ended

$S_{21}= S_{12}$: insertion loss, single ended

$S_{31}= S_{13}$: near-end cross talk

$S_{41}= S_{14}$: far-end cross talk

Differential S-Parameters

1 ―― 2

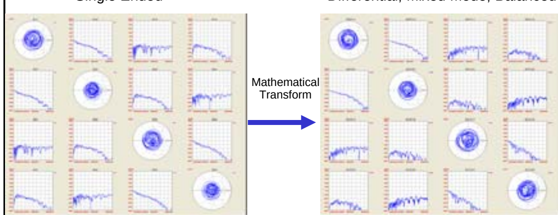
3 ―― 4 (and their return paths!) = Differential Pair Port 1 ―― Differential Pair Port 2 (and their return paths!)

			Stimulus			
			Differential Signal		Common Signal	
			port 1	port 2	port 1	port 2
Response	Differential Signal	port 1	SDD11	SDD12	SDC11	SDC12
		port 2	SDD21	SDD22	SDC21	SDC22
	Common Signal	port 1	SCD11	SCD12	SCC11	SCC12
		port 2	SCD21	SCD22	SCC21	SCC22

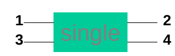
4-Port S-Parameter Matrices

Single Ended

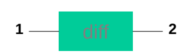
Differential, Mixed Mode, Balanced



Differential Insertion Loss: SDD21



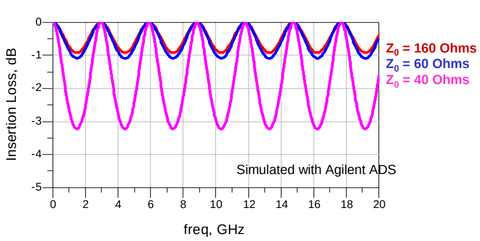
Measure the single ended S parameters values



Sdd11(2,1) = 0.5 x (S(2,1) - S(2,3) - S(4,1) + S(4,3))

Minimizing Insertion Loss Principle #1: Match Differential Impedance to 100 Ohms

1. Uniform impedance interconnect
2. Match socket to 100 Ohms
3. Keep: 60 Ohms < Z_0 < 160 Ohms and insertion loss will never be greater than -1 dB



7 Principles of Socket Design for Optimized Differential Insertion Loss

1. Match differential impedance of socket to 100 Ohms
2. Keep the impedance constant through socket
3. Optimize (minimize) pad stack up capacitance
4. Keep socket short (shorter is better, but long may be good enough)
5. Dielectric loss of socket not critical
6. Conductor loss of socket not critical
7. Contact resistance of socket not critical

Summary

- Differential impedance will proliferate
- Differential impedance target is 100 ohms
- -1 dB Insertion loss bandwidth is a universally used metric for socket performance
- It is only a rough approximation to the end use performance
- Same intuition about single ended bandwidth performance applies to differential insertion loss bandwidth performance

The End

SYNERGETIX

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