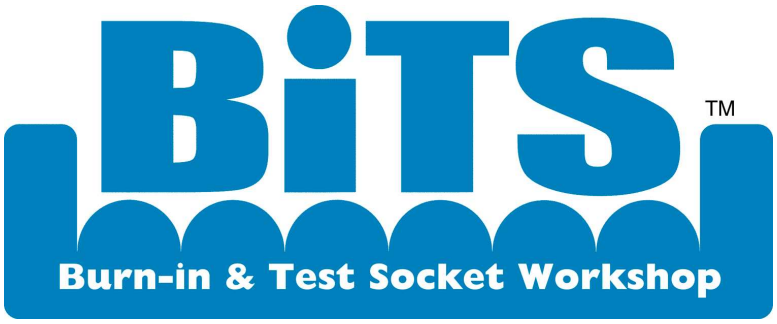


ARCHIVE 2006

Session 8

Test And Burn-in Efficiency Initiatives

"Enabling High Volume Testing Of MCP Memory"
Ken Karklin — Agilent Technologies

"An Alternative Test For Verifying Connectivity On High Pin Count Devices During Burn-in"
Rick Larson, PE — Texas Instruments, Inc.
Bunny Gaab — Enplas Tesco, Inc.

"Minimizing Spring Probe Operational Cost Using Optimized Maintenance Techniques"
Erik Orwoll — Nu Signal LLC

Enabling High Volume Testing of MCP Memory

Efficiency Initiatives Session

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Agilent Technologies

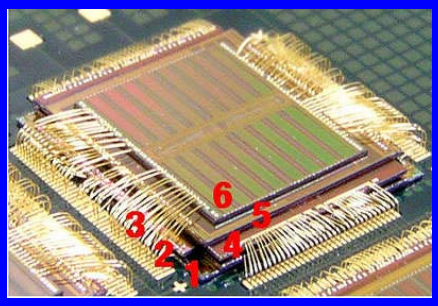
Ken Karklin
Test Cell Integration Manager, MTS

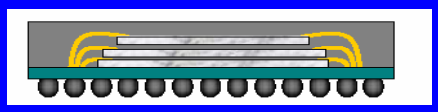
Outline

- Mobile Memory / MCP Growth
- Need for More Effective Solutions
- The Matrix MCP Solution
- Massive Parallelism = Massive Connections
- Complex Electromechanical Challenges
- Achieving Signal Performance at the DUT
- Handler Roadmap & Conclusion

Mobile Memory / MCP Growth

- Fueled by the mobile device market
- These Multi-Chip Packages (MCP) devices combine multiple memories in one stacked unit
- By 2009, nearly ½ of all FLASH memory will destined for a MCP





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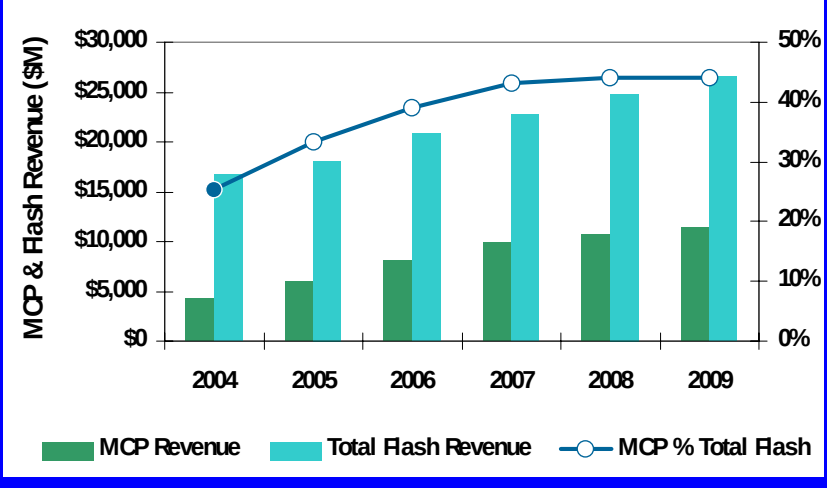
MCP Growth (continued)



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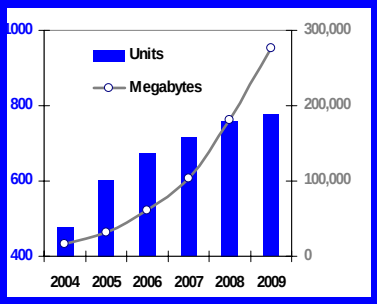
MCP Growth (continued)

High Mix/Low Volume vs. Monolithic Memory
… and likely to stay that way!

- "We counted 200 million MCPs shipped in 2003, and that number could easily exceed 500 million in 2008." – ***Richard Gordon, Gartner/Dataquest (Dec '04)***
- "MCP unit shipments should remain in the 600-800 million range over the 2005-09 forecast period." ***– iSuppli (Feb '05)***



Data: iSupply

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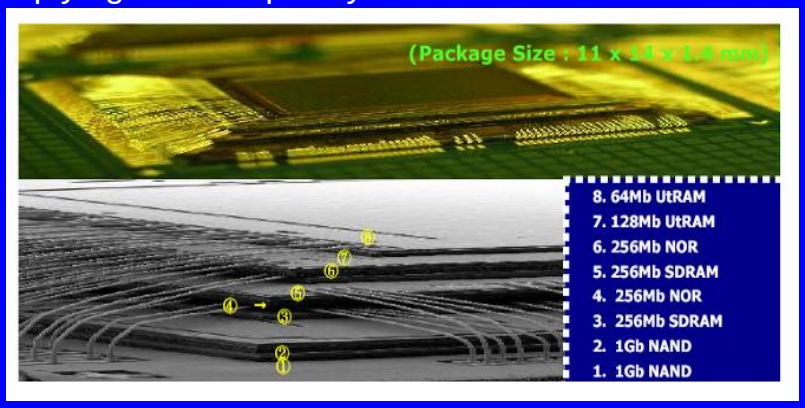
Multiple Types of Memories in MCPs

Multiplying the Complexity of the Test Problem



Source: Courtesy of Samsung Semiconductor, Inc.

- Requires a 123 pin/Site tester with 200Mb/S performance and Flash test capability.

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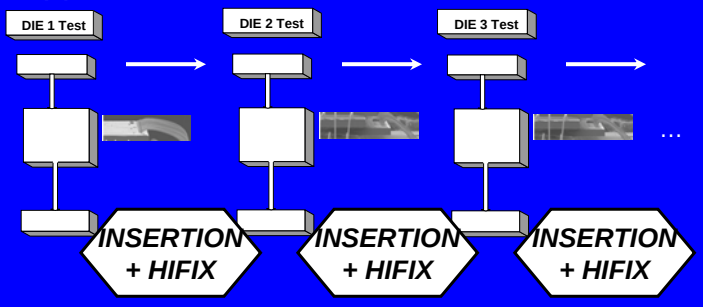
Need for More Effective Test Solutions

- Traditional Memory Tester Operational Flow Applied to MCP



- Alternative? Highly custom HiFix with << //
  - Thousands of discrete relays, cooling, cost, << reliability

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One MCP focused Solution:

- V5500 = 4096 I/0
- Matrix = x 6 resource multiplier
- Effective ***24,586*** I/O at test plane

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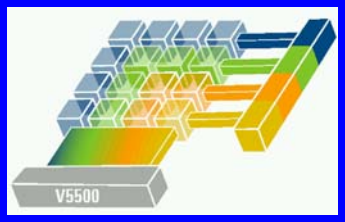
... Matrix Interface Solution (continued):



- Each I/O channel selectable switching to any/all of 6 DUT resource locations
- Alternatively, switch any DUT resource to one of 8 programmable voltage levels
- MCP tested in one insertion – Global test program execution

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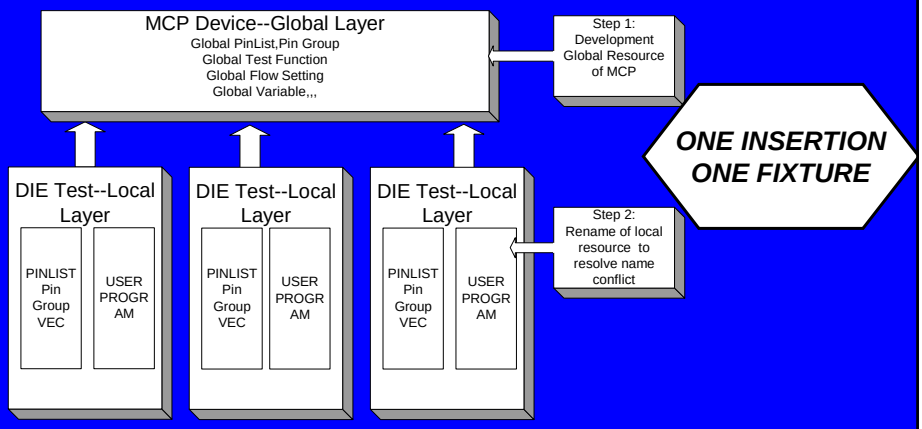
Matrix Interface Application Test Flow Combine Into One



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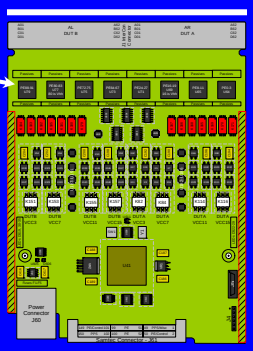
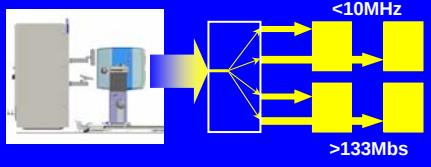
… Matrix Interface Solution (continued):

- HW Core of Solution:
  - Kiowa Custom ASIC
    - Located ~2" from DUT
    - Low leakage
    - High Bandwidth
  - Ultra High Density Interconnect

DUT Plane





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… Matrix Interface Solution (continued):

768 I/O + + Per Slice

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Is This Really Different?

Haven't we been doing this with relays for years?

- How is this different than what has been done with relays?
  - All channels can be switched: equivalent ~60k relays
  - Universal: doesn't increase cost of each load board
  - Relays don't provide high performance fan-out
  - Provides ability to maintain state of switched pins
- Why not put this on the load board?
  - Reliability becomes impossible
  - Cost, Lead-Time
  - Only manufacturable way to do in load-board/Hifix is to dramatically reduce parallelism

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… Matrix = Parallelism @ DUT Plane

- x320 DUT // MCP for TW320 Handler Pictured
- Up to 512 DUT Possible
- Only limited today by handler solutions

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Matrix = Massive Resources at DUT Plane … and Big Electromechanical Challenges

- >55,552 total contacts @ ~40gf
- 5 ton total force across minimal stroke
- Leverage 4-bar linkage w/ cam x 2 DUT attach planes
- Manually actuated simple and robust

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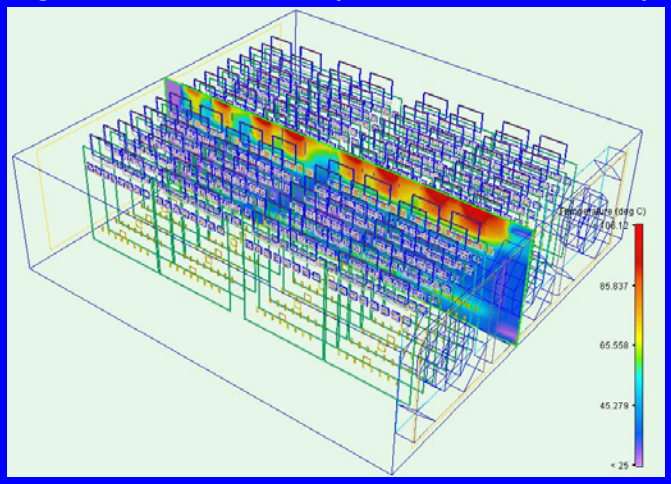
Matrix Thermal Challenges Addressed

- Designed / tested for up to 150C test temperature



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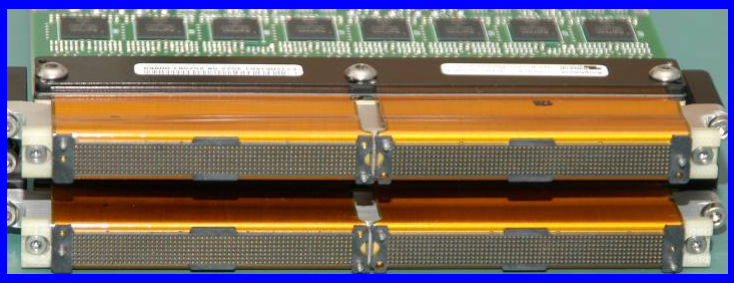
Electromechanical Challenges: … Contact Performance a *Statistical* Game

- Reliability, Modularity, Replace-ability
- Integrated Commodity Interposer Technologies



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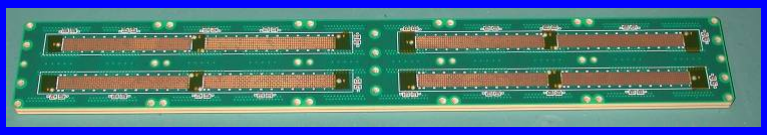
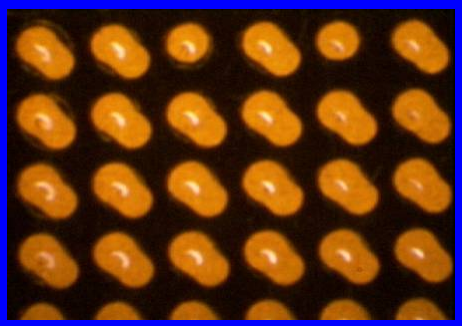
Matrix Socket Board Density

- Alignment challenges solved across temperatures





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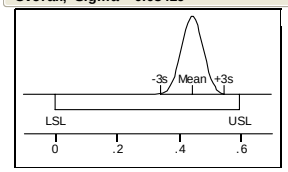
Matrix Interface Performance

– DC Performance (ohms): Including Flex, Interposer Contact to DUT Board

Capability Analysis

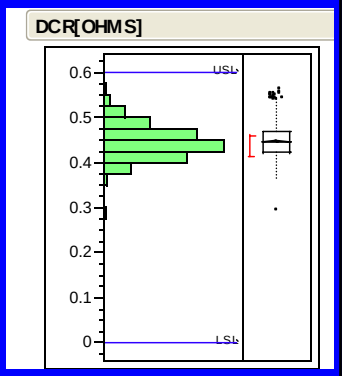
Specification	Value	Portion	% Actual
Lower Spec Limit	0	Below LSL	0.0000
Upper Spec Limit	0.6	Above USL	0.0000
Spec Target	.	Total Outside	0.0000

Overall, Sigma = 0.03419



Capability	Index	Lower CI	Upper CI
CP	2.925	2.841	3.009
CPK	1.504	1.459	1.549
CPM	.	.	
CPL	4.346	4.221	4.471
CPU	1.504	1.459	1.549

Portion	Percent	PPM
Below LSL	0.0000	0.0000
Above USL	0.0003	3.1999
Total Outside	0.0003	3.1999



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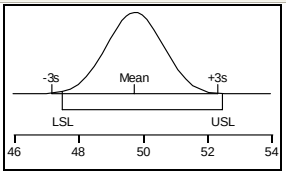
Matrix X-Mission Line Performance

– Zo Performance (ohms): Including Flex, Interposer Contact to DUT Board

Capability Analysis

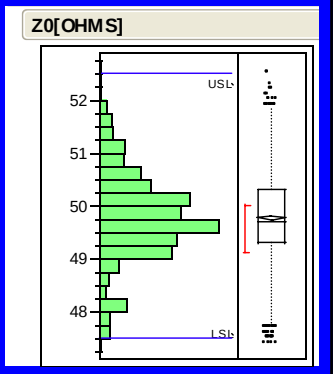
Specification	Value	Portion	% Actual
Lower Spec Limit	47.5	Below LSL	0.1674
Upper Spec Limit	52.5	Above USL	0.0000
Spec Target	.	Total Outside	0.1674

Overall, Sigma = 0.85734



Capability	Index	Lower CI	Upper CI
CP	0.972	0.944	1.000
CPK	0.881	0.853	0.910
CPM	.	.	.
CPL	0.881	0.853	0.910
CPU	1.063	1.030	1.095

Portion	Percent	PPM
Below LSL	0.4094	4093.5506
Above USL	0.0717	716.8909
Total Outside	0.4810	4810.4415



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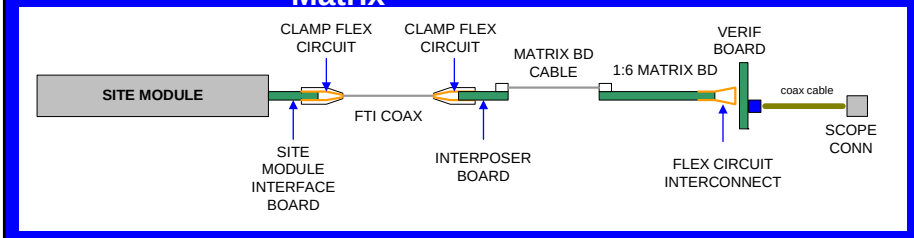
Driving Signals Through Matrix

Signal Path With 1:6 Matrix



BITS 2006 Enabling High Volume Testing of MCP Memory 21

Handler Roadmap

Handler "M1"
256-320 DUT

Handler "T1"
256-320 DUT

Handler "M2"
384+ DUTs

Nov	Dec	Jan	Feb	Mar	Apr	May	June	July	Aug	Sept
21 28	5 12 19 26	2 9 16 23	30 6 13 20 27	6 13 20 27	3 10 17 24	1 8 15 22 29	5 12 19 26	3 10 17 24 31	7 14 21 28	4 11 18 25

Handler "T2"
320 DUT

- Supporting available and evolving solutions
- **Each requires optimized electromechanical assembly**

Handler "T3"
384 DUT

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Summary

- MCP growth is substantial
- MCPs create test complexity
- The matrix MCP provides an efficient, low COT solution
- Extreme Parallelism challenges solved:
  - Novel ASIC design / placement
  - Electromechanical innovation
  - Breakthrough interconnect technology
- Integrate to multiple handlers
- Enabling the mobile-device MCP memory explosion !

BITS 2006 Enabling High Volume Testing of MCP Memory 23

Acknowledgements

- Sanjeev Grover, Agilent, for tireless debug, data taking & superb high density electrical design
- Todd Sholl and Steve Bellato, Agilent, for innovative mechanism design, debug and product validation
- Vick Kovacevic, Ben Morris and Kurt Gusinow, for helping me to understand the economic dynamics on MCP test
- Mirae Corporation for their cooperation
- TechWing Co. Ltd, for their cooperation

BITS 2006 Enabling High Volume Testing of MCP Memory 24

AN ALTERNATIVE TEST FOR VERIFYING CONNECTIVITY ON HIGH PIN COUNT DEVICES DURING BURN-IN

2006 Burn-in and Test Socket Workshop

Rick Larson
Texas Instruments, Inc.

Bunny Gaab
Enplas Tesco, Inc.

Agenda

- Objective
- Test description
- Pattern development & evaluation
- Test results
- Set up requirements
- Advantages & disadvantages
- Conclusions

2

Objective

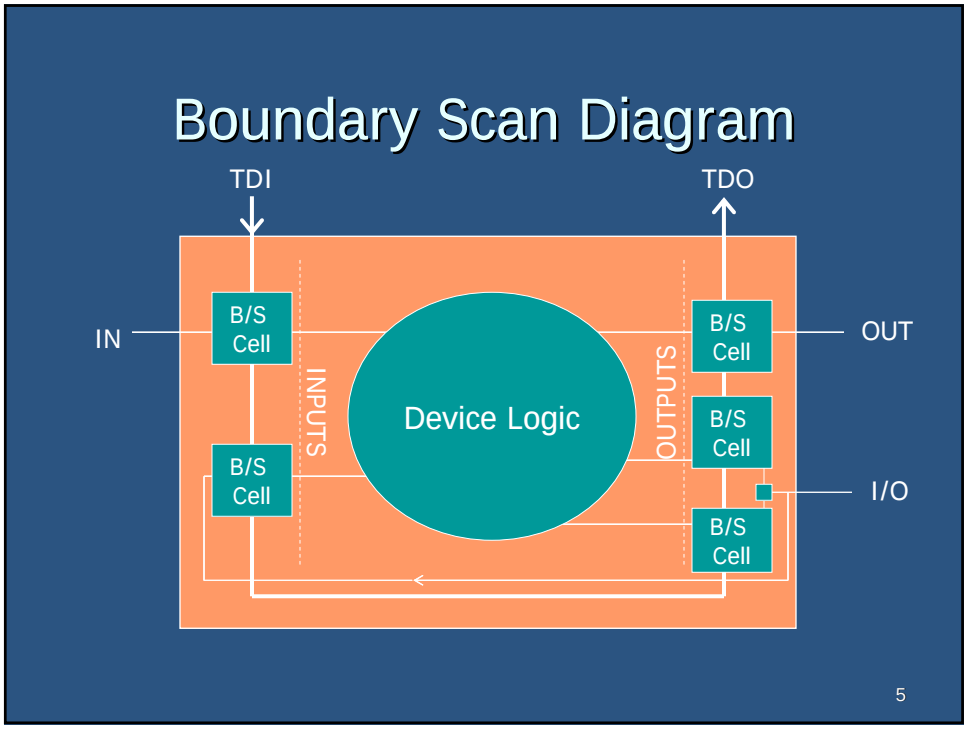
- To find a method for quickly isolating a contact related failure at a burn-in socket position for a minimal amount of cost
- To be able to verify connectivity of a high-pin count DUT at burn-in temperatures

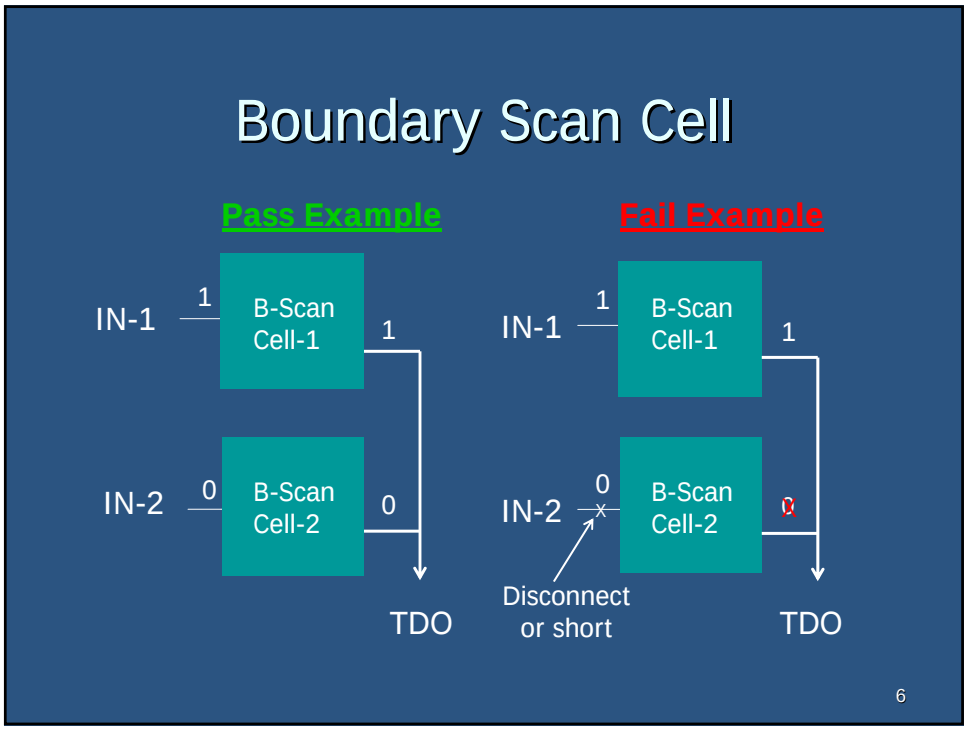
3

Test Used

- JTAG Boundary Scan
  - IEEE 1149.1 Standard Test
  - Typically used by board manufacturers for verifying IC-to-PCB interfacing

4


Boundary Scan Diagram
TDI
TDO
IN
B/S Cell
INPUTS
Device Logic
OUTPUTS
B/S Cell
B/S Cell
OUT
B/S Cell
B/S Cell
I/O
B/S Cell
5

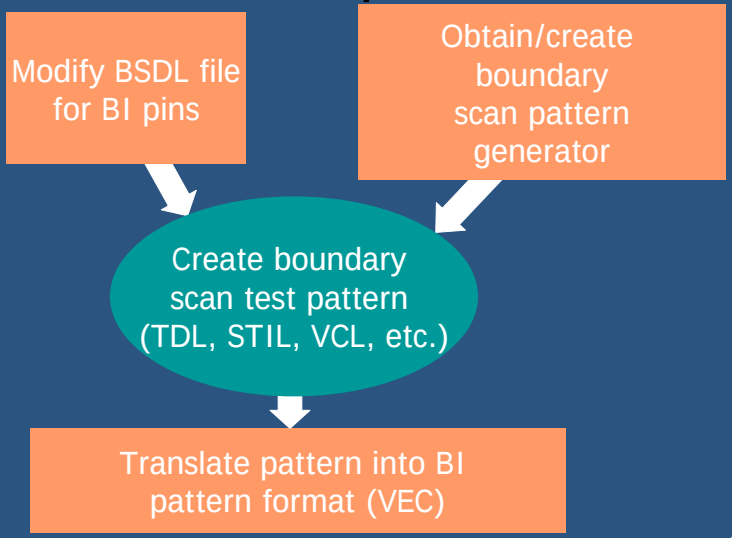

Boundary Scan Cell
Pass Example
Fail Example
IN-1
1
B-Scan Cell-1
1
IN-2
0
B-Scan Cell-2
0
TDO
IN-1
1
B-Scan Cell-1
1
IN-2
0
B-Scan Cell-2
0
Disconnect or short
TDO
6

Test Set Up

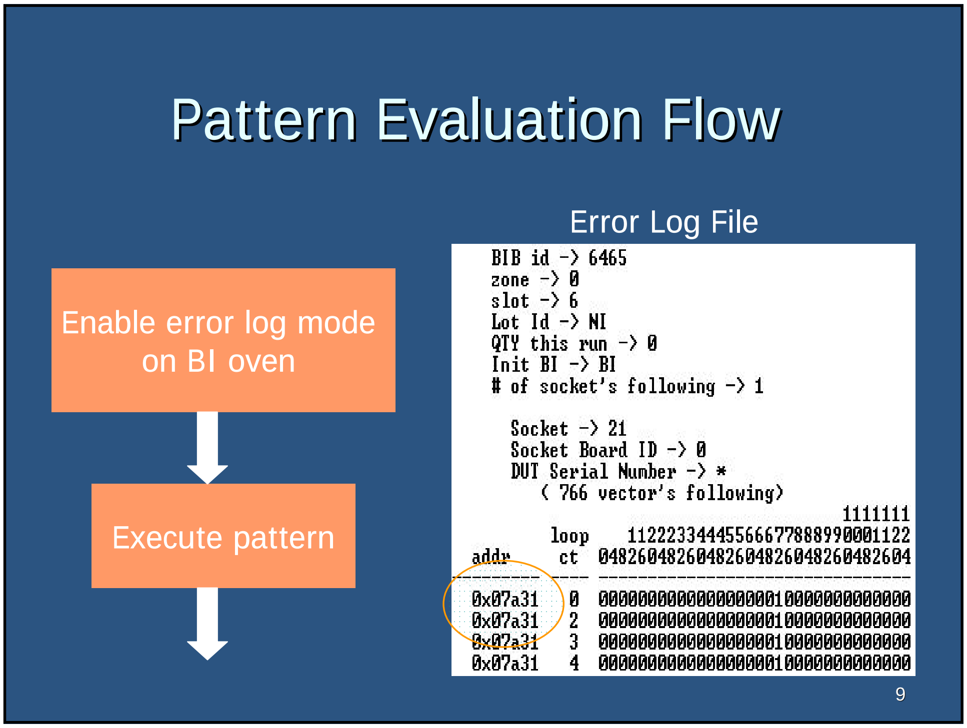
- Device
  - Niagara (Sun Microsystems)
  - 1933 pin LGA with a 1mm pitch (51mm body)
- BI Stress Needs
  - Scan & BIST (~100 pins)
- Burn-in oven
  - MCC HPB-3
- Socket
  - Clam shell compression mount socket

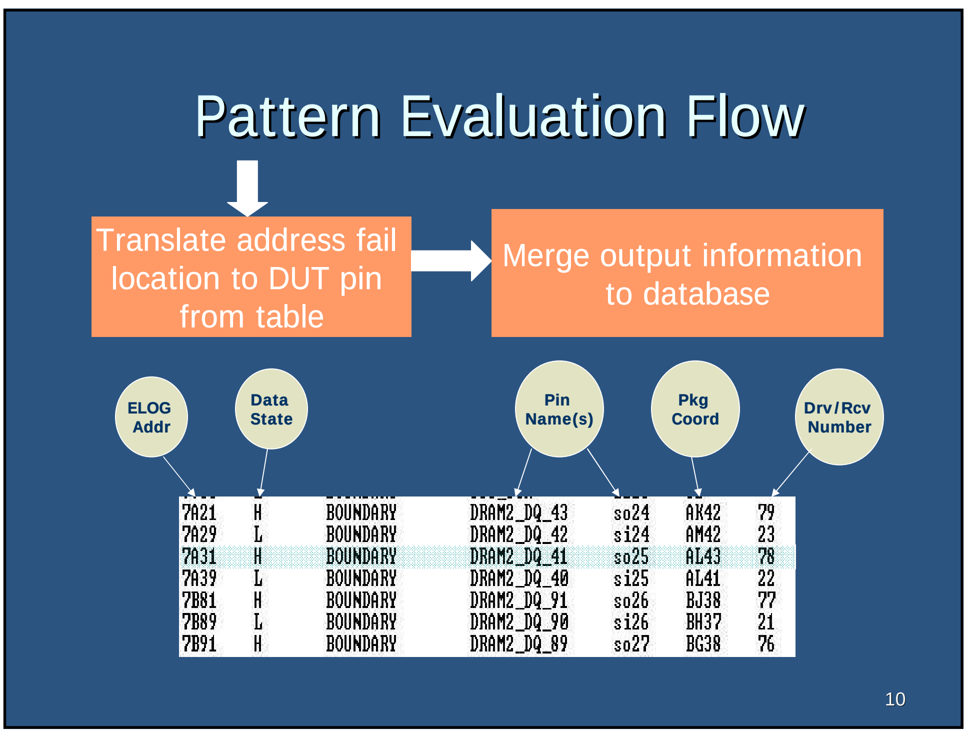
7

Pattern Development Flow



8


Pattern Evaluation Flow
Enable error log mode on BI oven
Execute pattern
Error Log File
BIB id -> 6465
zone -> 0
slot -> 6
Lot Id -> NI
QTY this run -> 0
Init BI -> BI
# of socket's following -> 1
Socket -> 21
Socket Board ID -> 0
DUT Serial Number -> *
(766 vector's following)
1111111
loop 11222334445566677888990001122
addr ct 04826048260482604826048260482604
0x07a31 0 00000000000000000001000000000000
0x07a31 2 00000000000000000001000000000000
0x07a31 3 00000000000000000001000000000000
0x07a31 4 00000000000000000001000000000000
9


Pattern Evaluation Flow
Translate address fail location to DUT pin from table
Merge output information to database
ELOG Addr
Data State
Pin Name(s)
Pkg Coord
Drv/Rcv Number
7A21 H BOUNDARY DRAM2_DQ_43 so24 AK42 79
7A29 L BOUNDARY DRAM2_DQ_42 si24 AM42 23
7A31 H BOUNDARY DRAM2_DQ_41 so25 AL43 78
7A39 L BOUNDARY DRAM2_DQ_40 si25 AL41 22
7B81 H BOUNDARY DRAM2_DQ_91 so26 BJ38 77
7B89 L BOUNDARY DRAM2_DQ_90 si26 BH37 21
7B91 H BOUNDARY DRAM2_DQ_89 so27 BG38 76
10

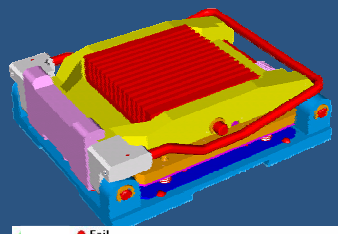
Development Results

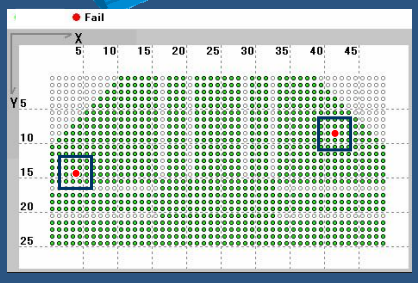
- Quickly identified broken isolation resistors on burn-in board

11

Development Results

- Enabled socket supplier to isolate exact contact location of problem sockets during prototype evaluations …

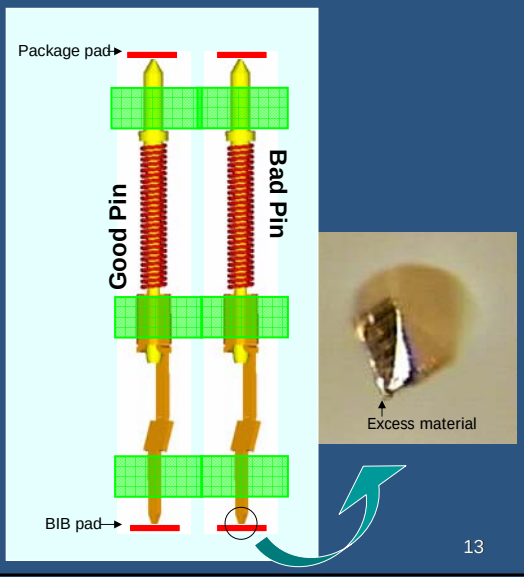




12

Development Results

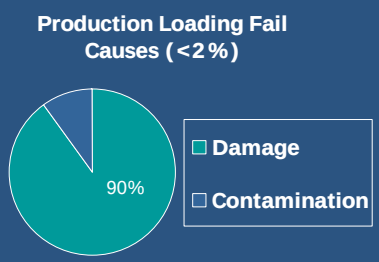
- .... analyzing only 2-5 pins out of the possible total of 1933 pins per socket.

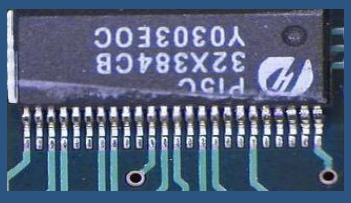


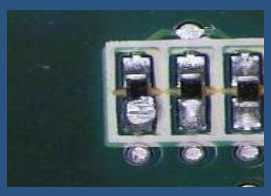
13

Production Results

- Majority of failures attributed to parts being dropped during manual loading & unloading of BIBs

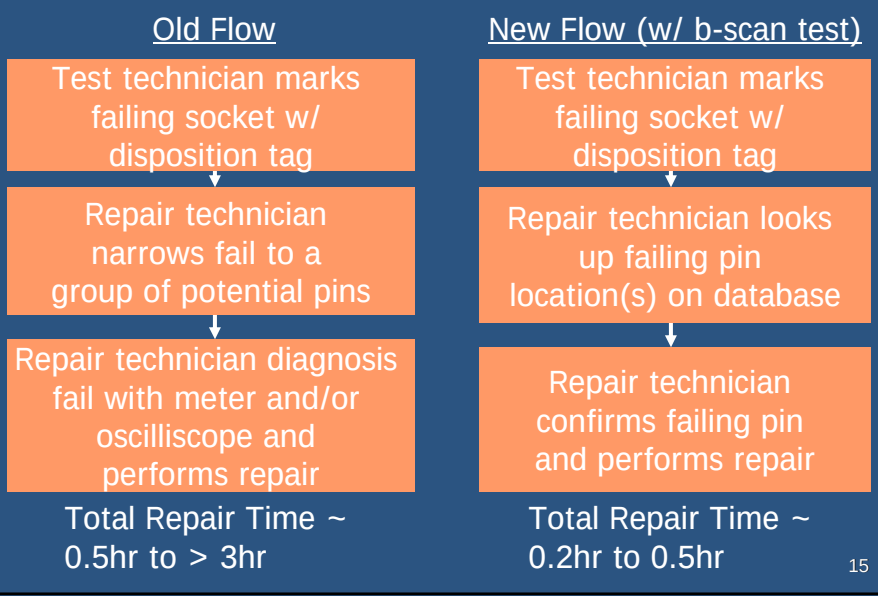






14

Repair Time Savings



15

Boundary Scan Requirements

- Designed into device
- Burn-in oven that can log failing output address locations to a pin channel
- Boundary Scan Description Language (BSDL) file
- Translators –
  - create JTAG pattern
  - convert pattern to burn-in oven format
  - modify error log output to device pin name & location

16

Advantages

- Enables a fast method for identifying contact related problems
- Test can be performed at burn-in conditions with actual devices
- No additional equipment costs required

17

Disadvantages

- Not able to verify connectivity on JTAG pins (TDO, TDI, TMS, TCK, TRST) or other pins not connected to boundary scan chain
- Initial development time to create custom pattern & translators

18

Conclusions

- Using a boundary scan test during burn-in has been found to a valuable tool for quickly identifying contact problems during burn-in development
- Performing a boundary scan test during production checkout has enabled BIB repair times to decrease by as much as 6x

19

Future Development

- Setup boundary scan test for non-driven IO pins
- Add in real-time translation and reporting of error log results during program executions

20

Acknowledgements

- Bunny Gaab - Enplas Tesco (socket)
- Micro Control Company (burn-in oven)
- Robert Young – TI (BI technician)

21

Minimizing Spring Probe Operational Cost Using Optimized Maintenance Techniques

2006 Burn-In and Test Socket Workshop
March 12 - 15, 2006

BiTS Burn-in & Test Socket Workshop

Erik Orwoll - Nu Signal LLC

Discussion Points

- *Where Do Probes Fail?*
- *Failure Modes / Causes*
- *Options To Address Failures*
- *Production Yields*

Failure Points

- *PCB Pad*
- *Spring Probe / PCB Interface*
- *Internal Probe Wear & Fatigue*
- *DUT Interface*

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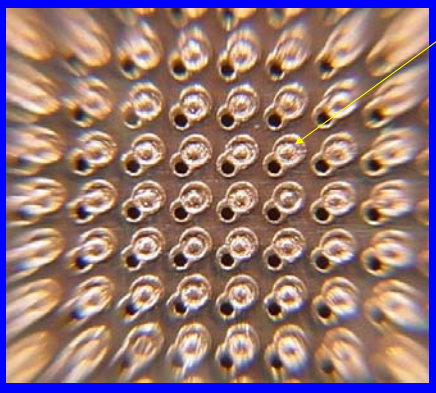
PCB Pad Wear



Abrasive Wear
Gold and Nickel Layers Compromised

Initial

Re-Plated

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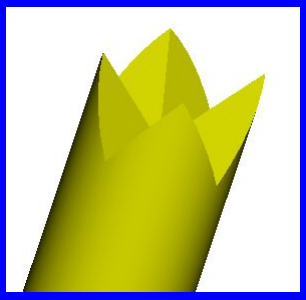
DUT Interface
Failure Modes

- Contamination
- Mechanical Wear
- Mechanical Damage



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DUT Interface
Contamination Sources

- Solder
- Resin
- Glycol
- Flux
- Dirt
- Device Binders / Adhesives
- Residue from alcohol and cleaning products

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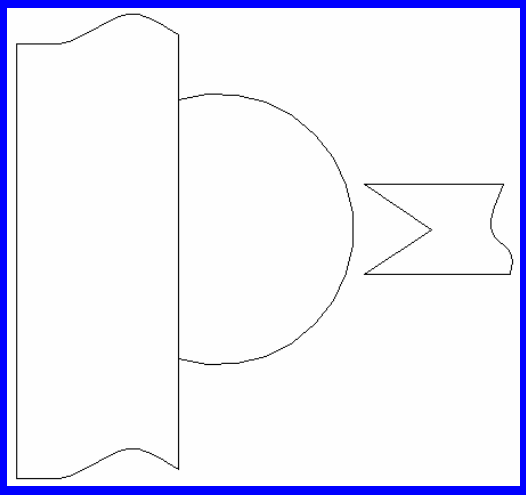
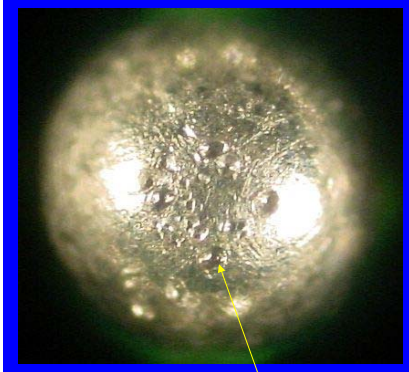
DUT Interface





Crown Point Witness Marks (Ambient)

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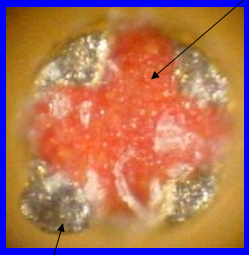
DUT Interface Contamination

Solder Contamination & Flattened Crown Points



Impregnated Resin

Damaged Point

Oxidized Solder

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Maintenance Methods Observed

- *Mechanical Cleaning*
  - *Abrasive Pads / Abrasive Media*
  - *Brushing*
  - *Adhesive (Sticky) Pads*
- *Chemical Contact Cleaners*
  (Oils result in device contamination)
- *Ultrasonic*
- *Air Hose / Air Blast*

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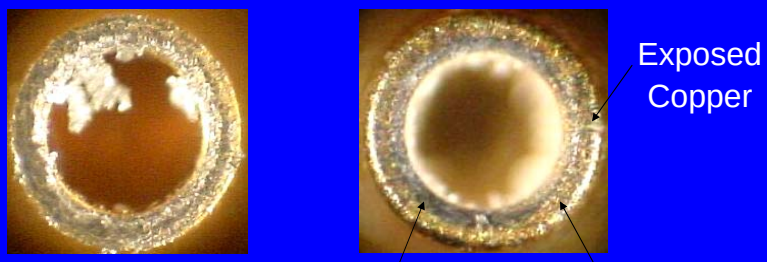
Brush Cleaning

- *Removes surface oxides*
- *Damages plating*

Solder Contamination **Solder Removed**



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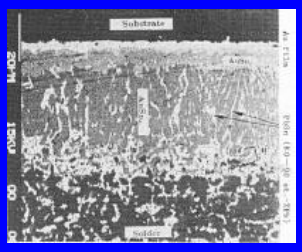
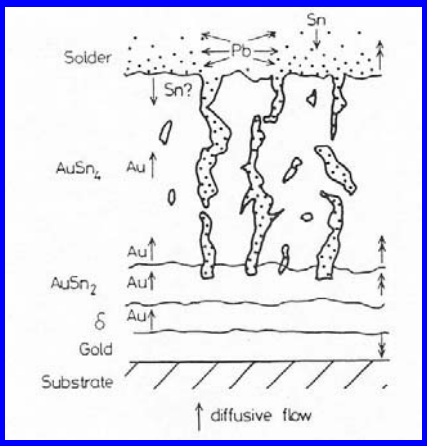
Solder Diffusion & Intermetallic Au-Sn Compound Formation





Source: Materials Science and Technology, September 1992, Vol. 8

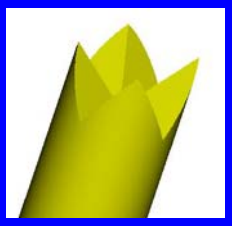
Solder Diffusion & Intermetallic Compound Formation

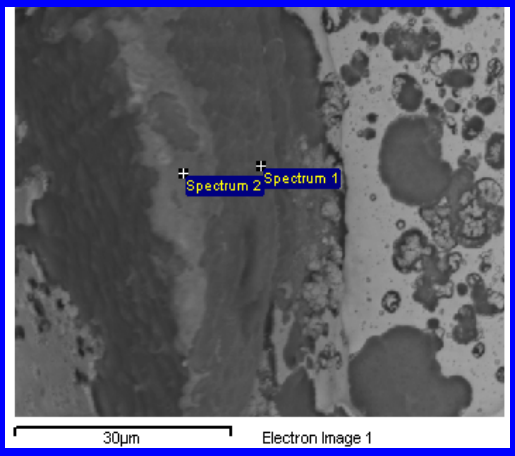
Solder Contamination QFP Contact

Solder Extracted Intermetallic Compounds Exposed

Non-Conductive Crystalline Structure

Gold Loss - Contact Tip





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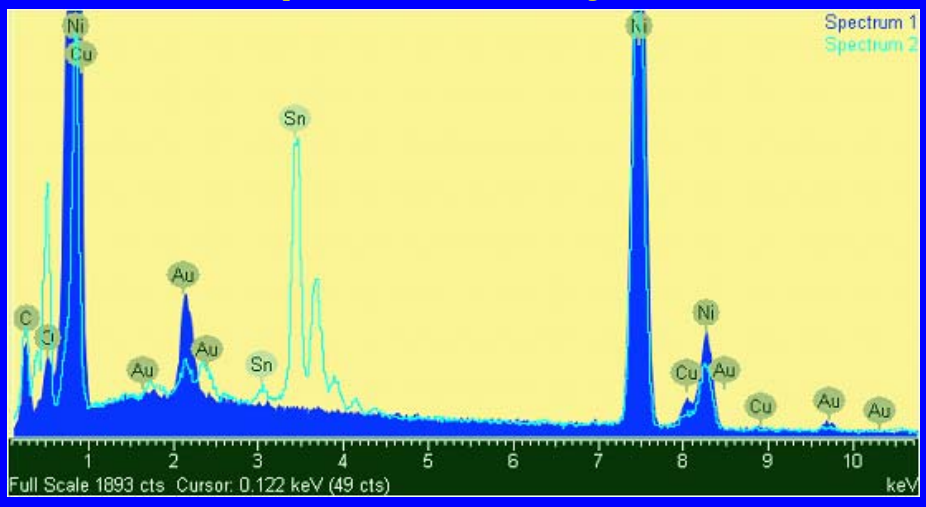
Spectrum Analysis



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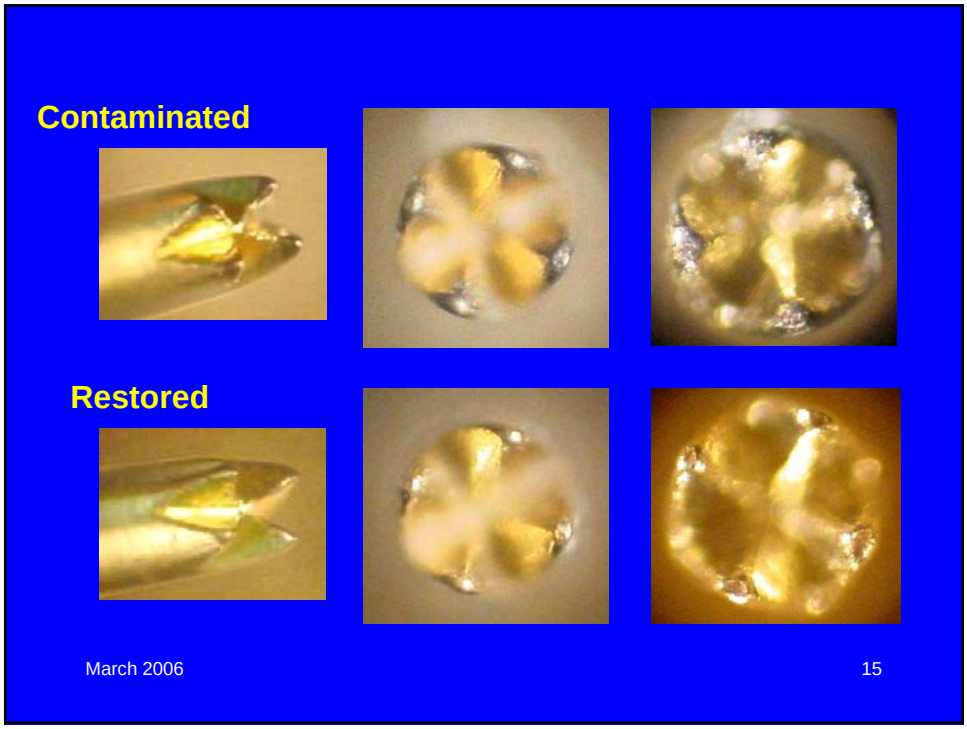
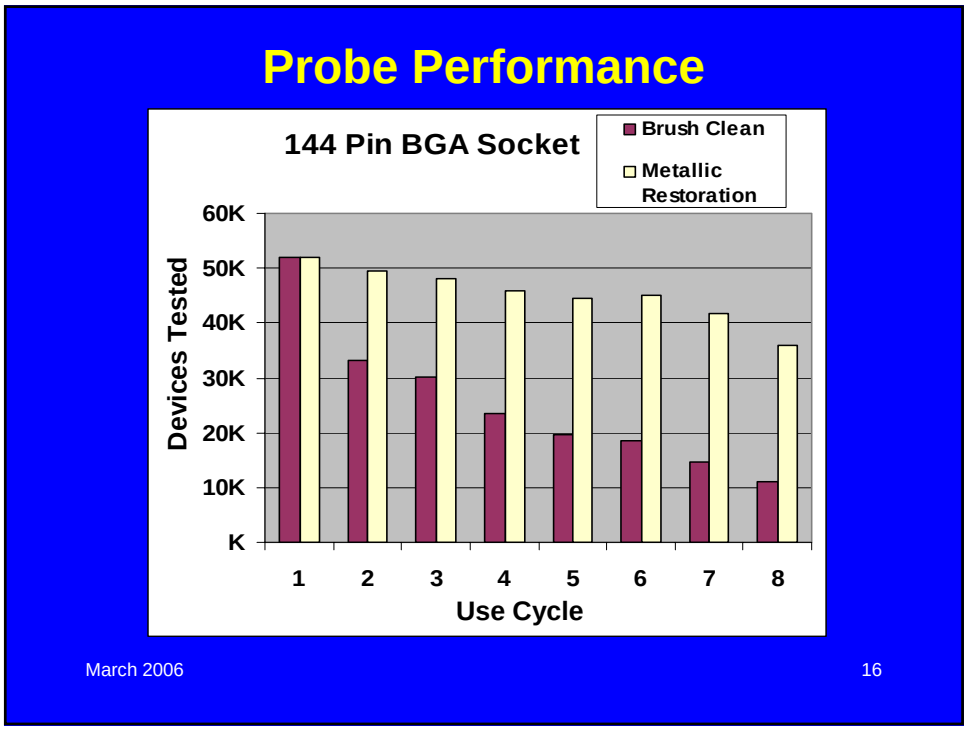
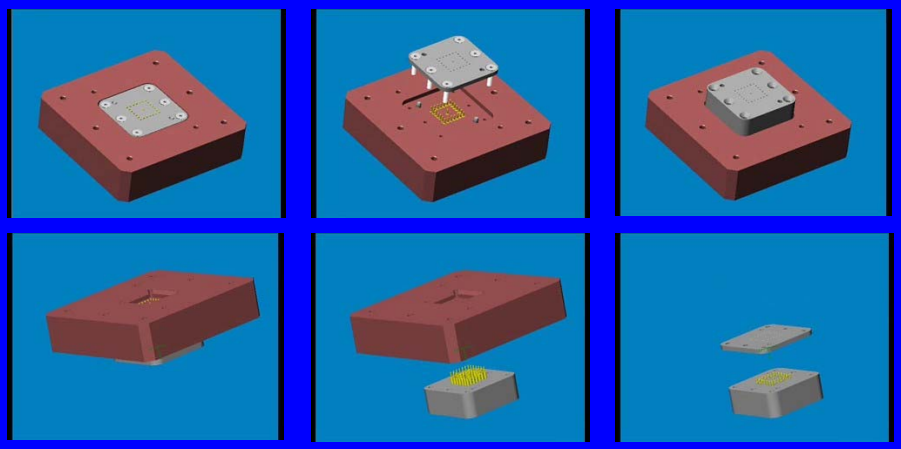

Contaminated
Restored
March 2006
15


Probe Performance
144 Pin BGA Socket
Brush Clean
Metallic Restoration
Devices Tested
60K
50K
40K
30K
20K
10K
K
1
2
3
4
5
6
7
8
Use Cycle
March 2006
16

Maintenance Fixtures



Fixture Allows Socket To Remain In Use

Probe Maintenance Performed Off-Line

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Thank You!

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