BiTS™
Burn-in & Test Socket Workshop

ARCHIVE 2006

Session 7

Thermal Management Advances

"DUT Thermal Management - An Overview Of Applied Passive Thermal Control Technology For Integrated Circuit Test"
F. D. Boatright — Delta Design, Inc.

"Thermal Control Units: Development Of An Analytical Model And Experimental Validation To Optimize The Voltage Input"
Sudhir Kumar, Khaled Elmadbouly, Praba Prabakaran
Kulicke & Soffa Industries

"Using A High Performance Micro-channel Cold Plate For Test And Burn-in"
Zahed Sheikh — Mikros Technologies

"Managing The Thermal Budget During Burn-In – A New Concept For Control"
Chris Lopez, Dr. James Forster, Trevor Moody
UMD Advanced Test Technologies

DUT Thermal Management

An Overview of Applied Passive Thermal Control Technology for Integrated Circuit Test

F. D. Boatright
Handler Applications Engineering
Delta Design A Cohu Company

2006 Burn-in and Test Socket Workshop
March 12-15, 2006

Delta Design, Inc *San Diego, CA*

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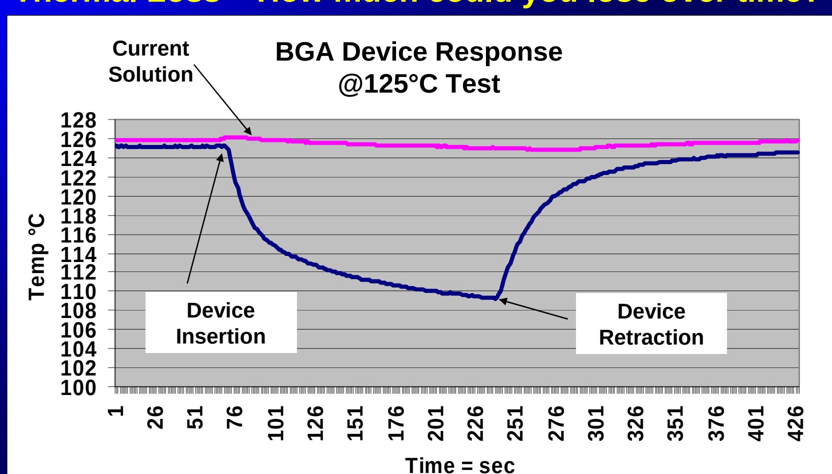
Leader in Worldwide Semiconductor Test Handling Solutions

Problem: Thermal Losses at the DUT

Thermal Loss – How much could you lose over time?



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DUT Thermal Management

Device Thermal Losses During Test

- Focus Areas for Root Cause
- Various Approaches for Limiting Losses
- Sample Test Data Sets
- Conclusions
- Summary

Page 3

Root Cause Analysis

- Thermal Losses Occur at the Point of Contact of the Device Lead to the Socket Probe.
- There are a Number of Variables Involved with this Phenomenon.
- Most All Device Handling Solutions Need Additional Features That Maintain DUT Temperature from Soak Through Test.
- Devices Under Functional Test that Dissipate Minimal Power (<100mW) are Most Vulnerable.

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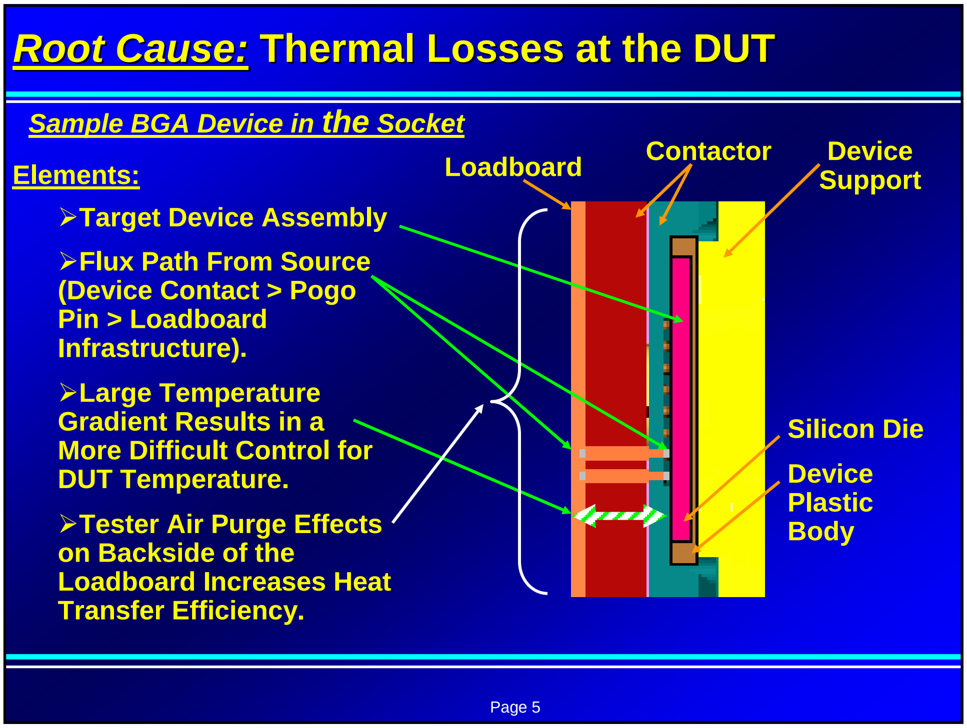
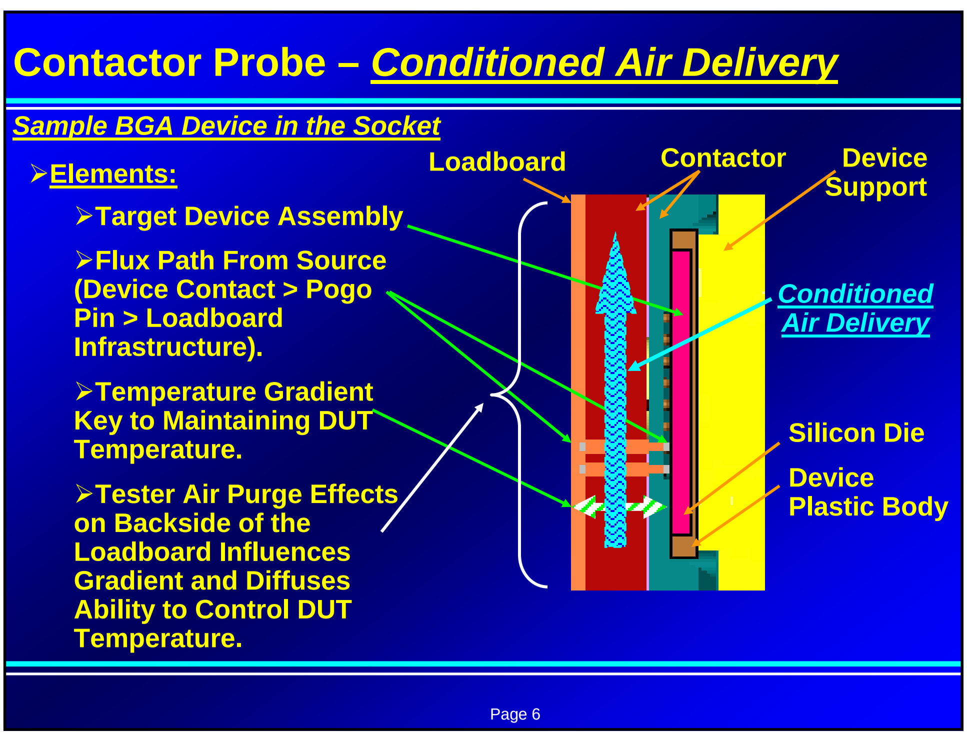

Root Cause: Thermal Losses at the DUT
Sample BGA Device in the Socket
Elements:
➢Target Device Assembly
➢Flux Path From Source (Device Contact > Pogo Pin > Loadboard Infrastructure).
➢Large Temperature Gradient Results in a More Difficult Control for DUT Temperature.
➢Tester Air Purge Effects on Backside of the Loadboard Increases Heat Transfer Efficiency.
Loadboard
Contactor
Device Support
Silicon Die
Device Plastic Body
Page 5


Contactor Probe – Conditioned Air Delivery
Sample BGA Device in the Socket
➢Elements:
➢Target Device Assembly
➢Flux Path From Source (Device Contact > Pogo Pin > Loadboard Infrastructure).
➢Temperature Gradient Key to Maintaining DUT Temperature.
➢Tester Air Purge Effects on Backside of the Loadboard Influences Gradient and Diffuses Ability to Control DUT Temperature.
Loadboard
Contactor
Device Support
Conditioned Air Delivery
Silicon Die
Device Plastic Body
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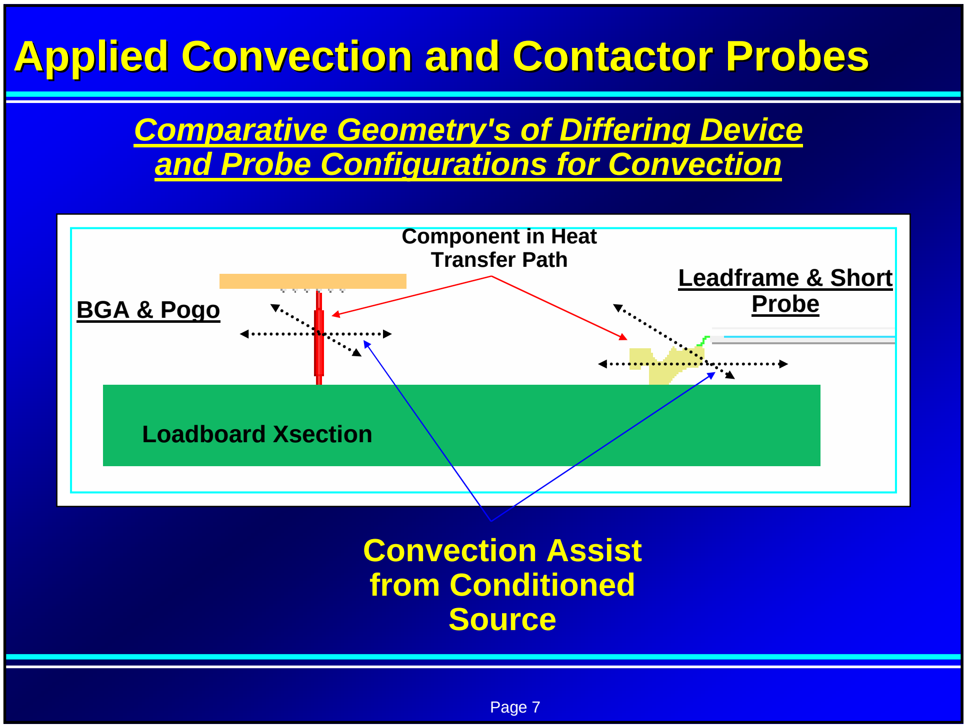
Applied Convection and Contactor Probes
Comparative Geometry's of Differing Device and Probe Configurations for Convection
Component in Heat Transfer Path
BGA & Pogo
Leadframe & Short Probe
Loadboard Xsection
Convection Assist from Conditioned Source
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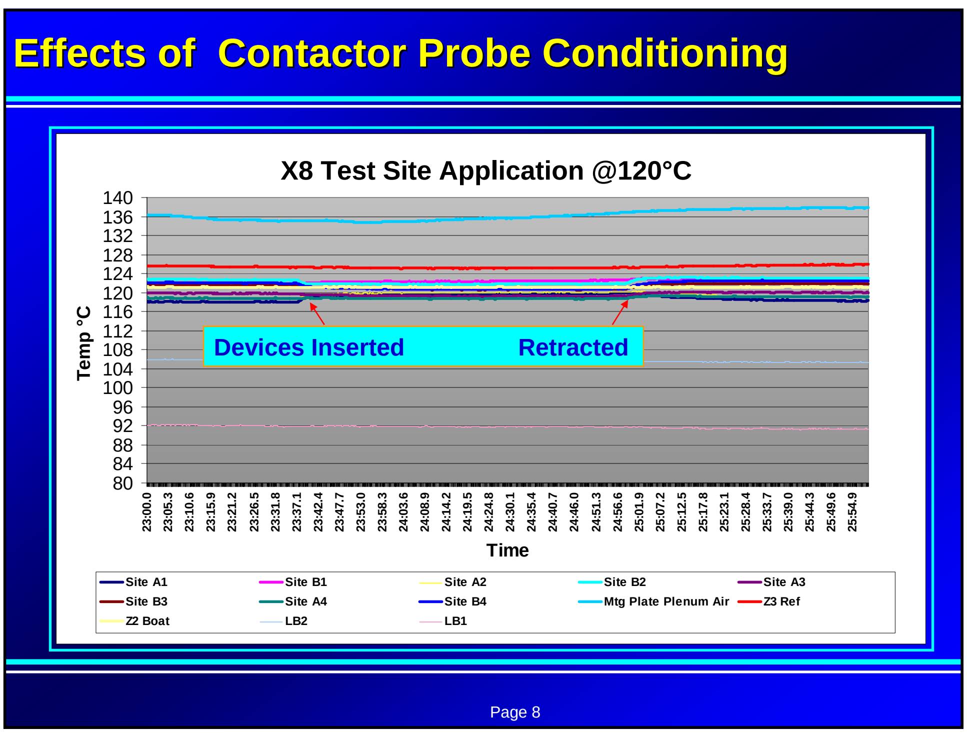
Effects of Contactor Probe Conditioning
X8 Test Site Application @120°C
Temp °C
140
136
132
128
124
120
116
112
108
104
100
96
92
88
84
80
Devices Inserted
Retracted
23:00.0
23:05.3
23:10.6
23:15.9
23:21.2
23:26.5
23:31.8
23:37.1
23:42.4
23:47.7
23:53.0
23:58.3
24:03.6
24:08.9
24:14.2
24:19.5
24:24.8
24:30.1
24:35.4
24:40.7
24:46.0
24:51.3
24:56.6
25:01.9
25:07.2
25:12.5
25:17.8
25:23.1
25:28.4
25:33.7
25:39.0
25:44.3
25:49.6
25:54.9
Time
Site A1
Site B1
Site A2
Site B2
Site A3
Site B3
Site A4
Site B4
Mtg Plate Plenum Air
Z3 Ref
Z2 Boat
LB2
LB1
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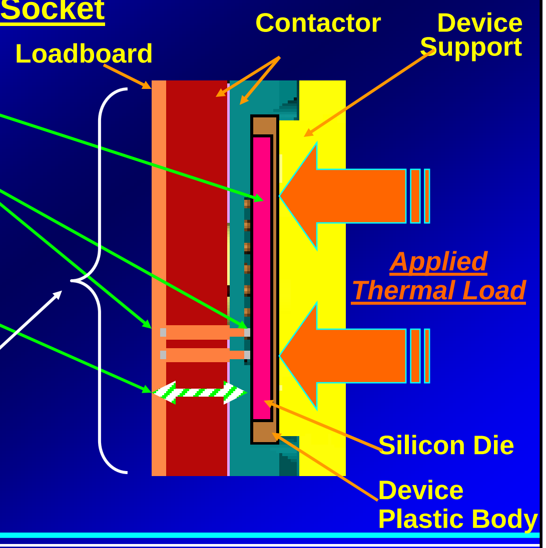
DUT Package – *Applied Thermal Load*

Sample BGA Device in the Socket

Elements:

- Target Device Assembly
- Flux Path From Source (Device Contact > Pogo Pin > Loadboard Infrastructure).
- Temperature Gradient Key to Maintaining DUT Temperature.
- Purge Effects on Backside of the Loadboard Influences Gradient and Changes Device Response in the Socket.



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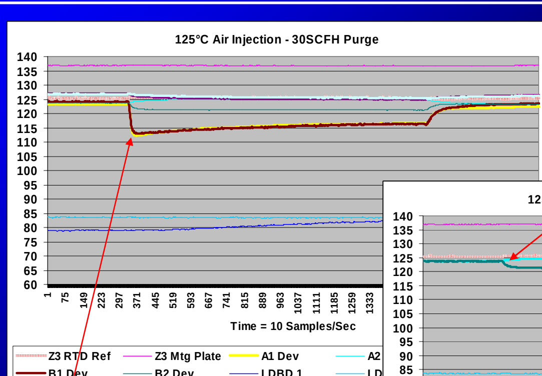
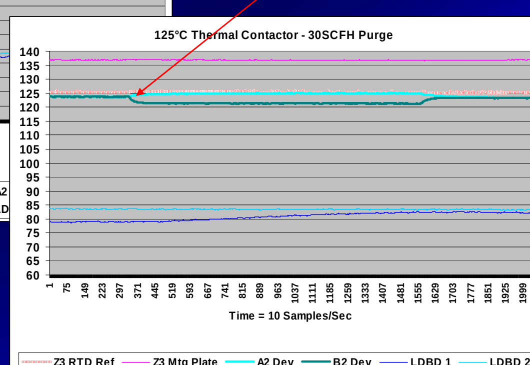
Comparison of DUT Air Impingement and Contactor Probe Conditioning



Thermal Contactor:

Average Insertion Loss @2°C w/ 45°C Gradient



Air Injection:

Average Insertion Loss @11°C w/ 45°C Gradient

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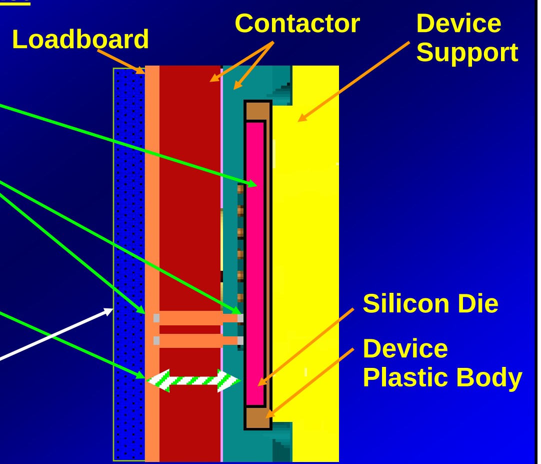
Paper #1

DIB Backside – *Sealed Cover (Purge Cap)*

Sample BGA Device in the Socket

- **Elements:**
  - Target Device Assembly
  - Flux Path From Source (Device Contact > Pogo Pin > Loadboard Infrastructure).
  - Temperature Gradient key to maintaining DUT Temperature.
  - Cover protects area adjacent to test sites from extraneous air currents and allows control of loadboard gradient.



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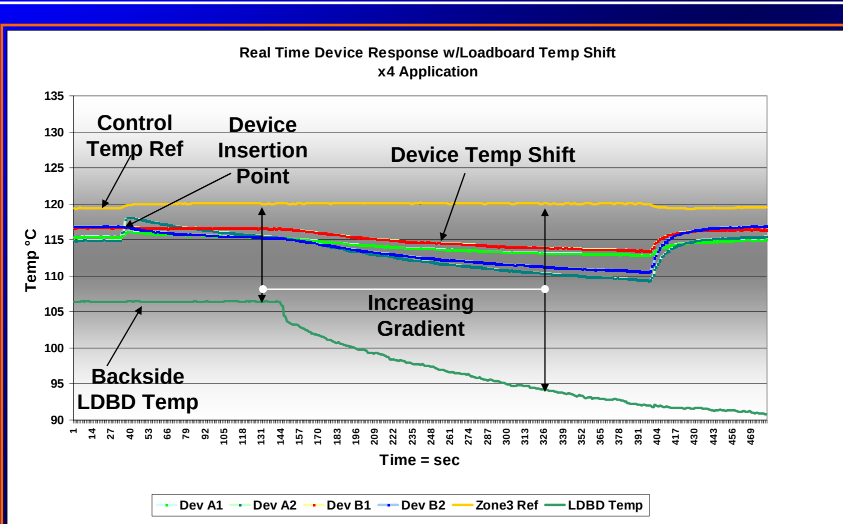
Loadboard Temperature Gradients & Effects on the DUT



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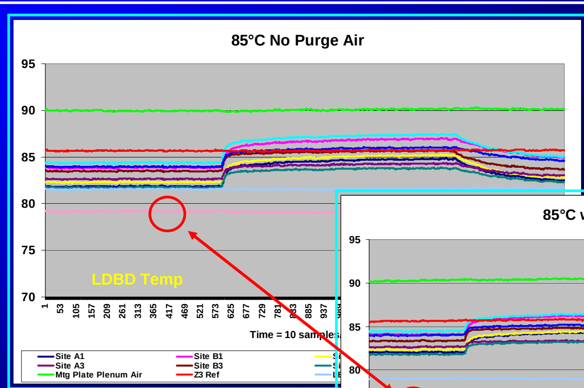
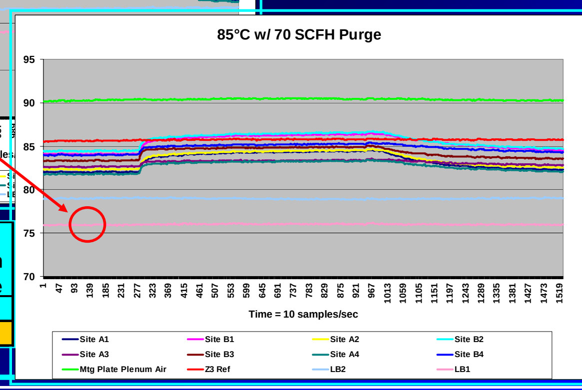
Effects of Purge Air w/ Multi-site Test Applications





	Gradients p-p °C	Step Change in Response
No Purge	3.55	2.62
70 SCFH	3.25	1.78

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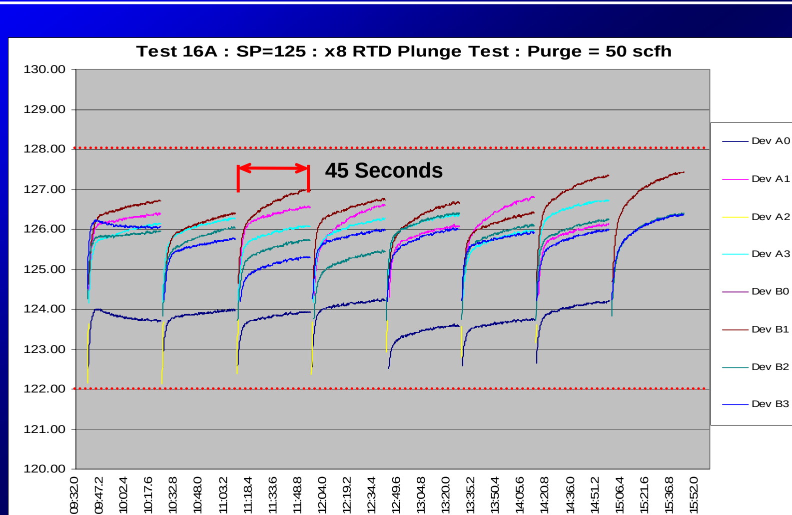
Dynamic Test Results Using Embedded RTD Test Vehicles



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Summary of Approaches and Conclusions

Contactor Probe Conditioning

- Optimal in minimizing transient effects from temperature mismatches from the DUT contacts and test probes.

DUT Applied Thermal Load

- In the convection mode, a small contributor to overcoming the heat transfer effects from the socket and loadboard.

DIB Cover (Purge Cap)

- Effective in maintaining the gradient across the contactor probes and loadboard.
- Eliminates extraneous air currents induced by test head purge and test cell environment.

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DUT Thermal Management - Summary

- Contactor probe conditioning in conjunction with a DIB cover (purge cap) has been found as the combination of choice.
- All applications vary and do require characterization for optimal operating setup.

Test site thermal solutions have been in service since mid 2002. Current installed base (>200) covering x1 thru x16 test applications in engineering and production sites include all handlers developed by Delta Design.

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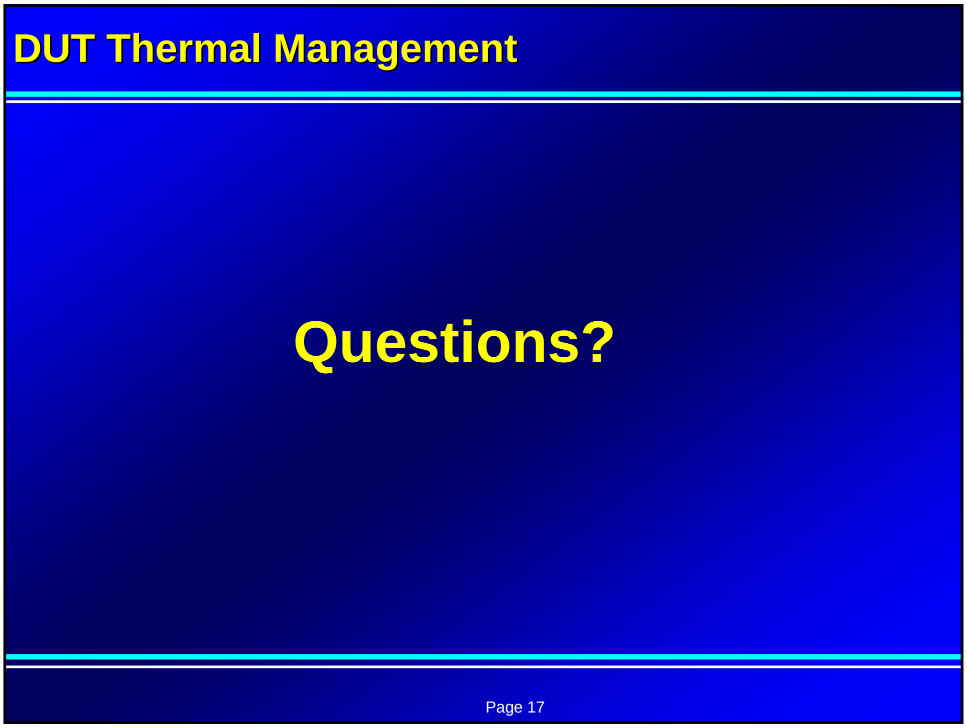
DUT Thermal Management
Questions?
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Thermal Control Units: Development of an Analytical Model and Experimental Validation to Optimize the Voltage Input

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Ph: 480-333-1500

Your Complete Connection

03/15/2006 BiTS 2006 Presentation

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- Introduction
  - Thermoelectric Cooler Basics
  - Thermal Control Unit
- Temperature Variation in a TCU
- Analytical Model
  - TEC Details
  - Sub-Assemblies Details
  - Features and Capabilities
- Optimal Voltage Simulation

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Contents

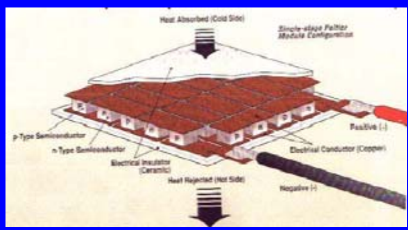
- Experimental Validation
  - Testing Equipments
  - Schematic of the Experimental Setup
  - Graphic Output
  - Results
- Conclusions
- References

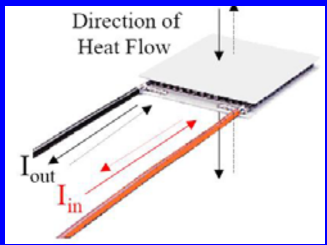
3

Introduction

Thermoelectric Cooler Basics

- Thermoelectric Coolers (TECs) are solid state heat pumps working on the Peltier effect.
- It contains an array of p and n-type semiconductor pellets, connected electrically in series.
- A DC current or voltage is supplied to the device.





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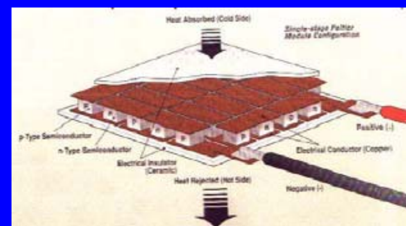
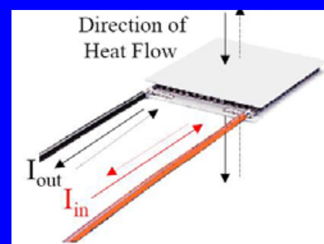
Introduction

Thermoelectric Cooler Basics

- Heat is transported from top to bottom face or vice versa depending on the direction of the current flow.
- In other words, it can work as a cooler or a heater depending on the direction of the current flow.
- Hence, it can be used in the applications requiring thermal control.





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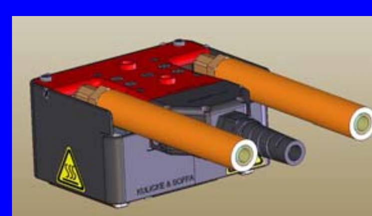
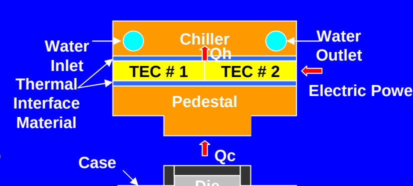
Introduction

Thermal Control Unit

- Thermal control unit (TCU) consists of a liquid heat exchanger, contactor plate and TEC assembly and it facilitates the control of package case temperature in the IC device test sites.
- A contactor plate with a pedestal lies on the cold or the bottom side of TEC assembly and makes the contact with IC device.
- TEC assembly usually contains two TECs arranged mechanically in parallel and electrically in series configuration.





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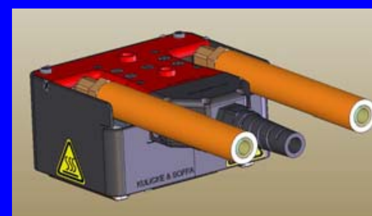
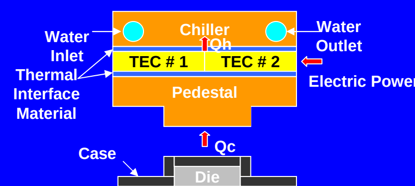
Introduction

Thermal Control Unit

- The liquid cooled heat exchanger lies on the hot or the top side of the TEC assembly.
- The water inlet and outlet and the electric cable port are separate.
- The K&S TCU features compact size and small footprint that makes it easy to integrate with IC device test sites





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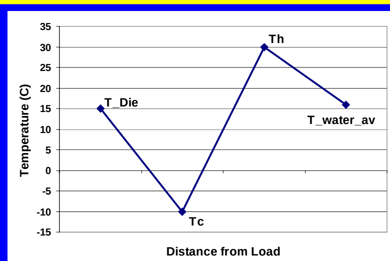
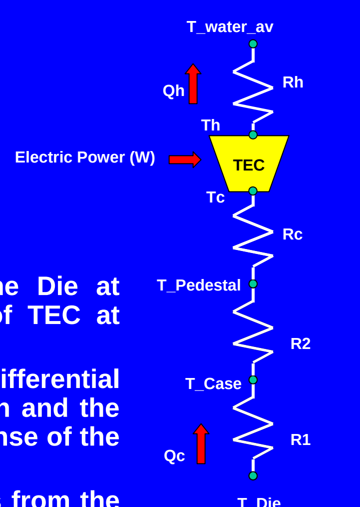
Temperature Variation in a TCU





- The Heat Load Qc transfers from the Die at temperature T_Die to the cold side of TEC at temperature Tc.
- The TEC generates a temperature differential between the hot side at temperature Th and the cold side at temperature Tc at the expense of the electric power W.
- The resultant heat Qh (Qc+W) transfers from the hot side of TEC at temperature Th to the coolant water at temperature T_water_av.

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Analytical Model

TEC Details

- KNS has developed an elaborate analytical model of the TEC developed in EES (Engineering Equation Solver) to simulate its performance for any electrical and thermal inputs.
- The driving equations are

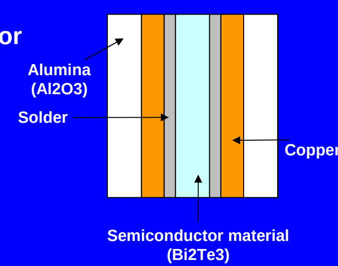
$$\frac{Q}{2*N} = Sm*I*Tc - 0.5*I^2*\rho*\gamma - \frac{\lambda}{\gamma}*(Th-Tc)$$

$$\frac{V}{2*N} = I*\rho*\gamma + Sm*(Th-Tc)$$

$$\gamma = \frac{h}{a^2}$$

- Where:

Q = Heat Load
I = Current
V = Voltage
Th = Hot Side TEC Temperature
Tc = Cold Side TEC Temperature
a = Length/Breadth of Thermoelectric Pellet
h = Thickness of Thermoelectric Pellet = 0.8 mm
γ = Geometry factor
N = Number of Thermocouples
Sm = Seebeck coefficient = $2.068 * 10^{-4}$ V/K
ρ = Electrical Resistivity = $1.029*10^{-5}$ Ohm-m
λ = Thermal Conductivity = 1.614 W/m-K



Material	Thickness (mm)
Alumina	0.8
Copper	0.3
Solder	0.1
Bismuth Telluride	0.8
Solder	0.1
Copper	0.3
Alumina	0.8
Total	**3.2 mm**

Layer stack-up of the TEC

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Analytical Model

Sub-Assemblies Details

- Heat transfer analysis is done for the water chiller to determine the average water temperature.
- The internal thermal resistance of the TEC is also calculated and taken into account.
- One dimensional thermal resistance models of the sub-assemblies are developed and integrated with the TEC model.

$$Qh = \dot{m}*Cp*(T_{water,\,out} - T_{water,\,in})$$

$$T_{water,\,av} = \frac{T_{water,\,in} + T_{water,\,out}}{2}$$

$$R_{TEC} = R_{Alumina} + R_{Copper} + R_{Solder}$$

$$Qc = 2*Q$$

$$P = V*I$$

$$Power = 2*P$$

$$Qh = Qc + Power$$

$$Qc*(\frac{R_{TEC}}{2} + Rc + R_1 + R_2) = T_{Die} - Tc$$

$$Qh*(\frac{R_{TEC}}{2} + Rh) = Th - T_{water,\,av}$$

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Analytical Model

Features and Capabilities

- The model simulates the Peltier effect of TECs very accurately.
- It is generic and can be used for any TEC once its geometric and material properties are known.
- It can be used to generate the characteristic performance curves of the TECs.
- It is integrated with one-dimensional thermal resistance models of the cold and hot side sub-assemblies and thus a complete system level modeling of the TCU can be done.
- It can be used to do thermal analysis and determine the temperatures at different layers.

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Analytical Model

Features and Capabilities

- The model can also be used to change the dimensions of various layers and see its effect on the thermal performance. Hence, it can be used for the design and optimization purposes.
- Besides geometric and thermal parameters, electric inputs can also be analyzed and optimized with the help of this model.
- The model contains non-iterative procedures and the results are obtained in a very short time.
- It can be used only for steady state analysis.

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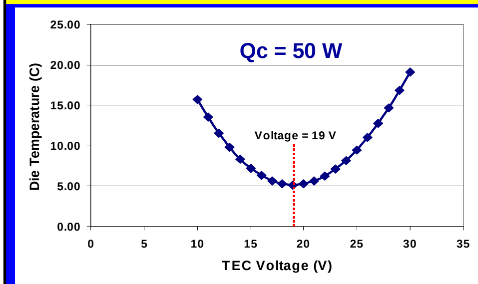
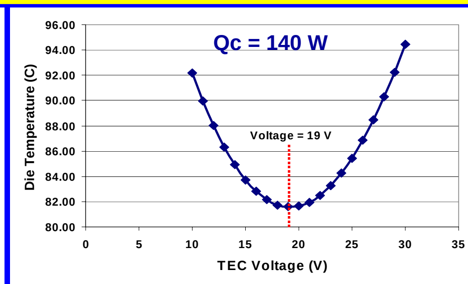
Optimal Voltage Simulation





- **One of the parameters that influence the performance of TECs is the operating voltage input.**
- **In this analysis, the complete system level analytical model of the TCU is used to determine the variation of the die junction temperature versus the TEC operating voltage for the heat loads of 50 W and 140 W.**
- **The optimal voltage is determined as 19 V for both the heat loads. It is observed that as the operating voltage is increased beyond the optimal voltage, internal Joule heating takes over the thermoelectric effect and the TCU thermal performance decreases.**

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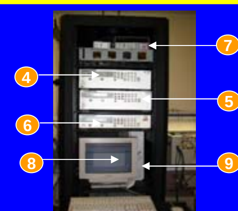
Experimental Validation

Testing Equipment

Chiller Tower



Rack containing other equipments

Ref. No.	Equipment
1	IC Device Test Site
2	Mother Board with Device
3	Thermal Controller
4	Power Supply
5	Power Supply
6	Power Supply
7	Data Acquisition Switch/Unit
8	Data Acquisition Software
9	Computer/Monitor and Accesories
10	Chiller Tower
11	TCU

- **In the second phase of the project, detailed experimental testing is done to determine the optimal voltage and validate the simulation results.**
- **The equipment used in the testing are listed and shown here.**
- **There are three different power supply units to supply power to mother board , TCU Thermal Controller and the pneumatic actuator.**

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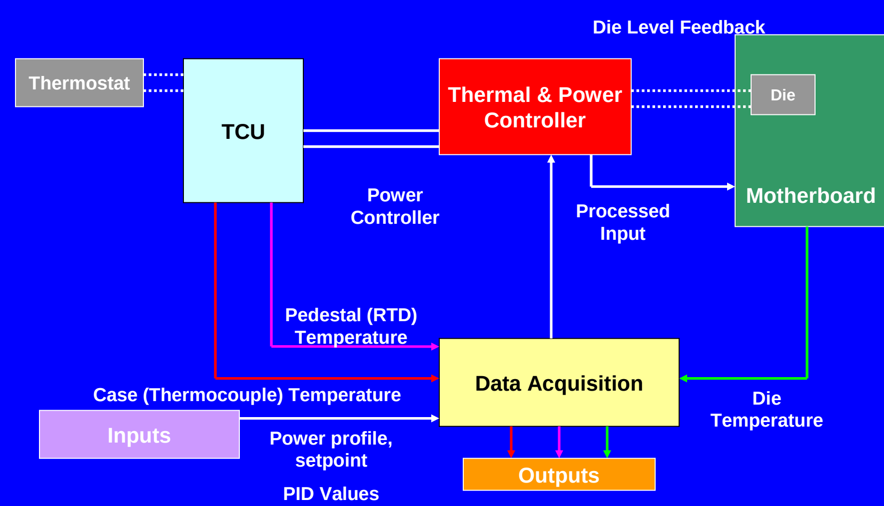
Experimental Validation

Schematic of the Experimental Setup



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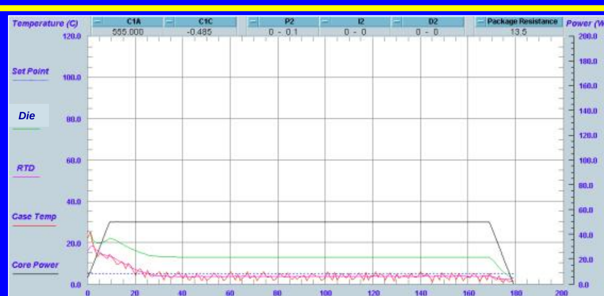
Experimental Validation

Graphic Output



- A sample graphic output is displayed above.
- In this test,
  - Heat Load = 50 W
  - Input Voltage = 12 V per TEC or 24 V per TCU
- The test duration is 3 minutes to let the system reach steady state.
- Besides graphic output, it also saves the output to a text file. The output die temperature in this particular test was 14. 7 °C.

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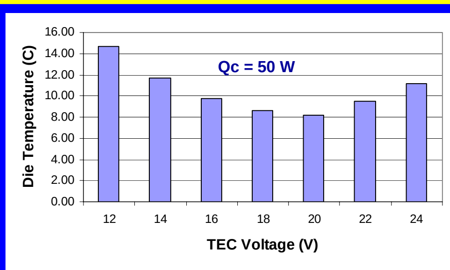
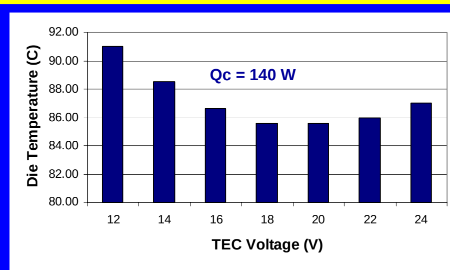
Experimental Validation

Results





- The die temperature reading in the steady state test decreases as the TEC voltage is increased. It reaches an optimal value at voltage around 19 V.
- As the voltage is increased further internal Joule heating takes over the Peltier effect and the die temperature rather increases.
- The trend is same for Qc = 50 W and Qc = 140 W. Also the trend matches with the predicted results of the analysis.

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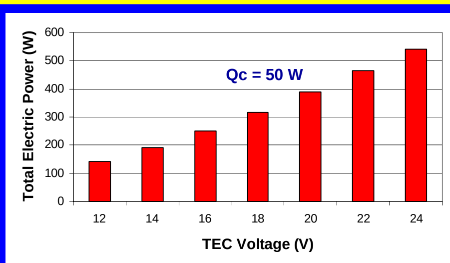
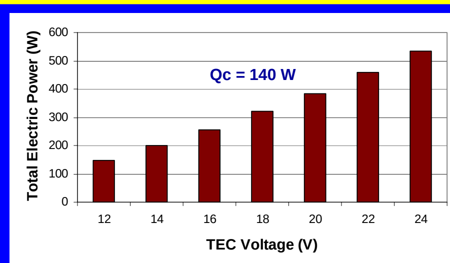
Experimental Validation

Results





- The total voltage and current readings were experimentally determined and multiplied to obtain the total electrical power input into the TECs.
- As the TEC voltage increases, the electrical power increases rapidly for both Qc = 50 W and 140 W.
- For 140 W, the electrical power is slightly more than corresponding figure for 50 W. For Qc = 140 W, the temperature inside the TEC is higher. As the thermoelectric material heats up, its electrical resistivity decreases. Hence, the current and power increases for the same voltage.

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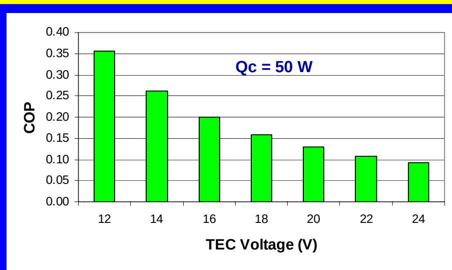
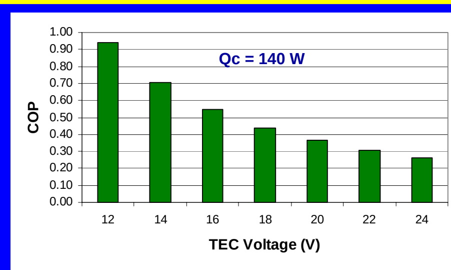
Experimental Validation

Results





- The coefficient of performance indicates the performance of a heat pump and is defined as Qc/Work. Here, the "Work" refers to the total electric power supplied to the TECs.
- For a given heat load, COP decreases as the TEC voltage and the electric power increases.
- For a given voltage, COP would be higher for the higher heat load. It can also be interpreted that as the heat load increases, temperature difference (Th-Tc) decreases and hence the performance of the heat pump increases.

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Conclusions

- TECs are solid state heat pumps working on the Peltier effect. They are very effective means of thermal management and control.
- A TCU consists of a liquid heat exchanger, a contactor plate and TEC assembly and it facilitates the control of package case temperature in the IC device test sites.
- KNS has developed an elaborate analytical model of the TEC. The model is also integrated with the one-dimensional thermal resistance models of sub-assemblies and thus a complete system level modeling of the TCU can be done.
- The model can be used for the thermal analysis and optimization with respect to geometric, thermal and electrical parameters.

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Conclusions

- The system level model of the TCU is used to determine the variation of the die junction temperature versus the TEC operating voltage for the heat loads of 50 W and 140 W. It was found that the optimal voltage input is 19 V per TEC.
- Subsequently, experimental validation is done and it is observed that simulation results of the model are quite accurate. The optimal voltage is found to be 19 V per TEC experimentally also.
- Besides die temperature, variation of other parameters like electric power, COP with respect to TEC voltage was also studied for the heat loads of 50 W and 140 W.

21

References

- *Allan D. Kraus, Avram Bar-Cohen*, "Thermal Analysis and Control of Electronic Equipment," Hemisphere Publishing Corporation, New York.
- *Michael Ohadi,* "Lecture notes of ENME 765: Thermal Management of Electronics," University of Maryland, College Park.
- *Philip Yu. Takhistov*, "Using of Thermoelectric Modules for Heat Exchange Intensification," 20^{th} International Conference on Thermoelectrics 2001, pp 467 – 469.

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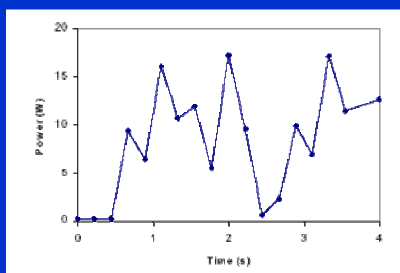
Presentation Topics

- Issues in Temperature Control during Test and Burn-in
- Current Solutions
- Flow-based control
- Normal Flow Micro-channel

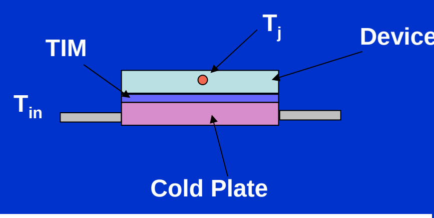
2

Issues in Temperature Control

- Controlling T_j when the power changes
- Controlling T_j across many devices given the variability in device power dissipation, environmental conditions and thermal resistance values



Tadayon, 2000



$$T_J = T_{in} + \dot{q}''(R''_{cp} + R''_{TIM} + R''_d)$$

3

Maintaining T_j for High Power Devices

$$T_J = T_{in} + \dot{q}''\left[R''_{flow} + (R''_{core} + R''_{TIM} + R''_d)\right]$$

$$R''_{cp} = R''_{flow} + R''_{core}$$ Core Resistivity

$$R''_{flow} = \frac{1}{\dot{m}''Cp}$$ Flow Resistivity

•If the core resistivity is small, then the cold plate thermal resistivity is inversely proportional to the flow rate

•By controlling the flow rate we can control the cold plate resistivity

4

Temperature Variation in a Burn-in Chamber

- Variation in T_j leads to longer BI time
- Tight T_j distribution increases yield
- Sources of variation:
  - Variation in inlet T to the cold plate
  - Variation in power dissipation of components
  - Variation in the thermal resistance of the device and the interface
  - Variation in the CP/HS thermal resistance

5

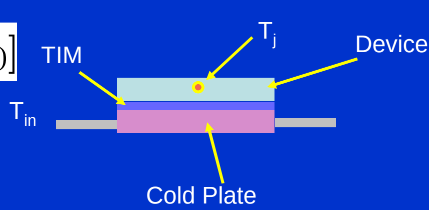
Controlling T_j Distribution

$$T_J = T_{in} + (\dot{q}_a'' + \Delta \dot{q}'')\left[R''_{flow} + (R''_{core} + R''_{TIM} + R''_d)\right]$$

Function of Hardware

Manufacturing

Large variations in these will amplify the power variation



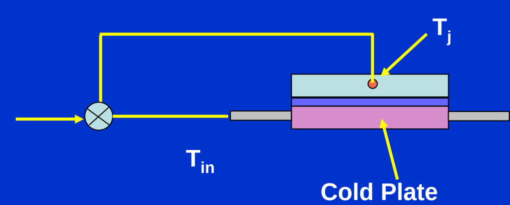
T_{in} is determined by the maximum heat flux.

6

What If?

- The resistance of the cold plate can be controlled in real time using the die temperature?

$$T_J = T_{in} + (\dot{q}_a'' + \Delta \dot{q}'')\left[R''_{flow} + (R''_{core} + R''_{TIM} + R''_d)\right]$$



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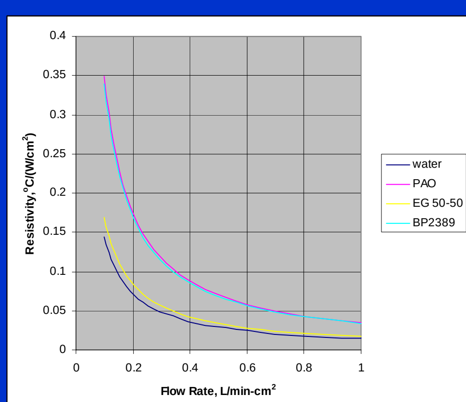
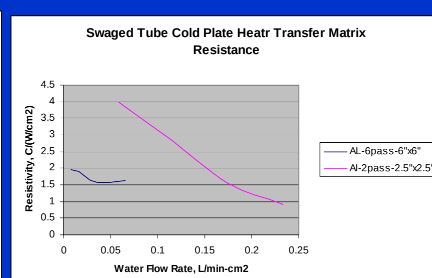
A typical HP Swaged Tube Cold Plate

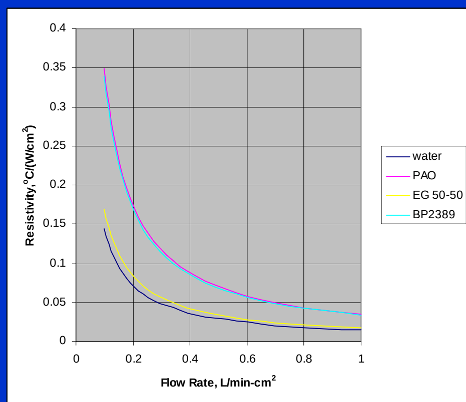


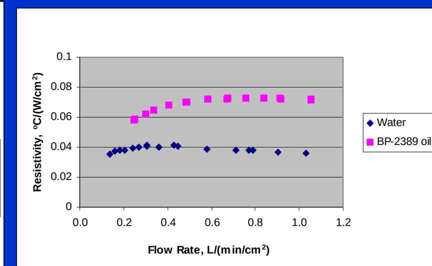


$$R''_C \equiv R_{CP} \cdot A_{CP} - R''_F$$

8

A Cold Plate Based on Normal Flow





$$R''_C \equiv R_{CP} \cdot A_{CP} - R''_F$$

9

Thermal management using a Liquid Cold Plate

10

The Temperature Budget

T_j Functionality Limit

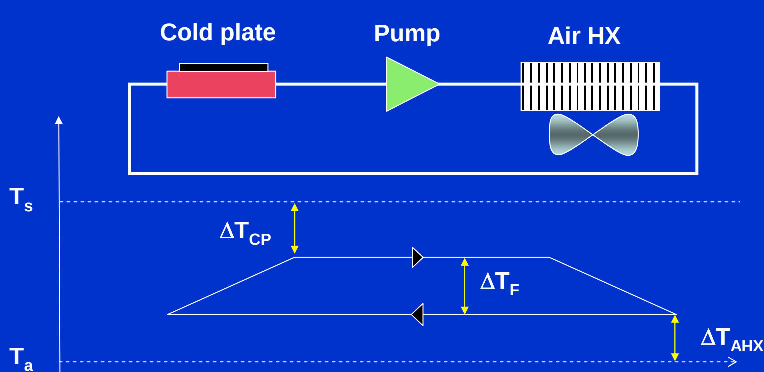
T_s Cold Plate Surface Temperature

Loop Performance

T_a Ambient temperature

11

Liquid Loop Heat Spreading



ΔT_F and ΔT_{AHX} can be reduced at will by increasing size of pump and air HX

$$R''_{\min} = R''_i + \underbrace{\frac{\Delta T_{CP}}{\dot{q}''}}$$

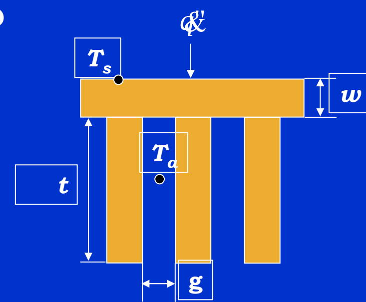
Cold Plate Core Resistivity: ***R''**$_{core}$*

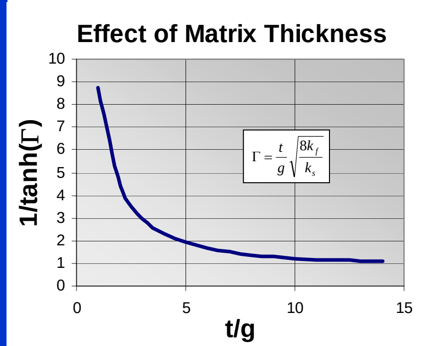
12

Paper #3

Why Microchannels?

$$R''_{core} = \frac{T_s - T_a}{\dot{q}''} \approx \overset{\text{wall}}{\frac{w}{k_s}} + \overbrace{\frac{g}{\sqrt{2k_s k_f}}\left[\frac{1}{\tanh(\Gamma)}\right]}^{\text{matrix}}$$





$$R''_{core,\min} = \frac{g}{\sqrt{2k_s k_f}}$$

$$\frac{t}{g} \approx 10$$

13

Normal Flow Pressure Drop

$$R''_{core,\min} = \frac{g}{\sqrt{2k_s k_f}}$$

$$\Delta P \propto \frac{L}{g} V$$

For parallel flow L (channel length) is constant and V is inversely proportional to the gap size. So, $\Delta P \propto \frac{1}{g^2}$

For normal flow, the flow path is H, the channel height.

$$\Delta P \propto \frac{H}{g} V$$

In normal flow arrangement, V is constant and H is proportional to g so ΔP stays constant

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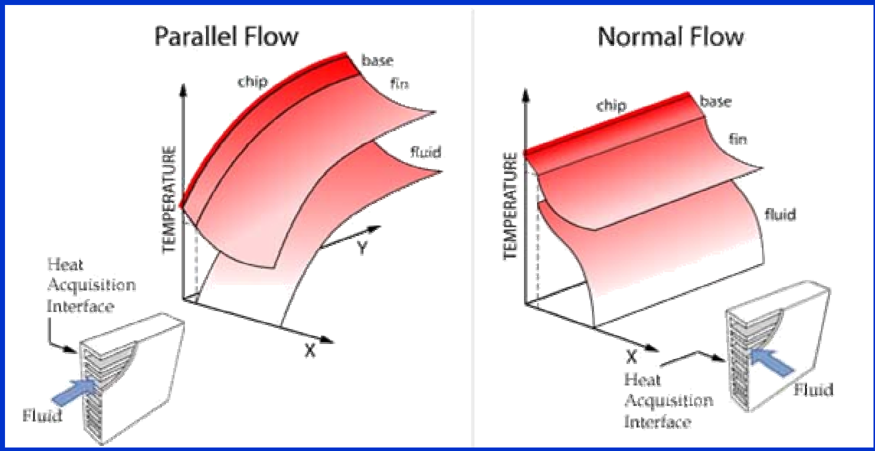
Normal Flow Technology



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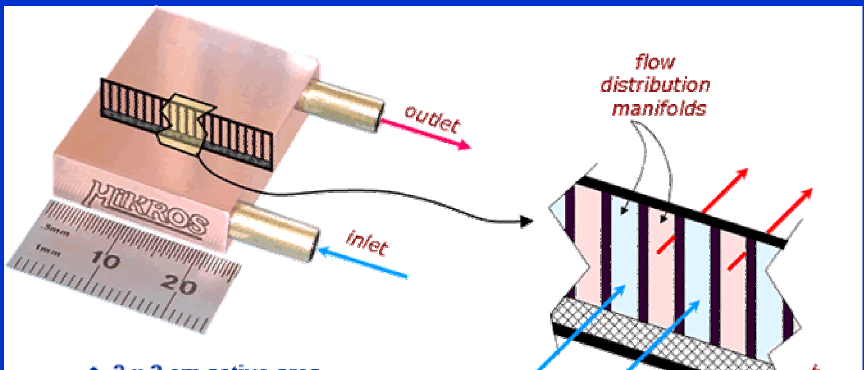
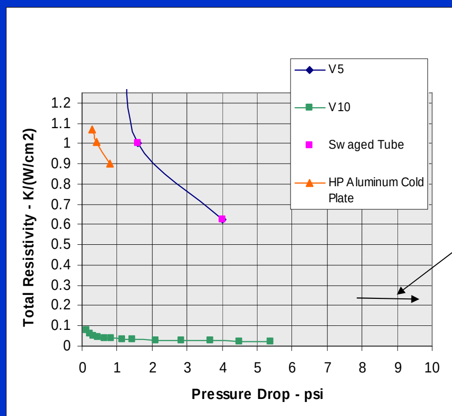
Internal Design

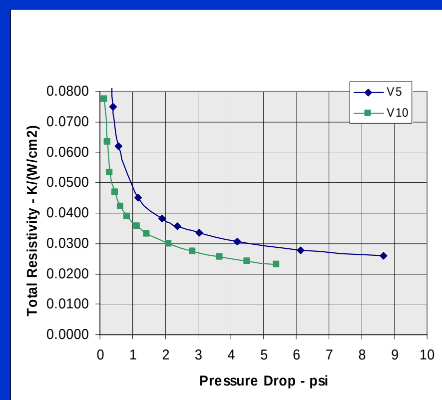


- 2 x 2 cm active area
- copper
- 30 gm
- 23 x 31 x 8 mm

16

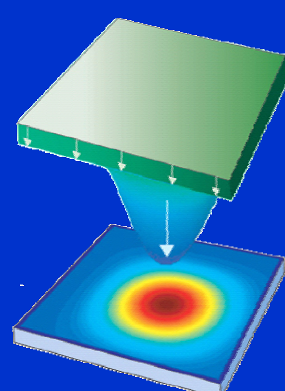


Tuckerman & Pease
15-35 psi



Managing “Hot Spots”

- Tailor Resistivity to heat dissipation
  - Uniform coolant inlet temperature
  - Local control of flow rate
- Reduce temperature gradient
- Reduce flow and pressure drop



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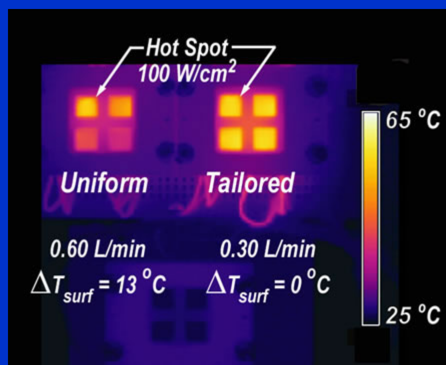
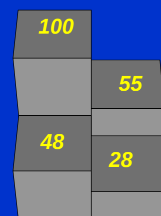
"Hot Spot" Demo





Heat Flux Distribution (W/cm^2)

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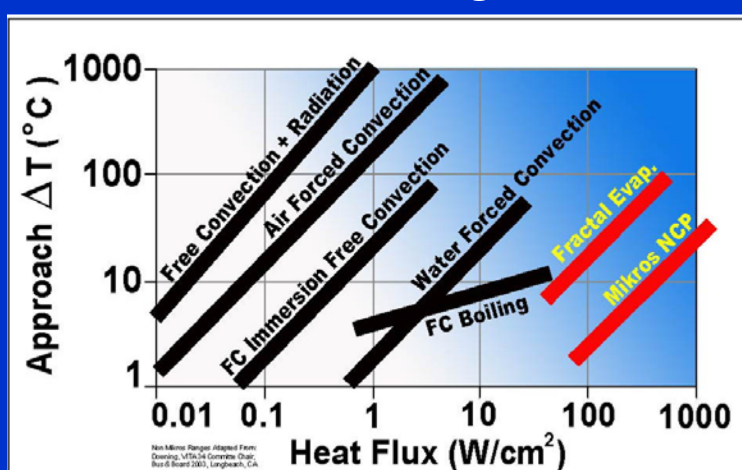
Comparison with other Technologies



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Conclusions

- A cold plate based on the Normal Flow Technology has very low thermal resistance
- For the proper ranges of the interface and device resistance, the junction to ambient resistance can be controlled by varying the flow rate through the cold plate
- They key to successful control remains to be a low value of interface resistance
- Normal Flow arrangement lends itself to managing hot spots

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UMD Advanced Test Technologies

Managing the Thermal Budget During Burn-In
A New Concept for Control

Chris Lopez, UMD
Dr. James Forster, UMD
Trevor Moody, UMD

BiTS Burn-in & Test Socket Workshop

2005 Burn-in and Test Socket Workshop
March 12 - 15, 2005

AGENDA

- **Burn-in today**
- **Thermal Resistance – A Quick Lesson**
- **The Challenges of Today's Burn-In**
- **The Thermal Budget**
- **Advanced Thermal Management**
- **Thinking outside the Box – Variable Thermal Resistance (VTR) Technology**
- **Closing Remarks on the Future**

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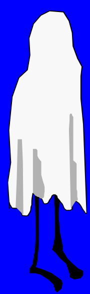


“The Cost of Test is Approaching the Cost of Silicon”

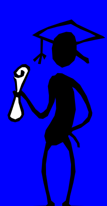
-Senior Semiconductor Manager

“Google's Energy Bill for its Servers Now Exceeds the Cost of the Equipment.”

-Business Week Online

Thermal Management

- Definition
  - The art by which heat is controlled and removed by various means such as air or liquid and carried to an alternate location



The First Law of Thermodynamics (Conservation) states that energy is always conserved, it cannot be created or destroyed. In essence, energy can only be converted from one form to another.

The Modern Burn-In Facility
Low-to-Medium Power

- Conventional Burn-in chambers
  - Box with recirculating air, usually cooled by air-to-air or air-to-liquid heat exchangers
  - Thermal Management consists of adding as big of a heat sink as possible (typically)

Images from previous BiTS presentations

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Modern Burn-In Facility
High Power

- High Power Burn-in chambers
  - Box with impinged air or liquid chilled heads
    - Thermal Management consists of impinging air onto heat sink or making contact with package via a thermal head
    - Active monitoring for devices

Images from previous BiTS presentations

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Technology Drivers

- Increase yields
- Maximize visibility
- Eliminate the need for sort
- Maximize utilization
- Meet increasing demands of higher power, higher variance devices

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Technology Drivers

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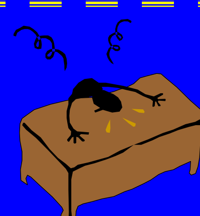

DECREASE THE COST PER UNIT THAT BURN-IN GENERATES

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Test Equation
Cost of Test (COT)

$$\frac{\left(\begin{array}{l}\text{Cost of test/burn-in capital}\\ \text{- Test engineering expense}\\ \text{- ATE}\\ \text{- Fixtures}\\ \text{- Software}\\ \text{- Thermal units}\end{array}\right) + \left(\begin{array}{l}\text{Total Labor}\\ \text{- Personnel}\\ \text{- Operating Expenses}\\ \text{- Electricity}\\ \text{- Etc.}\end{array}\right)}{\left(\begin{array}{l}\text{Yield}\\ \text{- Throughput}\\ \text{- Failure rate}\\ \text{- Partitioning}\end{array} \; \text{X} \; \begin{array}{l}\text{Profit/part}\\ \text{- Engineering expense}\\ \text{- Engineering Capital}\\ \text{- Materials}\end{array} \; \text{X} \; \begin{array}{l}\text{Number of Parts}\\ \text{- Capital Reuse}\\ \text{- Life Expentency}\end{array}\right)} = \text{COT}$$

$$\frac{\text{Cost of test capital + Total Labor}}{\text{Yield x Profit/part x Number of Parts}} = \text{Cost of Test}$$

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Test Equation
Cost of Test (COT)

$$\frac{\left(\begin{array}{l}\text{Cost of test/burn-in capital}\\ \text{- Test engineering expense}\\ \text{- ATE}\\ \text{- Fixtures}\\ \text{- Software}\\ \text{- Thermal units}\end{array}\right) + \left(\begin{array}{l}\text{Total Labor}\\ \text{- Personnel}\\ \text{- Operating Expenses}\\ \text{- Electricity}\\ \text{- Etc.}\end{array}\right)}{\left(\begin{array}{l}\text{Yield}\\ \text{- Throughput}\\ \text{- Failure rate}\\ \text{- Partitioning}\end{array} \; \text{X} \; \begin{array}{l}\text{Profit/part}\\ \text{- Engineering expense}\\ \text{- Engineering Capital}\\ \text{- Materials}\end{array} \; \text{X} \; \begin{array}{l}\text{Number of Parts}\\ \text{- Capital Reuse}\\ \text{- Life Expectancy}\end{array}\right)} = \text{COT}$$

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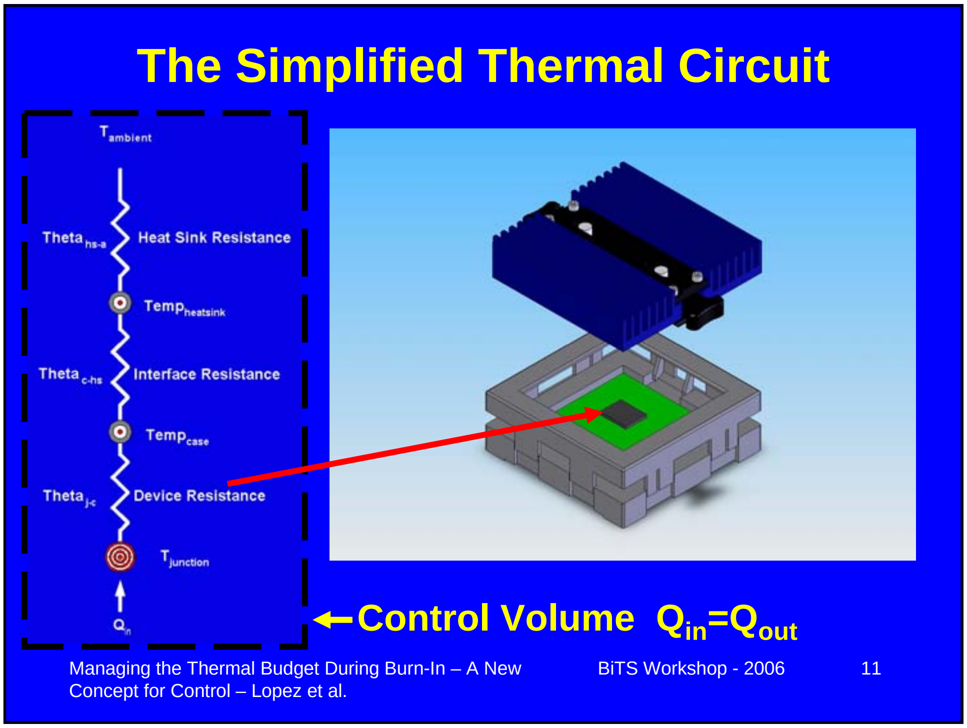
The Simplified Thermal Circuit
$T_{ambient}$
$Theta_{hs-a}$
Heat Sink Resistance
$Temp_{heatsink}$
$Theta_{c-hs}$
Interface Resistance
$Temp_{case}$
$Theta_{j-c}$
Device Resistance
$T_{junction}$
Q_{in}
Control Volume $Q_{in}=Q_{out}$
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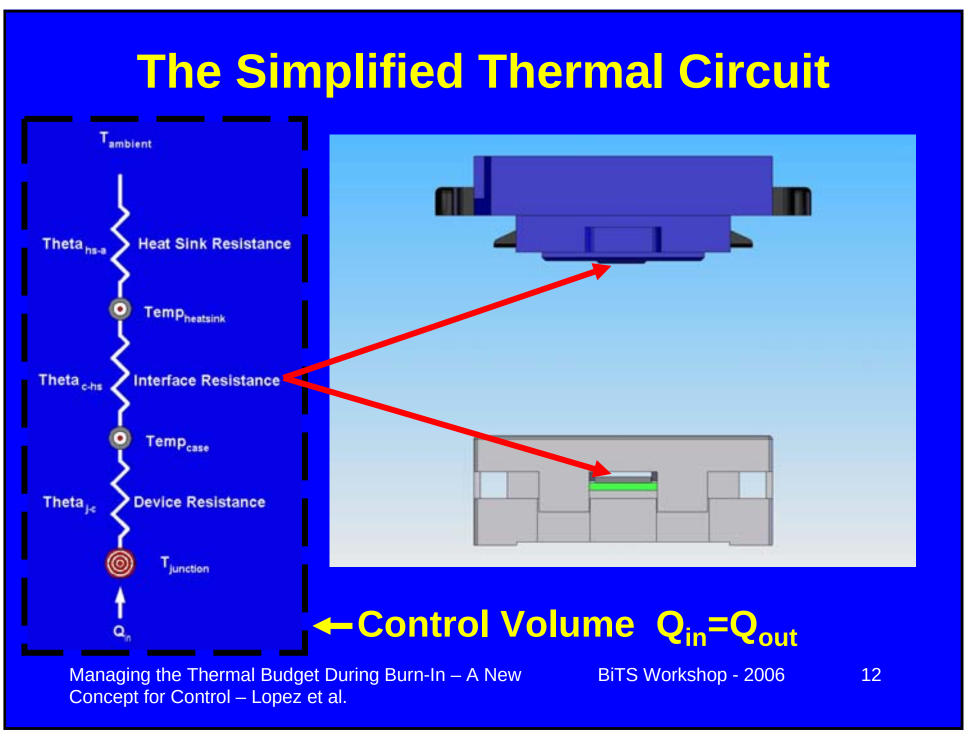
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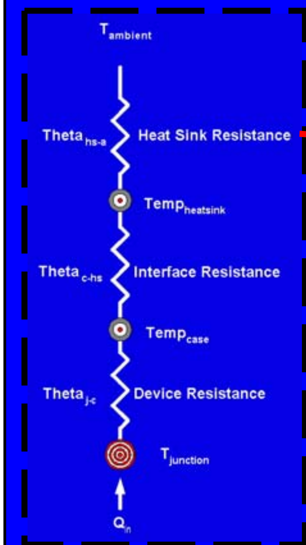
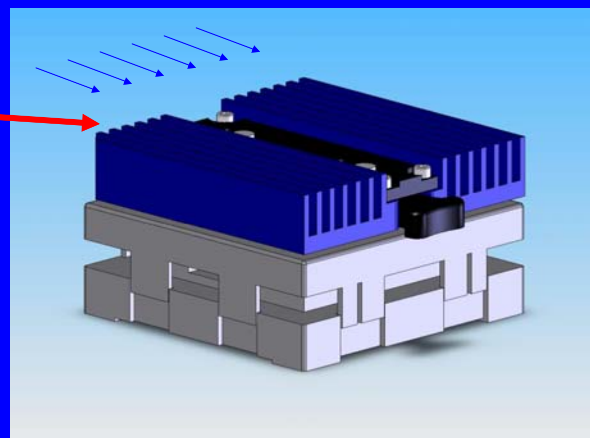
The Simplified Thermal Circuit





←Control Volume $Q_{in}=Q_{out}$

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The Problem
Passive Heat Sinks

HIGH TEMPERATURE
HIGH POWER
REDUCE JUNCTION TEMPERATURE

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The Problem

- Today's batch process is becoming a thing of the past for even low power devices
- Because of wide power variations in today's products devices need to be binned in order to be processed in conventional burn-in systems
- Binning is inefficient and economically bad
  - Throughput suffers
  - The bins are not always apparent up front

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The Problem

- Device
  - 10W nominal logic device
  - Integrated heat spreader
- Conventional Burn-In
  - .4 C/W Package Resistance
  - 1.2 C/W Interface Resistance
  - 1.5 C/W Heat Sink Resistance @ 800 lfm (Chamber Spec.)
  - Total = 3.1 C/W
  - 31 C rise
  - Set chamber to 94 C
  - Device running at 125 C junction temperature
- Sounds Easy…

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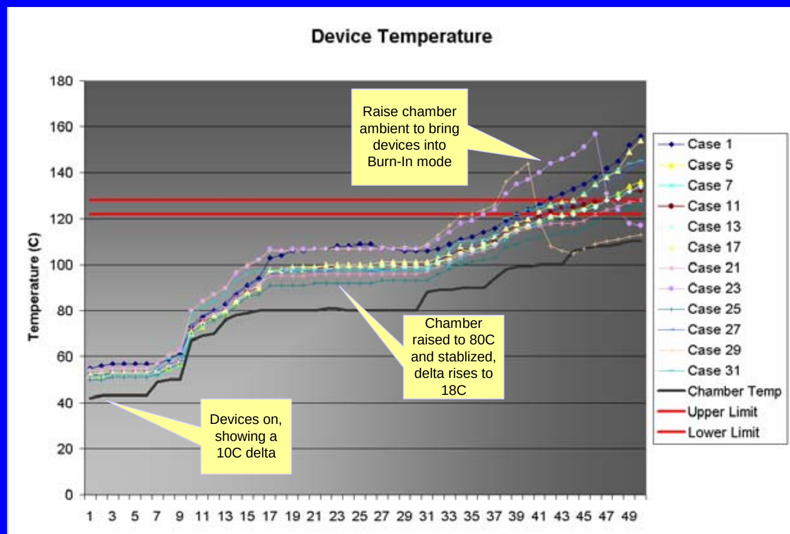
The Problem



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The Problem

- Conventional Reality
  - Device Varies from 5W to 15W
  - .4 C/W Package Resistance
  - 1.2 C/W Interface Resistance
  - 1.5 C/W Heat Sink Resistance @ 800 lfm (Chamber Spec.)
  - Total = 3.1 C/W
  - 15 C rise to 46 C rise
  - Set chamber to ??? C
  - Device running at ??? C junction temperature
- The "other" factors
  - What about airflow variances?
  - What about devices heating up downstream devices?
- And oh yeah and all these calculations are at room temperature as device heats up so does the variance…..

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The Solution

- So what do we do
  - Well there's binning….again
    - BUT that's unacceptable
- The Solution
  - Control the local environment
    - Active closed loop thermal control
    - (e.g. iSocket)

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The Problem

HIGH TEMPERATURE
HIGH POWER
REDUCE JUNCTION TEMPERATURE

+

DEVICE POWER VARIATION
AIRFLOW VARIATION
INTERFACE VARIATION
DOWNSTREAM DEVICE HEATING

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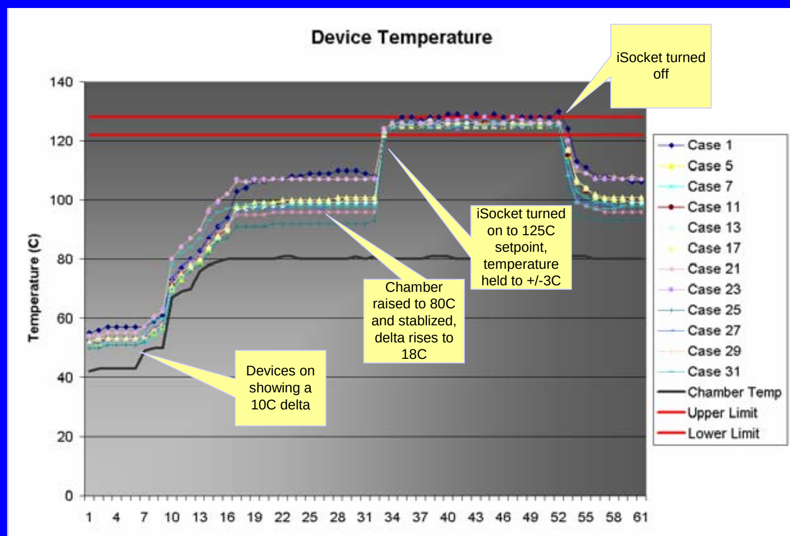
The Solution



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The Thermal Budget

- But, we're not done…
  - Yet another issue arises when you need to consider the thermal budget of the chamber
  - Since a chamber is a finite control volume ……. the following must be true

Qin = Qout

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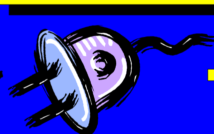
The Problem
Advanced Thermal Control

HIGH TEMPERATURE
HIGH POWER
REDUCE JUNCTION
TEMPERATURE

+

DEVICE POWER VARIATION
AIRFLOW VARIATION
INTERFACE VARIATION
DOWNSTREAM DEVICE HEATING



+

POWER SUPPLY
MANAGEMENT
THERMAL BUDGET

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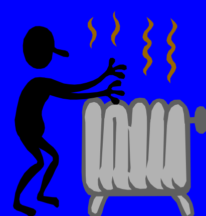
The Thermal Budget



- Examine a chamber
  - 20kW of heat removal capacity….
    - This is at 125C (air-to-air)
    - As ambient temperatures decrease the heat removal capability of chamber decreases.
    - This will be better for water chilled systems
  - This means we can process 2000 devices at 10W apiece right?
  - Wrong…

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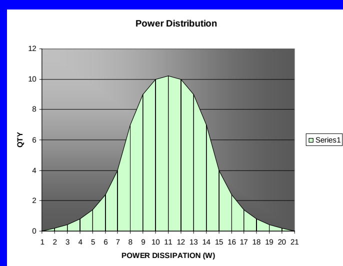
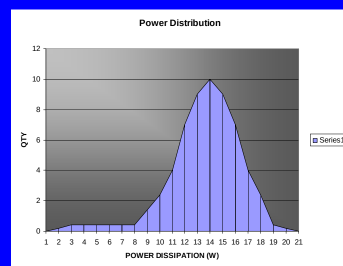
The Thermal Budget

– Don't forget the device variance
– There is no guarantee that we have a "perfect" distribution, -------- reality is never perfect.
– So what do we do… plan for the worst case scenario – probably a safe path to avoid chamber thermal runaway

PERFECT



REALITY



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The Thermal Budget

- Part of the thermal budget needs to be given to the thermal control, but how much?
- The intent is to add heat to each device so that they all "act" alike.
- We are able to process all the devices together, but the box becomes the limiter to the equation
- Given the 15W max due to variance we should plan on 1300 devices
- Reduce throughput by 35% when you don't necessarily need to…

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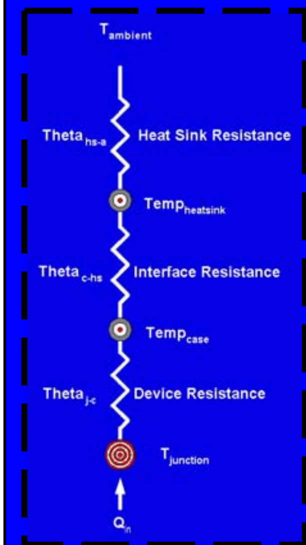
Advanced Thermal Management

- We could…
  - Liquid cooling
    - Expensive
    - Prohibitive upfront capital expenditure
    - Dedicated
    - Maintenance Heavy
  - Impinged air active control systems
    - Expensive
    - Prohibitive upfront capital expenditure
    - Low Density
    - Consumables at a high cost

Thinking Outside the Box

- Variable Thermal Resistance (VTR) technology
  - Controls the thermal path
  - Tuned thermal resistance
  - Optimal thermal control
  - Device independent
  - Large capital avoidance

Thinking Outside the Box



- Treat each device as it's own burn-in box
- No special treatment to effectively increase the temperature of the product
- No box to constrain the upper power requirement

←Control Volume $Q_{in}=Q_{out}$

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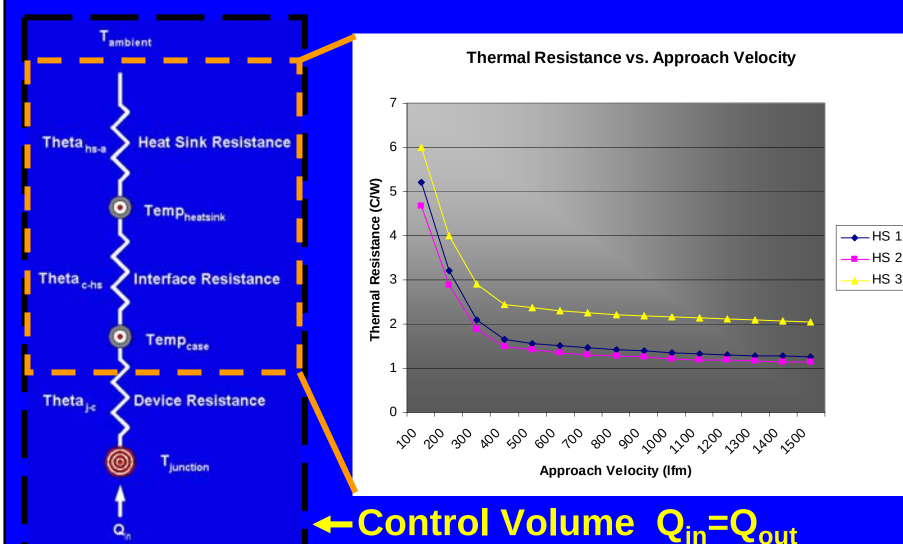
Thinking Outside the Box



←Control Volume $Q_{in}=Q_{out}$

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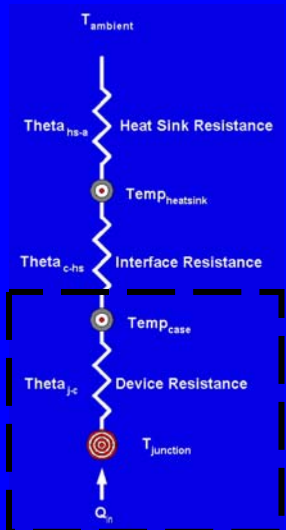
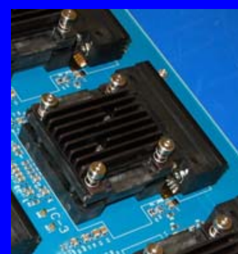
Thinking Outside the Box



- VTR Technology
- Let the device heat itself
- Create a mini-environment



Control Volume $Q_{in}=Q_{out}$

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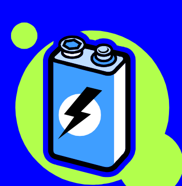
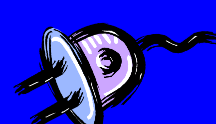
Thinking Outside the Box
The Mini-Environment

- Effectively we can process a 15W device next to a 5W device without all devices having to consume 15W.
  - Throughput increases
  - Operating costs decrease
  - Power supply sizing decreases
- “An independent burn-in environment for every device”





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The Benefits

- Full Entitlement
  - The capital expenditure can be used to it's full potential
  - The independence of processing "unlike" devices within the same environment becomes a reality
  - Device independent
  - Throughput
  - Reduced operating costs
- Cooling can be achieved on a bulk level versus a finite level

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Future Thoughts

- The burn-in environment will change as we move toward higher power, higher variance devices
- Thinking and moving outside the box will allow for more flexible upgradeable systems in the future
- Full Entitlement is a necessity to lower the cost of test in the future

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