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Session 6

Interfacing: Contacting The Device And Beyond

"Comparison Of Test Interface Unit For High Frequency Applications"
Doyce Ramey, Jimmy Vo — Texas Instruments, Inc.
Takuto Yoshida — Yokowo Co., Ltd.

"Improving Test Efficiency By New Device Interface Topology For High Parallel Testing"
Joachim Moerbt, Rose Hu — Advantest (Europe) GmbH

"Socketing The Impossible: A Very Fine, Very Dense Case Study"
Jon Diller, Kiley Beard — Synergetix
Takuya Tsumoto — NEC Electronics Japan

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Comparison of Test Interface Unit for High Frequency Applications

(Comparison of Coaxial Socket with Brass Body and Plastic Socket)

2006 Burn-in and Test Socket Workshop

March 12 - 15, 2006

Takuto Yoshida – Marketing Dept. GM
Yokowo Co., Ltd.
Doyce Ramey – RF Wireless Lab Manager
Texas Instruments, Inc.
Jimmy Vo – RF Wireless Test Engineer
Texas Instruments, Inc.

Agenda

- Introduction
- Solution
- Test Socket Experiment
- Test Interface Experiment
- Conclusions

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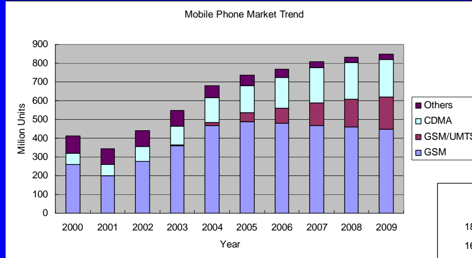
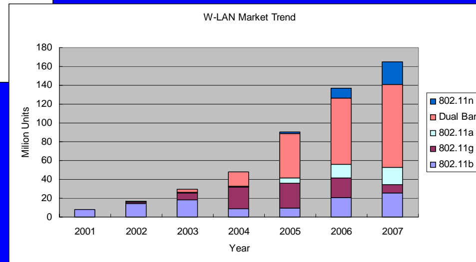
Market Trend (Wireless Applications)



Mobile Phone



WLAN

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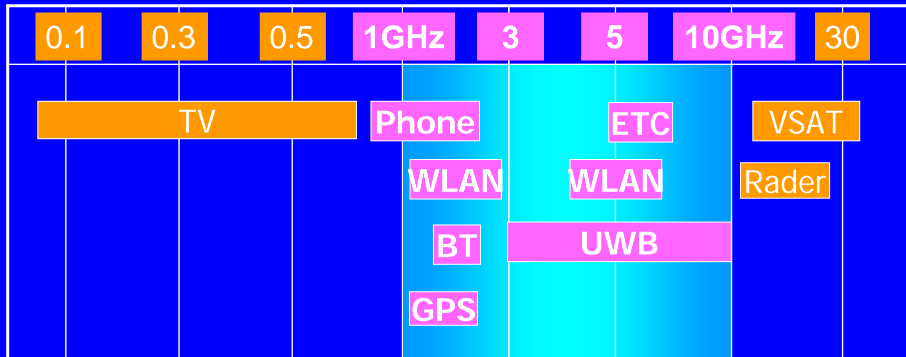
Map of Frequency Area of Device Applications



BT: Bluetooth
UWB: Ultra Wide Band

Due to increase of wireless applications, 1GHz to 10GHz high frequency application devices are increasing.

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Challenges with RF Testing

When testing frequency condition is higher to 0.8GHz → 2.4GHz → 5.2GHz …

- Sockets Introduce Poor RF Performance
  - → Difficult impedance control
  - → Margins to Specifications
  - → Low product yield
- Small compression travel for contact
  - → Difficult to handle in production

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Requirement for Test Sockets

Problems		Key Parameters	Desired Spec.
#1: Difficulty to match the circuit impedance.	→	Return loss	: < -10dB
		Inductance	: < 1nH
#2: Difficulty to set up test parameters.	→	Insertion loss	: > -1dB
		Return loss	: < -10dB
#3: Difficulty of multiple test at the same time.	→	Crosstalk	: < -25dB
#4: Difficulty of steady contact.	→	Compression travel	: > 0.25mm

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Solution for High Frequency Devices

Metal body coaxial socket solution

- Three different type pins for RF/Power/Ground
- Coaxial structure for RF (high frequency) signal
- Power pin can be used to low frequency signal
- Common metal ground body for lower Inductance
- Long compression travel for steady contact

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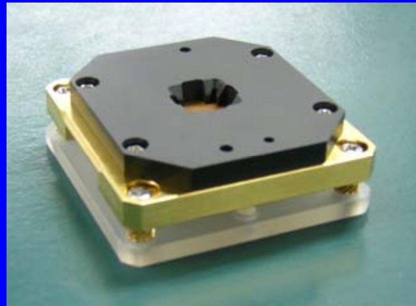
Socket Photo



Coaxial Socket

Pitch: 0.5mm
RF Coaxial Pin: 36pcs.
Power Pin: 36pcs.
Ground Pin: 72pcs.
Compression travel: 0.25mm

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Expected Performances of Socket

- Insertion loss > -1dB
- Return loss < -10dB
- Crosstalk < -25dB
- Compression travel length > 0.25mm

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Test Socket Experiment

- RF evaluation of 0.5mm pitch BGA socket
  (Coaxial socket and plastic socket)
- Insertion loss
- Return loss
- Crosstalk

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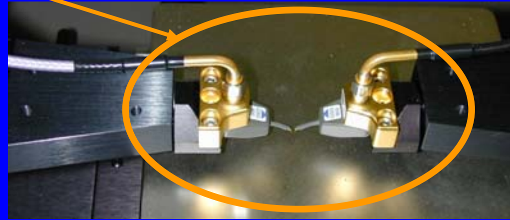
RF Evaluation System

VNA
(Agilent Technology)
Probe Station
(Cascade Microtech)

GSG Probe
(Cascade Microtech)
0.5mm Pitch



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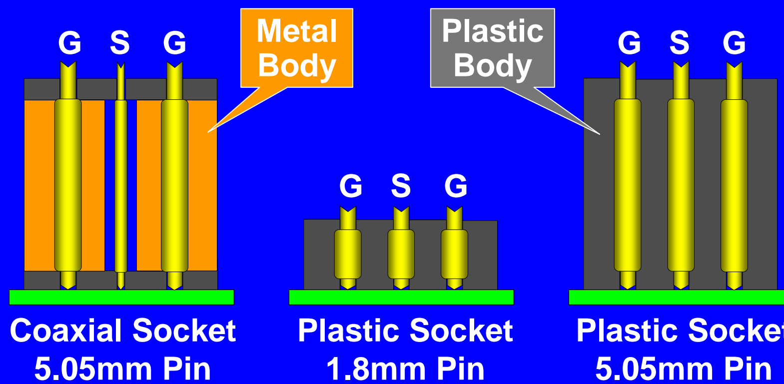
Socket Diagram



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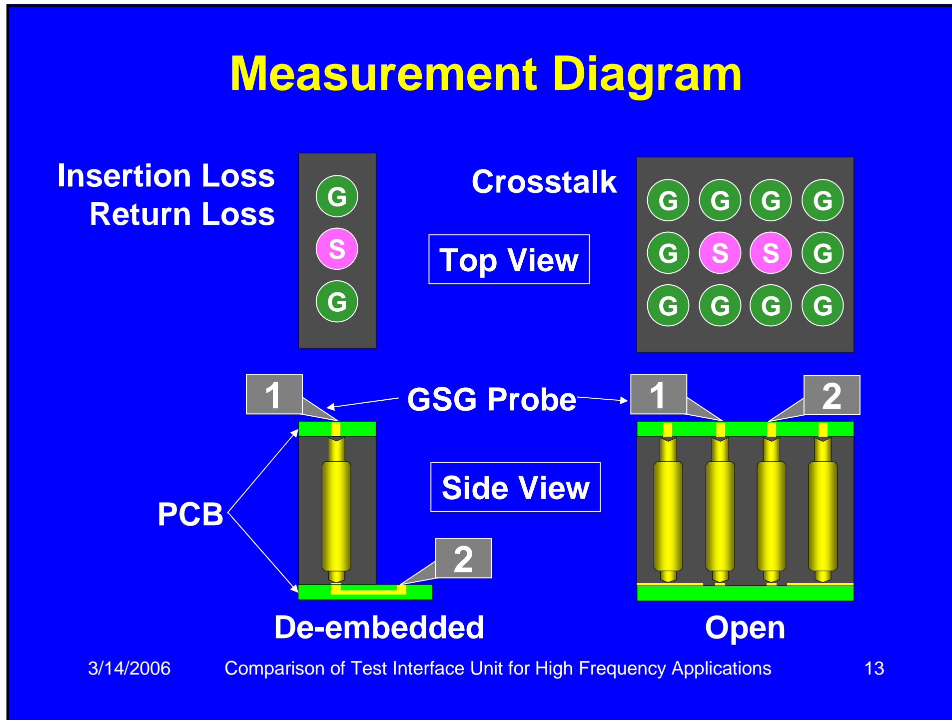
Measurement Diagram
Insertion Loss
Return Loss
G
S
G
Crosstalk
Top View
G G G G
G S S G
G G G G
1
GSG Probe
1
2
PCB
Side View
2
De-embedded
Open
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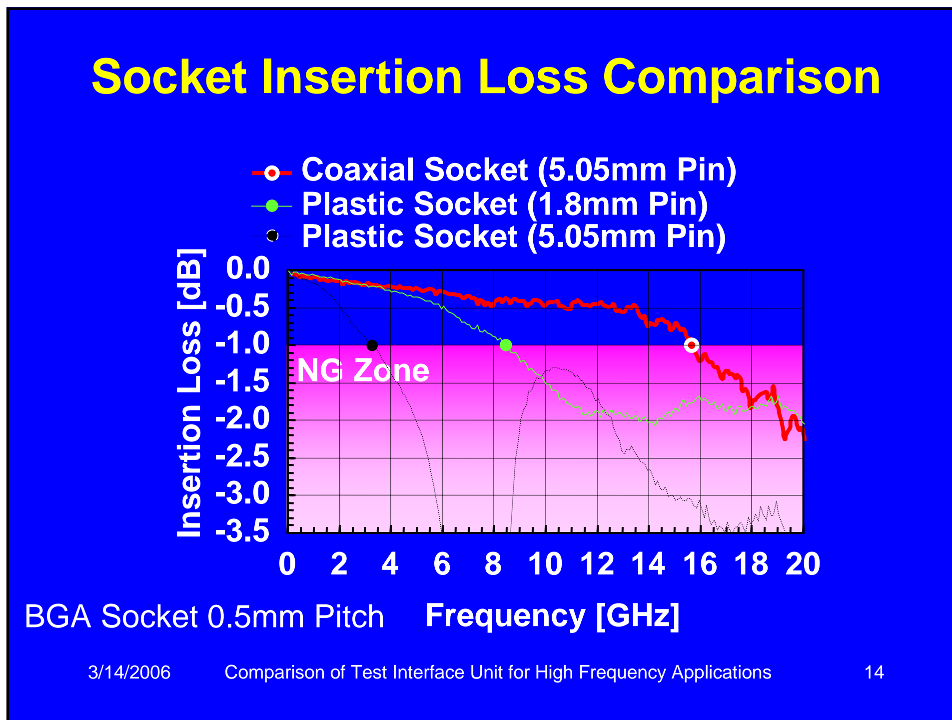
Socket Insertion Loss Comparison
Coaxial Socket (5.05mm Pin)
Plastic Socket (1.8mm Pin)
Plastic Socket (5.05mm Pin)
Insertion Loss [dB]
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-3.0
-3.5
NG Zone
0 2 4 6 8 10 12 14 16 18 20
BGA Socket 0.5mm Pitch
Frequency [GHz]
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Comparison of Test Interface Unit for High Frequency Applications
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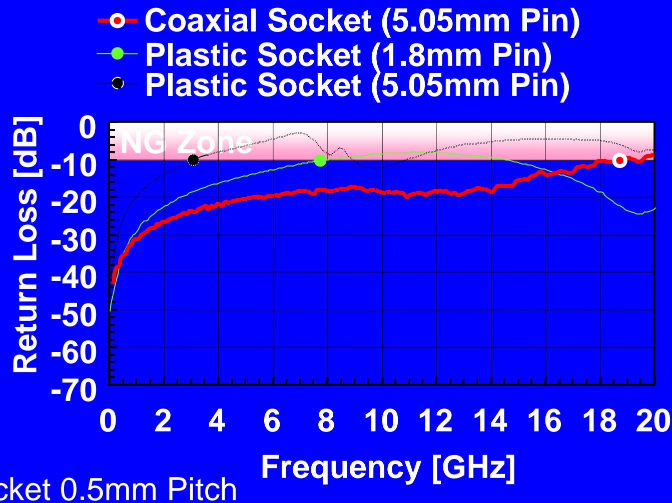
Socket Return Loss Comparison
Coaxial Socket (5.05mm Pin)
Plastic Socket (1.8mm Pin)
Plastic Socket (5.05mm Pin)
NG Zone
Return Loss [dB]
0
-10
-20
-30
-40
-50
-60
-70
0 2 4 6 8 10 12 14 16 18 20
Frequency [GHz]
BGA Socket 0.5mm Pitch
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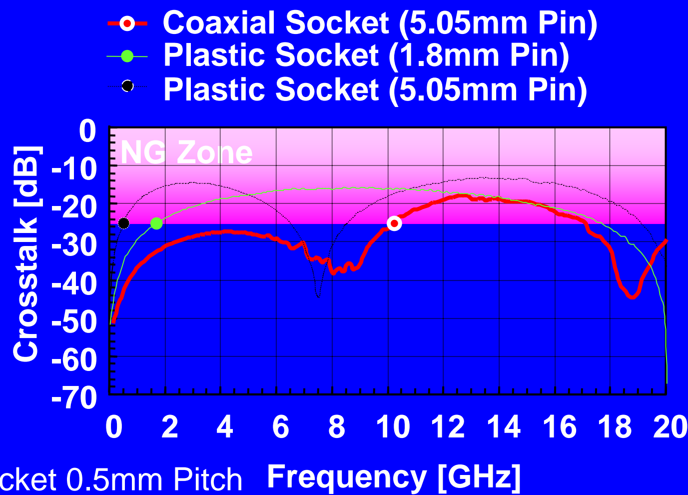
Socket Crosstalk Comparison
Coaxial Socket (5.05mm Pin)
Plastic Socket (1.8mm Pin)
Plastic Socket (5.05mm Pin)
NG Zone
Crosstalk [dB]
0
-10
-20
-30
-40
-50
-60
-70
0 2 4 6 8 10 12 14 16 18 20
Frequency [GHz]
BGA Socket 0.5mm Pitch
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Socket and Board Experiment

- DUT board design and validation for GPS/WSP receiver device.
- PCB Design Simplied
- DUT board tuning effort minimized
- Improvement of Repeatability of RF Parametric Data

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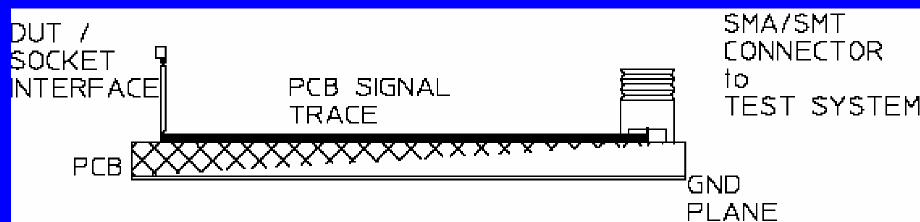
Signal Path Include the Interconnect to the Tester

RF Test Signal Path



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Data Comparison

- Design of DUT PCB solution can be brought to the test much faster because of the critical parameters that must be considered when designing PCBs using conventional plastic bodied sockets are better defined and repeatable.
  (i.e. return loss, insertion loss and crosstalk)

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Data Comparison

- Repeatability of critical RF Parameters such as noise figure, BER, intermod tests, phase noise, EVM tests can be improved with the Hi Giga socket.
  Improvements of 3d from 0.34dB to less than 0.15dB when measuring noise figure.

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Conclusions

- The 50 Ω coaxial RF pins and grounded pins to the metal case improves parametric performance when used on production test boards.
- Metal body of socket minimizes ground inductance.
- Coaxial pins provides a good 50 Ω path to the DUT for critical pins.

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Contact Information

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  Texas Instruments, Inc. (Applications and Data)
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Improving test efficiency by new device interface topology for high parallel testing

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Joachim Moerbt
Advantest (Europe) GmbH

Outline

- Target
- Proposals for high parallel testing
- Transmission Nets Topology
  - Resource Sharing Interface
  - Signal Integrity
- Device Interface Development
- Test and handling concept
- Limitations for Efficiency
- Benefits of the concept
- Conclusion

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Target

- **Prime target for IC manufacturers: Reducing test cost while ensuring product quality**
- **High parallel testing is the most important way to reduce cost of test**
- **Keep efficiency limitations at a minimum**
  - Availability of system resources
  - High cost of channel, power and interface
  - "Non-productive" times

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Proposals for high parallel testing I

High parallel testing with new system

- New generation of test systems
- Enormous test resources

960 DR
576 IO
64 PPS

3584 DR
3072 IO
640 PPS

- Best signal performance
- Additional resources in the test system
- Relatively high initial investment

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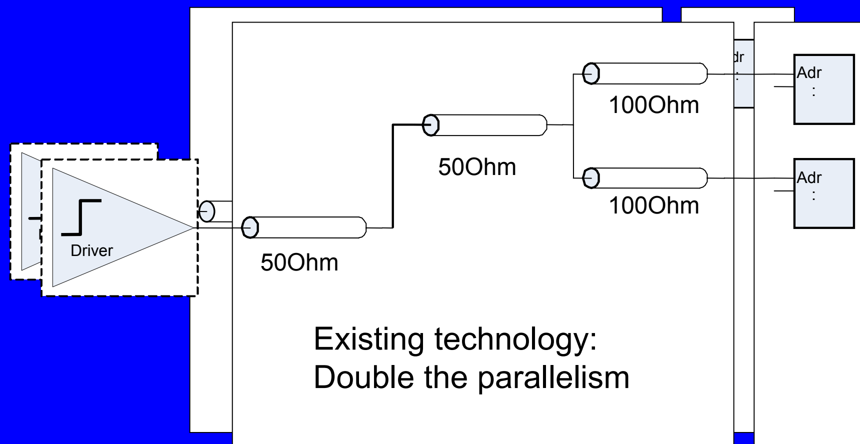
Proposals for high parallel testing II

High parallel testing using existing test system by sharing the tester resources through dedicated signal transmission net topology within the device interface

- Cost effective by using available tester resources
- Flexible device interface required to make the resources usable at the DUT
- Close collaboration with chip designer and test program developer required

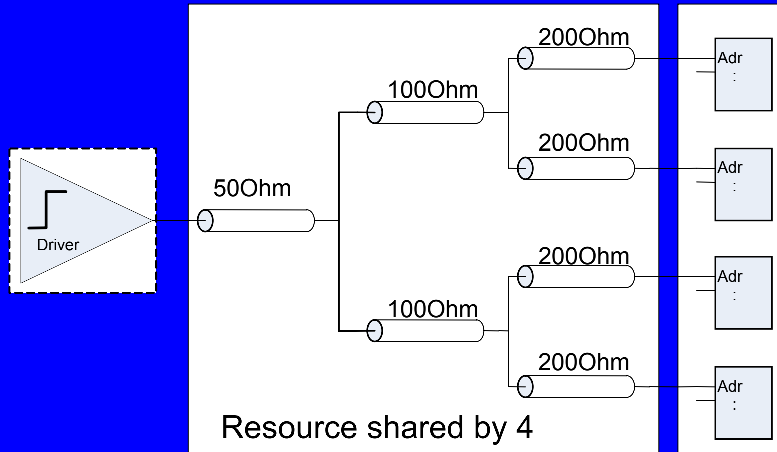
Resource Sharing Interface I

Test System	Device Interface	Device (DUT)
Signal Generator	Signal Transmission	Signal Reciever



Resource Sharing Interface II

Test System Signal Generator | Device Interface Signal Transmission | Device (DUT) Signal Reciever



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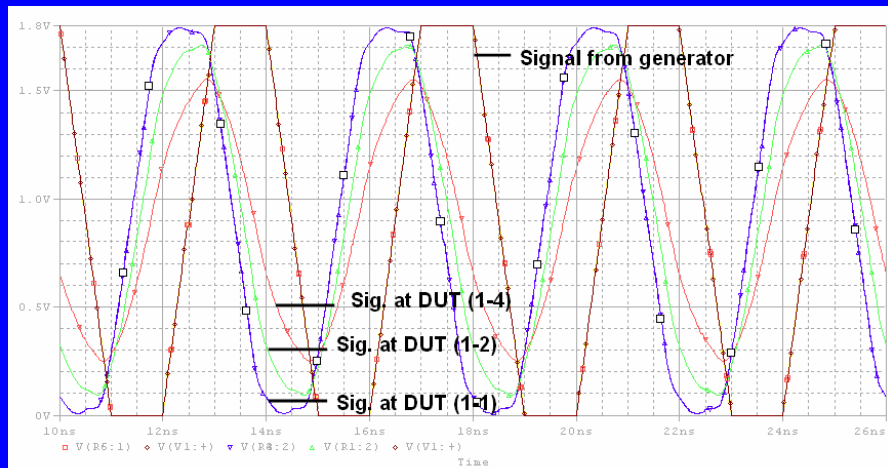
Signal Integrity Analysis I



Simulation of different interface structure at 250MHz

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Signal Integrity Analysis II

Theoretically

- With full impedance matched signal transmission line, signal performance should be independent from topology

However, simulation analysis indicates that the signal RF performance is also constrained by

- Material of transmission line (ε_r, tanδ, etc.)
- Inductive and capacitive load of sockets
- Interconnections and parasitic parameters
- Load of devices

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Device Interface Development

Considering requirements of testing:

- The maximum multiple structure that can be achieved until 250MHz is one to four.

Practically:

- Limitation of 200Ohm transmission line on a PCB by:
  - Cost-efficient available materials
  - Thickness of the PCB
- A new device interface is required, considering
  - Signal performance
  - Manufacturability of PCB and device interface
  - Cost factor of PCB and device interface
  - Flexibility for reusability

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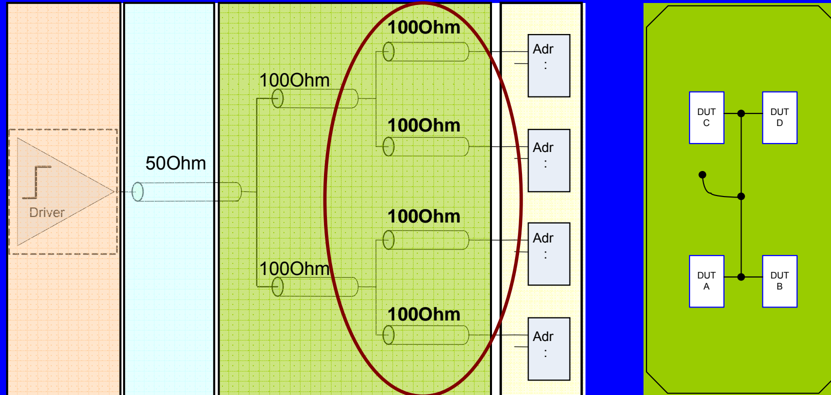
Modular design concept
Test System
Universal Base
Unique interface board (PCB)
DUTs
PCB Design Concept
Driver
50Ohm
100Ohm
100Ohm
100Ohm
100Ohm
100Ohm
100Ohm
Adr
DUT C
DUT D
DUT A
DUT B
Device Interface topology with impedance mismatch
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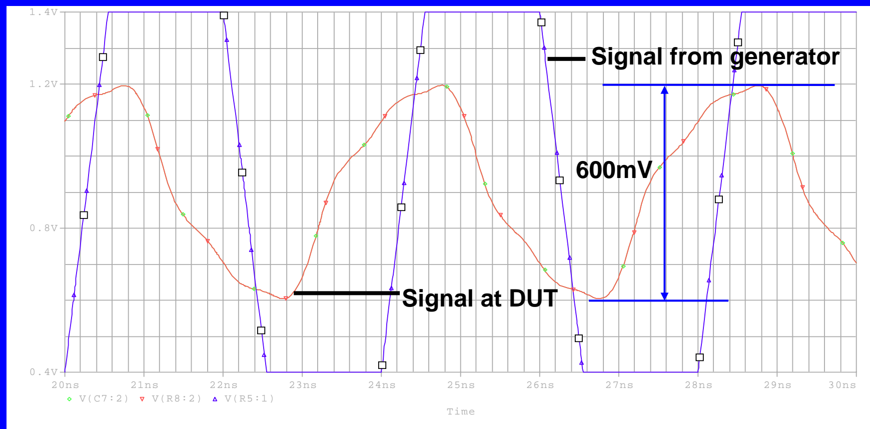
Simulation I
Signal from generator
600mV
Signal at DUT
Simulation of interface concept at 250MHz
with mismatched impedance
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Simulation II

Result:

Simulation waveform at 250MHz considering the test conditions

- Comparing with full impedance matched design, the device interface can achieve sufficient signal performance
- More than +/-250mV amplitude thresh-hold at the device even with mismatched impedance

Implementation I

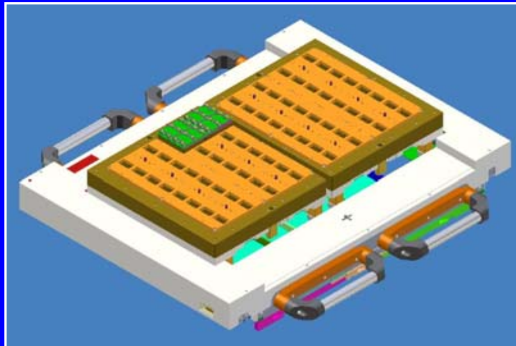
PCB - Layer stack-up

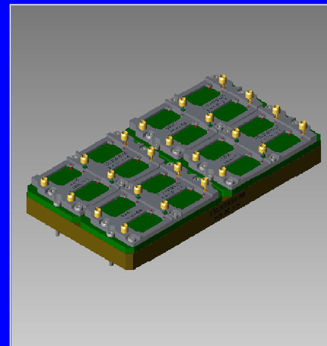
- Buried vias on individual cores avoid multiple pressing
- Dedicated impedance controlled strip line topology is applied to keep the board thickness
- Cross talks avoided by rectangle arrangement of strip lines in adjacent signal layers
- Excess inductance caused by increasing board thickness is eliminated
- Board is producible at acceptable cost

Implementation II

Flexible Device Interface consisting of:
Universal Base Unit

Exchangeable Socket Board Unit





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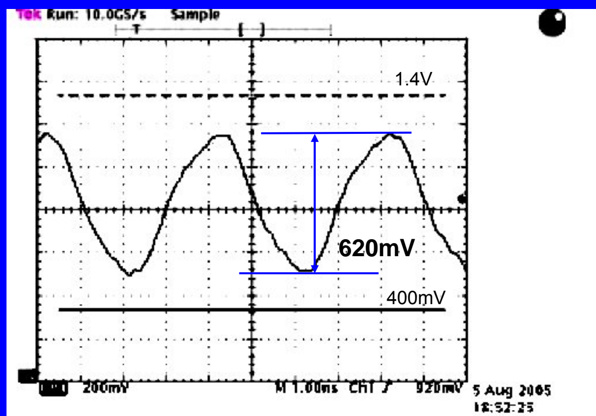
Implementation III

Measurement at 250MHz



Signal swing from Generator: 0.4V - 1.4V

Waveform measured with device under testing

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Benefits and Constraints I

- **Constraints of resource sharing:**
  - It is not feasible to distribute one resource to unlimited quantity of devices only with passive nets.
- **Test frequency is limited in shared resource testing, because of**
  - the impedance mismatching
  - device load
  - loss along the transmission lines

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Benefits and Constraints II

Advantages of the Implementation:

- Maximum frequency of 250MHz with 256 DUT
- Most flexible interface topology
  - Flexible signal distribution
  - Flexible resource arrangement
- Cost reduction by independent manufacturing of Base Unit and Socket Board Unit
- User friendly maintenance - reduced downtime, increased productivity
- Less warehouse space

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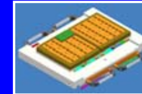
Test and Handling Concept

To judge the test efficiency, the total test cell must be considered

- 1 x Tester (Driver/IO/PPS)
- 2 x Testhead (station)
- 2 x HiFix (256 DUT)
- 2 x Handler and Change Kit (256 DUT)



Used system:

- Tester @ 250 MHz, HiFix 4-shared driver, 4 I/O per DUT;
- Handler: 256 DUT per station
- 2 step testmode: Device core test separated from speed test

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Limitations for Efficiency I

Existing throughput losses at device test

- Lot size effects (~12%)
  - Loading/Unloading the lot
  - Handler/Temperature setup and shut down time
- Scheduled/unscheduled downtime (~6%/~6%)
  - Preventive maintenance/cleaning/daily checks
  - Equipment down (jam/repair/waiting on parts)
- 2 station synchronisation (~6%)
  - Test cell as fast as slowest handler
  - Lot ends are not synchronized
- Flexibility/Granularity/Product Mix (~3%)

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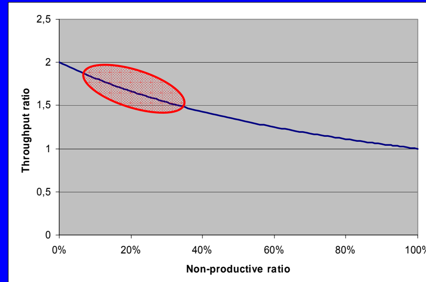
Limitations for Efficiency II

Throughput compared between 128 vs. 256 DUT per test station



Low "Non-productive time" is essential for test efficiency by increased parallelism

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Limitations for Efficiency III

4-shared concept limitations caused by test cell:

- Limited power supplies at existing tester
- Limited tester resources (driver and I/O channels)
- Frequency limited at 250MHz for core test
- Highest reliability required for tester, handling system and sockets
- Increased weight and size of device interface requires additional tooling

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Benefits of the concept

Efficient usage of existing tester resources by:

- Increasing parallelism by 4-shared Flexible Device Interface at maximum tester speed
- Availability of high reliable high parallel handling system for highest utilisation of existing test stations
- Doubled the test capacity at nearly same production floor
- Reducing test cost per device
- Increasing total throughput by ~ 1.6
- Highest efficiency for high volume products

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Conclusion

Comment of our customer

"2x256 DUT is very promising … as long as it is running"

Special thanks to Mrs. Rose Hu, co-author and project leader of 4-shared HiFix development

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Socketing the Impossible

A Very Fine, Very Dense Case Study

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

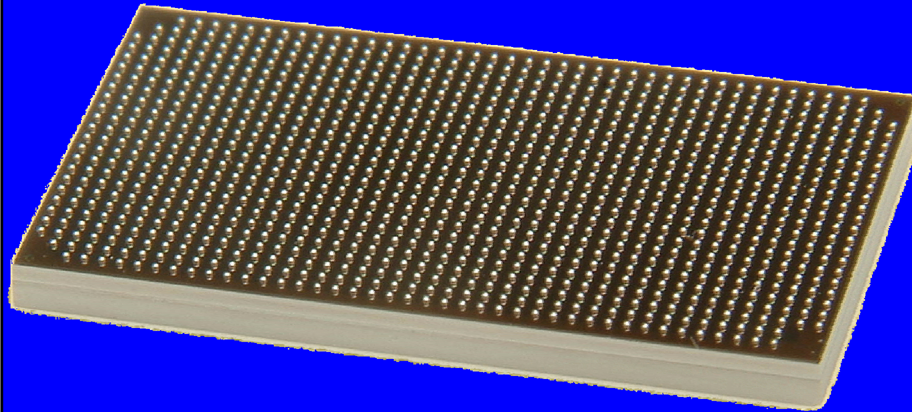
Jon Diller, Kiley Beard; Takuya Tsumoto
Synergetix; NEC Corporation

Project Overview

- "BGAs are easy"
  – Jon Diller, 2005
- Challenge: Socket a very dense device
  - Device description
  - Test platform considerations
  - Contact selection
  - Socket design
  - Actual results

March 14, 2006 Diller/Beard/Tsumoto: Socketing the Impossible 2

Device Description



- ‘nano’ BGA / WLCSP memory device
- >1000 0.12Ø balls on 0.28 mm pitch

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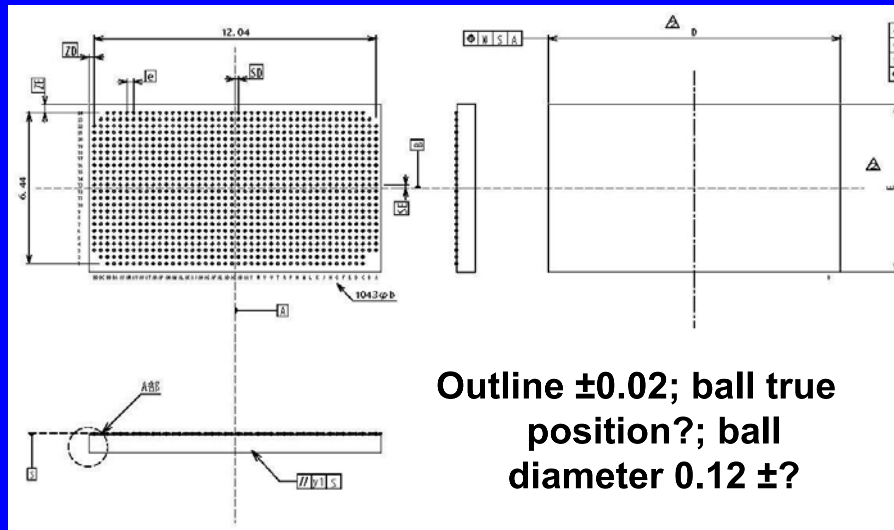
Device Description



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Platform Considerations

- Production test to be optically aligned with proprietary test handler
- Production sockets therefore pure interposer
- Add-on alignment ineffective
- Separate manual test socket for development

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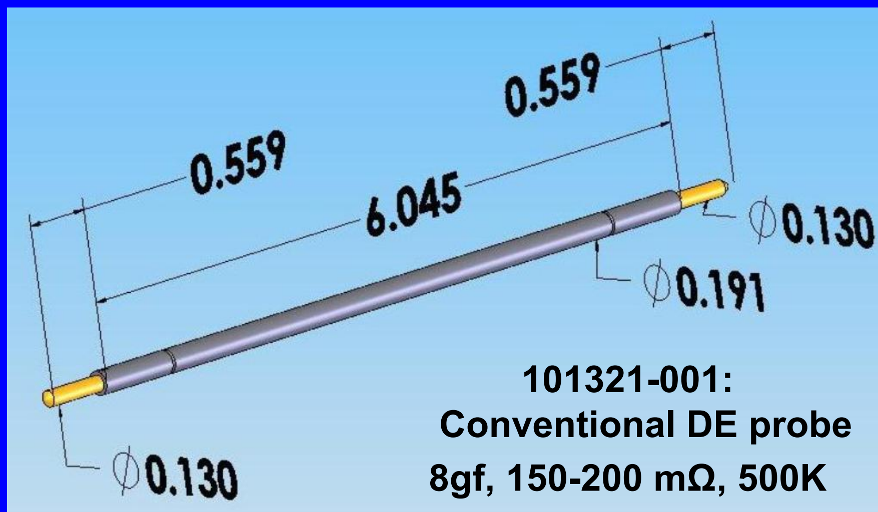
Contact Selection



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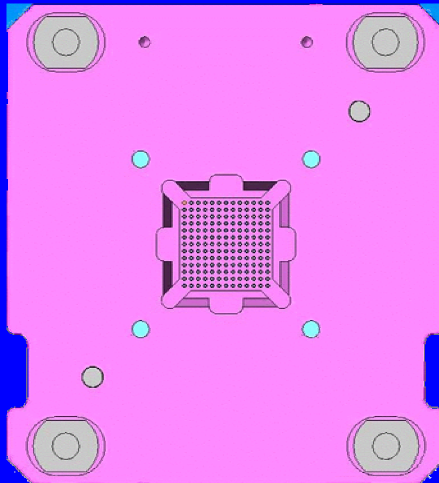
Socket Construction

Fixed Device Alignment Pocket



- Simplest
- Mechanically strong
- Exposed probes
- Relies on edge alignment
- Clearance produces shift

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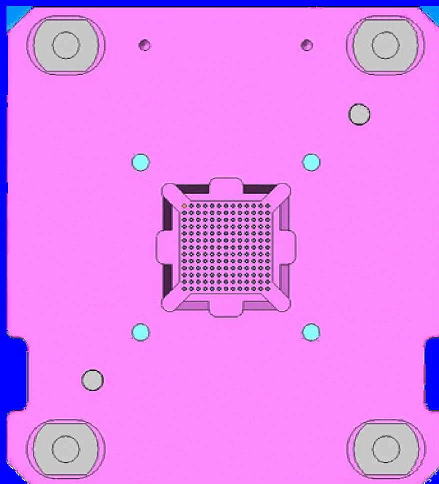
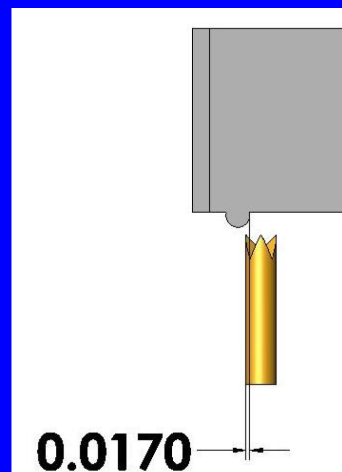
Socket Construction

Fixed Device Alignment Pocket





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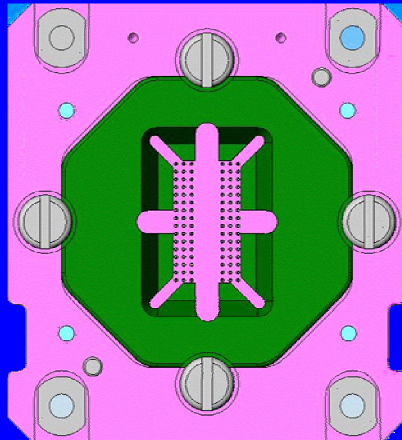
Socket Construction

Windowpane Floating Nest



- Alignment from leads
- Normally preferred for BGAs
- Probe too short
- Edge < TP + Ø

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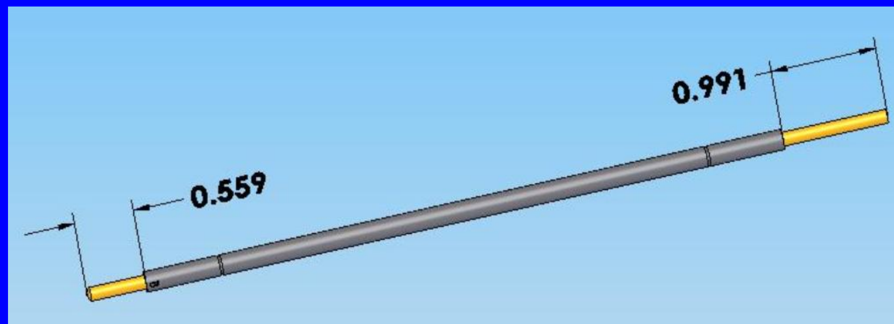
Contact Respecification

101405-001



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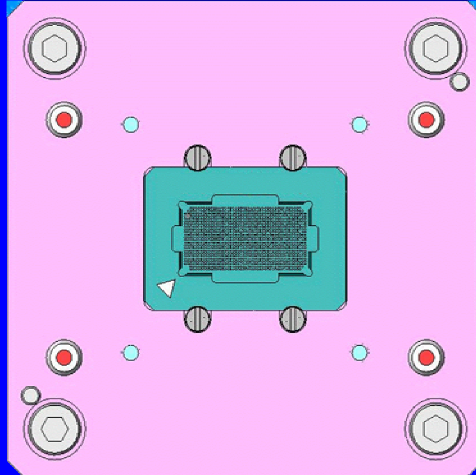
Socket Construction

One-Ball-One-Hole



- Controls flagpoling
- Miss limited to probe diameter minus hole diameter
- Prevents overcompression

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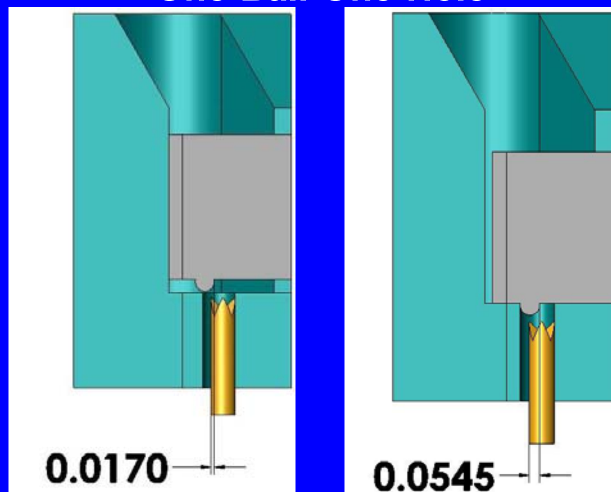
Socket Construction

One-Ball-One-Hole



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Accuracy Results

Actual Dimensions

- Measured ball TP no worse than 0.005
- Ball diameter 0.1126 to 0.1150
- Nest substrate alignment +0.015 / +0.020 vs. nominal
- Average nest hole TP no worse than 0.007
- Nest hole Ø -0.001 typical vs. nominal

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Accuracy Results

Test Process

- Cycle 10 sample devices 1x with HSL
- Review and record witness mark character and location
- Compare witness marks statistically

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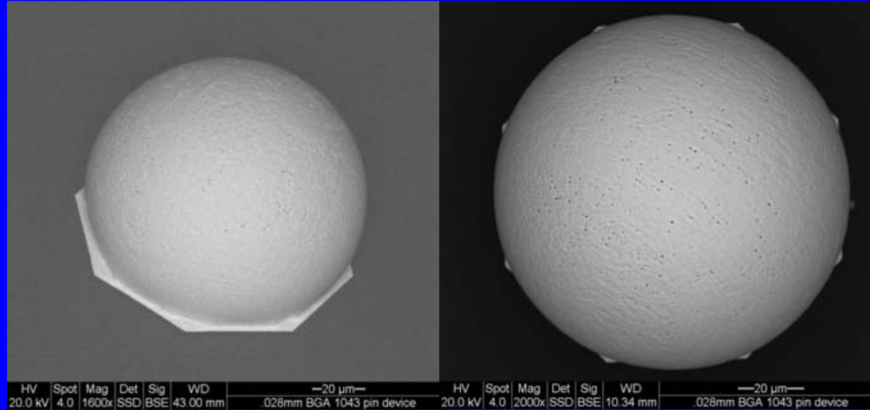
Accuracy Results

Witness Marks



Before cycling

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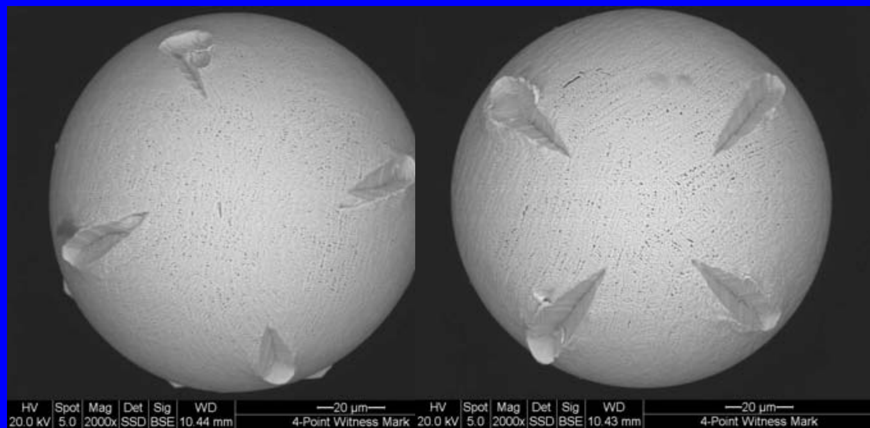
Accuracy Results

Witness Marks



Four points

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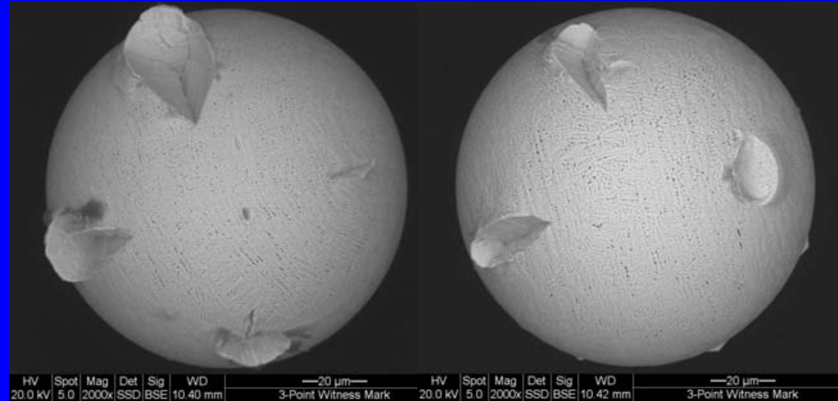
Accuracy Results

Witness Marks



‘Three’ Points

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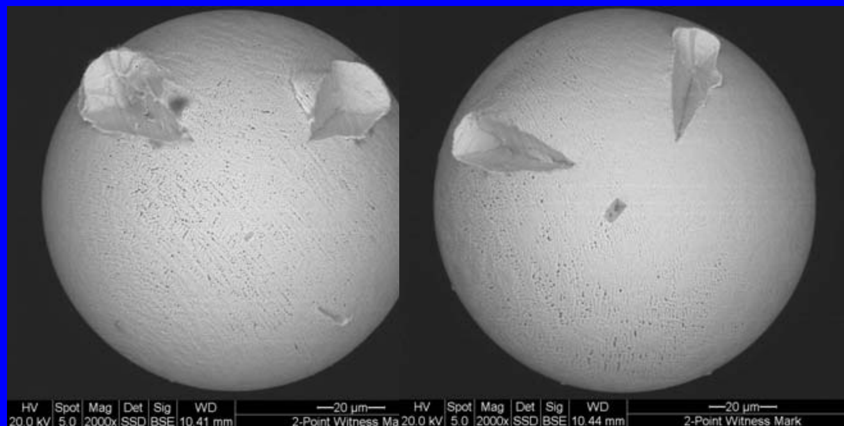
Accuracy Results

Witness Marks



‘Two’ Points

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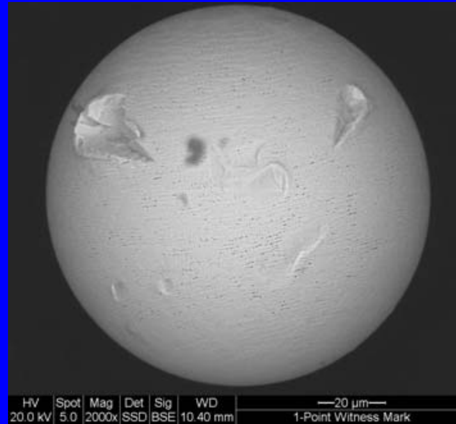
Accuracy Results

Witness Marks



'One' Witness Mark

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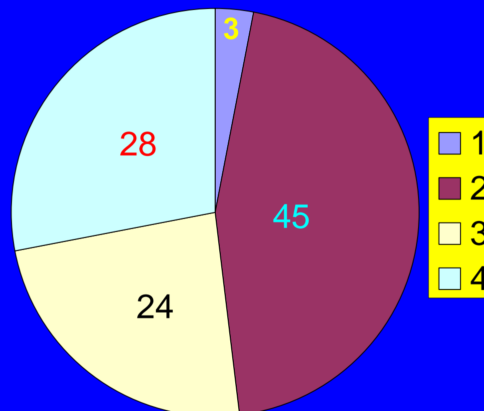
Accuracy Results

Witness Marks, %



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Conclusions

- Socket construction viable for contact
- Potential for significant wear, contamination
- Witness marks likely to be acceptable
- Shorter probes in interposer may mitigate plunger lean
- Socket now in evaluation at NEC

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