ARCHIVE 2006

Session 5

High Frequency Design And Measurement Considerations

"Properties Of Electrical Contacts At High Frequencies"
Roland S. Timsit, Ph.D., PE — Timron Scientific Consulting, Inc.

"Accuracy Improvements In Microwave Measurements By Double-Sided Probing"
Habib Kilicaslan, Bahadir Tunaboylu, David McDevitt
Kulicke & Soffa Industries

"Effects Of The Launch On Bandwidth"
Ryan Satrom — Everett Charles Technologies - STG

Properties of Electrical Contacts at High Frequencies

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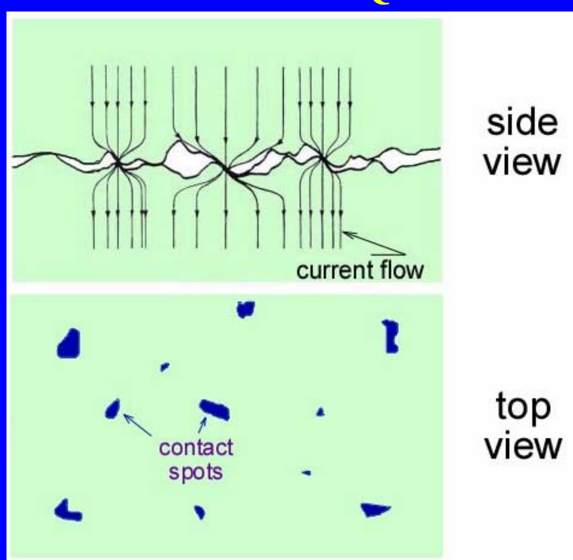
CONSTRICTION RESISTANCE AT DC AND LOW FREQUENCIES



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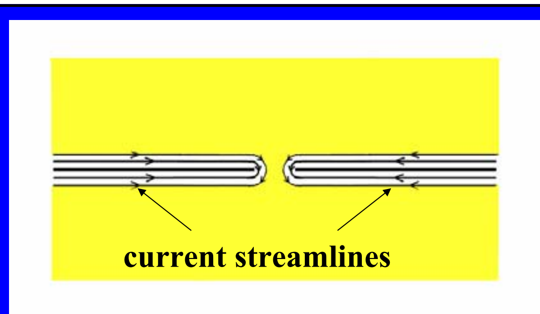
EFFECTS OF FREQUENCY: SKIN EFFECT



Under alternating current (AC) conditions, current penetrates into a conductor to an electromagnetic "penetration depth" δ

$$\delta = [\rho / \pi f \mu_0]^{1/2}$$

ρ = *resistivity*
μ_0 = *magnetic permeability of free space*
f = *excitation frequency in Hz*
δ = *2.2 µm in copper at 1 GHz*

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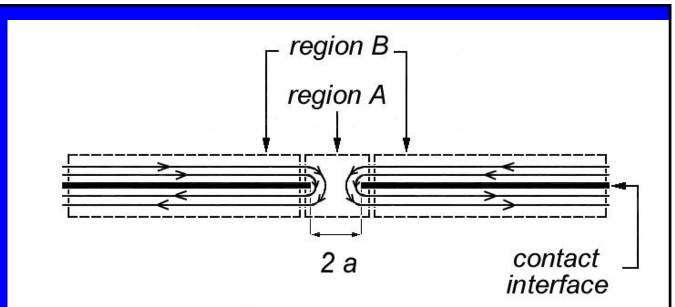
EFFECTS OF FREQUENCY



Total Connection Resistance **=**
Constriction Resistance **(R_δ in Region A) +**
Resistance of "External" Ring **(R_{bulk} in Region B)**

R_{bulk} = Resistance of "External" Ring = ($\rho / \pi \delta$) ln (R_{ring} / a')

δ = electromagnetic penetration depth
R_{ring} = outer radius of "External" ring
a' = inner radius of "External" ring
ρ = resistivity

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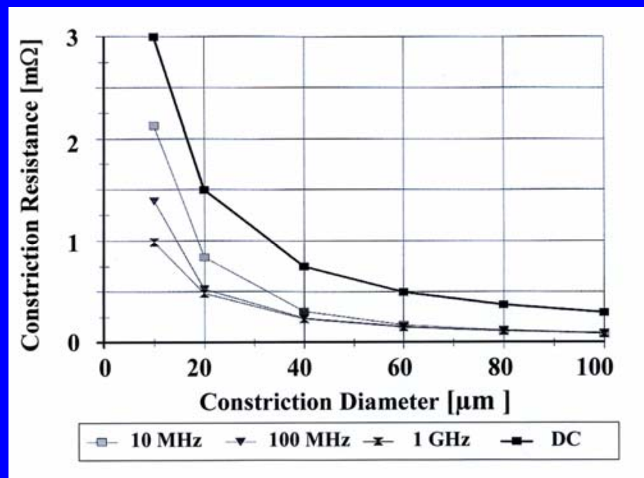
CONSTRICTION RESISTANCE R_δ AT HIGH FREQUENCIES



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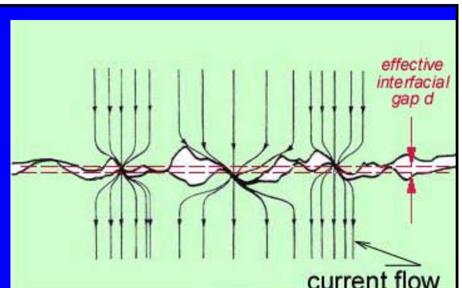
MODEL OF A CONTACT AT HIGH FREQUENCIES

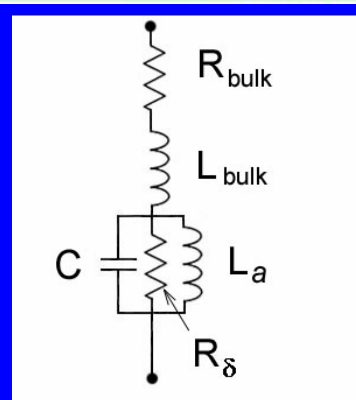


In addition to resistance, there are impedance components stemming from interfacial capacitance and constriction inductance

C $= \varepsilon_r \varepsilon_0 A / d$ where A is the nominal contact area

$L_{bulk} = (\mu_0 \delta / 8\pi) \ln(R_{ring} / a')$

$L_a = \mu_0 \delta / 4\pi$ = self inductance of constriction



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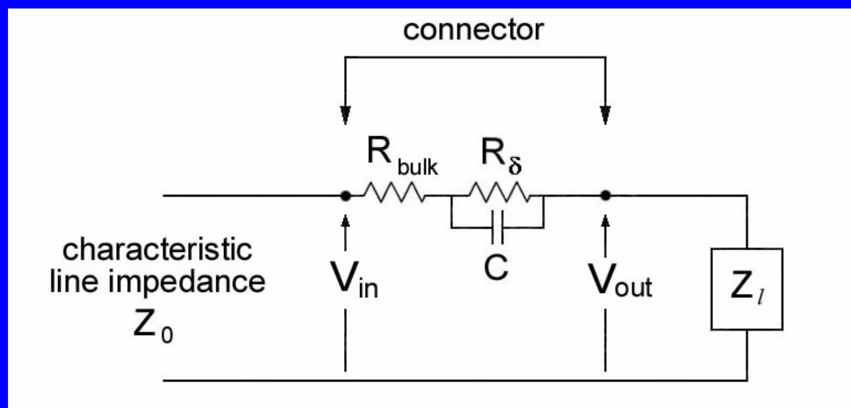
Paper #1



attenuation coefficient $\beta = V_{out} / V_{in}$

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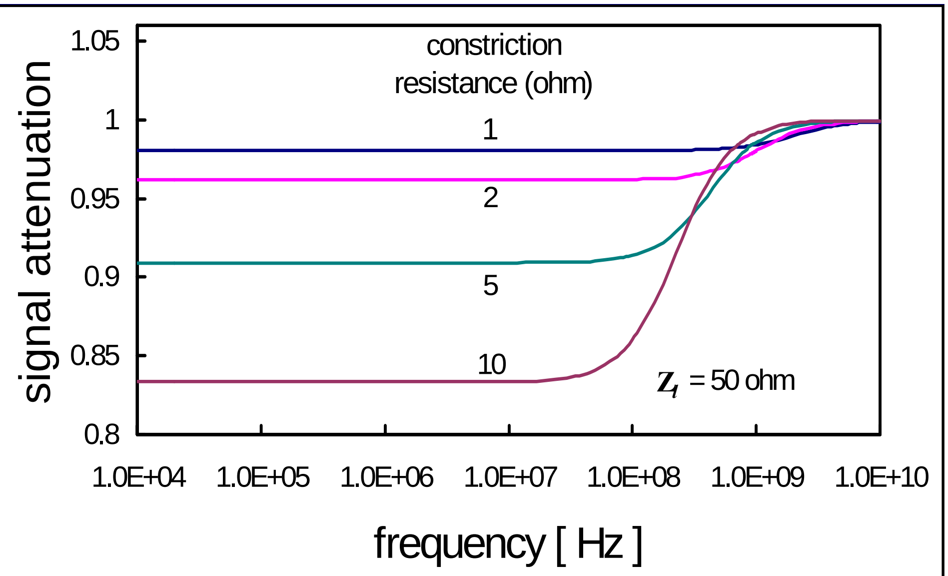
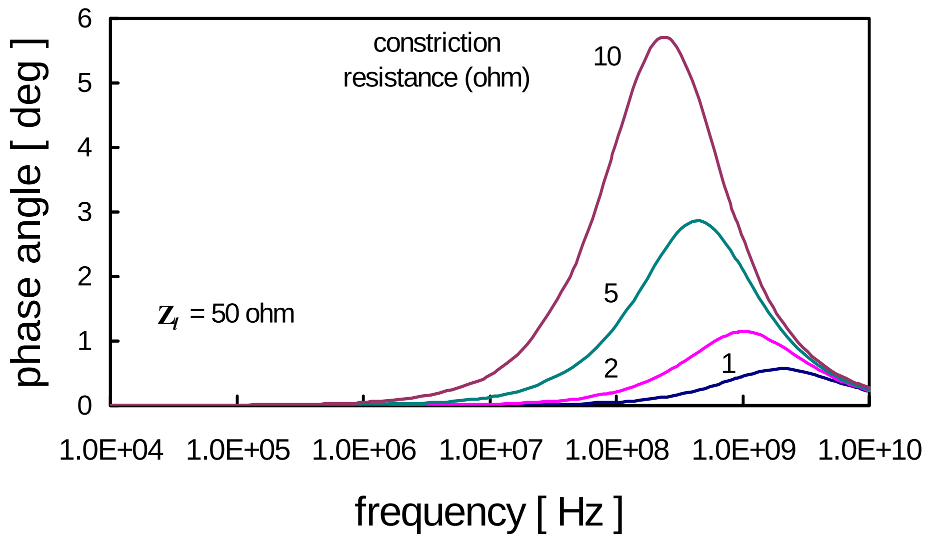


Dependence of the attenuation coefficient β on signal frequency for values of R_δ ranging from 1 to 10 Ω, on the basis of a load Z_l matched to the line impedance of 50 Ω.. C = 80 pF, R_{ring} = 100 µm, *a* = 5 µm. 8



Dependence of phase angle on signal frequency for values of R_δ ranging from 1 to 10 Ω, on the basis of a load Z_l matched to the line impedance of 50 Ω.

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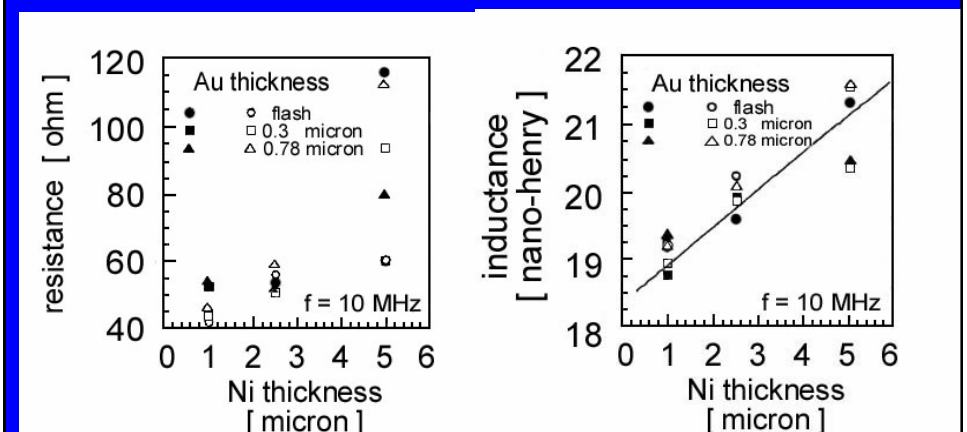
ELECTROPLATES IN HF CONNECTORS



(a) **(b)**

(a) Resistance of a nickel electroplate versus electroplate thickness, measured at 10 MHz,
(b) inductance properties of the electroplate in (a).
[*Yamaguchi et al, 1997*]

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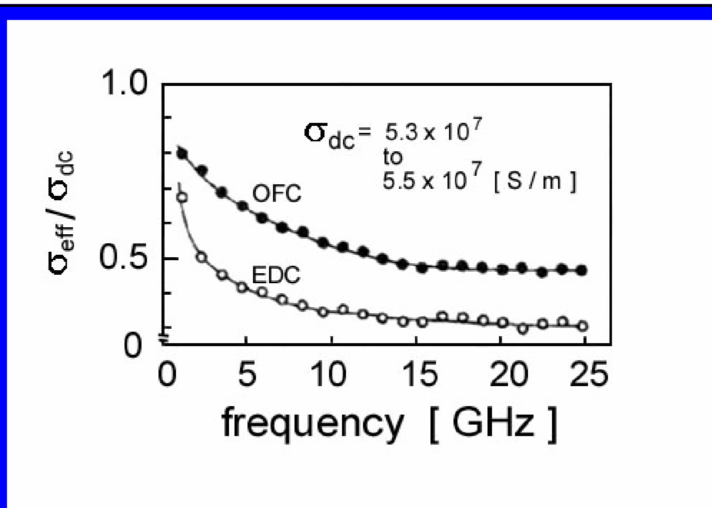

Dependence on frequency of the effective electrical conductivity of electrodeposited copper (EDC) characterized by a roughness (ra) value of 1.5 µm, and a smooth oxygen-free copper (OFC) surface characterized by a roughness value of 0.1 – 0.2 µm.

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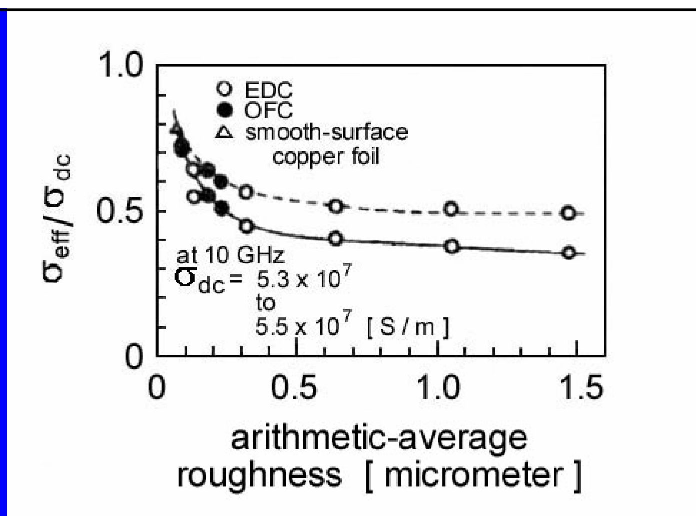

Dependence of the effective conductivity of EDC and OFC on surface roughness (ra), measured at a signal frequency of 10 GHz. [*Tanaka and Okada, 1989*].

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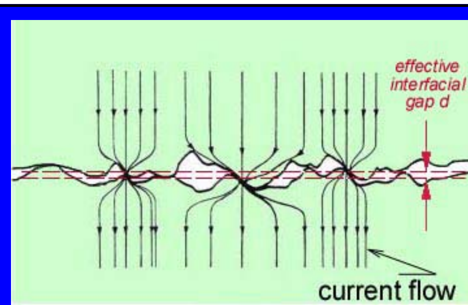
TEMPERATURE IN AN ELECTRICALLY-HEATED CONTACT



thermal risetime τ of a contact spot of radius "a"

$$\tau = C\, a^2 / 4\lambda$$

where C = conductor heat capacity

λ = thermal conductivity

For copper, C = 3.44 J cm^{-3} ^{0}C^{-1}

λ = 4 W cm^{-1} ^{0}C^{-1}

so that τ = 2.2 x 10^{-7} s for a contact spot with a = 10 µm

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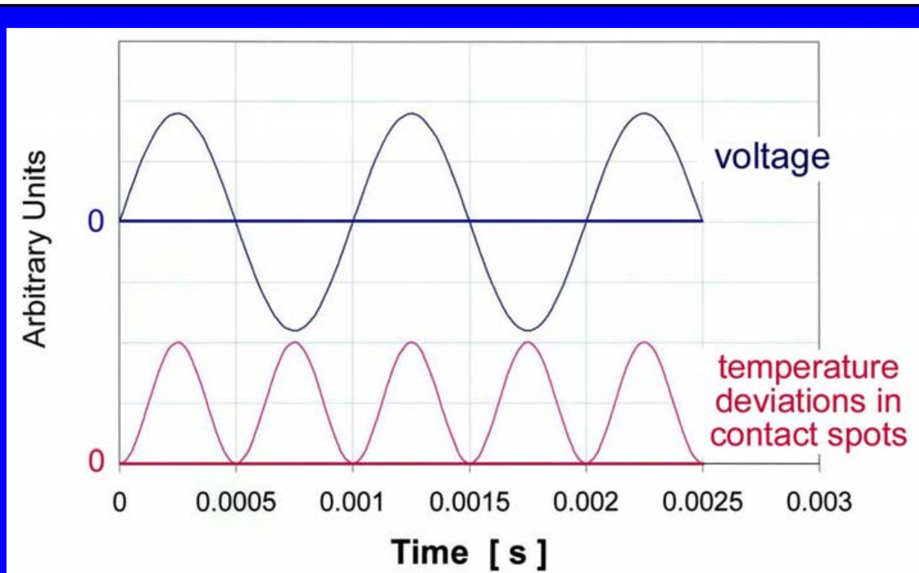

Illustrative effects of a 1 kHz signal on the voltage drop across a contact, and the associated temperature variations.

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TEMPERATURE IN AN ELECTRICALLY-HEATED CONTACT

- *in practice, the temperature variations in a contact spot due to an AC current will not be purely sinusoidal because resistivity increases with temperature*
- *harmonic signals are introduced*
- *third harmonics are strongest*

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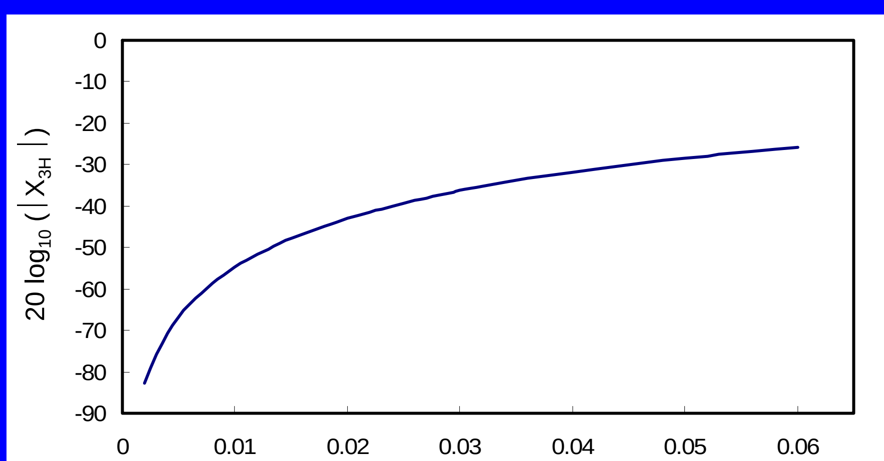
HARMONICS GENERATION



voltage amplitude V_0 [V]

Strength of third harmonic signal (relative to input signal) generated in a copper-copper contact due to contact heating.

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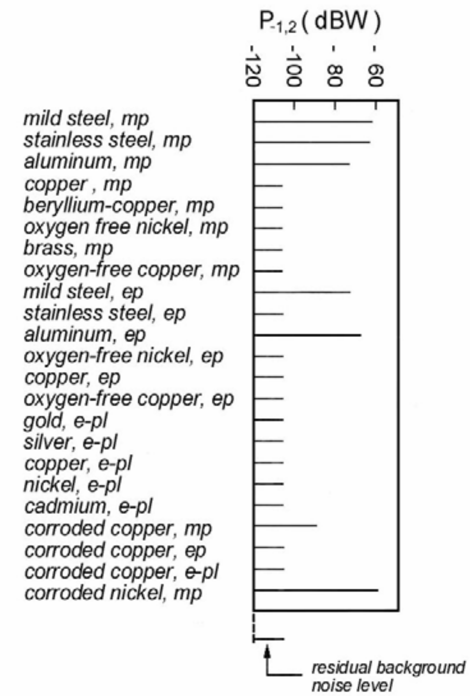
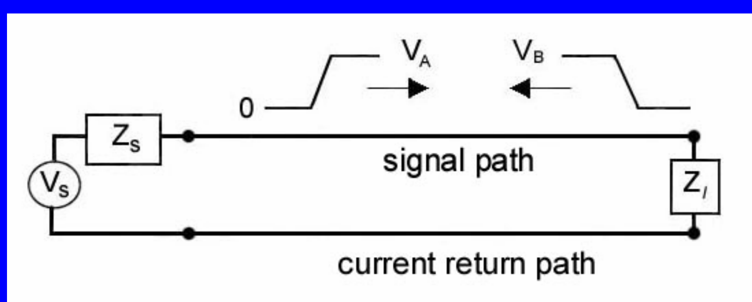
HARMONICS GENERATION

Relative 3rd-order inter-modulation product amplitudes for several metal-metal contacts at frequencies ranging from 1.5 to 6 GHz;
mp **– mechanically polished**
ep **– electropolished**
e-pl **– electroplated**
[*Arazm and Benson 1980*]

Note: conduction through insulating surface layers by electronic tunneling also give rise to 3rd-order harmonics





At the load

$$Z_l = V(l) / I(l)$$

and the reflection coefficient is given as

$$\rho_r = [Z_l - Z_0] / [Z_l + Z_0]$$

Z_0 = **line characteristic impedance**

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SIGNAL TRANSMISSION AT HIGH FREQUENCIES

Connectors are designed to be impedance-matched to the line, such that $Z_{con} \approx Z_0$, to minimize signal reflection and maximize the transmitted signal amplitude with minimal distortion

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SIGNAL TRANSMISSION AT HIGH FREQUENCIES

Connector impedance

$$Z_{con} = [\, L_{con} / C_{con} \,]^{1/2}$$

L_{con} and C_{con} contain respectively all stray inductance and capacitance i.e. between pins and connector housing/shield

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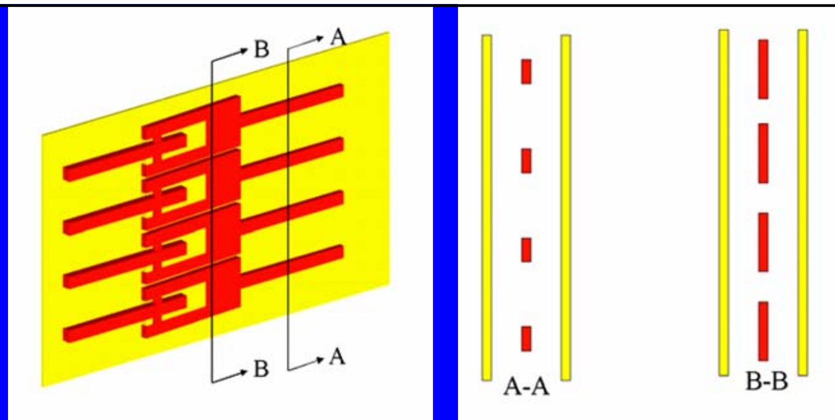

In many HF connectors, the change in geometry of connector elements in the contact region is minimized through the use of "tuning fork" receptacles. *However, the small but abrupt residual geometrical change (change in profiles at AA and BB) still introduces a small impedance mismatch. For a nominal connector impedance of 100 Ω, the change in contact profile may introduce a variation in Z_{con} of ~ 50 Ω.*

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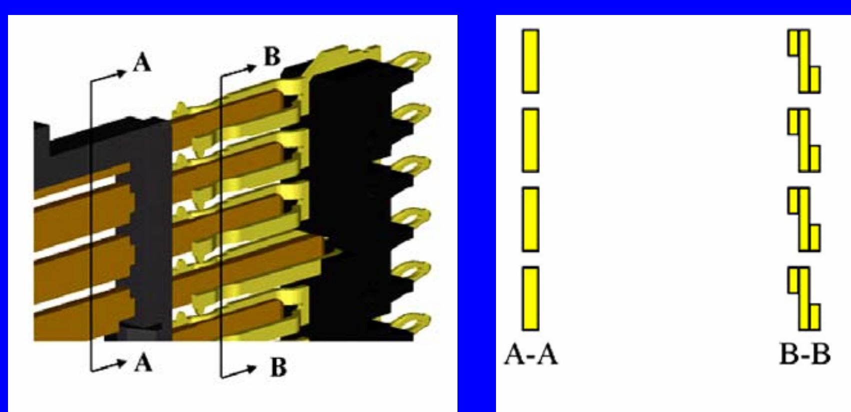
ADVANCES IN HF CONNECTOR DESIGN: COPLANAR WAVEGUIDE



In the coplanar waveguide design, the change in cross-sectional profile at the pin/receptacle is small and does not introduce a significant change in connector characteristic impedance.

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SUMMARY

- *electrical contacts are made at small contact spots*
- *control of surface roughness and contact geometry are important to minimizing both signal loss and signal distortion*
- *the presence of contaminant films on contacting surfaces not only increases contact resistance but also introduces 3rd-harmonic parasitics*
- *heating of contact spots also leads to 3rd-harmonic generation*

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SIGNIFICANCE OF BURN-IN IN HF ELECTRICAL CONTACTS

- *Pass a large current through contacts*

  possible beneficial effects:

  - slight overheating of contact spots, causing negligible metallurgical effect, may soften contact spots and increase the true contact area to reduce contact resistance

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SIGNIFICANCE OF BURN-IN IN HF ELECTRICAL CONTACTS

- *Pass a large current through contacts*

  possible deleterious effects:
  - *overheating of contact spots with possible metallurgical changes in the contact region*
  - *increased oxidation and increased parasitics*
  - *overheating of contact springs or connector components with possible decrease in contact force due to stress relaxation or metal-creep, with possible effect on Z_{con}*

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SIGNIFICANCE OF BURN-IN IN HF ELECTRICAL CONTACTS

- *Reciprocating motion of pin in socket while passing current, but without contact disconnect*

  major beneficial effect:
  - *disperse surface contaminant films and reduce contact resistance*

  possible deleterious effects:
  - *generate unwanted mechanical wear on contact surfaces and removal of thin protective electroplates*
  - *disturb contact geometry and affect the connector impedance Z_{con}*

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ACCURACY IMPROVEMENTS IN MICROWAVE MEASUREMENTS BY DOUBLE-SIDED PROBING

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Measurement challenges

- Different socket geometries need characterization
  - Socket-interconnect heights have large variations (1mm to 30mm).
  - Socket-interconnect pitches have large variations (0.4mm to 5mm).
- Socket bandwidth can be several tens of GHz at -1 dB insertion loss point requiring full utilization of existing VNA measurement bandwidth (40 GHz).
- Several pin configurations need to be characterized.

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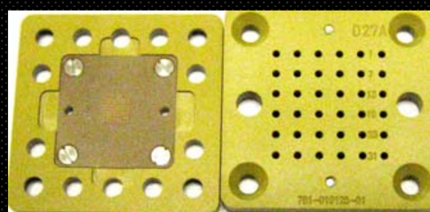
Measurement challenges

- For circuit analysis spice models have to be extracted matching measured S-parameters.
- Simulations should correlate with measurement results.
- If needed embedding and de-embedding calculations should be easily carried out.



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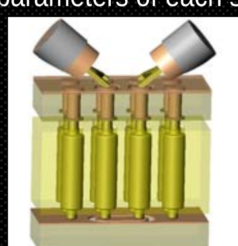
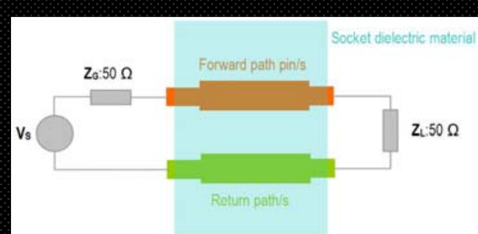
Measurement results

- To reduce measurement errors closed circuit path should be examined for additional board effects etc.
- For given measurement results forward and return path should be defined.
- S-parameters are used due to lack of ideal short or open.
- Embedding or de-embedding is always possible by knowing the S-parameters of each structure.





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Should board and package affects be added?

- Although pads and PCB traces could be emulated on fixture boards, real PCB and package design may be different from the fixture design.
- If measured together, to effectively use measurement results, PCB design and package design should match the fixture design, restricting design options.
- If only the socket S-parameters is known, PCB and package effects can be added by cascading.

$$[ABCD]_{TOTAL} = [ABCD]_{PCB} * [ABCD]_{SOCKET} * [ABCD]_{PACKAGE}$$

$$A = (1 + S_{11} - S_{22} - S_{11}S_{22} + S_{21}S_{12})/(2S_{21})$$
$$B = (1 + S_{11} + S_{22} + S_{11}S_{22} - S_{21}S_{12})Z_0/(2S_{21})$$
$$C = (1 - S_{11} - S_{22} + S_{11}S_{22} - S_{21}S_{12})/(2S_{21}Z_0)$$
$$D = (1 - S_{11} + S_{22} - S_{11}S_{22} + S_{21}S_{12})/(2S_{21})$$

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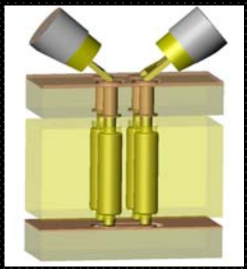
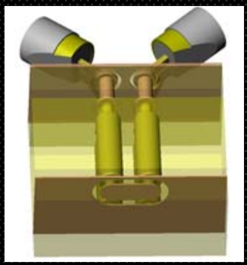
Existing measurement methods

METHOD 1 [1]

- Circuit loop includes landing board via effects and surrogate board effects. Loop through method.
- Although de-embedding is possible for vias (pose same difficulties similar to measuring a socket requiring double-side probing), de-embedding is difficult for surrogate board.
- Higher the socket pitch more the error introduced. Higher the socket height more the error introduced.
- GS-SG probe pair or GSG probes are used.
- Pin configurations are easy to implement on board. In general corner, edge and field configuration are implemented.





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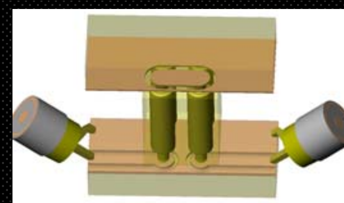
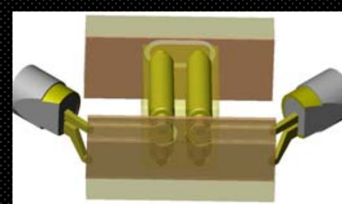
Existing measurement methods

METHOD 2

- ❑ To remove via effects CPW is added on both end of the circuit loop. Loop through.
- ❑ Routing CPW in between pins has inherent difficulties for fine pitches.
- ❑ De-embedding CPW effects is relatively easy
- ❑ De-embedding surrogate board effects is difficult so at large pitch creates error.
- ❑ GS-SG or GSG probes are used.
- ❑ Pin configurations can be implemented on board designs.





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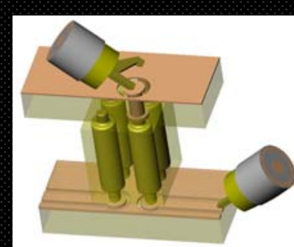
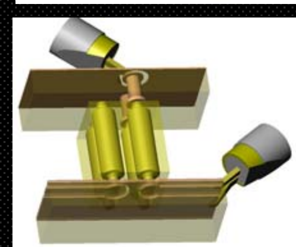
Existing measurement methods

METHOD 3 [2]

- ❑ To remove short effects from surrogate board landing board with vias is used. No loop through.
- ❑ Short effects are removed by using CPW on landing board.
- ❑ If via effects are de-embedded than it is error free measurement method (pose same difficulties as characterizing a socket).
- ❑ Pin configurations are easy to implement on board.





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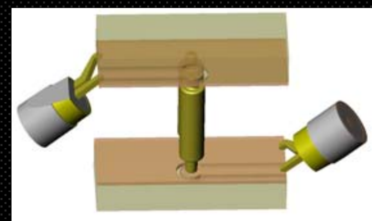
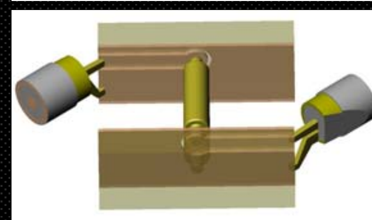
Novel measurement method

METHOD 4

- Via effects on landing board are eliminated by using CPW layout, requiring double-sided probing. No loop.
- After de-embedding of CPW lines, it is error free.
- Pin configurations are easy to implement on board.
- Fully utilize VNA bandwidth.
- By using inverted CPW structure double-sided probing no longer required.
- GS-GS or GSG probes are used.





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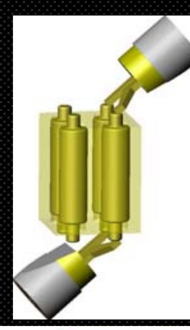
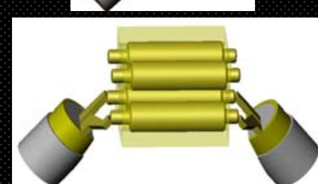
Direct

METHOD 5

- No board is used so no error introduced.
- Pin compression is achieved by microwave probes.
- Pins should be compressed to recommended pin compression distance.
- Pin configurations cannot be implemented. Mathematical calculations should be carried out.
- Fully utilize VNA bandwidth.
- GS-GS probe pair is used at horizontal setup. GS-SG probe set is used at vertical setup. GSG probes can be used with three pins as well.





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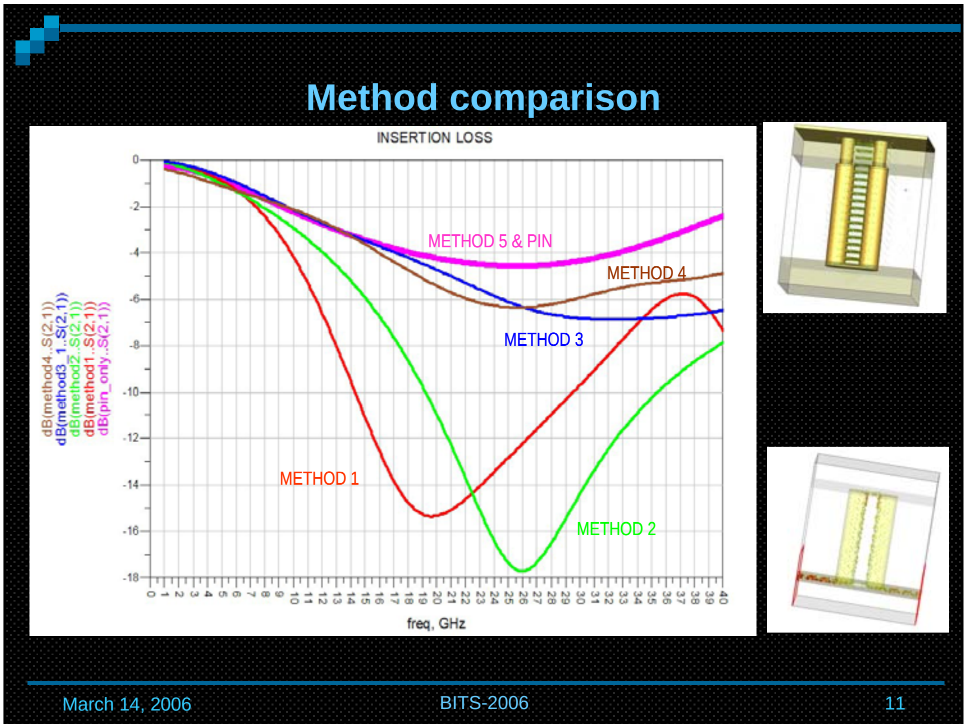
Method comparison
INSERTION LOSS
dB(method4..S(2,1))
dB(method3_1..S(2,1))
dB(method2..S(2,1))
dB(method1..S(2,1))
dB(pin_only..S(2,1))
freq, GHz
METHOD 5 & PIN
METHOD 4
METHOD 3
METHOD 1
METHOD 2
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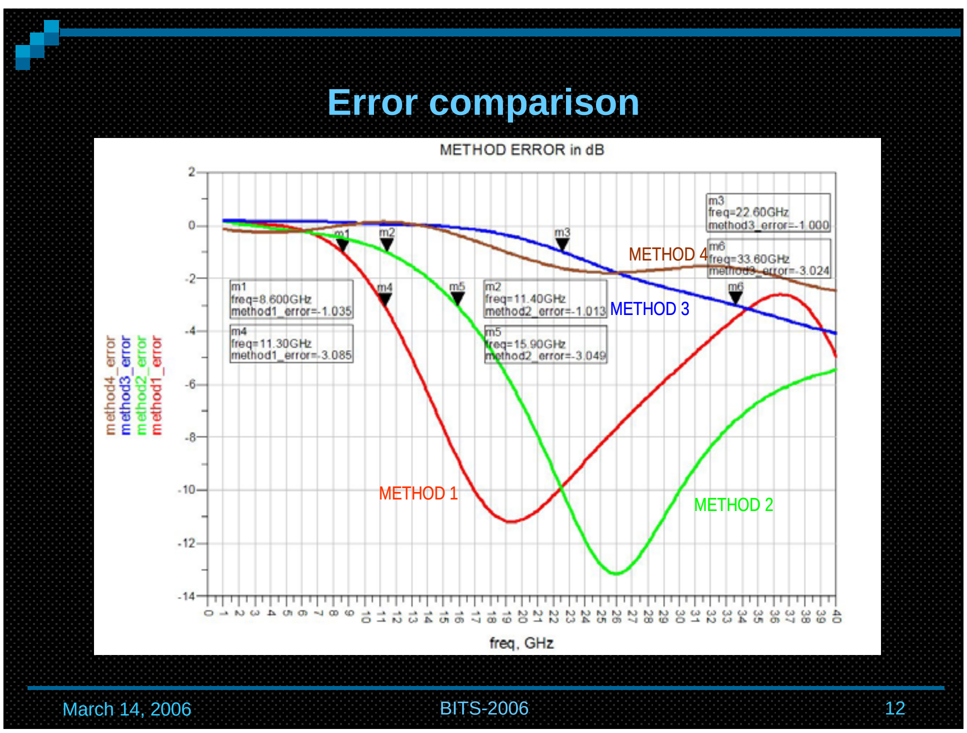
Error comparison
METHOD ERROR in dB
method4_error
method3_error
method2_error
method1_error
freq, GHz
m1
freq=8.600GHz
method1_error=-1.035
m4
freq=11.30GHz
method1_error=-3.085
m2
freq=11.40GHz
method2_error=-1.013
m5
freq=15.90GHz
method2_error=-3.049
m3
freq=22.60GHz
method3_error=-1.000
m6
freq=33.60GHz
method3_error=-3.024
METHOD 4
METHOD 3
METHOD 1
METHOD 2
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Pros and cons of double-sided probing

PROS

- Fully utilize VNA bandwidth so achieves the highest bandwidth possible.
- Error-free method.
- Fixture development is minimal so measurements can be taken relatively fast.

CONS

- Carries calibration and probing difficulties.

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Solutions to some problems

- Probe station is modified and bottom side microscope has been added. Reflected mirror image has been acquired by a monitor.
- Calibration is done first and one side probe reverse mounted. Vertical setup uses standard calibration.
- In general pin forces are less than microwave probe force. Desired deflection range can be achieved without damaging probes.

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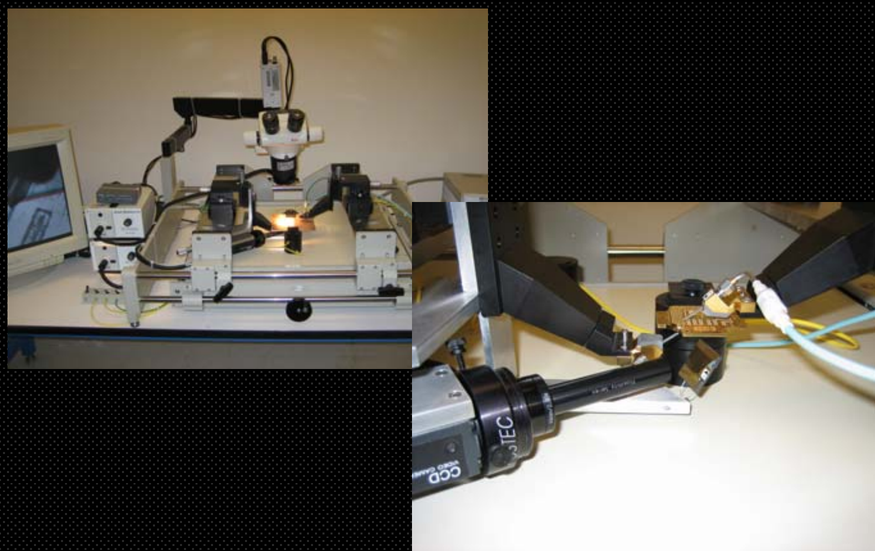
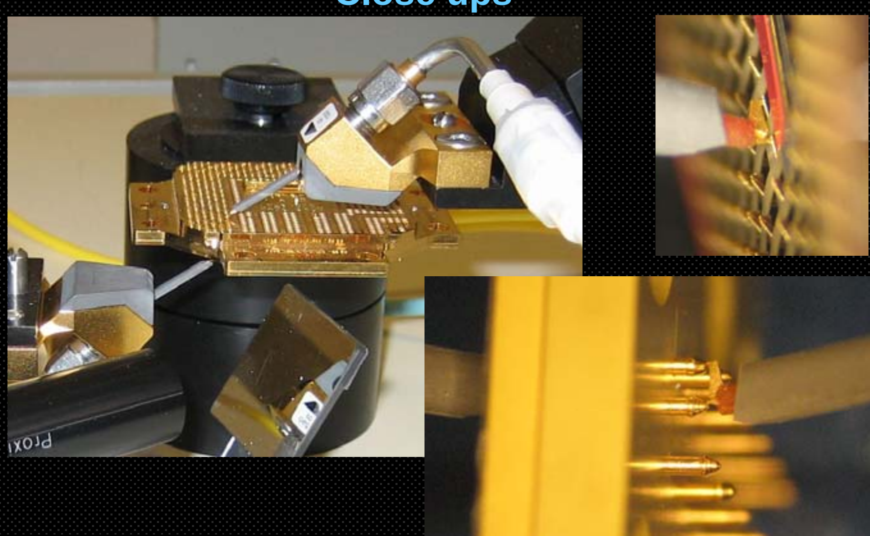
Probe station modifications

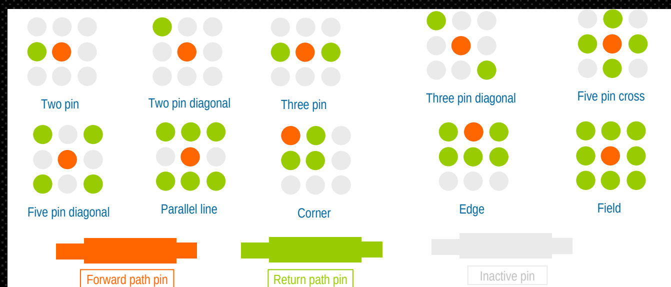


Close ups



Pin configurations

- Different pin configurations can be calculated mathematically from two-pin (GS) or three pin (GSG) measurement results.
- Different pin configurations have different characteristic impedance and RLGC values [3].
- Ten different pin configurations are calculated and more configurations can be added.



Calculations

- Propagation constant and characteristic impedance are calculated from measured S11 and S21.
- Transmission line model is used with variable component values (frequency domain) to extract spice models.
- Characteristic impedance recalculated for pin configurations.
- Extracted RLGC values are used to calculate pin configured RLGC values.
- From wave equation configuration S-parameters reconstructed.

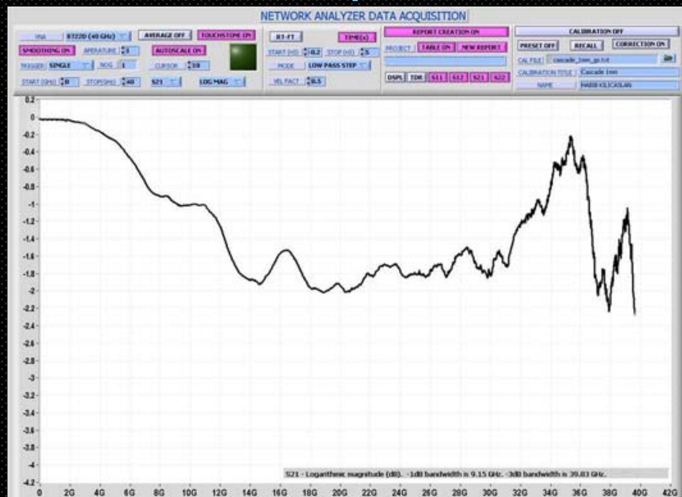
$$Z = Z_0 \sqrt{\frac{(1+S_{11})^2 - S_{21}^{\ 2}}{(1-S_{11})^2 - S_{21}^{\ 2}}}$$

$$\gamma = \sqrt{(R+jwL)(G+jwC)}$$

$$Z = \sqrt{\frac{(R+jwL)}{(G+jwC)}}$$

$$R = \mathrm{Re}\{\gamma Z\}$$
$$L = \mathrm{Im}\{\gamma Z\}/w$$
$$G = \mathrm{Re}\{\gamma / Z\}$$
$$C = \mathrm{Im}\{\gamma / Z\}/w$$

Data acquisition



Software is developed for fast acquisition from VNA and output is written to touchstone format for further calculations.

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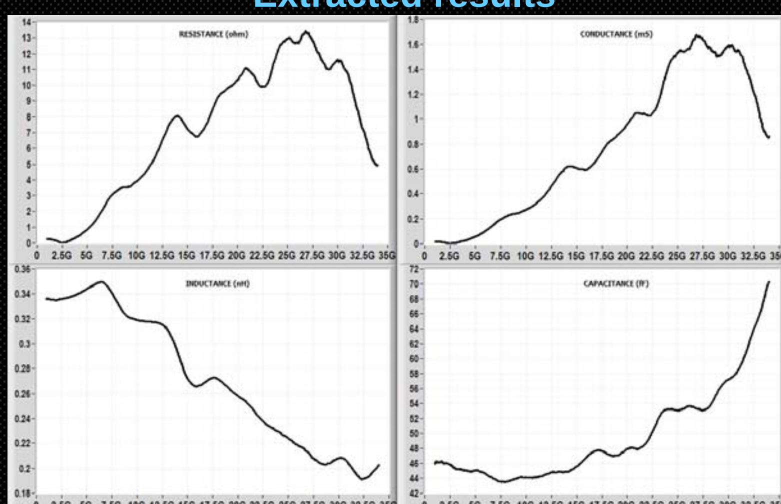
Extracted results



On resistance and inductance graphs, skin effects can be observed.

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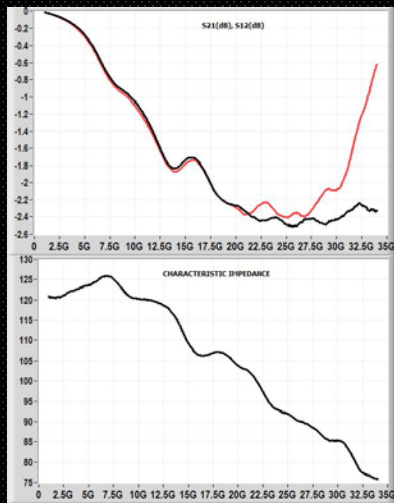
Result summary



SOCKET PARAMETER	VALUE	UNIT
Pin reference number	623-XXXX	-
Pin connection configuration	Two pin	-
Pin compressed height	1	mm
Socket pitch	1.09	mm
Socket dielectric coefficient	4.30	-
Socket magnetic permeability	1.00	H/m
Pin equivalent serial inductance (one pin)	0.34	nH
Pin equivalent parallel capacitance (one pin)	47	fF
Two pin line impedance	116	ohm
Rise time	0.01	pS
-1.0 dB bandwidth	9.15	GHz
-3.0 dB bandwidth	39.8	GHz
-10.0 dB return loss point	13	GHz

Calibration and cable errors can be observed from reciprocity deviation.

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Crosstalk measurements

- Crosstalk measurements are taken by double-sided probing in same way.
- Although 4 port VNA is more effective, a 2 port VNA can also be used with high bandwidth 50 ohm loads.
- Further end crosstalk (FEXT) is commonly measured due to the ease of calibration and probing.
- Configuration calculations are more cumbersome.

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Conclusions

- Double-sided probing methods introduce zero error.
- Pin configurations can be calculated mathematically from two-pin configuration without physically measuring.
- Spice model are extracted thorough transmission line model and fitted to measured S-parameters having frequency dependent component values.
- Measurements can be taken in relatively short time compared to other methods.
- Measurement related design cost is minimal.

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References

[1] Practical Techniques for measuring high bandwidth electrical models of test sockets

Eric Bogatin, Kevin Deford and Meena Nagappan, BITS 2005.

[2] A method for contactor characterization to 25 GHz.

Tim Swettlen, Orlando Bell, Gary Otonari, Eric Bogatin, BITS 2004.

[3] Characteristic impedance of unbalanced TDR probes

James A. R. Ball ; IEEE transactions on instrumentation and measurement.

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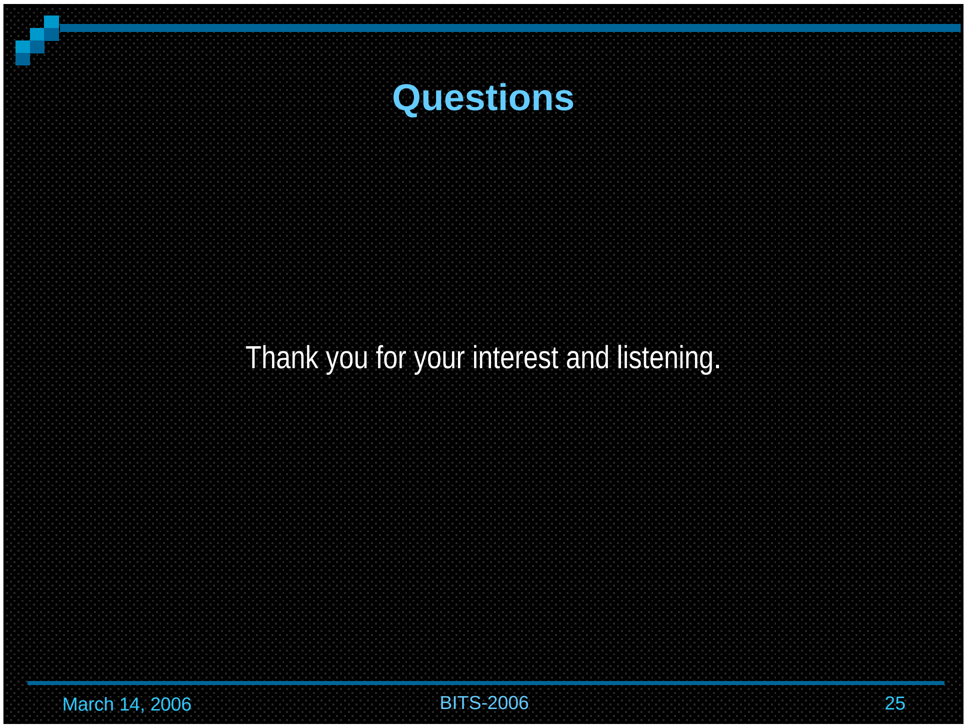
Questions
Thank you for your interest and listening.
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Effects of the Launch on Bandwidth

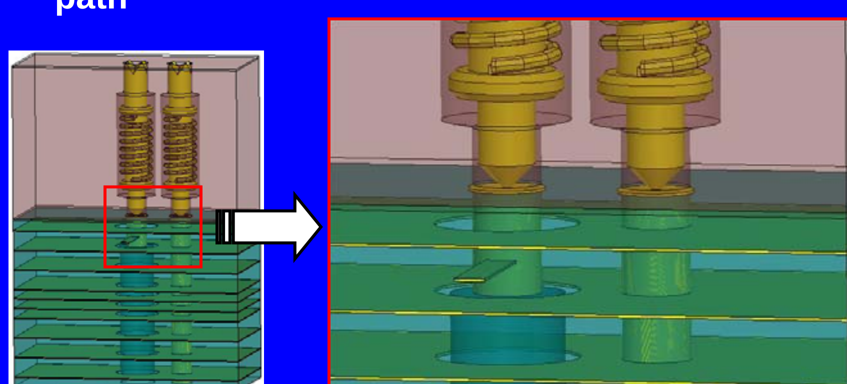
Ryan Satrom
ECT - Semiconductor Test Group, MN

Everett Charles Technologies
Testing the Limits

Burn-in & Test Socket Workshop

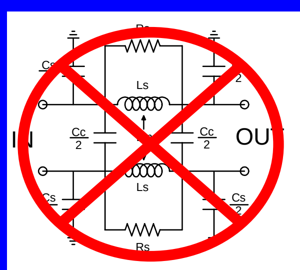
Description of "The Launch"

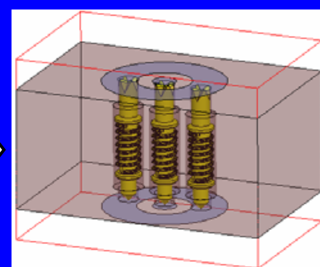
- The launch is the transition from the PCB to the contactor
- Creates unavoidable impedance mismatch due to significant change in reference to return path



High Speed Challenges

- Simulation results are only as accurate as the models used
- Accurate high frequency modeling requires additional resources
- Contactor models move from equivalent circuit to behavioral models (S-Parameters)





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Overview of Discussion Points - Important High Speed Concepts

#1. A lumped element model will not sufficiently account for the parasitics of a launch. Launch should be included in 3D EM Model

#2. Mismatch from launch will not be significantly affected by small changes in launch geometry

#3. One should NOT assume a test interface will perform at the contactor's specified bandwidth

#4. Ground via must be as close to signal as possible to minimize discontinuity

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Concept #1 - Modeling Launch as Lumped Element

- A lumped element will not sufficiently account for the parasitics of a launch
  - The launch and contactor are separated into two independent electrical components
- Launch-Contactor must be viewed as one system. Interactions between them significantly affect system performance
  - 3D EM model required
- Often “full system” models neglect the launch-contactor transition. This inaccuracy will be reflected in the simulation results.

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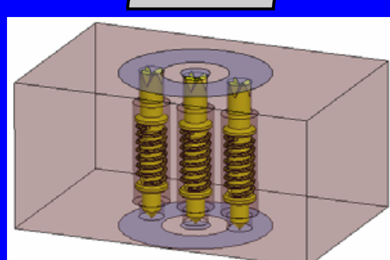
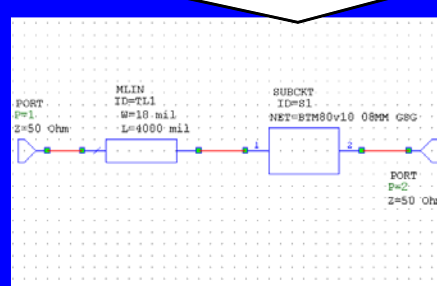
Concept #1 - Trace-Contactor Example

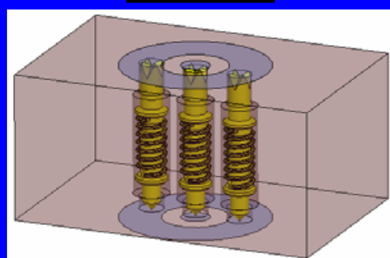
- Case 1: Trace plus HFSS
  - 4” microstrip trace
  - Launch is neglected
  - Imported HFSS S-Parameter model of contactor only

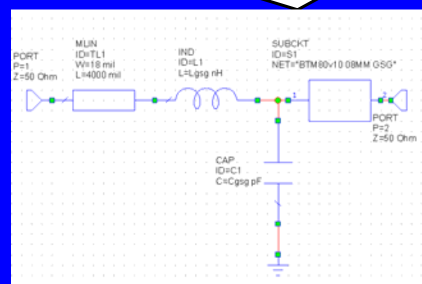




Concept #1 - Lumped Element Launch

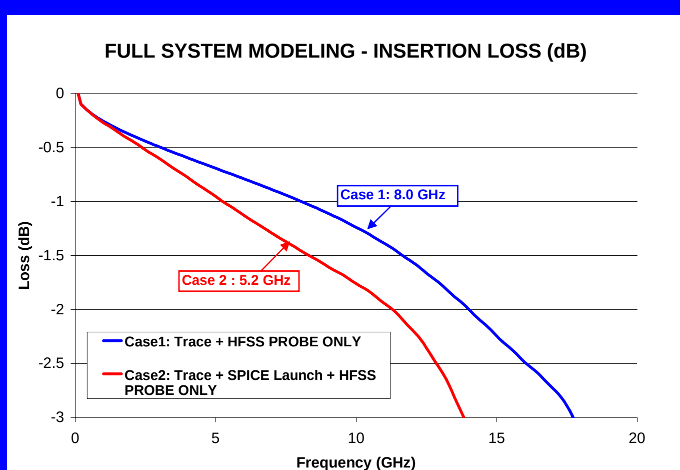
- Case 2: Add launch as SPICE model
  - 4” microstrip trace
  - Launch as a lumped element
  - Imported HFSS S-Parameter model of contactor only





Concept #1 - Simulation Results

- Including simple SPICE Launch will impact simulation results



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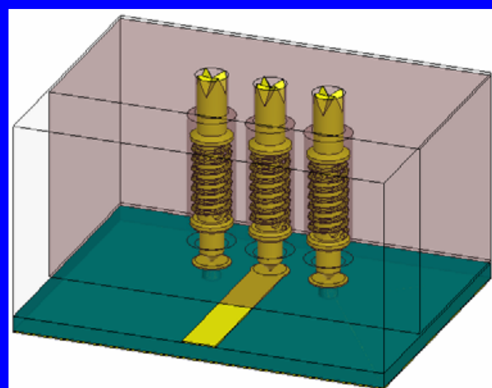
Concept #1 - Full wave Model

- Case 2: HFSS 3D EM Model
  - Includes transition from Board to Contactor
  - Full wave simulation accounts for interaction between launch and contactor



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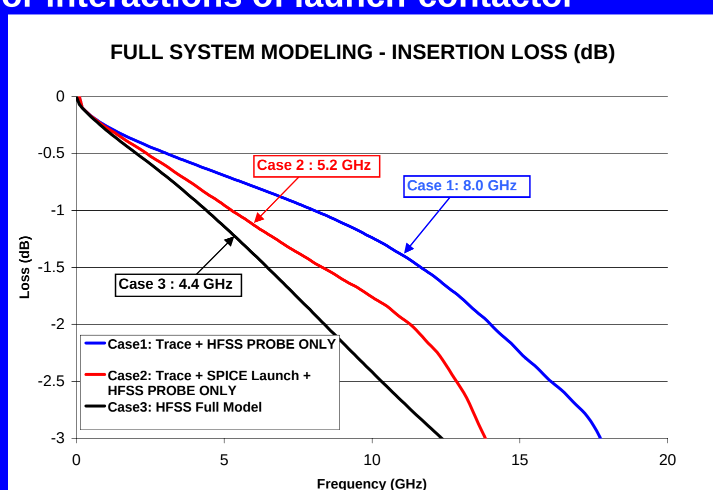
Concept #1 - Simulation Results

- Full wave model must be used to fully account for interactions of launch-contactor



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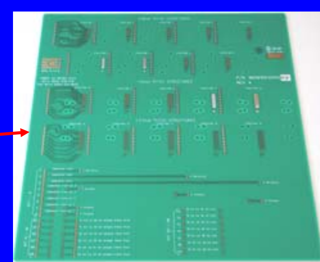
Paper #3

Concept #2 - Launch Mismatch

- The impedance discontinuity at the launch is due to the change in ground reference from a plane to a via/pogo pin
- Changing the antipad diameter, via diameter, or pad diameter will only result in a negligible change in performance
- The impedance discontinuity is dominated by ground configuration.

ECT Launch Test Board



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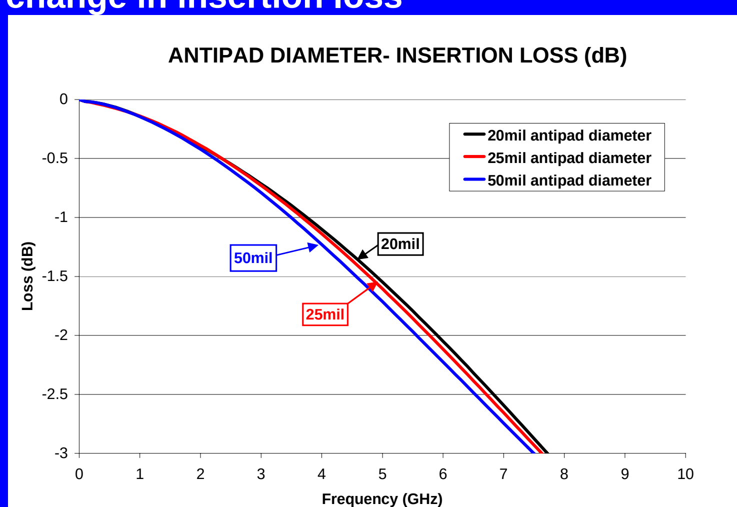
Concept #2 - Antipad Example

- Changing the antipad diameter shows no change in insertion loss



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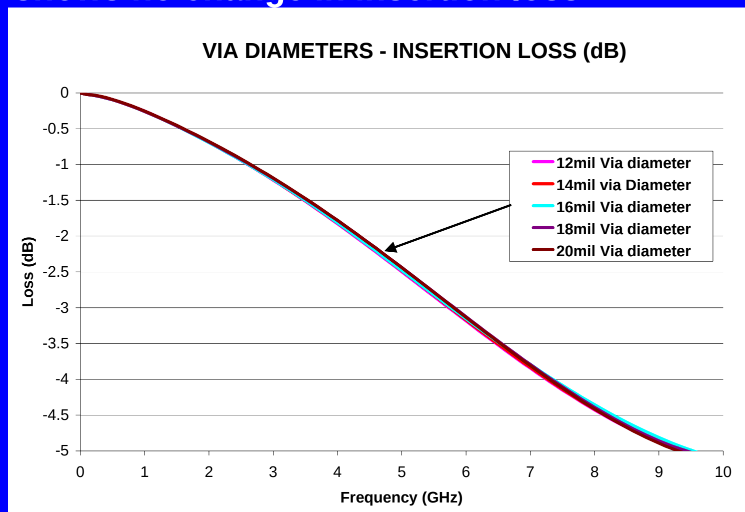
Concept #2 - Via diameter example

- Changing the via diameter from 12mil to 20mil shows no change in insertion loss



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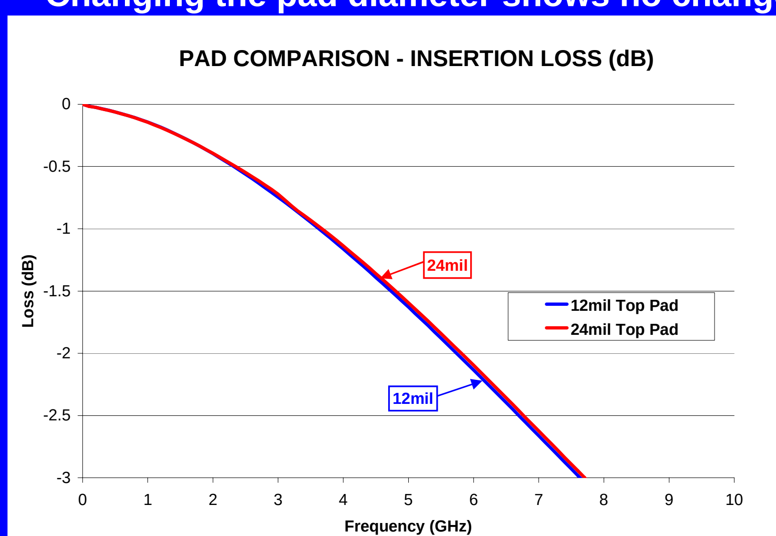
Concept #2 - Pad diameter Example

- Changing the pad diameter shows no change



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Concept #3 - Contactors specified bandwidth

- One should NOT assume a test interface will perform at the specified bandwidth of the contactor
  - Bandwidth includes only the short transmission path through the contactor
  - Typical configuration is GROUND-SIGNAL-GROUND, which may or may not be the configuration of the actual device.
  - Does not take into account any discontinuity due to the transition from board to contactor
  - Does not consider PCB line length and other connectors

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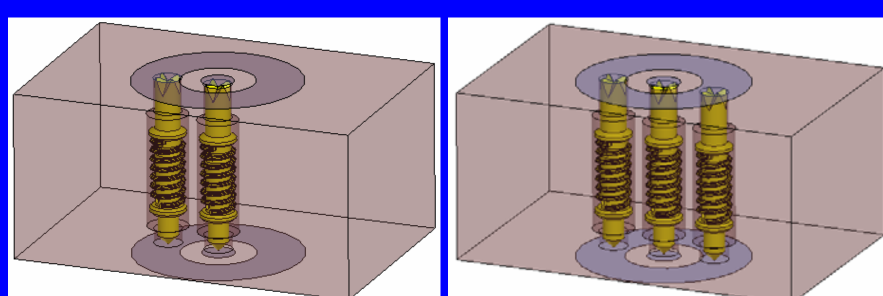
Concept #3 - Bandwidth example

- Case 1: Standard test configuration
  - Probes Only in GROUND-SIGNAL configuration
  - Probes Only in GROUND-SIGNAL-GROUND configuration



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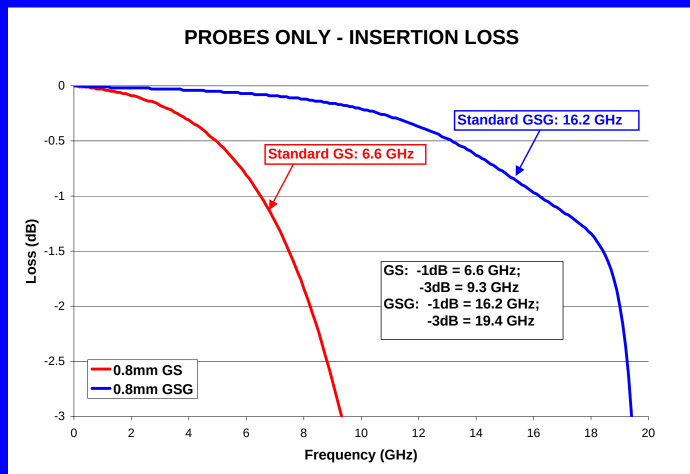
Concept #3 - Bandwidth Results

- GND-SIG configuration shows 60% decrease in bandwidth from GND-SIG-GND configuration



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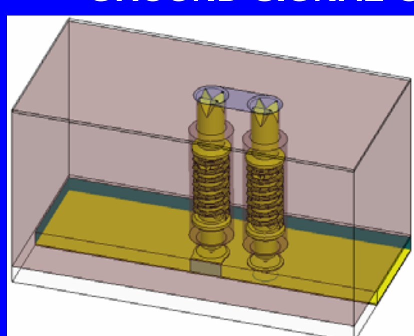
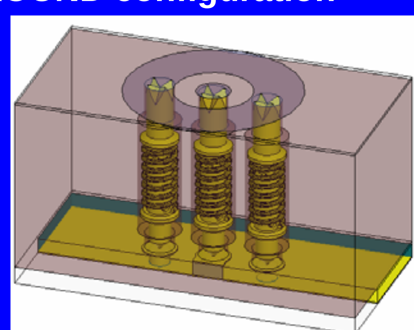
Concept #3 - Bandwidth continued...

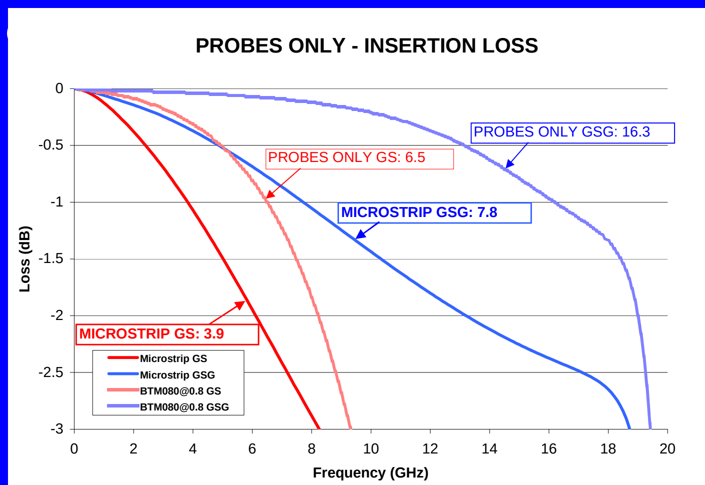
- Case 2: Microstrip launch through probes
  - Short length microstrip through probes in GROUND-SIGNAL configuration
  - Short length microstrip through probes in GROUND-SIGNAL-GROUND configuration





Concept #3 - Bandwidth Results

- Both configurations show over 50% decrease in bandwidth from standard test



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Concept #4 - Location of ground via

- The mismatch at the launch will be minimized by placing a ground via as close to the adjacent signal as possible.
- Poor ground via placement may cause very significant discontinuity.
- Goal is to minimize inductance of path.
- Including additional ground vias will further minimize impedance mismatch.

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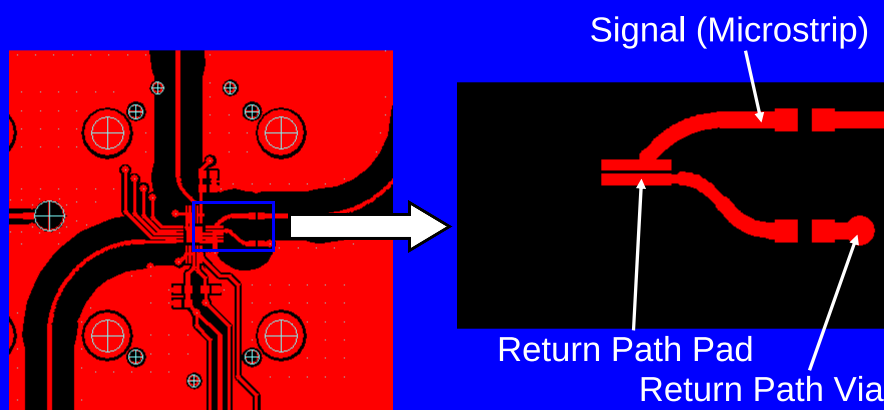
Concept #4 - Ground via Example

- Actual Board failure
- Requires > 5GHz bandwidth



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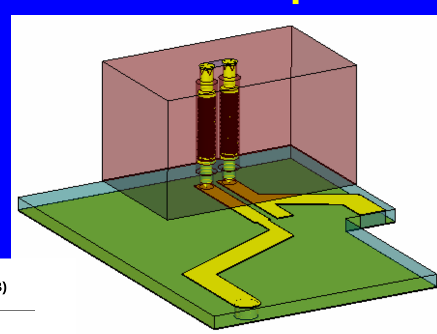
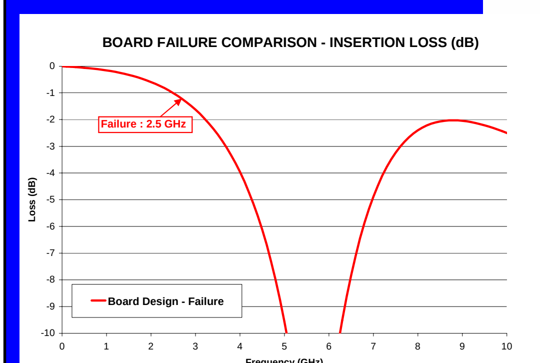
Concept #4 - Ground via Example

- HFSS Simulation





- Bypass capacitors neglected for this model

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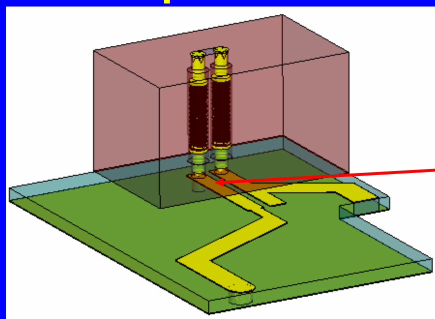
Concept #4 - Board Redesign - Two cases

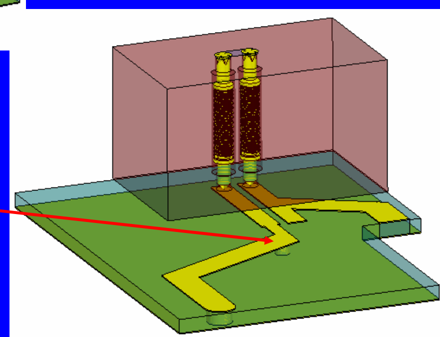


- Redesign 1:

Ideal ground via placement

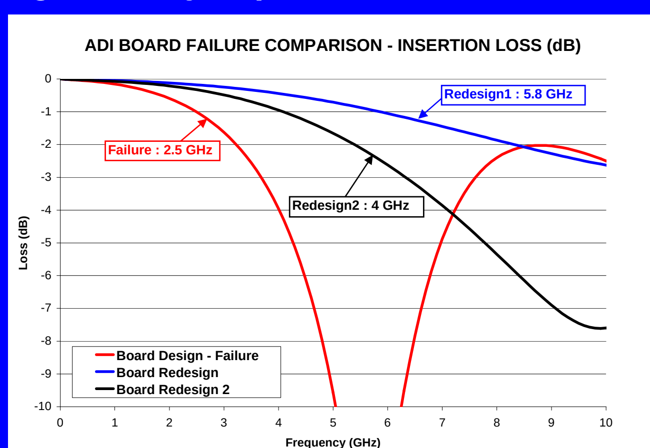
- Redesign 2:

Improved and mechanically feasible ground via placement



Concept #4 - Ground via Example

- 1dB bandwidth increases from 2.5GHz to 5.8GHz
- Significantly improves bandwidth



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Future Direction

- Extensive simulation to measurement validation and correlation
- Move focus from frequency domain to time domain
  - 2D EDA software to analyze time-domain
- Include non-ideal models for Tester and Device
  - Currently perfect 50-ohm I/O is assumed
  - Non-ideal I/O will cause additional noise/reflections
- Multiple net analysis
  - Simulations to include crosstalk, noise, etc.

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Conclusion

- A lumped element model will not sufficiently account for the parasitics of a launch. Launch should be included in 3D EM Model
- Mismatch from launch will not be significantly affected by small changes in launch geometry
- One should NOT assume a test interface will perform at the contactor's specified bandwidth
- Ground via must be as close to signal as possible to minimize discontinuity

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