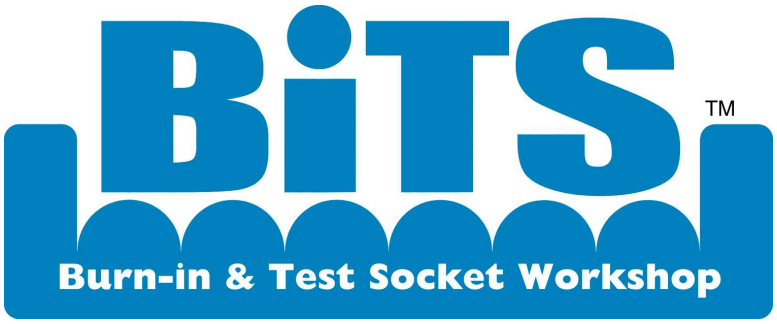

ARCHIVE 2006

Session 4

Managing Advanced Packaging Demands

"The Challenges Of Handling & Socketing Packaged Image Sensors"
Steve Hamren — Micron Technology

"Ultra Fine Pitch Socket Development Challenges"
Wei-ming Chi, Ken Kassa, Chak Fung Kon — Intel Corporation

"PCB's In The Test Environment"
Hardeep Heer — Everett Charles Technologies STG

"Are Sockets Required For Test And Burn-in?"
Belgacem Haba, Ph.D. — Tessera, Inc.

"The Challenges of Handling & Socketing Packaged Image Sensors"

Steve Hamren - Micron Technology
BiTS 2006 Technical Sessions Chair

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Agenda

- Applications & Brief History
- Basic Theory of Operation
- Mechanics of Handling Imager Sensors
- Hurdles & Challenges
- Conclusion

Applications for Image Sensors

- Cell Phone Cameras

- Digital Photography
  - Still Cameras
  - Camcorders
  - PC Cameras

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Applications for Image Sensors

- Automotive
  - Smart airbag deployment
  - Lane tracking
  - Side & Rearview mirror replacement
  - Collision avoidance/departure warning
  - Self parking cars
- Medical
  - Endoscopy
  - PillCam™

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Applications for Image Sensors

- **Security**
  - Surveillance cameras
  - Biometrics/ Finger print readers
  - Face recognition
  - Bomb Robots
- **Toys & Recreation**
  - Golf Swing Analysis
  - Web Cameras
  - Toy Robots

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History

CCD invented “by mistake” in 1969 at Bell Labs by George Smith and Willard Boyle. Since mass-produced memory did not exist, they were looking for other ways to store data on computers.

CMOS APS (active pixel sensor) invented in early 1990s at Nasa Jet Propulsion Laboratory.

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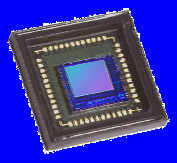
Theory of Operation



- **There are 2 types of Image sensors.**
  - **CCD** (Charge-coupled devices)
    Uses specialized, old VLSI process.
  - **CMOS** (Complementary Metal Oxide Semiconductor)
    Uses common technology used in today's processors and memory.
- **Both types capture light on the photosites during exposure. The basic difference between CCD & CMOS is the way the charge on the photosite is read & processed.**

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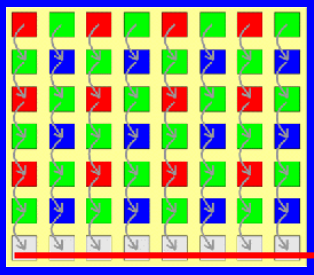
Theory of Operation

CCD



With CCD, the charges on the first row are transferred to a register. From there, the signals are fed to an off-chip amplifier and then on to an A/D converter. Once the row has been read, its charges on the register row are deleted. The next row enters the register, and all of the rows above move down one row. The charges on each row are "coupled" to those on the row above so when one moves down, the next moves down to fill its old space.

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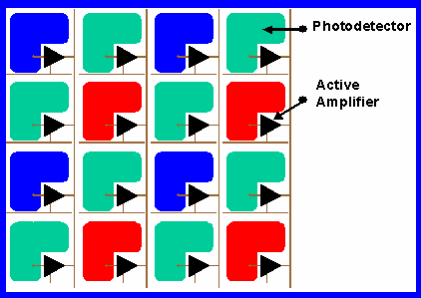
Theory of Operation

CMOS



With CMOS, each photosite has a built-in amplifier and can be read individually & randomly. The analog-to-digital converter is on chip so the output can be used without additional processing. Since CMOS technology is used, additional circuitry like Auto-focus, anti-jitter, etc…can be incorporated on the die. This results in lower cost, smaller cameras and less power consumption.

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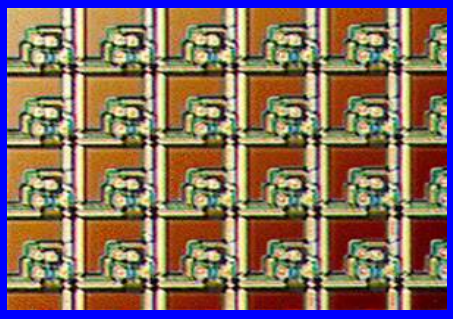
Theory of Operation



Since CMOS sensors have additional circuitry at each photosite, the area of that photosite devoted to collecting light is less than a CCD sensor. The percent of the photosite that can collect light is called the pixel's **fill factor**. CCDs have a 100% fill factor but CMOS cameras will have less.

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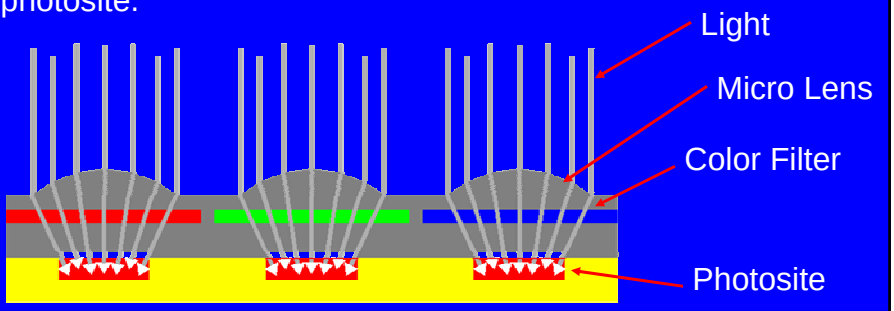
Theory of Operation

The lower the fill factor, the less sensitive the sensor is. Too low a fill factor makes indoor photography without a flash virtually impossible. To compensate for lower fill-factors, micro-lenses can be added to each site to gather light from the insensitive portions and spread it down to the photosite.



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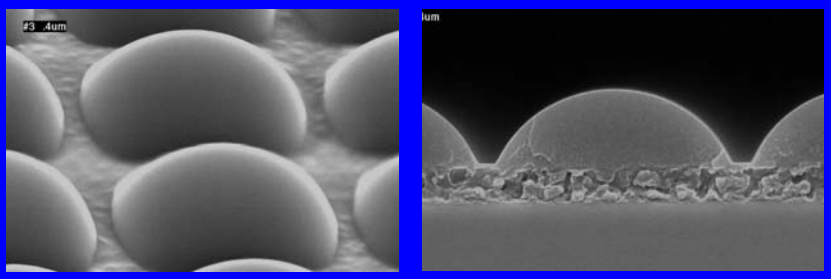
Theory of Operation



Sem images of CMOS Micro Lens

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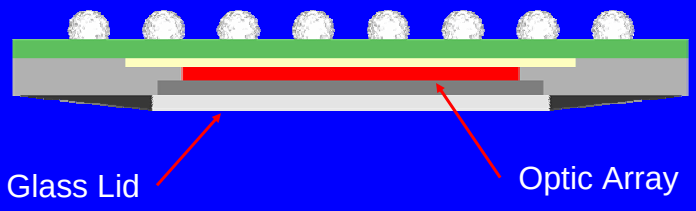
Mechanics of Handling Image Sensors

- **Dead bug handling**
  - Since the optic array needs to face outside the handler toward the illuminator, parts must be run "dead bug."



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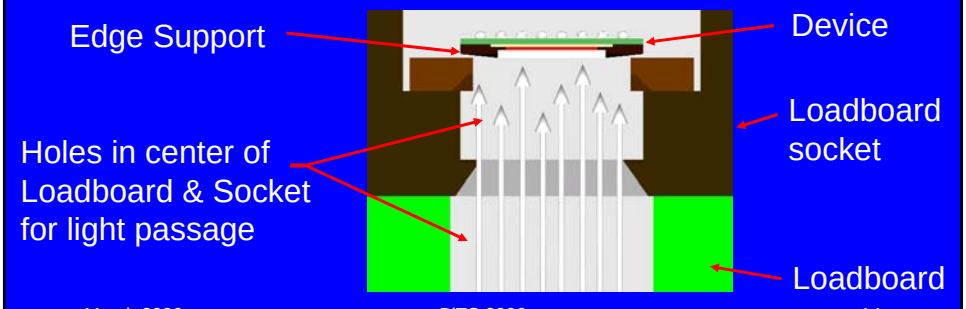
Mechanics of Handling Image Sensors

- **Access to optic array from external Illuminator**
  - Must be able to get light to the sensor during test.
  - Access holes in Loadboard & Sockets.
  - Device must be supported on edge.



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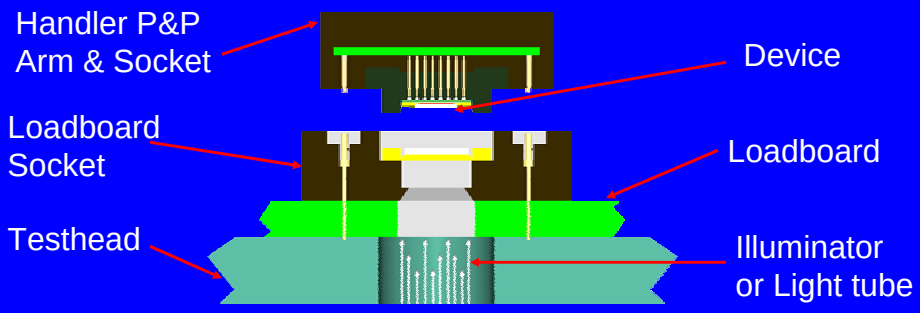
Mechanics of Handling Image Sensors

- **Dual Socket System**
  - Dead bug process requires a socket on the loadboard as well as a socket on the handler Pick & Place arm.



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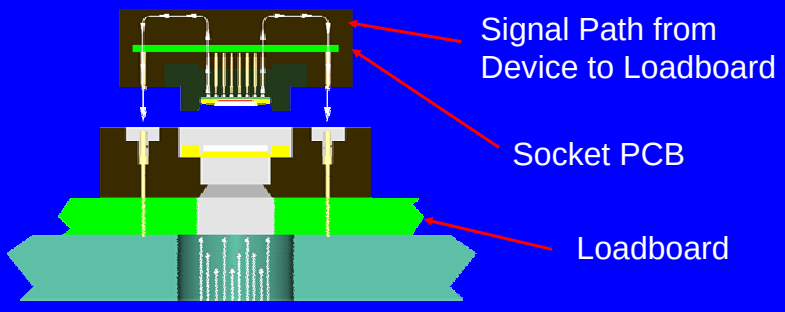
Mechanics of Handling Image Sensors

- **Signal Path from device to testhead**
  - Dead bug handling results in signals taking a “U” turn to & from the tester though a PCB in the socket.



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Mechanics of Handling Image Sensors

- **Cleanliness**
  - Devices, trays, sockets, inside of handler, etc… must be kept very clean to keep debris off the array. Particles on glass will cause false failures.

Photosites “pixels” are between 2um and 6um in size.

Human hair is ~25um to 100um.

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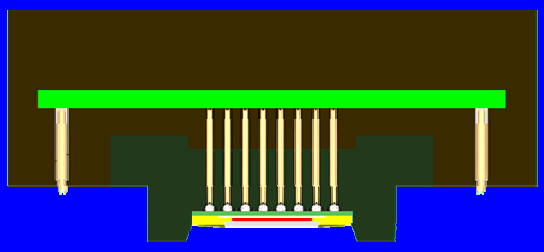
Hurdles & Challenges

- **Dead bug handling**
  - The handler Index Arm Socket must have Pick & Place capability as well as be able to align & contact the balls/leads of the Image Sensor Device



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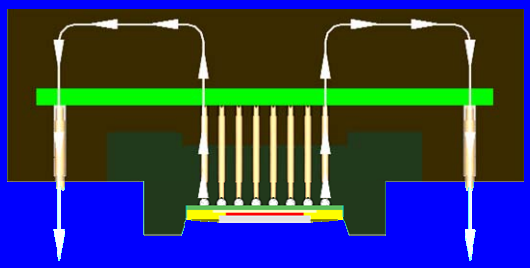
Hurdles & Challenges

- **Signal Routing**
  - The signal routing in the socket to get from the device to the Testhead adds complexity & cost but has not been a performance issue **yet.** Speeds are slow (<60mhz) except for devices with serial outputs. Serial outputs use LVDS signaling so are more forgiving.



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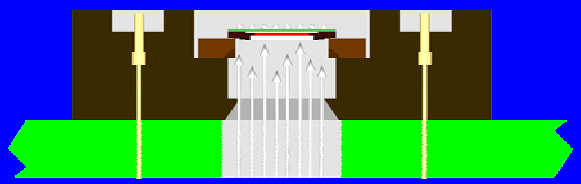
Hurdles & Challenges

- **Need two sockets per site**
  - Along with the Index-Arm Socket, there needs to be a socket on the loadboard. This loadboard socket supports the device during test, sets the focal point, holds the light diffuser if needed and provides a signal path from the Index-Arm Socket to the Loadboard.



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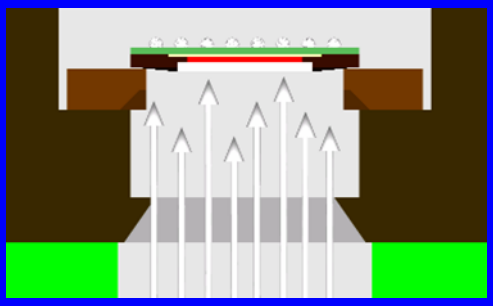
Hurdles & Challenges

- **Light source needs access to optic array**
  - Since the optic array needs to be open to the illuminator during test, the majority of the bottom of the device cannot be touched.



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Hurdles & Challenges

- **Can't support device on glass lid, can't chip or scratch glass lid**
  - Need enough support to be able to socket device without damage but also have enough clearance to get uniform light to avoid shadowing & vignetting.

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Hurdles & Challenges

- **Particles**
  - Everything the device comes in contact with or near must be clean. Trays, handlers, sockets, light sources, lens, etc… Dust & debris will cause parts to fail.

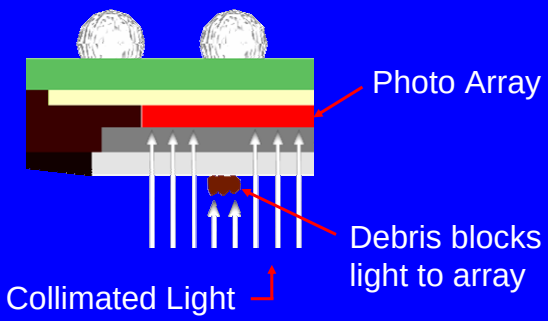

Image w/debris on glass

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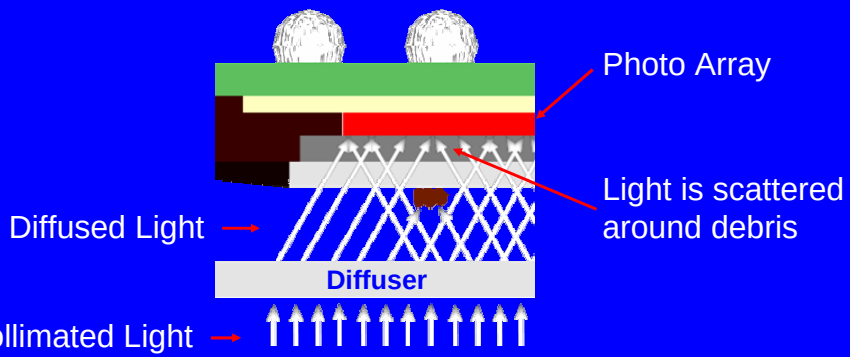
Hurdles & Challenges

- **Light diffusion**
  - Diffusers are sometimes used to avoid false failures caused by debris on the exterior of the glass lid.



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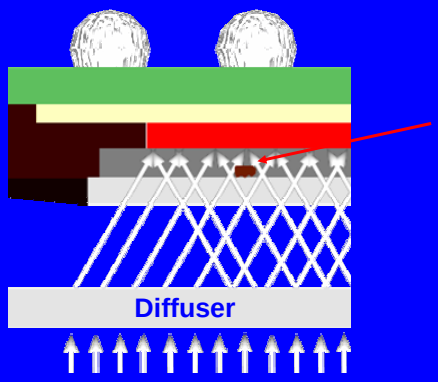
Hurdles & Challenges

- **Light diffusion**
  - However, diffusers can also result in hiding true defects like debris on the interior of the glass lid.



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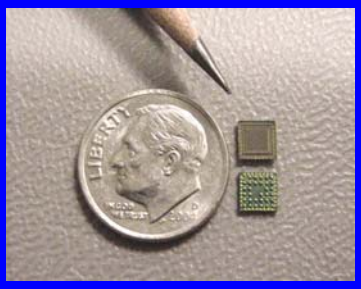
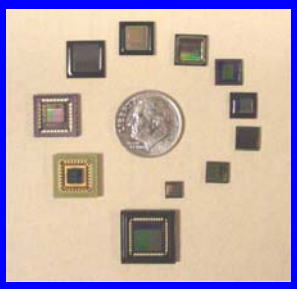
Hurdles & Challenges

- **Small packages & variety of package sizes**
  - Currently running packages <4.5mm Square.
  - New medical applications to be ~3.7mm Square
  - Many variations from 14mm and less.





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Hurdles & Challenges

- **Temperature**
  - Automotive Specification is -40°C to +85°C
  - Difficult to run hot with conductive heating since there is not much of the device you can touch to transfer heat.
  - Difficult to run hot with convection heating with the illuminator access hole in socket & loadboard.
  - Difficult to run cold without frosting up with the illuminator access hole in socket & loadboard.

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Conclusion

- Improvements in and demand for CMOS in the last few years have resulted in an estimated annual growth rate of 30%-60%. CMOS Imagers projected to be ~4 Billion in sales in 2006.
- Although CMOS Imagers are “easy” to test without the normal problems like High Power, High Pin Count, High Frequency and High Parallelism, they do have a whole new set of challenges to overcome.
- Like any expanding product, ongoing improvements to processes & hardware will be made.

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Ultra Fine Pitch Socket Development Challenges

Wei-ming Chi Intel Corp
Ken Kassa Intel Corp
Chak Fung Kong Intel Corp

March 14 2006

2006 Burn-in and Test Socket Workshop

Agenda

- Problem Statement
- Mechanical Requirement Roadmap
- Technical Challenges
- Stack Up Parameters and Methods
- Material Stability
- Potential Alignment Solutions
- Conclusions

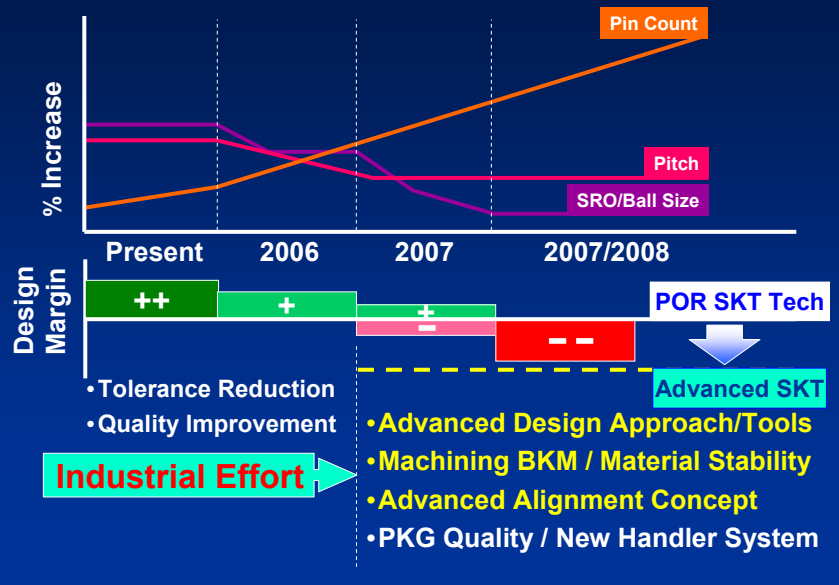
2

Problem Statement

- Future industry products show significant reductions in pad sizes for package and motherboard (MB), Solder Resist Opening (SRO), solder ball size, and pitch
- Mechanical alignment between socket contactor and SRO/Pad/Solder Ball is critical to testability
- Current alignment capabilities and assessment methodology are inadequate to fulfill future socket needs

3

Mechanical Requirement Roadmap



4

Technical Challenges

improve mechanical alignment accuracy

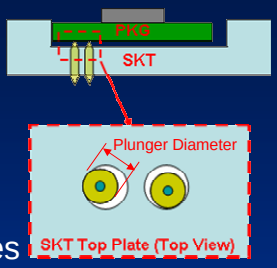
- **Determination on Machining Precision required for mechanical alignment**
  - Predictive Statistical Tools vs. Trial and Error
- **Machining Accuracy (Tolerance Control)**
  - CNC Machining Tolerance Control (Drilling BKM)
  - Material Issue
- **Pin Tip Size Reduction vs. Pin Tip Durability**
- **Advanced Alignment Feature**

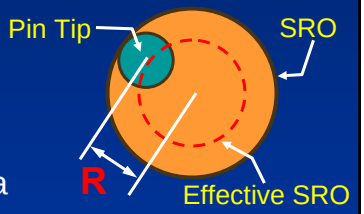
5

Factors Affecting Pin-Pad Alignment

→ Socket Alignment ≠ Pitch only

- Package Movement inside Socket
  - Package dimensions and tolerances
  - Socket inner dimensions and tolerances
- Pin Movement inside Socket Pin Holes
  - Pin (plunger) diameters and tolerances
  - Socket pin hole diameters and tolerances
  - Pin hole true positions
- SRO (Pad) Variations
  - SRO diameters and actual positions
- Pin Tip Size Variation
  - Pin tip size vs. Effective contact area





$$Cpk = \frac{R}{3\sigma} \quad \text{where} \quad \sigma = f(\text{nonimal size, clearnace, tolerance, true position})$$

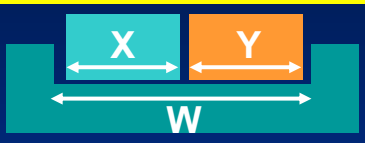
6

Alignment Accuracy Assessment

Root of Sum Square vs. Monte Carlo Based Cpk

Stack-Up Example

$R = W - X - Y \quad vs. \quad R \geq 0$



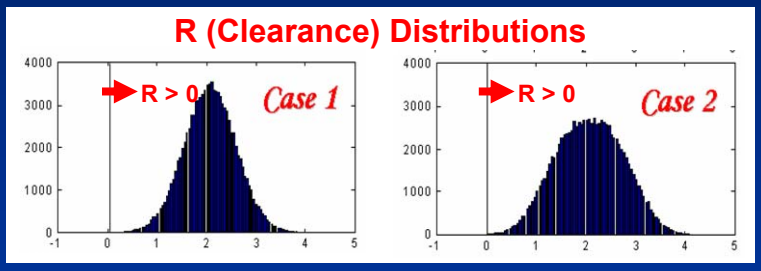
B.C. Input

X = 10.00 ± 0.9
Y = 5.00 ± 0.9

W = 17.07 ± 0.9

Back cal. per RSS yields to Cpk of 1.33

R (Clearance) Distributions



Clearance Distribution highly depends on input assumptions

7

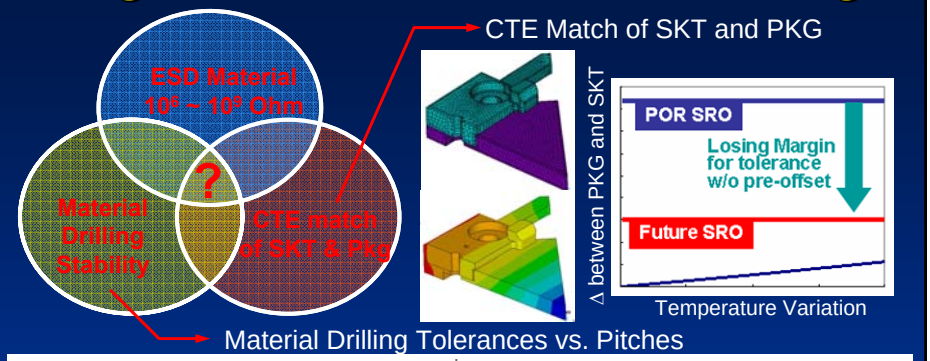
Comparison of RSS and MC

	Case 1	Case 2
W	Normal	Normal
X	Normal	Normal
Y	Normal	Random
CPK	1.33	1.03
DPM	30	290

- RSS only valid for estimating variances involving linear relations with independent normal distributions
- Violating any RSS assumption leads to over- or under-designs
- Limited design margin does require a tool better than RSS

8

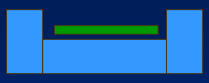
Drilling vs. Material Selection Challenges



9

Passive vs. Active Alignments

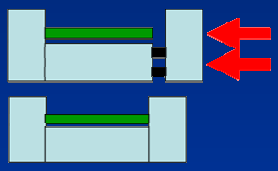
Passive Alignment **relies on clearance/tolerance control**



Assemble-ability (jam) vs. Alignment

(minimal socket cost added, but reach effectiveness limits)

Active Alignment **is to directly eliminate alignment error contributor(s)**



(moderate effectiveness, but more socket engineering work / machining)

Example:
Mechanically position package to eliminate the clearance of package and socket

Other Options: **advanced handler system ?**
guiding feature on package ?

10

Conclusions

- Ultra fine pitch with smaller SRO/Pads leads to greater challenges of mechanical alignment to industry
- Predictive statistical tools other than commonly used RSS is needed.
- Material selection is getting more challenging due to pitch/SRO reduction
- Advanced alignment features will be needed in the future (passive vs. active vs. others)

11

Acknowledgements

- Marc Berube INTEL Corp
- Jun Ding INTEL Corp
- David Shia INTEL Corp
- Tom Worley INTEL Corp
- Suppliers

12

PCB's in the Test Environment

ECT
BiTS Presentation

Hardeep Heer

EVERETT CHARLES TECHNOLOGIES
Testing the limits

Abstract

- PCB has always been Integral part of test interface equation.
- Electrical performances have pushed pitches below 0.5mm, forcing PCB manufacturer to develop new process strategies.
- This presentation will address
  - Material and Mechanical constrains
  - Via formation challenges including registration, leakage, reliability and signal integrity
  - We will discuss critical process capabilities and design rules that needs to be developed.

2

Test Industry Trends…

Device Package pitches are shrinking

(mm)	2005	2006	2007	2008	2009	2010	2011	2012	2013
CSP	0.3	0.2	0.2	0.2	0.2	0.2	0.15	0.15	0.15
QFP	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
QFN	0.4	0.4	0.4	0.3	0.3	0.3	0.3	0.3	0.3
FBGA	0.4	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3

Source: ITRS 2005

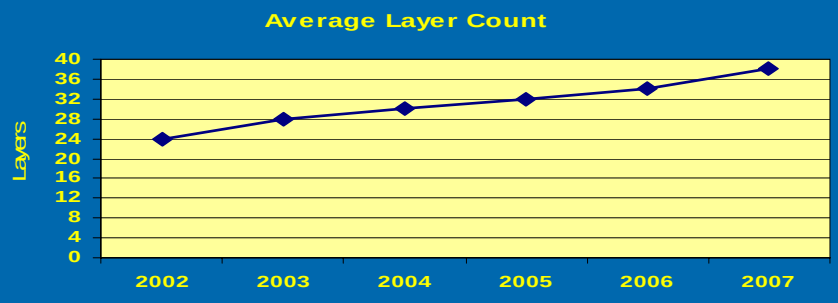
Device Package Pin Counts are growing, plus the steady drive to increase PARALLELISM (multi site test)

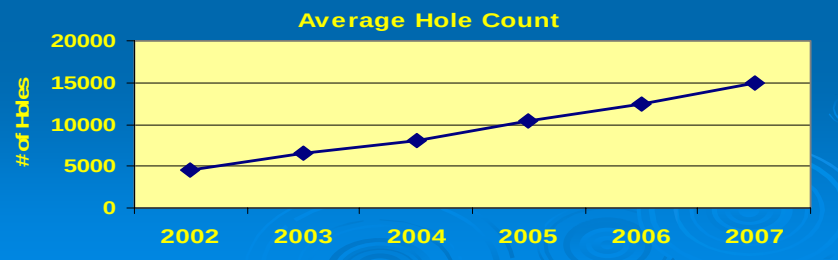
c/p	2005	2006	2007	2008	2009	2010	2011	2012	2013
PINS	<900	<990	<1088	<1198	<1318	<1450	<1596	<1754	<1930

Source: ITRS 2005

3

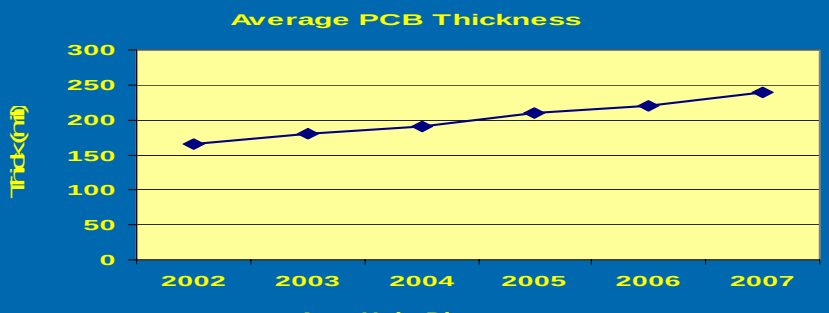
Test Industry Trends

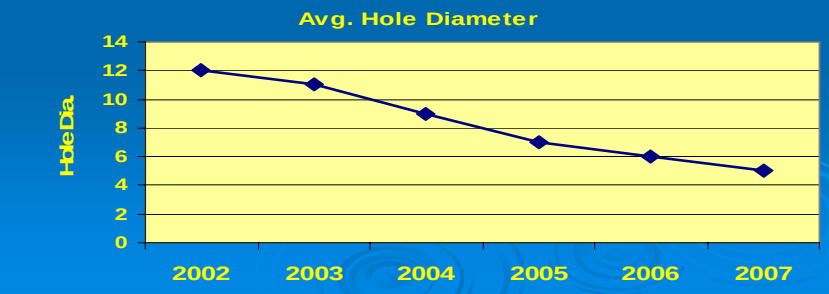




4

Test Industry Trends





5

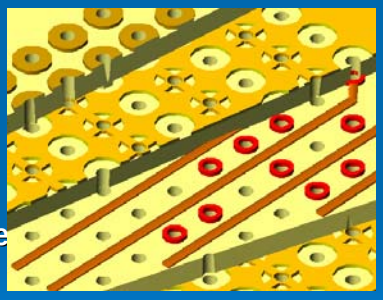
PCB Technology Comparison
Leading edge technologies

	PCB Std.	ATE PCB's
Overall Thickness	0.090"	0.200"
Min. Drill Size	0.010"	0.006"
Aspect Ratio	Up to 14:1	Up to 31:1
Impedance Tol.	10%	5%
Impedance Measured	Coupons	Up to 100% on Board of all net
Flatness	0.7%	Min 0.3%

6

PCB Design Characteristics for 0.5mm and 0.4mm pitch designs

- 0.5mm pitch
- .010” pad
- .006” drilled hole
- .0157”clearance
- .0035” line/space



- 0.4mm pitch
- .008” pad
- .004” drilled hole
- .0107” clearance
- .0025” line/space

7

Major Areas of ECT R&D Focus

- Process Tolerances
- Material Movement
- Exotic Materials
- Via Formation

8

Process tolerances

- Cumulative process tolerance between imaging and drilling.
  - Front to back registration - 0.002”
  - Punch accuracy - 0.001”
  - Cumulative Drill process - 0.005”*
  - Material movement - 0.003”**
  - Wicking - 0.002
  - Total 0.013”
  - * Includes drill wander / deflection for micro-drills
  - ** Varies with material / design, if not compensated

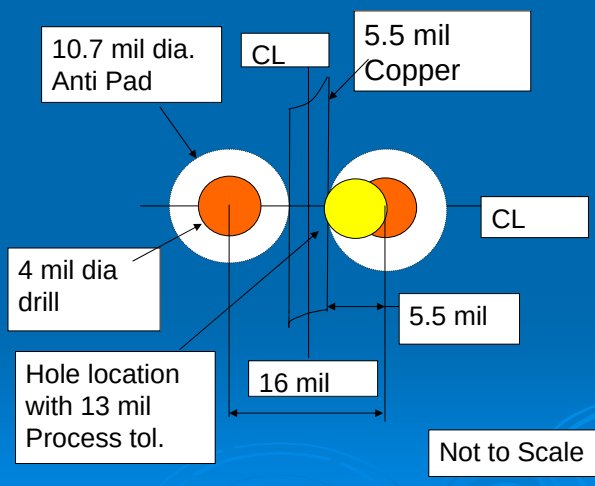
9

Anti pad Calculations

- Anti Pad for 5 mm pitch - based on process capabilities;
  - Anti Pad = Drill Size + cumulative tolerances
    = 0.006” + 0.013”
    =0 .019”
  - **Per design rules for minimum = 0.0157” inner layer pwr / gnd trace width**
- Anti Pad for 4mm pitch – based upon process capabilities;
  - Anti Pad = Drill Size + cumulative tolerances
    = 0.004” + 0.013”
    =0.017”
  - **Per design rules for minimum = 0.0107” inner layer pwr/gnd trace width**

10

4 mm Pitch



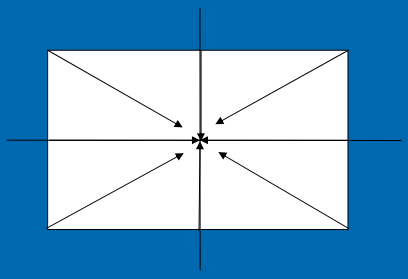
11

Key process strategies to combat Tolerance budget

- Laser Direct imaging to minimize front to back mis-registration.
- Post Etch punching to eliminate variability from processes prior to lamination.
- X-ray Optimizer to create fresh tooling holes to optimize each panel.
- Flip drilling to reduce drill deflection.
- Optimized drill parameters to reduce wicking.

12

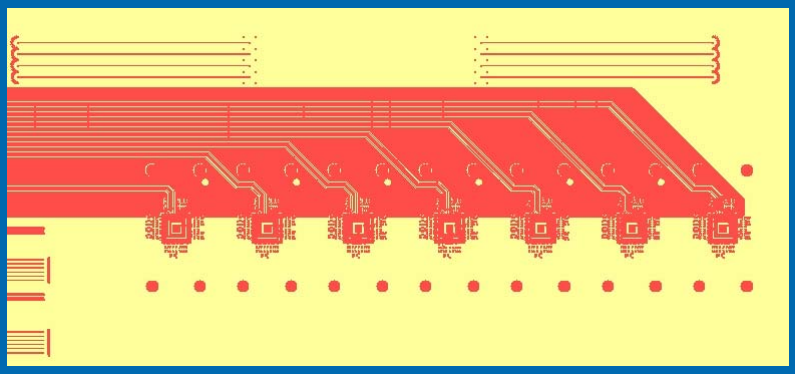
Material Movement



- Material moves towards centre in relationship to its warp and fill directions. – Best registration is always at the centre of the panel.
- As DUT's are added, DUT locations move away from the centre of the panel.

13

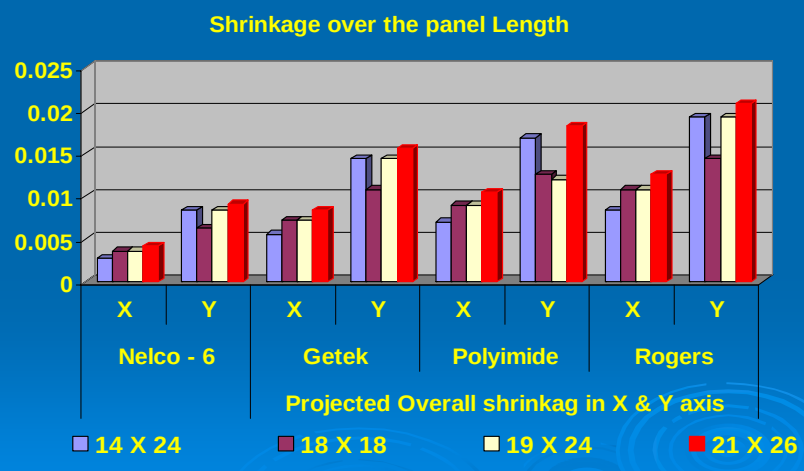
Multi DUT design on larger panel sizes



- Location is no longer in the centre of Panel
- For Rogers 4350 material, a DUT placed at 10" from the centre could see a material movement of 0.008" if not compensated accurately.

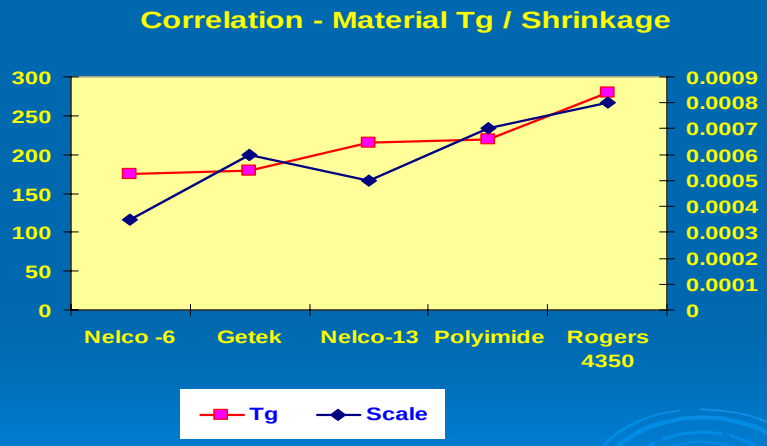
14

Effect of Panel Size and Material on Shrinkage



15

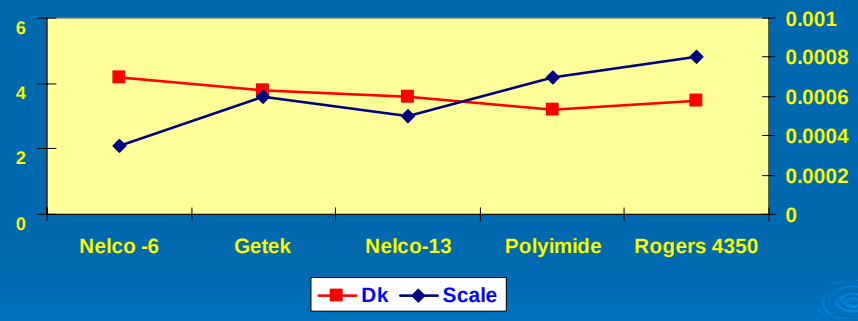
Material Movement compounded with higher Tg



As the Tg moves up, so does the material shrink factor

16

Material Movement compounded with reduced Dk



Lower the Dk, higher the material shrink factor;

- Material formulation plays a major role.

17

Key process strategies to combat Material Movement –

- Dynamic scaling Factor Data.
- Post etch punch.
- Tighter heat rise / cool down temperature controls in Lamination.
- Perfect test and X-ray Optimizer.
- Optical Drilling
- Accuracy of drilling machines.

18

Additional impact from Exotic Material

- Impact on Finer Pitch
  - On material reliability;
    - Drilling of densely populated holes in devices like DUT,s, BGA, do not allow the localized material temperature to cool down to below the Tg of the material before adjacent hole is drilled. This is known to have resulted in localized delamination.
  - On glass to resin bond;
    - Weaker bond provides passages for processing chemistries to seep in. This effects the long term reliability of the board.

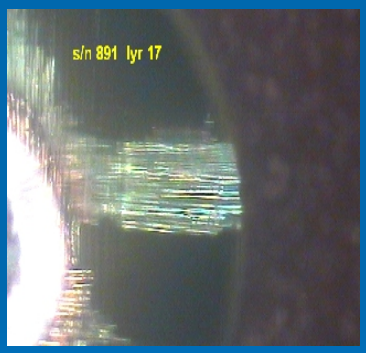
19

Exotic Materials

- Impact of Finer Pitch (contd.)
  - Drilling
    - of small pitch holes in materials increases wicking and have poor fill/plate properties.
      - Wicking / lamination voids opens up the passage for chemistries to seep along the glass bundles.
      - This could result in a short during PCB manufacturing or could later result in CAF failure

20

Exotic Materials - CAF



Wicking to ground

CAF path/leakage

21

Key Strategies to address Exotic Materials

- Selection / recommendation of materials is done to improve better fill / bond.
- Tg selection is critical.
- Drilling optimization (de-optimization in this case) to reduce the effect of heat generation.
- Drilling parameters and tools to best suit each type of exotic material.
- Critically placed bake cycles at various process steps to seal material gaps caused by drilling.

22

Via Formation

- Drilling and Hole Preparation
- Plating

23

Via Formation - Drilling

- Smaller pitch leads to smaller drill diameters, which leads to
  - Flute length constrain for Thick boards
  - Drill deflection
  - Debris control and removal
  - Higher occurrences of Drill breakage

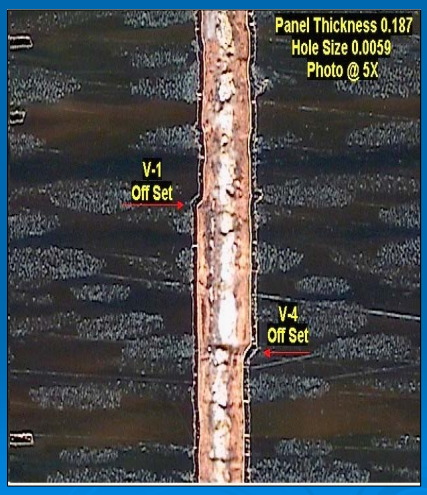
24

Flute constraints and Deflection

- Flip Drilling
  - Half of the hole depth is drilled from one side then the panel is flipped and balance of the hole depth is drilled from second side.
  - Necessity to control the overlap. Otherwise it causes
    - Mis-aligned hole
    - Debris entrapment
    - Poor plating quality
    - Shorts

25

Via Formation – V1/V4 drilling



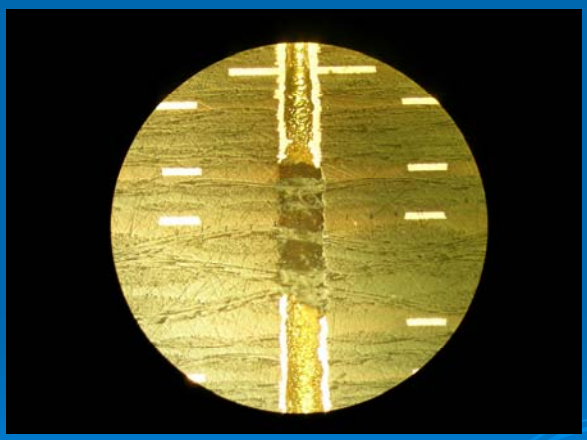
26

Via Formation – Hole Preparation

- Challenges resulting from smaller diameters
  - Drill debris removal
    - Must be removed before wet processing
    - Plugged holes will result in partial / full voids
    - Reduces hole sizes due to glass fibers / debris
  - Entrapped gas bubbles are harder to dislodge;
    - results in voiding of the holes
  - Hole wall preparation and Smear removal
    - Harder for processing chemistries to penetrate, making it harder to have good hole wall preparation and smear removal.
    - Smear will cause interconnect separation

27

Via Formation



Debris void

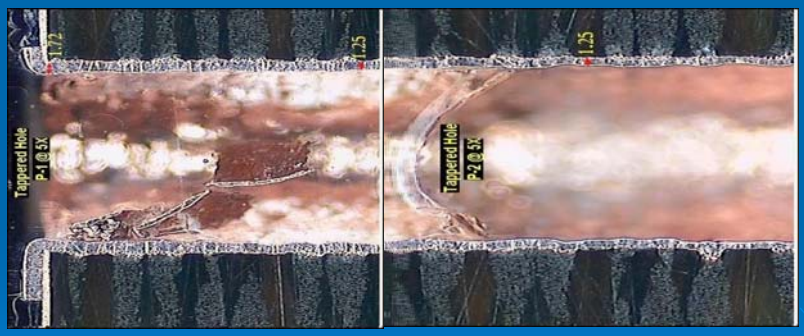
28

Via Formation - Plating

- Plating
  - Higher aspect ratios limits flow of plating chemistries
    - Results in hourglass type of holes
  - Unbalanced plating distribution on surface and between surface and holes;
    - Etching of traces is inconsistent, resulting trace width variation on the board and between boards.
    - Effect impedance.

29

Via Formation – Plating – Hourglass Effect



30

Key strategies to address Plating of high aspect ratio holes

- Improve throwing power of plating chemistries.
- Fluid transfer mechanism to further improve the throwing power of chemistries.
- Ability to plate at lower ASF to improve distribution
- Barrel plating process to reduce plating on the surface. This process also improves the impedance of the surface layer.
- Via plugging process after copper plating to overcome process limitations of hard Nickel / Gold baths.

31

Summary

- Tolerance Budget
  - Design requirement far exceeds process / Material / equipment capabilities;
    - Laser Direct imaging
    - Post Etch punching
    - X-Ray optimizers
    - Flip Drilling
    - Improved Drill bit design and Drilling parameters

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Summary

- Material Movement
  - High performance materials and More DUT / board requirements, make's material movement very critical.
    - Dynamic shrink factors
    - Improve layer to layer alignment using PEP
    - Controlled Heat rise and cool down in lamination press
    - X-Ray optimization
    - Optical Drilling

33

Summary

- Exotic Materials
  - Demand for Higher Tg's and lower Dk's has exposed Material formulation's limitations in relation to it bond strength, movement, fill characteristics and resistance to chemicals.
    - Selection of material with Tg, fill characteristics and bond strength.
    - X-Ray Optimization of each panel
    - Optical drilling and newer higher accuracy drilling machines
    - Process improvements to reduce material damage during processing.

34

Summary

- Via Formation
  - Higher aspect ratio, micro vias challenges not only registration process capabilities but also exposes limitation of Hole preparation and Plating Processes
    - Improve drill bit design to reduce deflection and better debris extraction
    - Drilling parameters for cleaner holes
    - Single head drilling machine with CCD camera
    - Proprietary process to improve chemistry flows and throwing powers
    - Specialized processes to improve plating distribution.

35

Conclusion

- Semiconductor Roadmap presents significant challenges to PCB fabrication techniques.
- ATE PCB requirements are more stringent than end user application PCBs.
- Investment is necessary to address all of the areas discussed today.
- Expect a cost and lead time impact when dealing with fine pitch devices with high layer counts.

36

Are Sockets Required for Test and Burn-in ?

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Belgacem Haba, Ph.D.
Tessera, Inc.

Agenda

- Background
- Micro Contacts Technology
- Results and Discussion
- Conclusion

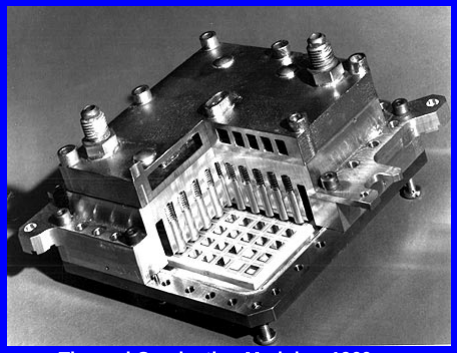
Agenda

- **Background**
- Micro Contacts Technology
- Results and Discussion
- Conclusion

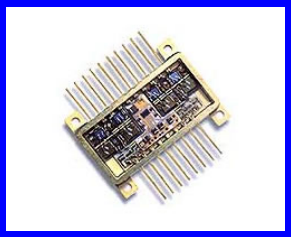
Bel Haba 3

Driving Technical Innovation

Historically, the military and aerospace markets were the dominant drivers of miniaturization …



Thermal Conduction Module – 1960s
Source: IBM



Thin Film Hybrid Microcircuits
Source: SatCom

Bel Haba 4

Worth 1/3 – 1/2 Their Weight in Gold: Miniaturization Commands a Premium

Consumer markets are the dominate driver of miniaturization today

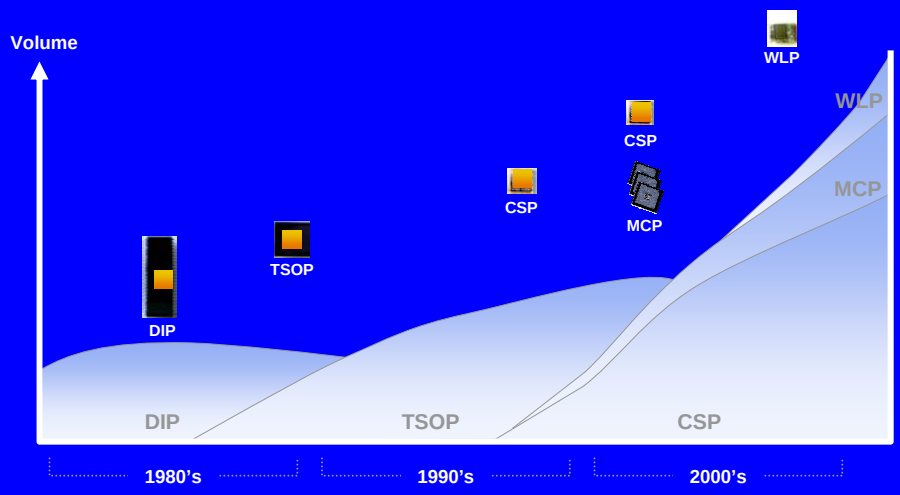
Source: Apple
Apple iPod Nano®
42 grams

Source: Motorola
Motorola Razr®
95 grams

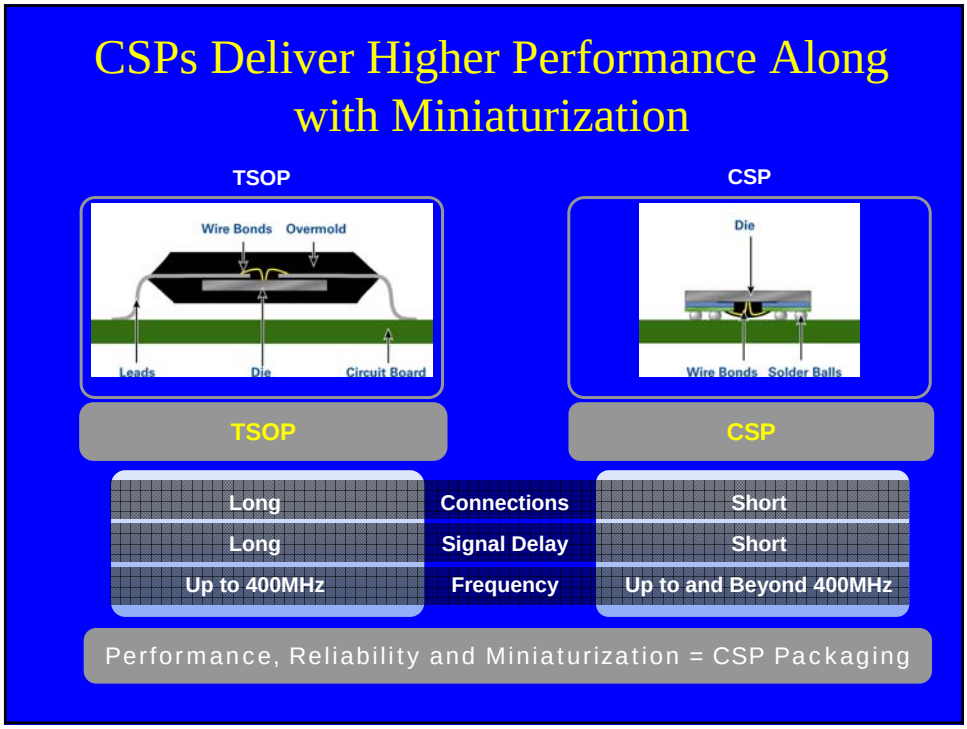
(Gold price ~$17/gram)

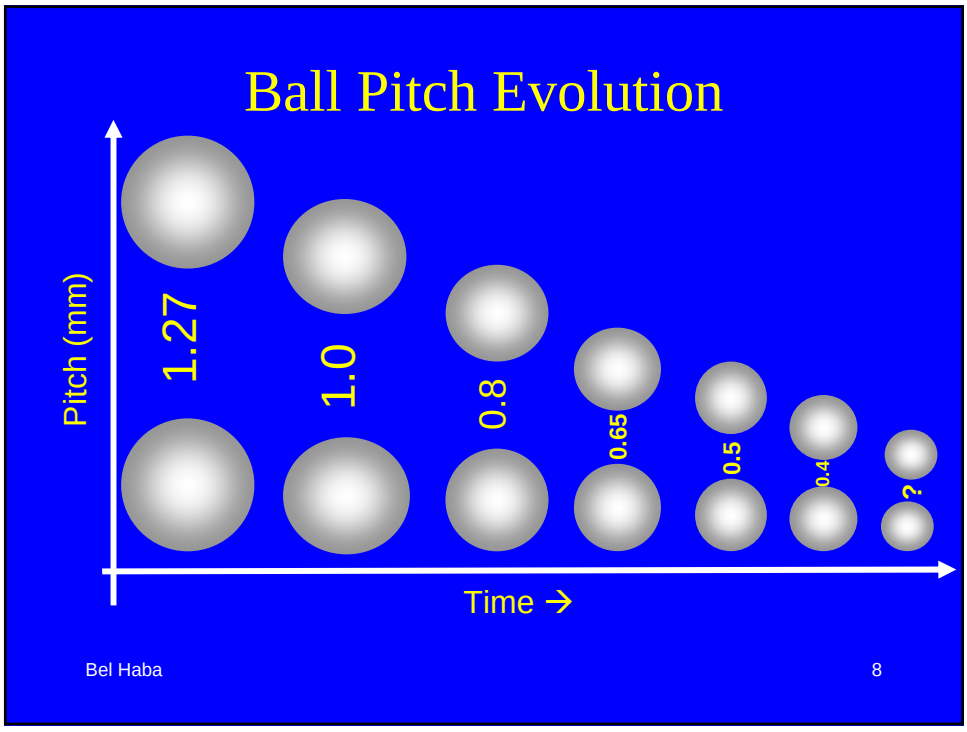
Bel Haba 5

Industry Conversion to CSP, MCP, WLP Technologies



Bel Haba 6


CSPs Deliver Higher Performance Along with Miniaturization
TSOP
CSP
Wire Bonds
Overmold
Leads
Die
Circuit Board
Die
Wire Bonds
Solder Balls
TSOP
CSP
Long
Connections
Short
Long
Signal Delay
Short
Up to 400MHz
Frequency
Up to and Beyond 400MHz
Performance, Reliability and Miniaturization = CSP Packaging


Ball Pitch Evolution
Pitch (mm)
1.27
1.0
0.8
0.65
0.5
0.4
?
Time →
Bel Haba
8

Shrinking Pitch Leads to Test/Burn-in Issues

- Packages are not getting any smaller and the number of I/O is increasing
  - Sockets are becoming increasingly complex
  - Greater socket force is required
- Chip processing speed is increasing
  - Very short socket pins required
- Finer pitch
  - Manufacturing and tolerance issues
  - Solder cleaning issues
- Cost is increasing

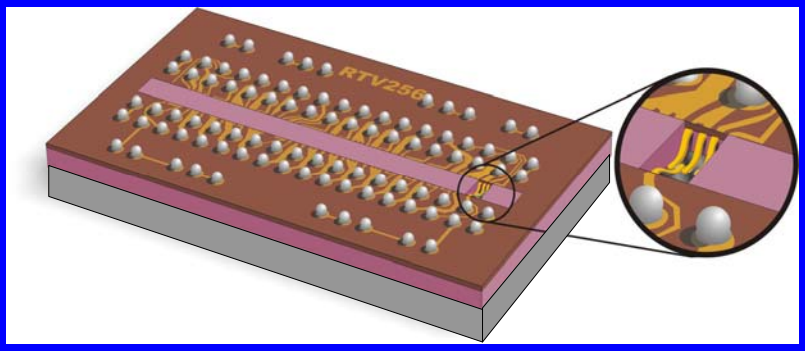
Bel Haba 9

Agenda

- Background
- **Micro Contacts Technology**
- Results and Discussion
- Conclusion

Bel Haba 10

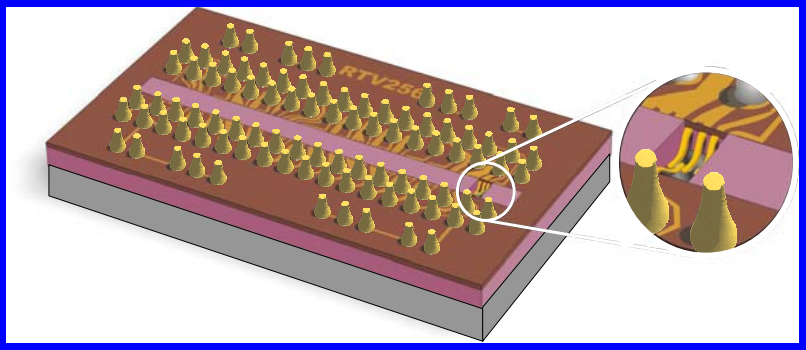
CSP Technology



Example of DRAM: 0.8 mm pitch balls

Bel Haba 11

Micro Contacts Technology

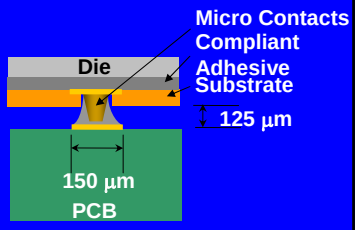


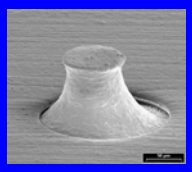
Example of DRAM: 0.8 mm pitch with micro contacts

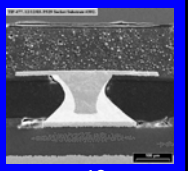
Bel Haba 12

Micro Contacts in Lieu of Solder Balls

- Co-planar contacts on a substrate
- Improved electrical performance
- Lower profile than traditional CSP
- No testing sockets required: simple pressure contact to PCB
- Enables fine pitch/wider routing channels
- Offers manufacturing advantages
  - Easy adoption into current infrastructure
  - SMT compatible
  - Resolves fine pitch, re-work problems
- Targeted Applications
  - Stacked Memory: Flash, DRAM, SRAM
  - Mixed Memory Stacking
  - Fine Pitch CSP: Digital, analog baseband
  - RF CSP: transceivers

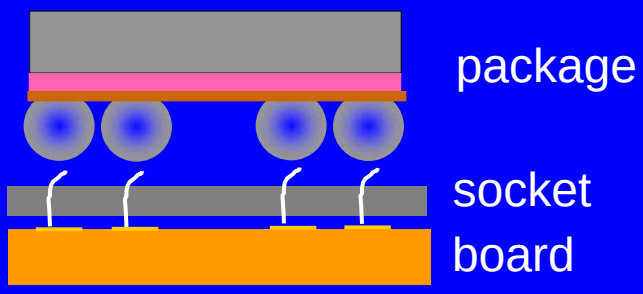






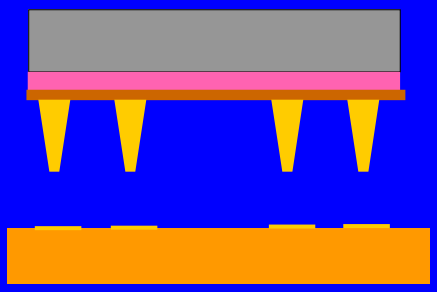
Bel Haba 13

Existing Testing and Burn-In



Bel Haba 14

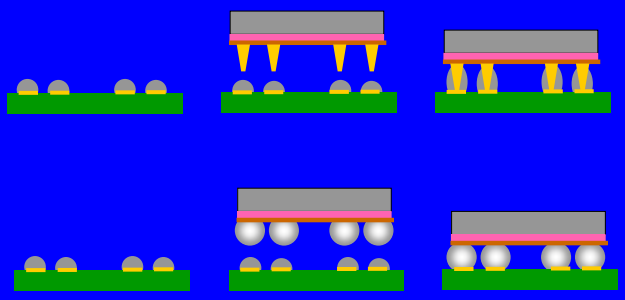
Micro Contacts Test and Burn-In



- No sockets required
- Tolerance issues mitigated
- Much lower cost

Bel Haba 15

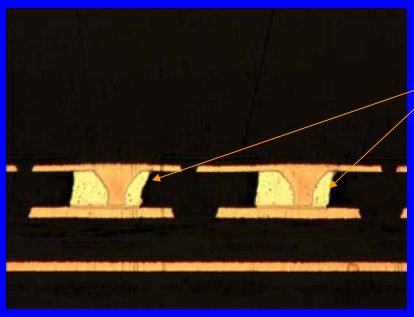
Standard Surface Mount to Board Assembly



Bel Haba 16

Solder Paste Stencil Optimization for Surface Mounting

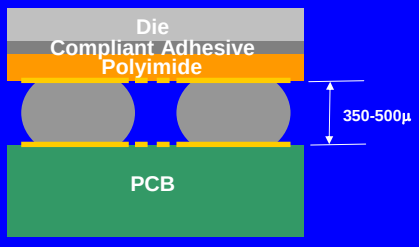
5 mil thickness, 300 μm dia. stencil



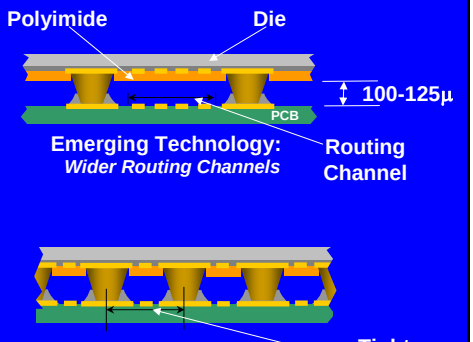
Well-formed solder columns

Bel Haba 17

Comparison to Conventional BGA Package



BGA: Solder-ball pads limit routing channels



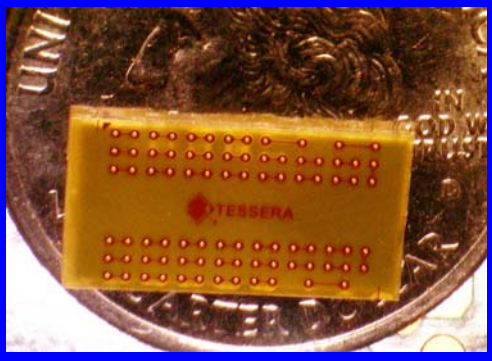
Bel Haba 18

Agenda

- Background
- Micro Contacts Technology
- **Results and Discussion**
- Conclusion

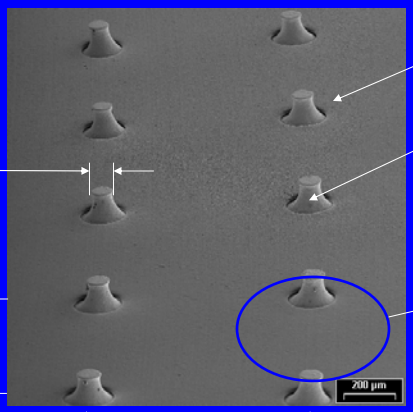
Bel Haba 19

Test Package: DDR2



Bel Haba 20

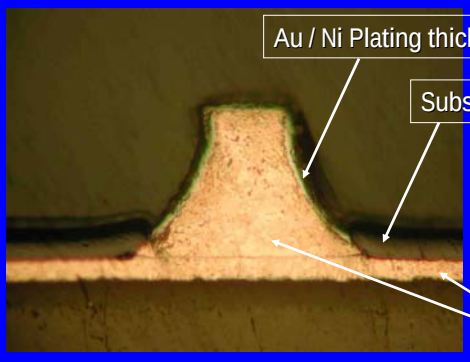
Micro Contacts: 0.8 x 0.8 mm pitch



Finer Pitch (<400µm)
Very feasible

Bel Haba 21

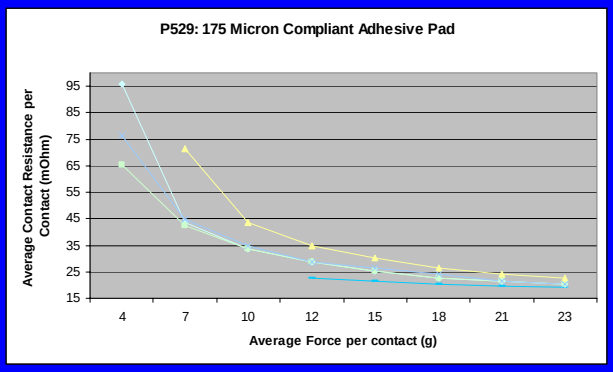
Micro Contact Substrate



Bottom diameter : ~180µm
Height : ~125µm, up to 250mm
Tip Diameter: ~80µm

Bel Haba 22

Resistance Testing



All micro contacts tested in 84 lead DDR II daisy chain test vehicle

Bel Haba 23

Mechanical Testing

- High Temperature Mechanical Cycling (measures wear on Component Burn-in Test boards)
  - > 26 grams/contact force
  - 530 cycles of package/PCB from 50C to 120C with 200mA bias current flowing through all contacts in daisy chain (4cycles/hr)
  - No PCB damage

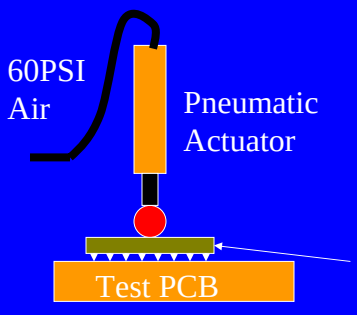
Bel Haba 24

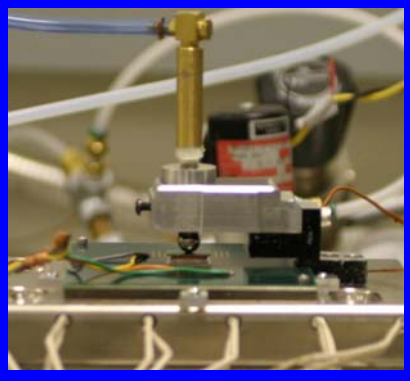
Mechanical Testing cont'd

- No Contact Sticking to burn-in PCB:
  - Mechanical force for 24 hours @150 C
  - > 26 grams/contact force
- Short Duration Mechanical cycling (measures wear on component final test boards)
  - > 26 grams/contact force
  - Over 23,500 pressure cycles with no PCB damage

Bel Haba 25

Mechanical Test Jig





Package under Test (~26 grams/contact force)

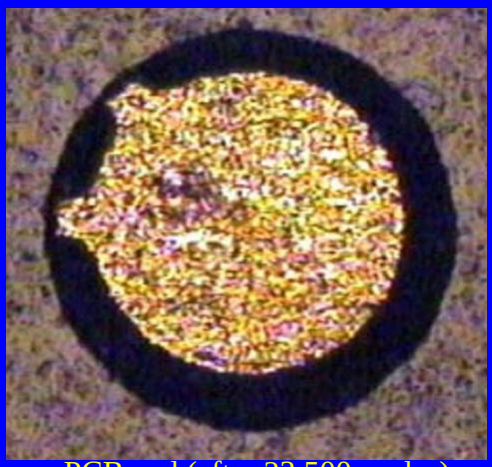
Bel Haba 26

High Temperature Mechanical Cycling

80 microns

Micro contact tip (expanded scale)

No damage after mechanical cycling testing

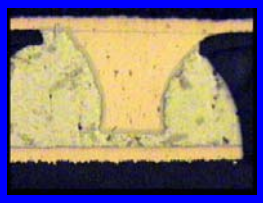


PCB pad (after 23,500 cycles)

Bel Haba 27

Module Assembly

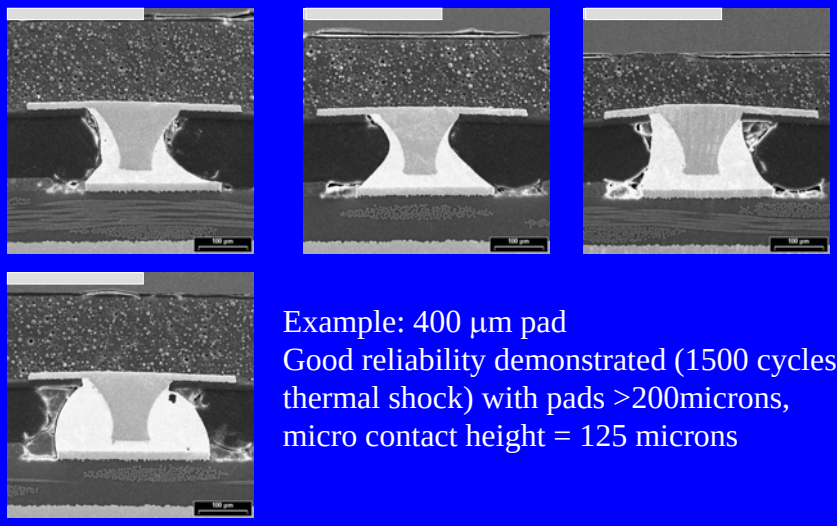
- Assembled PCB Thermal shock:
  - 1500 cycles (-65 +150C) [air to air]
  - 84 lead DDRII (0.8mm x 0.8mm pitch)
  - Pad sizes: 100, 125, 150, 175, 200, 275, 350, 400 microns
  - Solder stencil sizes: 100, 125, 150, 175, 200, 250, 350, 400 microns (125 microns deep cavity)



Typical soldered micro contact

Bel Haba 28

Solder Pad/Volume Examples



Example: 400 μm pad
Good reliability demonstrated (1500 cycles thermal shock) with pads >200microns, micro contact height = 125 microns

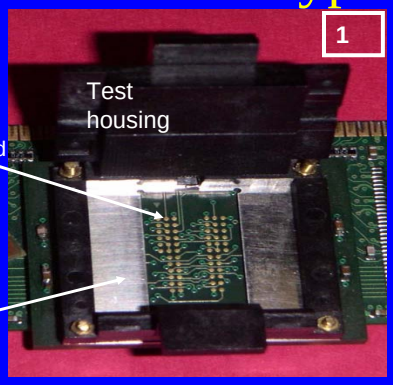
Bel Haba 29

Test and Burn-In

- **No testing socket interconnect required**
  - Simple pressure contact to PCB
  - 10 to 20 grams per contact pressure for contact
- **Eliminate socket interconnect and associated parasitics**
  - No test socket degradation of high speed devices
  - See prototype testing method (next slides)
- **Simplified rework of packages**
  - Micro contact remains with package substrate

Bel Haba 30

Prototype Testing

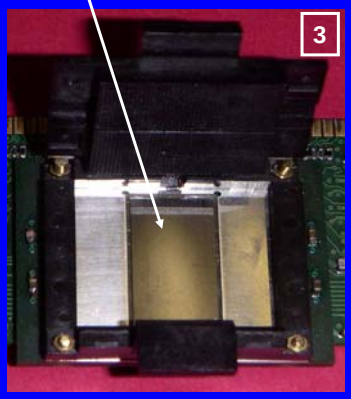


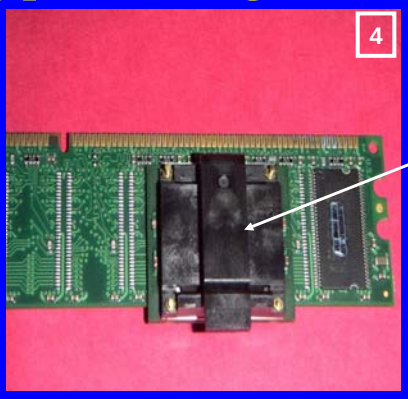
- Simple contact direct to board
- Similar housing could be used for Test/Burn-In

Bel Haba 31

Prototype Testing

Package placed in housing, micro contacts down





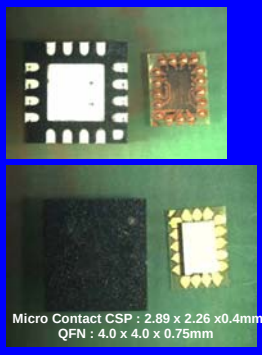
Top closed and package held in place ready for test

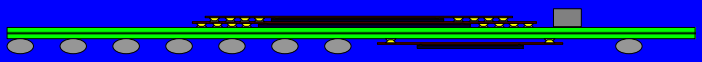
- Micro contacts placed down to board
- Range of 10 to 20 grams per contact

Bel Haba 32

POP Application: Baseband/GPS Reciever/Memory Stack

- Uses ultra low-profile packages to integrate all radio functions in less than 1mm high
- Uses a combination of solder ball and micron contacts
- Alternate approach to LTCC integration with the additional benefit of integrating baseband and digital functionality

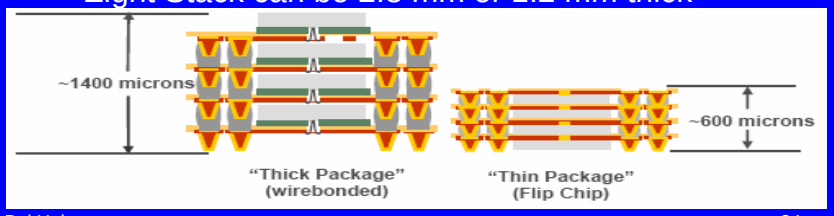




Bel Haba 33

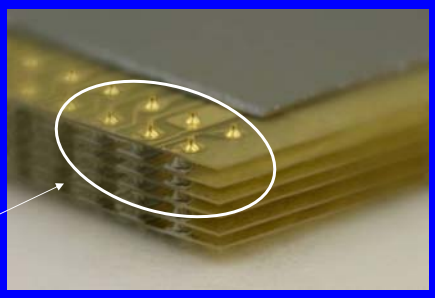
Next-Generation CSPs

- **Enabling up to 50% reduction in thickness compared to traditional CSPs such as FBGAs**
  - Each layer 0.15 – 0.35 mm thick
  - Allows for high-density 3-D integration while preserving full testability
    - No "Known Good Die" problem
  - Finer pitch (0.3 mm) allows for ~2x higher pin counts
  - Eight Stack can be 2.8 mm or 1.2 mm thick



Bel Haba 34

Micro Contact Stack Samples



Micro Contacts

6-Stack ~ 900 um

"Prototype sample"

Bel Haba 35

Summary

- Introduction of micro contact technology
- Scalability to fine pitch and high I/O
- Cost reduction path for test & burn-in
- Versatile approach can be leveraged in many applications
- Stay tuned…….

Bel Haba 36